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Password based door locking system using Verilog

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Abstract — ***Recently, burglary and robbery cases have been increasing and one of the factors that contributes to the growth of these cases is the weakness of the old-style home security system. The old-fashioned key and lock system may bring challenges to the effectiveness of the system since the keys are exposed to the risks of being lost and duplicated. The advancement of technology has introduced an electronic combination lock system in which only the house owner and selected people can unlock the doors. A main goal of this paper is to design and develop an electronic combination lock system using Verilog code. The entrance door of a house will only unlock if the user enters the correct secret code on the FPGA Board. If the password is correct then only it will let you enter in the room if not it will alarm the buzzer. This is a simulation based project.***

Keywords — *Door locking system , Home security, Xilinx, FPGA*

1. Introduction

A study made by our group had agreed that the old fashioned key and lock system may bring challenges to the effectiveness of the system since the keys are exposed to the risks of being lost and duplicated. This feature is believed to be insecure as break-in can easily occur when the keys are duplicated. The statistical analyses found that a house without a security system is more likely to be broken-in compared to the houses that had been well-equipped with security features. Normally, when an event such as intrusion occur, it presents itself arbitrarily, and there might be noticeable physical evidence is witnessed of their occurrence when completed or they pass without notice based on the purpose of the intruder

1.1 Door lock

The topic selected to be implemented in this report is: Door lock. In general, the requirements of the project are as follows: Realizing a door lock circuit using a state machine has the following functions:

- The password is a three-digit hexadecimal number from 0 to F.
- Digits are entered through the SWs.
- Only one digit is entered at a time, KEY1 is used to confirm the input one digit. The entered digit must appear on the 7-segment LED.
- The circuit operates in two modes: Set and Verify. In Set mode, the user will set the password. In Verify mode, the user enters the password and the system checks it. The two modes can be switched through the KEY2.
- In Verify mode: If the entered password is correct, the green LED will blink at 5 Hz. If the password is wrong, the red LED will blink at 1 Hz. Then the user has 2 more attempts. If in these 2 times, the user enters the correct password, the number of attempts will return to the original.Otherwise, the system will be locked and can only work again if the user presses the reset button (KEY3).

1.2 Tools used

Verilog language HDL Verilog is a hardware description language (Hardware Description Language) used in the design of digital systems, integrated circuits: such as RAM, microprocessors, etc.

Verilog was first introduced in 1984 by the company Gateway Design Automatic. Verilog is not standardized and is edited in most later versions from 1984 to 1990.

In 1995 Verilog was officially standardized by the IEEE.

Verilog is a language quite similar to C programming language. However, it still has superior advantages over C, especially for hardware design such as Verilog can execute instructions sequentially or in parallel. song.

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2. Literature Review

2.1 Idea

The idea of the keyless lock system proposed in this project was almost similar with the project of the application of the Field Programmable Gate Arrays (FPGA) on a smart home security system.

2.2 Home security system

In this study we agreed that a burglar usually tried to penetrate a private area such as a house by dodging the door lock. Various systems in the modern world consist of confidential data which need to be protected using password. Most of the burglary‘s cases reported are the aggressive break-in cases because a burglar only needs 8 to 12 minutes to break conventional locks. Thus, smart home security control systems have become crucial in everyday life.

2.3 Field programmable gate arrays (FPGA)

FPGAs have started to take its place in new applications with their high-performance features for parallel computing and signal processing. The biggest advantage of using the FPGA device as a new component in the industrial environment is that the different hardware features of FPGA (flexible and reusable integrated circuit, computing parallel tasks, cost efficiency, multiple input/output capability etc.) that can be designed by a developer for different application platforms after production. FPGA can provide a wide opportunity for modern applications. Besides, FPGA provides an impacted size and low power consumption solution. FPGAs use dedicated hardware for processing logic and do not have an operating system. On the other hand, FPGA is very suitable for time-critical systems applications because every task on the FPGA hardware can utilize a different set of logic to be simultaneously run. Based on a study, FPGA is one the preferred implementation platform in many industrial applications because it can support high-speed, short time-to-market, good cost-performance and availability of specialized intellectual property (IP). The FPGA is able to be programmed over two ways: straightforwardly starting with An PC utilizing the around board stage flash ROM or through the USB port. A “smart home” technology is one realization of home automation ideals that employs the integrated digital systems such as FPGAs technology.

2.4 Hardware description language (HDL)

HDL helps the engineers to design a circuit logically and also functionally thus making it easier to simulate and calculate accurately the performance of the circuit. HDL is a computer-based language that had been widely used in order to describe the structure and behavior of electronic circuits and digital logic circuits. One of the benefits of using HDL to simulate digital processing of any logical inputs is because of the immediate FPGA based hardware implementation. It looks like the common computer programming such as the C language, however HDL is specifically used to describe the structures of a hardware and the behavior of logic circuits. In public domain, there are two standard HDLs that are supported by IEEE which are VHDL and Verilog. As for this project, the keyless lock system is being designed using Verilog coding. Verilog coding can support the logic control for production and the specification of the hardware circuitry as well as simulation and testing.

3. Methods

This project is software based simulation. The software required for this project is Xilinx ISE 14.7. Simulation and implementation are done in Xilinx ISE 14.7.

3.1 Design simulation process

A Verilog code of a keyless lock system is being designed and developed in Xilinx ISE. A testbench coding is required in order to simulate the designed Verilog code of the keyless lock system. The purpose of simulation is to do functional verification as well as to implement the required system behavioral correctly. The simulation part will take place in ModelSim Software, a simulator developed by Mentor Graphics that offers a simulation environment to simulate HDL designs. The results of the simulation were in the form of testbench waveforms.

• led7_decoder(): first, signal enable = 0, then enable = 1 and all 4-bit numeric values from 0 to F are tested.

• pass_decoder(): first, signal enable = 0, then enable = 1 and 16 values Random value of the password to be tested.

• LED_blinker(): with frequency 5Hz, first, enable signal = 0, then signal enable is held to 1 for a period of time.

• state_decoder(): all 6 states of the state machine are tested.

• password_getter_sync(): first, the circuit is reset, then 5 random digits are passed in.

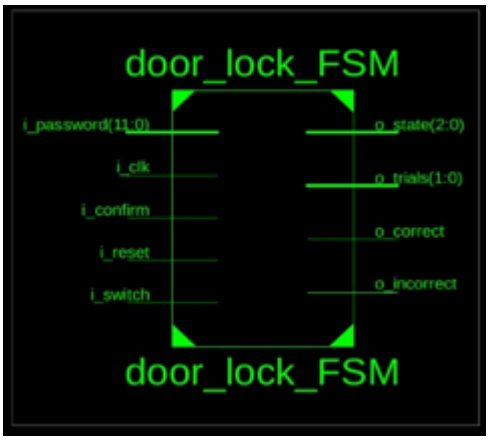
• door_lock_FSM(): state machine is tested as follows: reset -> INITIAL state -> VERIFY state with correct password -> VERIFY state with wrong password 3 times -> FREEZE state -> reset -> SET status -> VERIFY status with new password.

• door_lock_top(): test similar to state machine.

3.2 Programming and configuring FPGA device

In order to implement the designed Verilog code of the keyless lock system, the FPGA device needed to be programmed and configured. The RUN/PROG switch is set to the RUN position to run this step. Ensure that the mode

selected is in JTAG mode. Then, the .sof file created from the previous step is being selected. Once the START button is clicked, the configuration data will be successfully downloaded and the progress status shows —100% (Successful)‖.



Door Lock FSM

- It has various pins such as switch, reset, confirm, etc.
- Based on states SET, VERIFY and FREEZE the output waveform is generated.

4. Results

Figure.2 shows the flowchart of the keyless lock system.The digits are inputted in binary through switches SW[3:0], the confirmation signal for reading in a digit is generated by KEY[0]. The current value that the switches represent is shown on HEX4. The password is passed to the processing state machine when there is a confirmation signal from KEY[1]. The value of the inputted password is shown on HEX2 to HEX0, showing the password can be enabled/disabled using switch SW[4] . The design can operate in 3 different modes: SET, VERIFY and FREEZE. The first 2 modes are interchangeable using KEY[2]. The current operating mode will be shown on HEX7.

In order to unlock the door, the user needs to enter the password. The system will then compare the entered code with the setting code. If the entered code matches with the setting code, it will proceed to the next stage which is comparing the code length of the entered code with the code length of the setting code. If the code length of the entered code matches with the code length of the setting code, the door will be unlocked. Otherwise, the attempt counter will be increased by 1 and the system will restart to allow the user to enter a new code for the second time. On the other hand, if the code length of the code entered by the user does match with the code length of the setting code, the system will start to count the number of unsuccessful attempts. If the number of unsuccessful attempts has reached more than three attempts, the system will automatically sleep. However, if the number of the unsuccessful attempts did not reach three times, the system will be reset to allow the user to enter a new code. Thus, the objective of this paper is to introduce an electronic combination lock system to replace the old-fashioned key and lock security system.

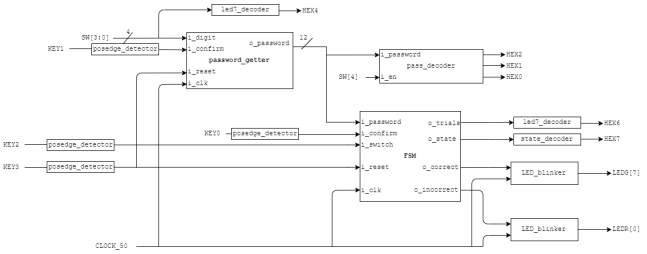


figure.1

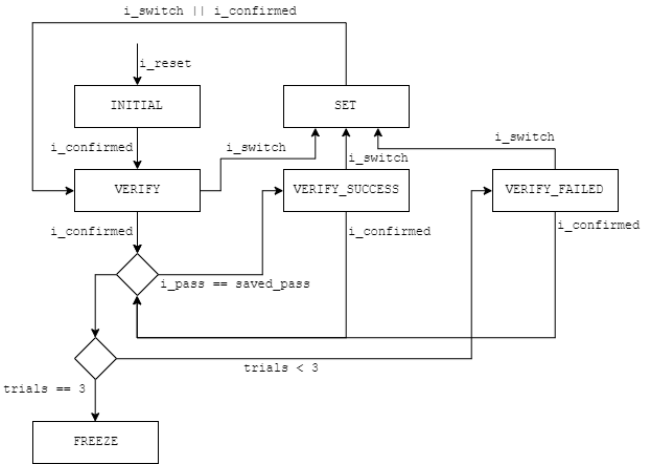
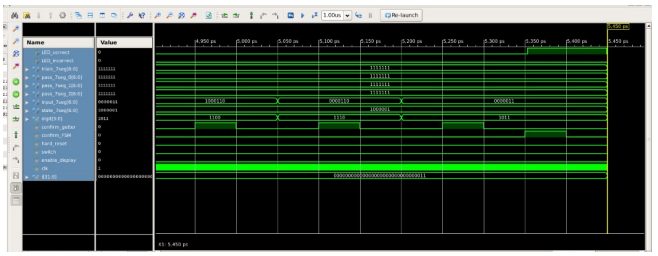


figure.2



Output waveforms

5. Conclusion and Future Work

In conclusion, an electronic combination lock system had been successfully designed using Verilog code. The output waveforms of the system had been verified and presented in Xilinx 14.7 software. The output results simulated are equivalent with the designed testbench codes. The Verilog code of the keyless lock system had been implemented on the Xilinx ISE. Trainer Board. For future work, it is recommended that this project can be extended to the sound of alarm after three wrong inputs were key-in. The sound of the alarm can alert the neighborhood that the possibility of robbery occurred in their vicinity. Then, this warning can be linked directly to the owner of the house via the handphone. Therefore, the alert and trigger system will be more effective in order to educate the community to help police decrease the number of reported crime cases.

Acknowledgment

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CE student @ HCMUT | CTF player @ Team Efiens | Reverser | Pwner

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