

# INDIAN INSTITUTE OF TECHNOLOGY ROPAR



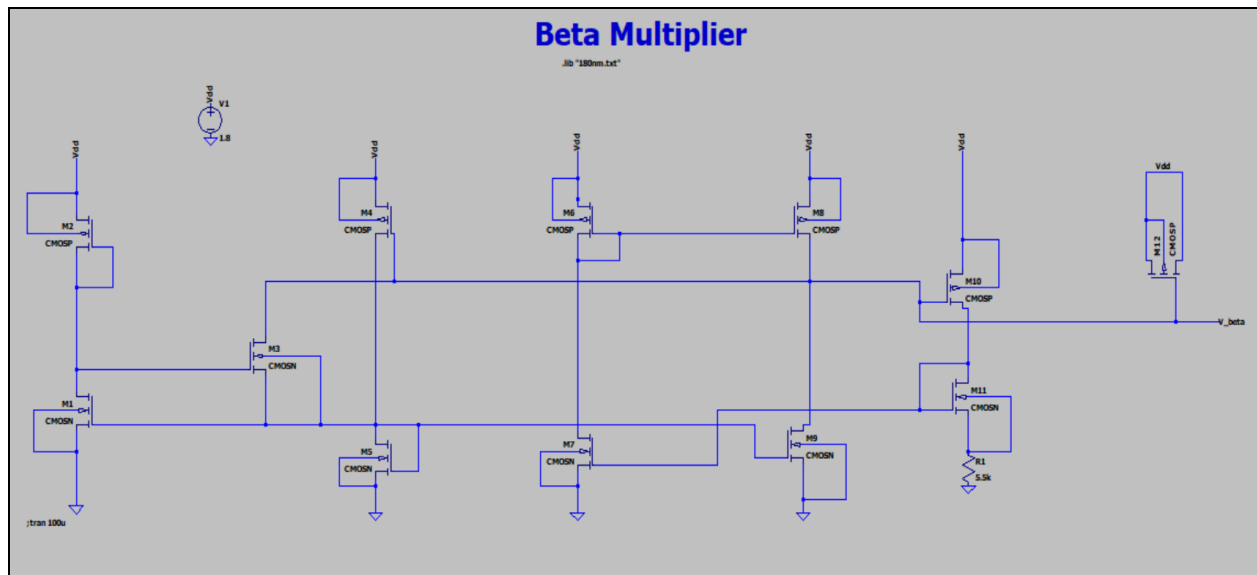
## EE-301: Analog Circuits PROJECT REPORT

**Vivek Chadgal** (2021EEB1222)

**Objective:** Design of cascode amplifier and cascode current mirror in schematic and layout using LTSpice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

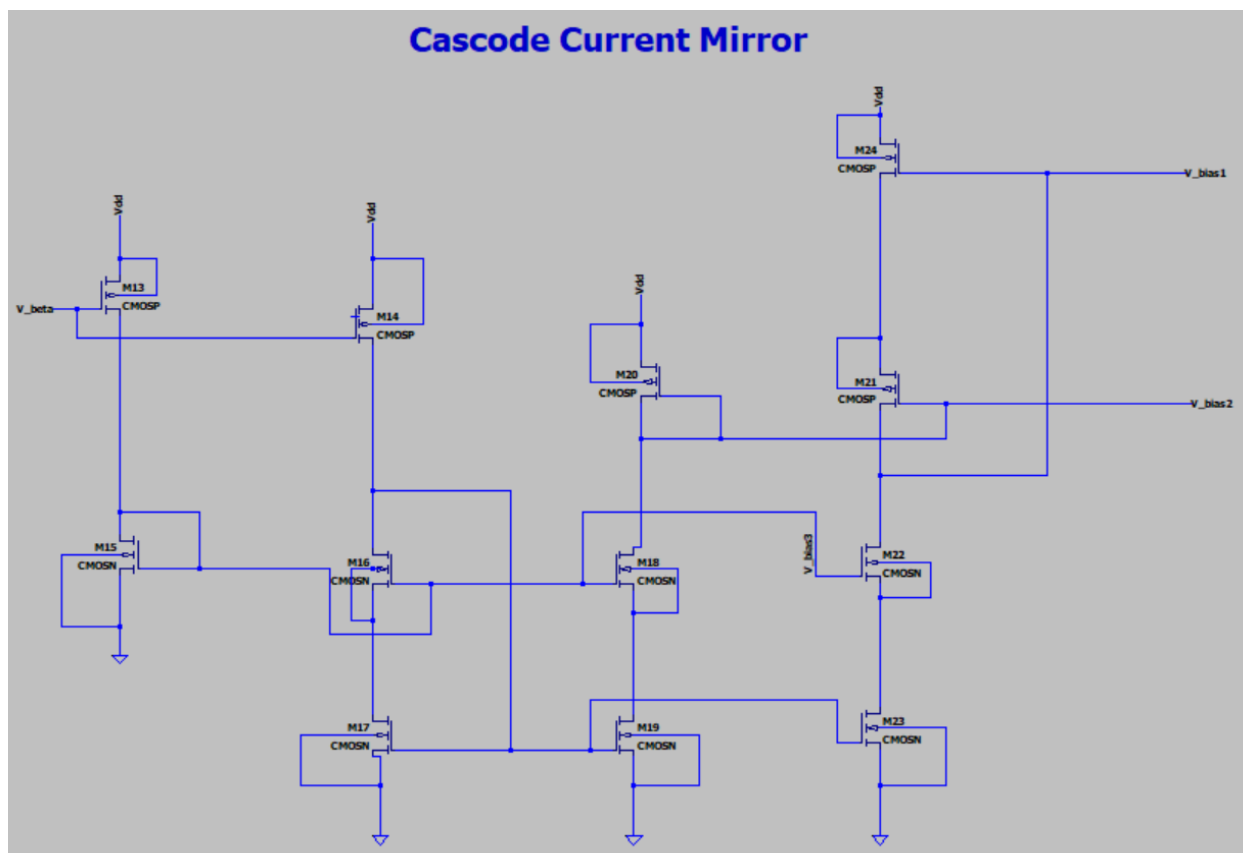
**Circuits [180nm]:**

Beta Multiplier:



The Vbeta obtained via simulation was *1.197V*.

Cascode Current Mirror:



After Simulation:

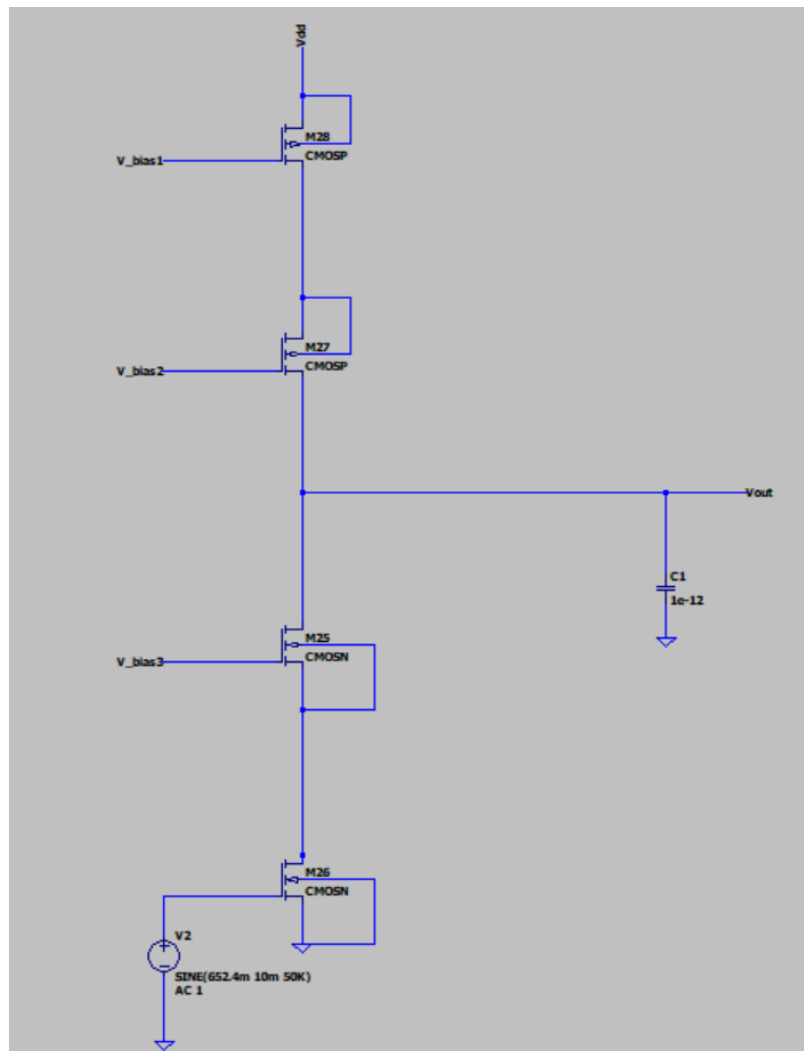
**Vbias1 = 1.16V**

**Vbias2 = 1.06V**

**Vbias3 = 629mV**

**Vbias4 = 652mV**

Cascode Amplifier:



### Calculations:

Given: gain,  $A_v = 20 \text{ V/V}$  ;  $C_L = 1 \text{ pF} = 10^{-12} \text{ F}$  ;  $V_{DD} = 1.8 \text{ V}$   
 Power Dissipation  $\leq 5 \text{ mW}$  (for 180nm)

$$\Rightarrow I_D(\text{max}) = \frac{5}{1.8} = 2.78 \text{ mA}$$

$$\Rightarrow \boxed{I_D < 2.78 \text{ mA}}$$

for UGB [Unity Gain Bandwidth] more than 500 kHz.

$$f_{\text{cutoff}} = \frac{1}{2\pi R_{\text{out}} C} > 500 \text{ kHz}$$

$$\Rightarrow \boxed{R_{\text{out}} < 318.4 \text{ k}\Omega}$$

$$\text{Now, } A_v = g_{m(\text{cas})} \cdot R_{\text{out}}$$

$$\boxed{g_m > 62.84 \mu\text{S}}$$

To operate in saturation

$$V_{ds} > V_{gs} - V_{thn} \rightarrow (\text{NMOS})$$

$$|V_{ds}| > |V_{gs}| - |V_{thp}| \rightarrow (\text{PMOS})$$

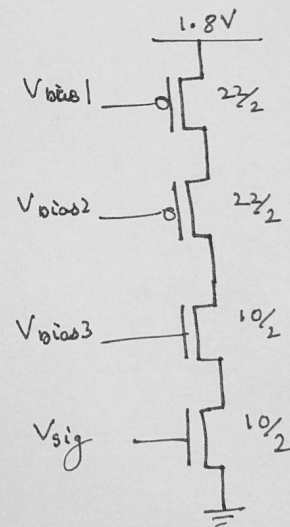
As per the simulation results.

$$\boxed{\text{Gain is } 26 \text{ dB}} \text{ \& has } \boxed{\text{UGB} = 5.32 \text{ MHz}}$$

$\Rightarrow$  All conditions satisfied

Power Dissipation  $10.7 \mu\text{W}$

$$\boxed{I_D (\text{swings}) = 10.7 \mu\text{A}}$$



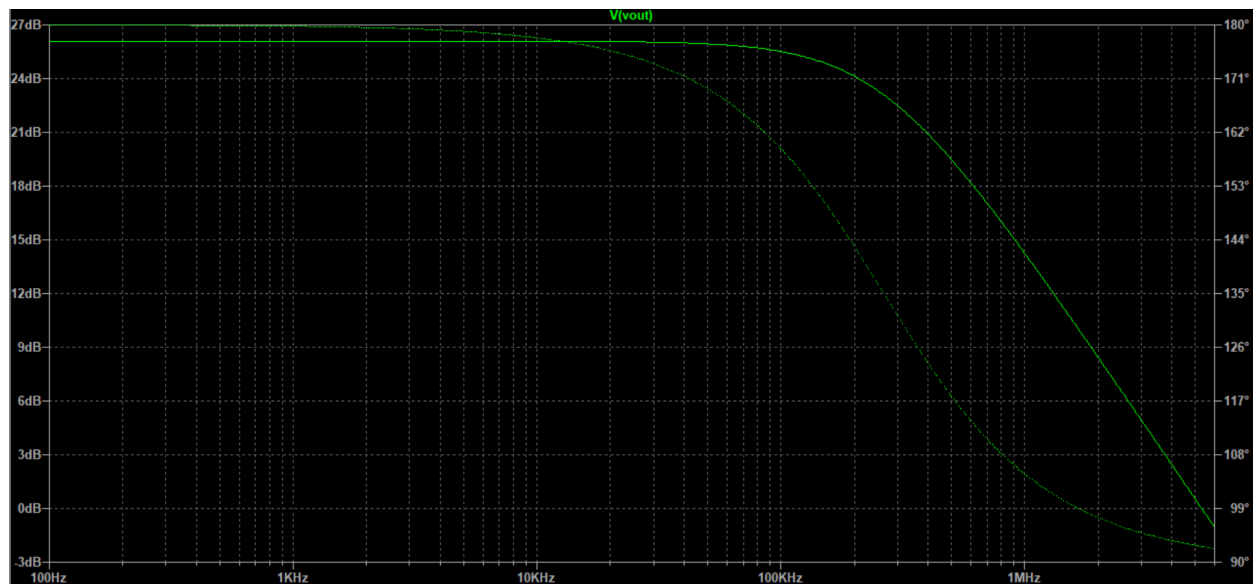
### Results:

Gain = 26 dB = 20 V/V

Unity Gain Bandwidth = 5.32 MHz

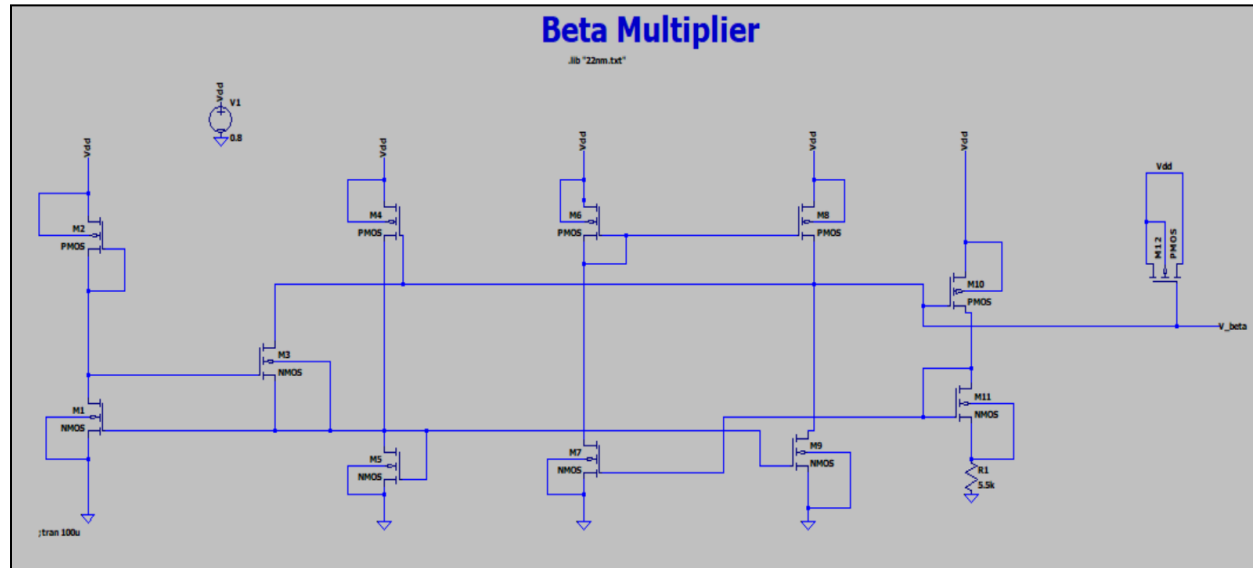
Power Dissipation = 19.4  $\mu\text{W}$

The frequency response is shown below:



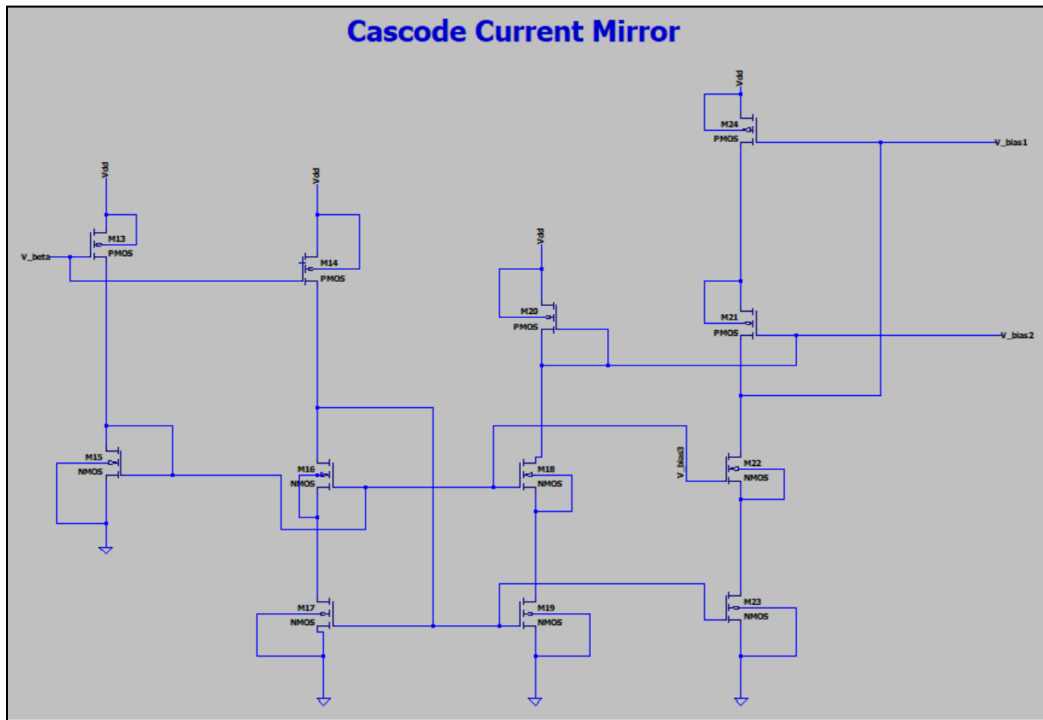
## Circuits [22nm]:

### Beta Multiplier:



The  $V_{beta}$  is 228.9mV.

### Cascode Current Mirror:



**The bias voltages obtained were:**

**Vbias1 = 225.4mV**

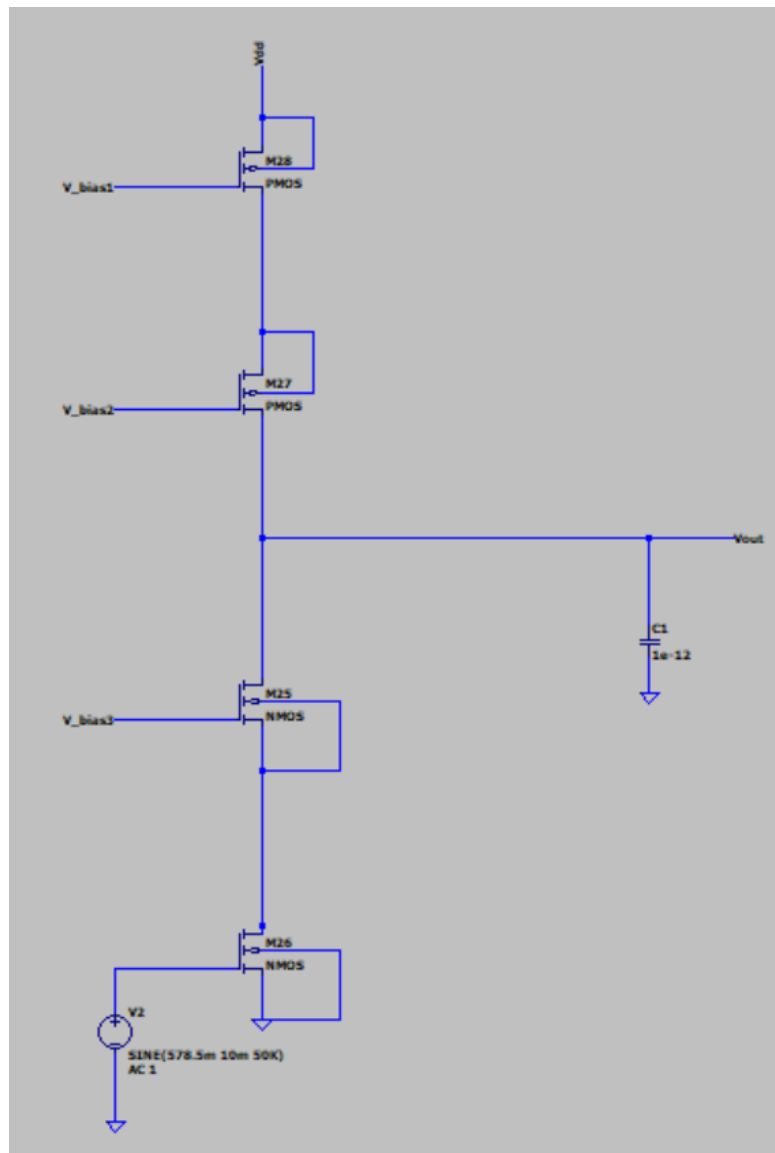
**Vbias2 = 118.05mV**

$$V_{bias3} = 612.83\text{mV}$$

**Vbias4 = 605.12mV**

These are the voltages used to bias the transistors in the cascode amplifier.

### Cascode Amplifier:



### Results:

**Gain = 26 dB = 20 V/V**

**Unity Gain Bandwidth less than 500kHz**

**Power Dissipation = 83.1  $\mu$ W**

Here is the frequency response:



MAGIC LAYOUT SNAPSHOT:

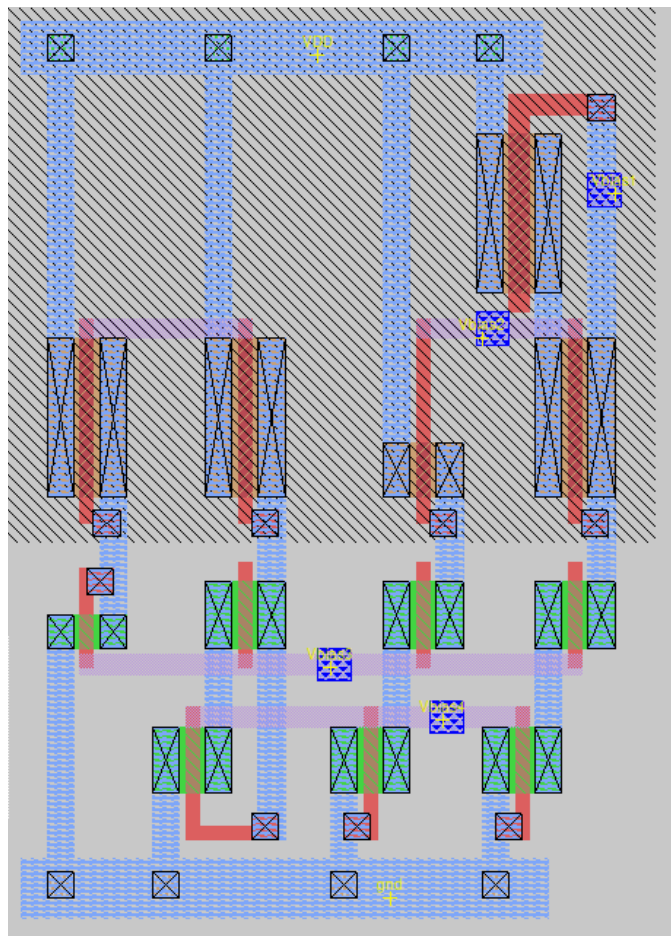


Fig: Magic Layout Cascode Current Mirror



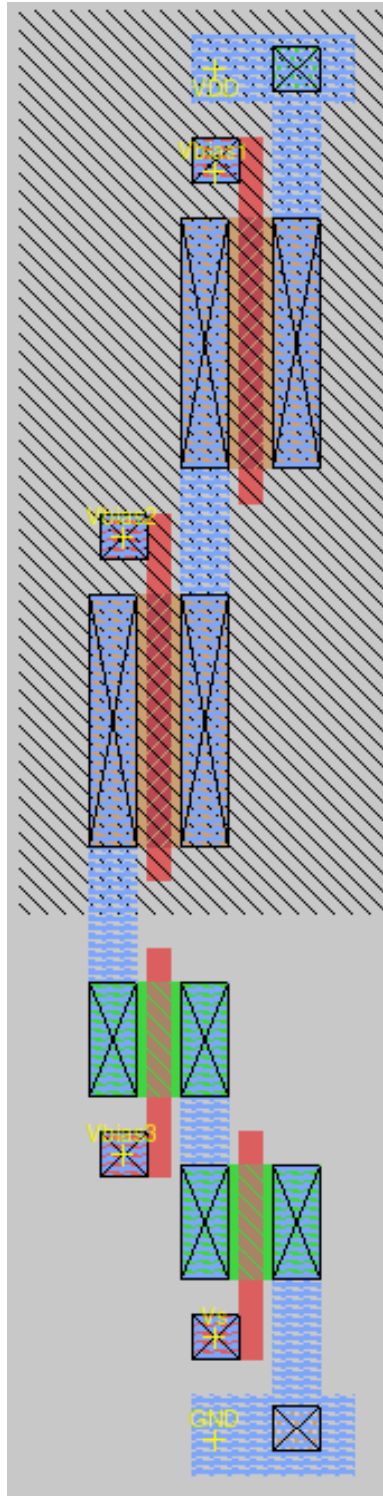


Fig: Magic Layout Cascode Amplifier