# **Shift Registers**

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**Div** : **SE** - 4

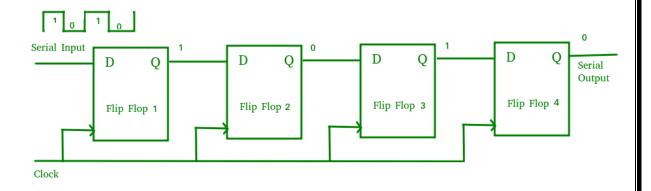
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A shift register is a fundamental digital circuit used to store and manipulate data in the form of binary bits. It operates by shifting the stored data in a specific direction, either left or right, in response to clock pulses. Shift registers are typically composed of flip-flops, which are basic memory elements that can store one bit of data each. They are widely used in digital systems for tasks such as data storage, data transfer, and signal processing. There are various types of shift registers, including Serial-In Serial-Out (SISO), Serial-In Parallel-Out (SIPO), Parallel-In Serial-Out (PISO), and Parallel-In Parallel-Out (PIPO), each designed to handle different input and output requirements. Their ability to shift and store data makes them essential components in devices like microprocessors, communication systems, and digital signal processor

### **Types of Shift Registers:**

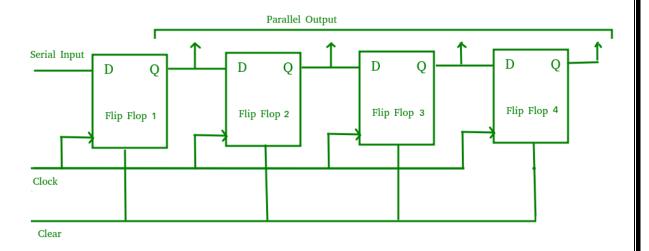
# 1) Serial-In Serial-Out Shift Register (SISO)

A Serial-In Serial-Out (SISO) shift register is a type of digital circuit that processes data in a sequential manner. It accepts input data bit by bit through a single data line and produces an output in the same serial fashion. As the name suggests, the SISO shift register has only one output, and data exits the register one bit at a time. In the logic circuit diagram below, you'll find a representation of a serial-in serial-out shift register. This circuit comprises four D flip-flops connected in series. Notably, all these flip-flops operate synchronously—they share the same clock signal for coordinated data movement



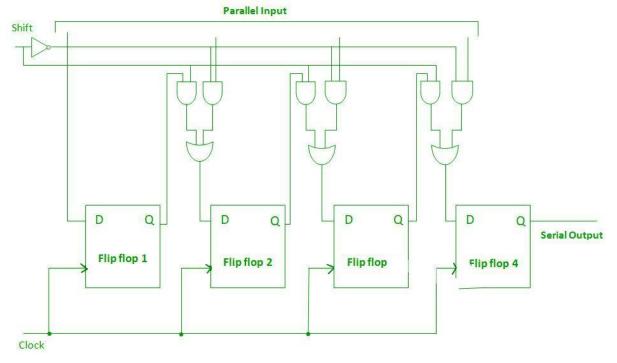
# 2) Serial-In Parallel-Out Shift Register (SIPO)

The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as the Serial-In Parallel-Out shift register. The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all 4 flip flops in order to RESET them. The output of the first flip-flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip-flop.



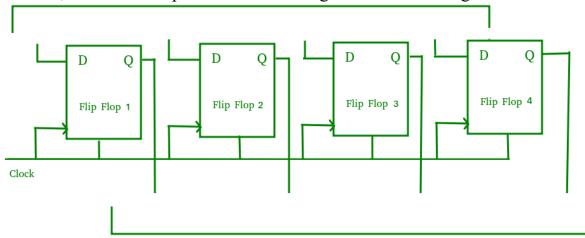
### 3) Parallel-In Serial-Out Shift Register (PISO)

A shift register that accepts parallel input (where data is provided to each flip-flop separately and simultaneously) and generates a serial output is called a Parallel-In Serial-Out (PISO) shift register. The logic circuit shown below illustrates this type of shift register, consisting of four connected D flip-flops. The clock input is shared by all the flip-flops, while each flip-flop receives its data input individually through a multiplexer (MUX). The input to the MUX is a combination of the previous flip-flop's output and the parallel data input, with the MUX output feeding into the next flip-flop. All the flip-flops operate synchronously, as the same clock signal is applied to each one.



#### 4) Parallel-In Parallel-Out Shift Register (PIPO)

A shift register that accepts parallel input (where data is provided to each flip-flop separately and simultaneously) and produces a parallel output is called a Parallel-In Parallel-Out (PIPO) shift register. The logic circuit below demonstrates the configuration of such a register, consisting of four connected D flip-flops. Both the clear (CLR) and clock signals are shared across all four flip-flops. In this type of shift register, there are no interconnections between individual flip-flops, as no serial data shifting is required. Each flip-flop receives its own separate data input, and the output is collected individually from each flip-flop. PIPO shift registers are commonly used when simultaneous input and output of multiple bits are needed, making them ideal for applications requiring fast parallel data transfers, such as microprocessor interfacing and data buffering.



Parallel Output