

Low Pass filter Using MOS Active Resistor

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Documentation And Reference

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Analog and Mixed Signal VLSI Design

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Aim: The primary purpose of this project is to design an Active Low Pass Filter, of given specifications using Metal oxide semiconductor as a resistor in SPICE. As a further improvement capacitor itself can be designed using MOS. Circuit topology including elements and their values can be freely selected. *SPICE* is industry standard software to design and simulate electrical circuits. It is derived from original SPICE program where, SPICE is acronym for *Simulation Program with Integrated Circuit Emphasis*.

Design Parameters: The LPF should follow following constrains:

Parameter	Value	Unit	Specification
F_c	1	KHz	Cutoff Frequency
V_{in}	500	mV	Peak Amplitude of Input Signal

Table 1. Low Pass Filter Parameters

Furthermore we have following constrains:

S. No	Constrain
1	We may or may not use OP-AMP and active capacitors
2	Any other voltage source in the circuit must not exceed 5V
3	The cut-off frequency must be within $\pm 5\%$ of the given value

Table 2. Circuit Constrains

Required Output: This problem requests an output plot between Gain (dB) & Frequency. Any other appropriate simulation result may be included.

Theoretical Analysis: Filters are a key component of analog designing. Filters process an input signal and removes unwanted features (frequency/noise) base on its characteristics. Low pass filters can be constructed in many ways. However, for this lab we are specified to use active resistors. LPF and active resistors are briefly explained below:

- Low pass Filters: Low pass filters are characterized such as they pass low frequencies up-to f_c and attenuate frequencies, which are above f_c , where f_c is the cutoff frequency of the filter.

Conceder the circuit shown below, which shows a first order passive LPF:

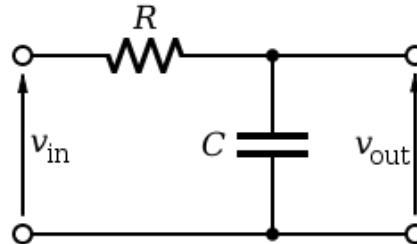


Figure 1. A passive first order LPF

In this circuit values of R & C dictate cutoff frequency. The output is obtained across capacitor. Since capacitive reactance decreases with frequency, the RC circuit exhibits attenuation towards high frequencies. Thus only low frequency component of the input signal can be obtained at

output. However it should be noted that this attenuation is not sudden as desired. Signal amplitude generally falls off -6dB/oct beyond the cutoff frequency. If steeper cut of is desired higher order filters should be used.

The Cutoff frequency of a LPF is give as:

$$F_c = \frac{1}{2\pi RC};$$

Where;

F_c = Cutoff Frequency

R = Resistance

C = Capacitance

- Active Resistor: Active devices such as BJT and MOS can be biased to obtain a constant current.

This current is however; constant over a small range of input thus the biasing of device should be done properly to place its Q-point in correct region of operation. As a result these active devices can be converted to and used as a two-terminal active resistor for a small variation in input voltage. Fortunately input voltage variation in most small signal (AC) models is small thus within that region these devices can perform well as an active resistor. An advantage of this configuration is that MOS or BJT require smaller area as compared to poly-silicon or diffused resistor, thus these devices can simulate a resistor in much smaller area.

Active resistor can be implemented by simply connecting the gate of NMOS or PMOS device to its drain as shown in the figure below:

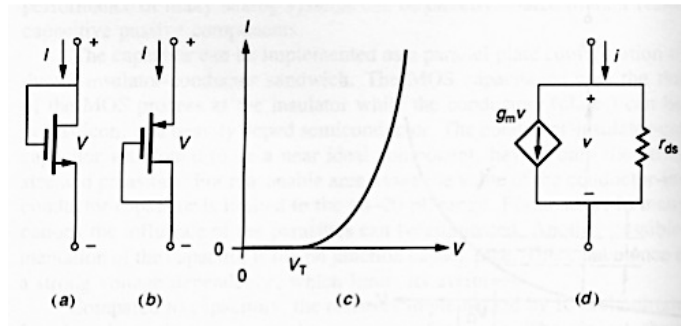


Figure 2. NMOS & PMOS as an active resistor

Where, the resistance offered by transistor is given as

$$r_o = \frac{1}{g_m + g_{mbs} + g_{ds}} \approx \frac{1}{g_m};$$

$$g_m = \sqrt{2k' \frac{W}{L} I_D}$$

Where;

I_D = Drain Current

g_m = Transconductance

$$k' = \mu_n \frac{\epsilon_{ox}}{t_{ox}}$$

$$W/L = \frac{\text{Width}}{\text{Length}} \text{ of transistor}$$

Theoretically Anticipated Values: We have to calculate R & C such that the cutoff frequency of the circuit is as specified (1 KHz). We know that MOS offers a very high resistance for gate voltages lower than threshold voltage. This result can be easily anticipated from the above trans conductance equation. When gate and drain of MOS are tied together the drain current is very low (~ 0 A) resulting in a very high resistance.

Let us arbitrarily choose C to be 10pF and calculate required resistance for LPF with f_c 1 KHz. The calculation below reveals that R is in orders of M ohm. This high resistance can be obtained by using sub threshold characteristics.

$$r_o = \frac{1}{2\pi f_c C}$$

$$r_o = \frac{1}{6.283 \times 10^{-8}}$$

$$r_o = 159.9 \text{ M}\Omega$$

We can equate trans conductance equation to obtain device parameters. However to get a better insight into device operation and non-ideal effect we will simulate MOS. We use trivial device parameters for our device ($KP = 25\mu$, $W = 50\mu\text{m}$, $L = 2.5\mu\text{m}$, $V_{TO} = 0.7\text{V}$, $LAMBDA = 0.005$) and simulate MOS in *HSPICE*. Results from simulation indicated that $g_m = 80.0259\text{n}$, which results in $r_o = 12.49 \text{ M}\Omega$.

We can now adjust the value of C such that we can obtain desired cutoff frequency of 1 KHz. By equating equation for the cutoff frequency we obtain $C = 12.7365\text{pF}$. For simplicity we use $C = 12.5 \text{ pF}$.

Thus for the given r_o of $\sim 13\text{M}\Omega$ we will have $C \sim 12.5\text{pF}$. We can now simulate LPF circuit by using these parameters. However proper connection of various nodes of MOS is essential to get correct result. We have to tie body to source to eliminate body effect.

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *HSPICE*.

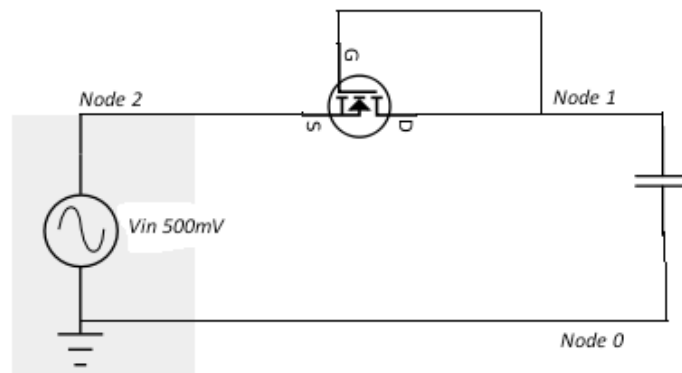


Figure 5. LPF as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions:

Frequency	Input Voltage	Deviation	Gain	R	C
Desired	1KHz	-	- 3 dB	13M ohm	12.73pF
Obtained	1.019KHz	19.40 (+1.9%)	0.486	12.5M ohm	12.50pF

Table 4. Deviations of F_c from desired values

It is clear from the above data that the observed error is negligible and depends on precision of fabricating these devices.

Conclusion: Low pass filter using active resistor was designed and simulated using SPICE Level 1 model in *HSPICE* successfully. Results obtained from these simulation show the Gain vs. Frequency plot and are in good accordance with theoretical analysis.

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*****Low Pass Filter Using*****
*****MOS Active Resistor*****
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***Low Pass Filter using MOS Active Resistor ***
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*****
*****This Project is listed under Analog & Mixed Signal VLSI*****
*****
***Circuit parameters are given as :--> ***
*** ***
*** ***
***-->1. M1 = Model 'NMOS' ***
***-->2. C = 12.5 pF ***
***-->3. ro = 13.0 Mega ohm \\ Simulated Resistance MOS \\ \\ Active\\ ***
***-->4. Fc = 1.00 KHz \\ Filter Cutoff Frequency \\ \\ Active\\ ***
*****
***Output results :--> ***
***Obtain requested Low Pass filter and verify results. ***
***The cut-off frequency must be within +/- 5% of the given value ***
*****
*****SPICE-Code*****
** Input Voltage AC (Vin=500mV)
Vin 2 0 AC 500mV
**MOS (NMOS) as a resistor with W/L=20
M1 1 1 2 2 NMOS L=2.5u W=50u
**Load Capacitor
CL 1 0 12.5pF
**MOS Model (VT0= Threshold Voltage, KP=u.cox LAMBDA=1/Va)
.MODEL NMOS nmos (VT0= 0.7V KP=25u LAMBDA=0.005)
** Set output conditions for simulation analysis
.OP
** Set Analysis required (AC) from 10Hz to 10^6 Hz
.AC DEC 20 1HZ 1000000HZ
** Set print variables (These variables will be stored in the output log)
.PRINT V(1,0)
** Terminate all sequences and end simulation
.END

```

