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Comparator

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Implementation of Comparator using Op-Amp (LM741)

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Documentation And Reference

Analog and Mixed Signal VLSI Design

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Aim: The primary purpose of this project is to design a comparator circuit using *Op-Amp* in SPICE. *SPICE* is industry standard software to design and simulate electrical circuits. It is derived from original SPICE program where, SPICE is acronym for ***S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis*.

Design Parameters: This project deals with implementation of *Op-Amp* as a comparator. As specified by the circuit we have following parameters available:

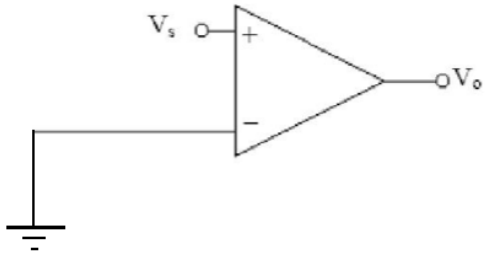


Figure 1. Circuit implementation of Op- Amp as Comparator & Ground as reference

Circuit parameters are as follows:

Parameter	**Value**	**Unit**	**Specification**
V_s	2.5 @ 1KHZ	V	AC SIN Input Voltage
Op- Amp Biasing Parameters			
Parameter	**Value**	**Unit**	**Specification**
LM741	-	-	Sub circuit from National Semiconductors
V_{cc} (V+)	12	V	Positive Bias Voltage
V_{ee} (V-)	-12	V	Negative Bias Voltage

Table 1. Circuit Parameters

Required Output: We are required to observe and verify that the output is a square wave. Moreover we have to observer difference in period if any.

Theoretical Analysis: A comparator is a simple circuit that compares two input signals and outputs a discreet signal indicating which one of them is larger. Comparators uses the high open loop-gain property of *Op- Amps* and thus are extremely sensitive to small variation in input voltage. Generally reference signal is supplied on one of the inputs of *Op- Amps* and the other input signal is compared to it. Output signal is in accordance with the input terminal (inverting or non-inverting).

In the given design problem V_{ref} is taken as ground. Thus for all the values of input signal that are greater than V_{ref} the output will be V+ (open loop gain $\approx \infty$). When input signal drops below the V_{ref} output signal will also drop to V-. Thus resulting in a square wave. For a periodic signal the input and output period should be same as output closely follows variation in input signal.

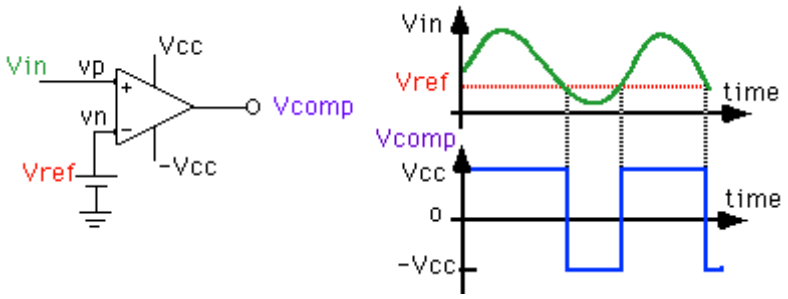


Figure 2. Theoretically anticipated output

Theoretically anticipated values: Ideally the output from comparator is V_{cc} & V_{ee} for any input voltage greater or smaller than V_{ref}. However, due to offset voltage, current and other non-ideal effects the output voltage will be smaller. We will call this error and attribute it to non-ideal behavior of Op- *Amp*.

Voltage Source	**V_s Input Voltage**	**V_o Output Voltage**	**Unit**
V_s (AC)	$0 < V_s \leq 2.5$	+12	V
	$-2.5 \leq V_s < 0$	-12	V

Table 2. Theoretically anticipated output voltages

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

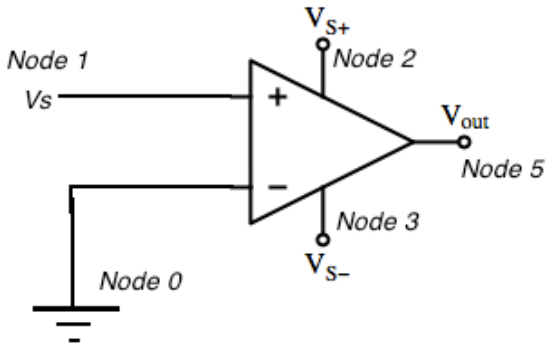


Figure 3. Comparator as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions:

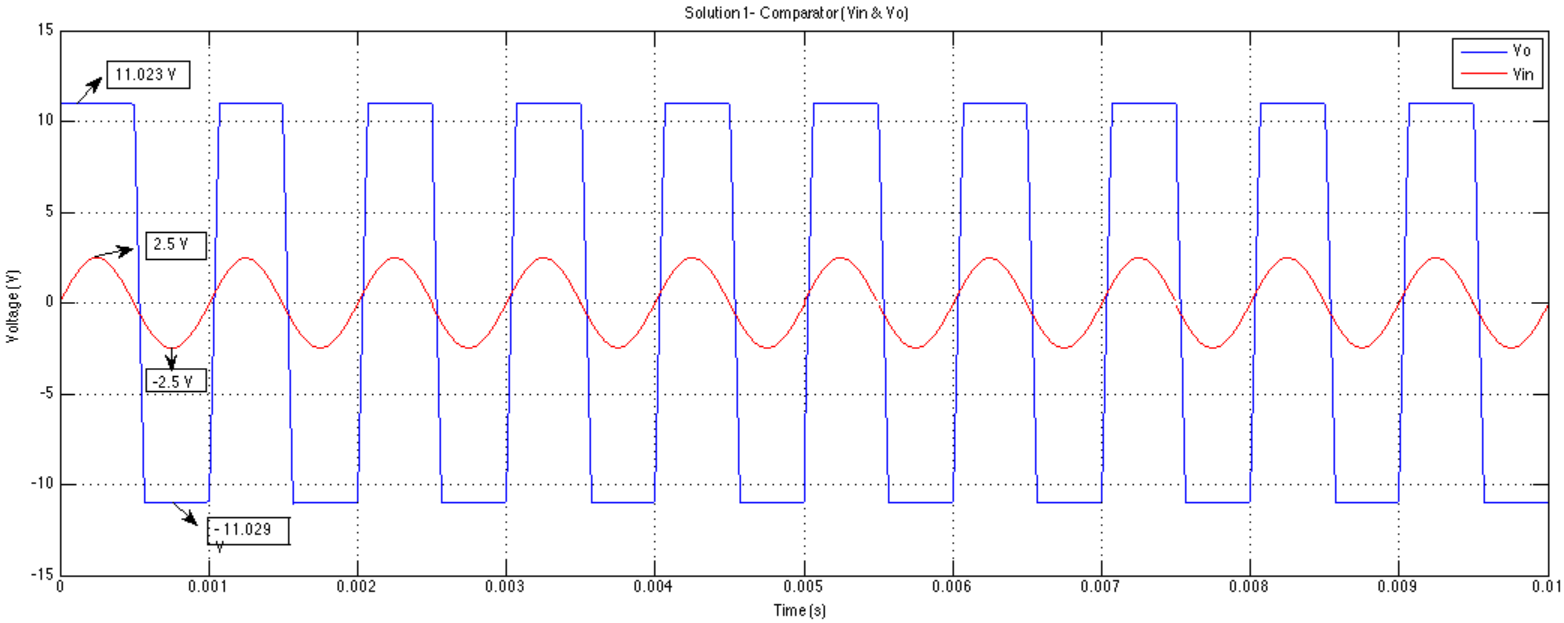
Frequency	Input Voltage	Predicted Output Voltage (Peak)	Actual Output Voltage (Peak)	Error (V Peak)
2.5V @1KHz AC	2.5	12	11.023	0.977 ≈ 1
	-2.5	-12	-11.029	-0.971 ≈ -1

Table 3. Deviations of V_s from predicted values

It is clear from the above data that the observed error is ± 1 V and can attribute it to non-ideal behavior (saturation) of Op- *Amp.*

Conclusion: The circuit for Comparator was designed and simulated in *HSPICE* successfully. Following conclusions can be drawn from simulation:

- The observed error is small and can attribute it to non-ideal behavior of Op- *Amp.*
- The output signal is a square wave as expected.
- Period of output signal is same as input signal.


Solution 1- Comparator (Vin & Vo)
Vo
Vin
11.023 V
2.5 V
-2.5 V
-11.029 V
Voltage (V)
Time (s)
15
10
5
0
-5
-10
-15
0
0.001
0.002
0.003
0.004
0.005
0.006
0.007
0.008
0.009
0.01