Spring 14

Audio Amplifier

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Documentation And Reference

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Analog and Mixed Signal VLSI Design

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Aim: The primary purpose of this project is to design a *two channel audio amplifier* in SPICE. Circuit topology including elements and their values can be freely selected. *HSPICE* is industry standard software to design and simulate electrical circuits. It is derived from original SPICE program where, SPICE is acronym for ***S**imulation **P**rogram with **I**ntegrated **C**ircuit **E**mphasis*.
We are provided some specs for amplifier, our task is to design amplifier within these specs.
The specs for the amplifier are as given below:

- The input can be stereo or mono from any low impedance audio source. Furthermore, it should not exceed maximum voltage level of 250mV peak.
- The overall system should be able to drive two 8-Ohm speakers. Minimum and maximum gain of the overall stage should correspond to –3dB and 20dB. This corresponds to 0.7V/V and 10V/V in terms of amplitude.
- Furthermore, there can be no more than a +/- 1 dB gain difference over the audible range of 300Hz 10 kHz without any distortion.
- Each channel should be able to control volume digitally, with three input bits on each channel and there must be 4-stage LED indicators corresponding to 0.25V, .5V, 1V, and 2V output levels for each channel as well.
- The system should be able to run from the normal household wall socket supply of 120 VRMS at 60Hz

Finally we have to observer and plot the output voltage across 8-ohm load resistance. Furthermore, we have to observer deviation from desired specs.

Sections: The design problem is divided into five problems that are further dividend into subsections:

- Power Source.
- Volume Control.
- Voltage Amplifier.
- Power Amplifier
- LED Display

We design each of these modules separately and then interface them together to obtain whole system. As specified in design problem, metric of device for integration is specified at the end of report.

Power Source

Design Parameters: This part of audio amplifier deals with implementation of constant power supply. As specified by the circuit we have following parameters available:

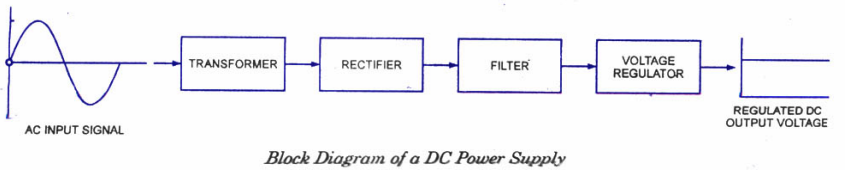


Figure 1. Block diagram of DC power supply

Circuit parameters are as follows:

Parameter	Value	Unit	Specification
V_{in}	120 VRMS @ 60 HZ	V	AC SIN Input Voltage
Output Voltages required			
Parameter	**Value**	**Unit**	**Specification**
V_{out}	+/- 15	V	Regulated DC output

Table 1. Circuit Parameters

Required Output: We will observe and verify that the output is constant and maintained at +/- 15 V without too much ripple. Moreover, we have to make sure that response time (rise and

fall time) of power supply should be small.

Theoretical Analysis: Power supply is a simple circuit that generally draws input from household sockets and converts it to desired output. Power supplies as shown in figure 1 consists of input transformer, rectifier circuit, filter network and voltage regulators. The input transformer is generally a step down or center tap transformer depending on the specific needs of the design. Rectification circuit does converts input AC signal to DC. This circuit generally employs bridge rectifier, as they are more efficient than other rectification networks. Filter network comprises of ripple rejection capacitors for rectification. Finally, constant voltage regulators can be employed to maintain output voltage precisely controlled.

We follow this design methodology for our power supply. Since we will utilize op-amps (741 IC's) in various parts of our design, we design our power supply to drive +/- 15 V. Op-Amps can be safely driven using only 12 V, however this high voltage is utilized in power amplifier stage to provide good current amplification

Theoretically anticipated values: Ideally the output voltage should not vary at all. However, we can expect some ripple in output voltage due to finite nature of circuit elements. However, due to offset voltage, current and other non-ideal effects the output voltage will be smaller. We will call this error and attribute it to non-ideal behavior of Op- *Amp*.

Voltage Source	**V_{in} Input Voltage**	**V_o Output Voltage**	**Unit**
V_{in} (AC)	120 VRMS @ 60 Hz	+15	V
		-15	V

Table 2. Theoretically anticipated output voltages

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

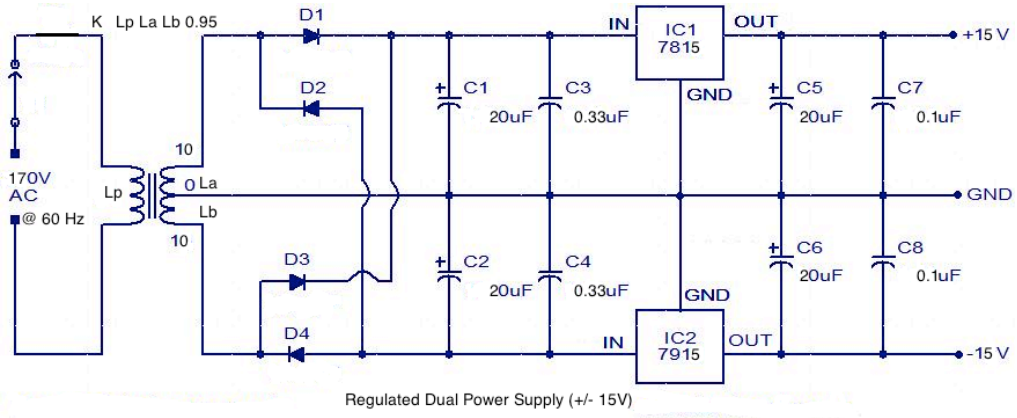


Figure 3. Regulated power supply as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions:

Input Voltge	Predicted Output Voltage (Peak)	Actual Output Voltage (Peak)	Error (V Peak)
120VRMS @60 Hz AC	15	14.958	0.042
	-15	-14.987	-0.013

Table 3. Deviations of V_{out} from predicted values

It is clear from the above data that the observed error is negligible and can attribute it to non-ideal behavior of circuit elements.

Conclusion: The circuit for Power Supply was designed and simulated in *HSPICE* successfully. Following conclusions can be drawn from simulation:

- The observed error is small and can attribute it to non-ideal behavior of circuit elements and ripple.
- The output signal is maintained at DC +/- 15V as expected.
- The response time is around 5 ms.

Fabrication parameters: The circuit elements used in designing power supply are economic and easily fabricated on IC. No large resistances were used thus promoting fabrication. However, excess power dissipated in voltage regulators should be dissipated efficiently by suitable heat sink.

Volume Control

Design Parameters: This part deals with designing volume control. This stage of amplifier circuit will take input audio signal and pre-process it according to the requirements of the amplifier gain. As specified by the problem we have following specs:

Parameter	Value	Unit	Specification
Gain	-3 ~20	dB	Output gain
Voltage	0.7~10	V	Output Voltage
To provide precious gain control we employ a constant gain voltage amplifier circuit. Thus the gain of this stage is modified accordingly.			
Volume control Parameters			
Parameter	**Value**	**Unit**	**Specification**
LM741	-	-	Sub circuit from National Semiconductors
V_{cc} (V+)	15	V	Positive Bias Voltage
V_{ee} (V-)	-15	V	Negative Bias Voltage
$R_{constant}$	14.28	K	Constant resistance
R1	7.96	K	Bit 1 resistance
R2	3.85	K	Bit 2 resistance
R3	1.92	K	Bit 3 resistance
Rf	1	K	Feedback resistance

Table 1. Circuit Parameters

Required Output: The volume control must be able to provide voltage levels from 0.07~ 1V (as next stage is voltage amplifier with constant gain of 10). The volume control is essentially a DAC circuit that convers digital input from user to an audio volume level. Linear gain in volume is verified by implementing circuit in *HSPICE*.

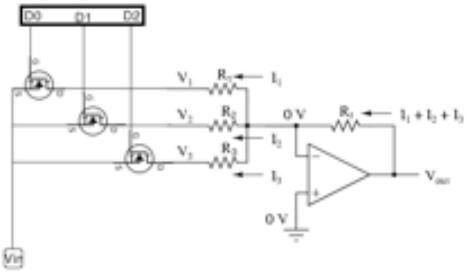


Figure 1. Circuit of DAC volume control with PMOS switches with Inverting Amplifier

Theoretical Analysis: Since maximum and minimum voltages were defined by design specs, we implemented this circuit to preciously satisfy those constrains. The above implementation of Op- *Amp* is an inverting amplifier with feedback and the transfer function as shown below:

$$i = \frac{V_s - V_o}{R_1 + R_2}$$

$$\therefore i = \frac{V_s - V_a}{R_1} = \frac{V_a - V_o}{R_2}$$

$$\therefore A_V = \frac{V_o}{V_s} = -\frac{R_2}{R_1}$$

$$V_o = -V_s\left(\frac{R_2}{R_1}\right)$$

Where V_a is inverting input voltage at *Op-Amp*. The designed resistance values provided following voltage gains.

Input Bits	Value (-ve)	Specification
000	0.07	Voltage Gain level at "000"
001	0.2	Voltage Gain level at "001"
010	0.33	Voltage Gain level at "010"
011	0.46	Voltage Gain level at "011"
100	0.59	Voltage Gain level at "100"
101	0.72	Voltage Gain level at "101"
110	0.85	Voltage Gain level at "110"
111	0.98	Voltage Gain level at "111"

Table 2. Volume Gain Parameters

Theoretically Anticipated Values: The gain of given circuit is -ve. The –ve sign indicates that the output will be 180° phase shifted wrt input. Following table shows the theoretically anticipated values:

Input Bits	Value (-ve)	Input Voltage	Output Voltage	Specification
000	0.07	250 mV	0.0175 V	Voltage Gain level at "000"
001	0.2	250 mV	0.050 V	Voltage Gain level at "001"
010	0.33	250 mV	0.0825 V	Voltage Gain level at "010"
011	0.46	250 mV	0.115 V	Voltage Gain level at "011"
100	0.59	250 mV	0.1475 V	Voltage Gain level at "100"
101	0.72	250 mV	0.180 V	Voltage Gain level at "101"
110	0.85	250 mV	0.2125 V	Voltage Gain level at "110"
111	0.98	250 mV	0.245 V	Voltage Gain level at "111"

Table 3. Theoretically anticipated output voltages

However, due to offset voltage, current and other non-ideal effects of op-amp the output voltage will be affected. We will call this error and attribute it to non-ideal behavior of *Op-Amp.*

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

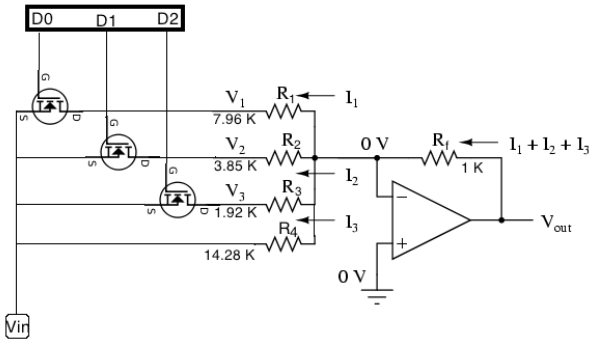


Figure 2. Circuit of DAC volume control with MOS switches as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions:

Voltage Source	V_s Input Voltage (Peak)	A_v Gain	V_o Output Voltage Predicted (Peak)	V_o Output Voltage (Peak)	Error
Vaud	250 mV	0.07	0.0175 V	0.0170 V	0.0005
	-250mV	0.98	0.245 V	0.239 V	0.006

Table 4. Deviations of V_o from desired values

There are small variations in gain offered by op-amp, however overall these values are in good accordance with the anticipated values. It is clear from the above data that the observed error is negligible and depends on non-ideal effects in these devices.

Conclusion: Volume control circuit involving inverting amplifier with negative feedback and PMOS switches was designed and simulated using HSPICE. Results obtained from these simulations are in good accordance with theoretical analysis. Following conclusions can be drawn from simulation:

- The observed offset is small and can attribute it to non-ideal behavior of Op- *Amp.*
- The output signal is 180° out of phase wrt input signal as expected.
- Gain is as expected.
- This stage will be just copied to supply two volume controls for stereo and mono input.

Fabrication parameters: The circuit elements used are economic and easily fabricated on IC. No large resistances were used thus promoting fabrication. However, PMOS logic is used to provide good pull up to digital volume control bits. This inverts the logic values, thus either an inverting stage of NMOS of suitable size should be used.

Voltage Amplifier

Design Parameters: This part deals with designing voltage amplifier. This stage of amplifier circuit will take input from volume control circuit and processes it according to the requirements of the amplifier gain. As specified by the problem we have following specs:

Parameter	Value	Unit	Specification
V_s	0.0175 ~0.245	V	Audio Input Voltage
V_{out}	0.175 ~2.5	V	Audio Output Voltage
Op- Amp Biasing Parameters			
Parameter	**Value**	**Unit**	**Specification**
LM741	-	-	Sub circuit from National Semiconductors
V_{cc} (V+)	15	V	Positive Bias Voltage
V_{ee} (V-)	-15	V	Negative Bias Voltage
Rf	10	K	Feedback resistance
R1	1	K	Input resistance

Table 1. Circuit Parameters

Required Output: The Voltage control must be able to provide overall voltage gain requested by the amplifier circuit. These levels are as shown in table above. The volume control is essentially a negative feedback amplifier circuit that amplifies input audio signal from volume control. Constant gain in voltage is verified by implementing circuit in *SPICE*.

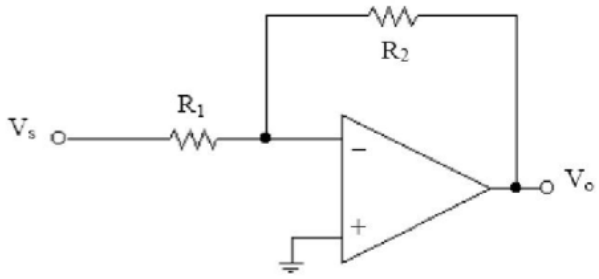


Figure 1. Circuit of Op- Amp as Inverting Amplifier with negative feedback

Theoretical Analysis: The above implementation of *Op-Amp* is an inverting amplifier with feedback. We can compute its transfer function as shown below:

$$i = \frac{V_s - V_o}{R_1 + R_2}$$

$$\therefore i = \frac{V_s - V_a}{R_1} = \frac{V_a - V_o}{R_2}$$

$$\therefore A_V = \frac{V_o}{V_s} = -\frac{R_2}{R_1}$$

$$V_o = -V_s\left(\frac{R_2}{R_1}\right)$$

Where V_a is inverting input voltage at Op- *Amp*. Thus the output voltage should have a constant gain of 10 as compared to the input signal.

Theoretically Anticipated Values: The gain of given circuit is -5. The –ve sign indicates that the output will be 180° phase shifted wrt input. Following table shows the theoretically anticipated values:

Voltage Source	V_s Input Voltage (Peak)	A_v Gain	V_o Output Voltage Predicted (Peak)
Vvol	0.0175 V	10	0.175 V
	0.245 V	10	2.45 V

Table 2. Theoretically anticipated output voltages

However, due to offset voltage, current and other non-ideal effects the output voltage can be affected. We will call this error and attribute it to non-ideal behavior of Op- *Amp.*

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

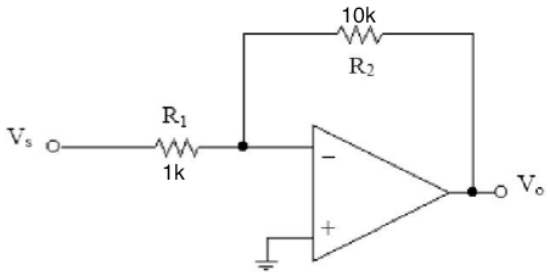


Figure 2. Non-Inverting Amplifier as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions:

Voltage Source	V_s Input Voltage (Peak)	A_v Gain	V_o Output Voltage Predicted (Peak)	V_o Output Voltage (Peak)	Error
Vvol	0.0175 V	10	0.175 V	0.168 V	0.007
	0.245 V	10	2.45 V	2.34 V	0.011

Table 3. Deviations of V_o from desired values

It is clear from the above data that the observed error is negligible and depends on non-ideal effects in these devices.

Conclusion: Voltage Amplifier was implemented as a non-inverting amplifier and simulated using HSPICE. Results obtained from these simulations are in good accordance with theoretical analysis. Following conclusions can be drawn from simulation:

- The observed error is small and can attribute it to non-ideal behavior of Op- *Amp.*
- The output signal is 180° out of phase wrt input signal as expected.
- Gain is as expected.
- This stage will be just copied to supply two voltage amplifiers for stereo and mono input.

Fabrication parameters: The circuit elements used are economic and easily fabricated on IC. No large resistances were used thus promoting fabrication. Moreover, LM741 model was used which is easily implement in integrated circuits.

Power Amplifier

Design Parameters: Fourth part deals with implementation of power amplifier to supply required current to the load speaker. As specified by the problem we have following specs available:

Parameter	Value	Unit	Specification
V_{in}	0.175 ~2.45	V	Audio Input Voltage signal from Voltage Amplifier
This stage should be able to provide required current to the load resistance			

Table 1. Circuit Parameters

Required Output: The Power Amplifier must be able to provide overall current gain requested by the amplifier circuit. The volume control is essentially a class AB amplifier with excellent current drive and efficiency. Current gain is verified by implementing circuit in *SPICE*.

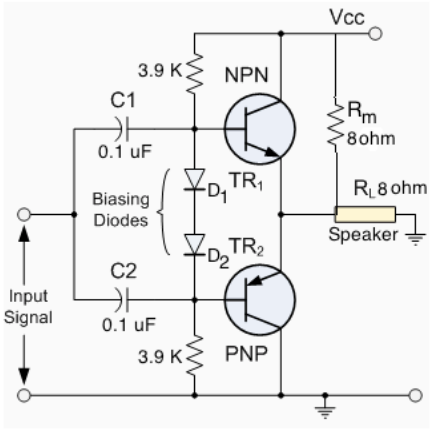


Figure 1. Power Amplifier Class AB

Theoretical Analysis: In the above circuit diode D1 & D2 provide necessary biasing needed to operate NPN & PNP BJT in correct region of operation. R_m is an 8-ohm resistance from power supply to speaker, which dc shifts output to required value. Small input capacitances are used to couple input signal from voltage amplifier. For best operation BJT's are perfectly match.

Theoretically Anticipated Values: Since the class AB power amplifier amplifies the current drive, we expect a gain in current. However input voltage is maintained as it is. This is the final stage of amplifier circuit and is feed to the 8-ohm resistors.

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

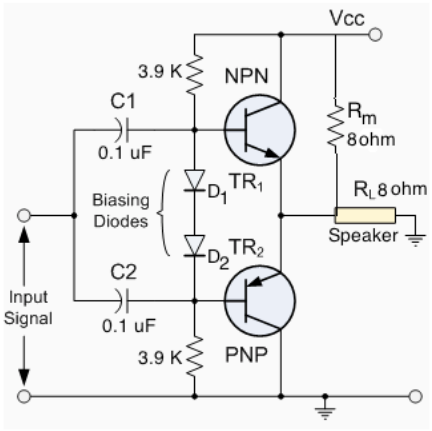


Figure 2. Power Amplifier as implemented in HSPICE

Error: We experienced a DC shift in output voltage and thus have to augment this shift by introducing a 8 ohms resistor from the power supply to the speaker. Apart from that there were no observed error and obtained values were in good accordance with theoretical analysis.

Conclusion: Power Amplifier was implemented as a class AB amplifier and simulated using HSPICE. Results obtained from these simulations are in good accordance with theoretical analysis. Following conclusions can be drawn from simulation:

- The observed error is small and can attribute it to non-ideal behavior of Op- *Amp.*
- The output signal follows changes in input signal closely as expected.
- Current gain is sufficient and delivers 4 W to the load resistance .
- This stage will be just copied to supply two volume controls for stereo and mono input.

Fabrication parameters: The circuit elements used are economic and easily fabricated on IC. No large resistances were used thus promoting fabrication.

However, BJT's along with PMOS (in the DPST switches) can be expensive. This is because the device migrates from analog domain to mixed signal domain.

LED Display

Design Parameters: Final part of problem deals with implementation of LED displays for both stereo and mono channels. As specified by the circuit we have following specs available:

Parameter	Value	Unit	Specification
LED1	0.25	V	Display voltage level
LED2	0.50	V	Display voltage level
LED3	1.00	V	Display voltage level
LED4	2.00	V	Display voltage level
Op- Amp Biasing Parameters			
Parameter	**Value**	**Unit**	**Specification**
LM741	-	-	Sub circuit from National Semiconductors
V_{cc} (V+)	15	V	Positive Bias Voltage
V_{ee} (V-)	-15	V	Negative Bias Voltage

Table 1. Circuit Parameters

Required Output: This problem requests to have 4-stage LED indicators corresponding to 0.25V, .5V, 1V, and 2V output levels for each channel. LED display is implemented by using comparator circuit and verified by implementing it in *HSPICE*.

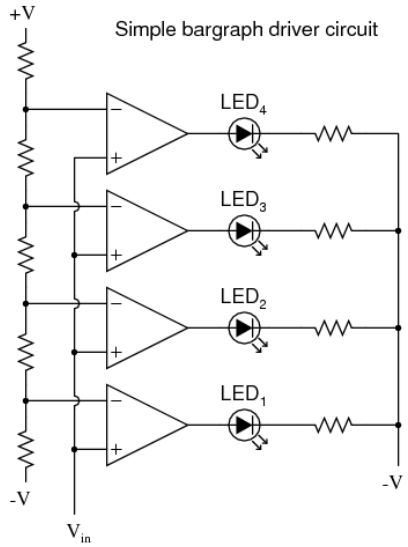


Figure 1. Circuit implementation of LED Display

Theoretical Analysis: The supply voltage is 15 V DC; reference voltages for op-amp will be obtained by dividing this voltage. Maximum and minimum voltages drop across the resistance ladder were defined by design specs.

Where V_{in} is input voltage from the power amplifier. The designed resistance values to provided required reference voltages are as follows:

Resistance	Value	Specification
R1	52 K	Voltage Drop of 13 V
R2	4 K	Voltage reference of 2V
R3	2 K	Voltage reference of 1V
R4	1 K	Voltage reference of 0.5V
R5	1 K	Voltage reference of 0.25V

Table 2. Voltage reference resistance ladder

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

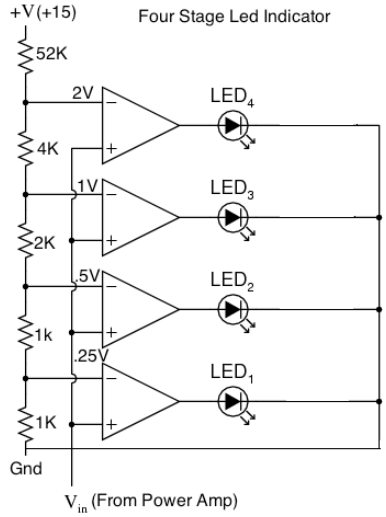


Figure 2. LED Display as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions. It is clear from the above data that the observed error is negligible and can attribute it to sampling of data.

Conclusion: LED Display was implemented as a comparator circuit and simulated using HSPICE. Results obtained from these simulations are in good accordance with theoretical analysis. Following conclusions can be drawn from simulation:

- The observed error is small and can attribute it to non-ideal behavior of Op- *Amp.*
- The LEDs have good response time and follows power amplifier circuits output closely as expected.
- This stage will be just copied to supply two volume controls for stereo and mono input.

Fabrication parameters: The circuit elements used are economic and easily fabricated on IC. No large resistances were used thus promoting fabrication. Moreover, LM741 model was used which is easily implement in integrated circuits.

Voltage Buffer instead of Power amplifier

Design improvements: It is observed that the op-amp voltage buffer has a unity gain and high current driving capabilities. Thus we can further improved on class AB amplifier by implementing voltage buffer. Following section deals with implementation of *Op*-Amp as a buffer. As specified by the problem we have following parameters available:

Parameter	**From**	**Unit**	**Specification**
V_{in}	Voltage Amplifier	V	Output Voltage Signal
Op- Amp Biasing Parameters			
Parameter	**Value**	**Unit**	**Specification**
LM741	-	-	Sub circuit from National Semiconductors
V_{cc} (V+)	15	V	Positive Bias Voltage
V_{ee} (V-)	-15	V	Negative Bias Voltage

Table 1. Circuit Parameters

Required Output: We observe the current available at the output of op-amp and verify it by implementing circuit in *HSPICE*.

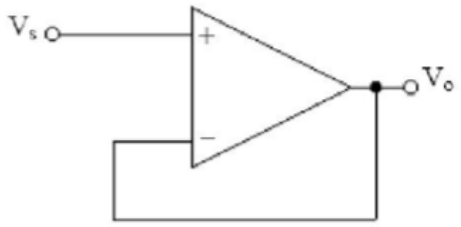


Figure 1. Circuit of Op- Amp Buffer

Theoretical Analysis: The above implementation of Op- *Amp* is a buffer. We can compute its transfer function as shown below:

$$V_a = \frac{R_1}{R_1 + R_2} \times V_o$$

$$\because V_a = V_s$$

$$\therefore \frac{V_o}{V_a} = \frac{R_1+R_2}{R_1}$$

$$\therefore A_V = \frac{V_o}{V_s} = \frac{R_1+R_2}{R_1}$$

$$V_o = V_s\left(\frac{R_1+R_2}{R_1}\right)$$

$$\because R_1 \rightarrow \infty \ \& \ R_2 \rightarrow 0$$

$$\therefore \frac{R_1+R_2}{R_1} = 1+0=1$$

$$\therefore V_o = V_s(1)$$

Where V_a is inverting input voltage at *Op- Amp*. Thus the output voltage should have a gain of 1 as compared to the input.

Theoretically Anticipated Values: Since the feedback resistor is equal to zero and input resistor is equal to infinity, the circuit will have a fixed gain of "1" as all the output voltage would be present on the inverting input terminal. This will then result in a special case of the non-inverting amplifier as a Voltage Follower or a buffer. The output voltage should be exactly same as input voltage with higher current drive. Moreover as the input signal is applied on the non-inverting terminal the output will have no phase shifted.

Nodal Circuit Diagrams: The circuit shown below is the nodal (representing 'nets') circuit as implemented in the *SPICE*.

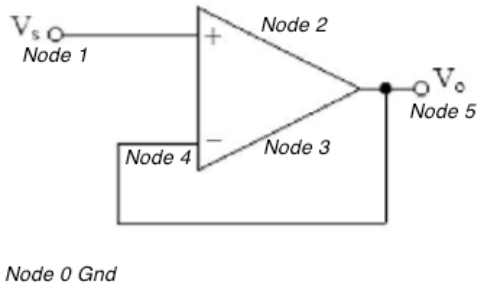


Figure 2. Non-Inverting Amplifier as a Buffer as implemented in HSPICE

Error: Table below shows the error in the output voltage as compared to the theoretical predictions:

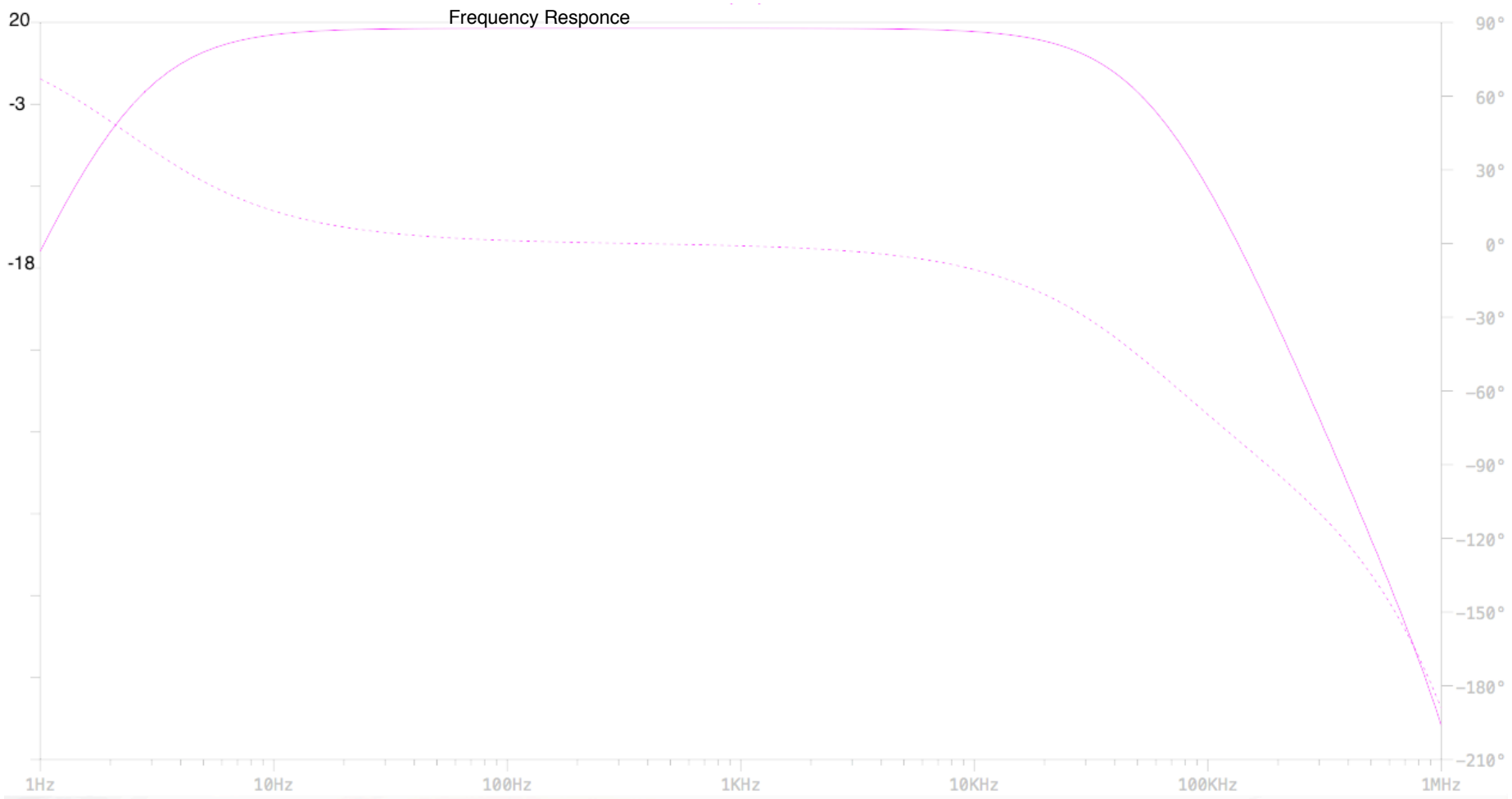
Voltage Source	**V_s Input Voltage (Peak)**	**A_v Gain**	**V_o Output Voltage Predicted (Peak)**	**V_o Output Voltage (Peak)**	**Unit**
V_s (AC)	2.5V	1	2.5	2.5	V
	0.175V	1	0.175	0.175	V

Table 3. Deviations of V_o from desired values

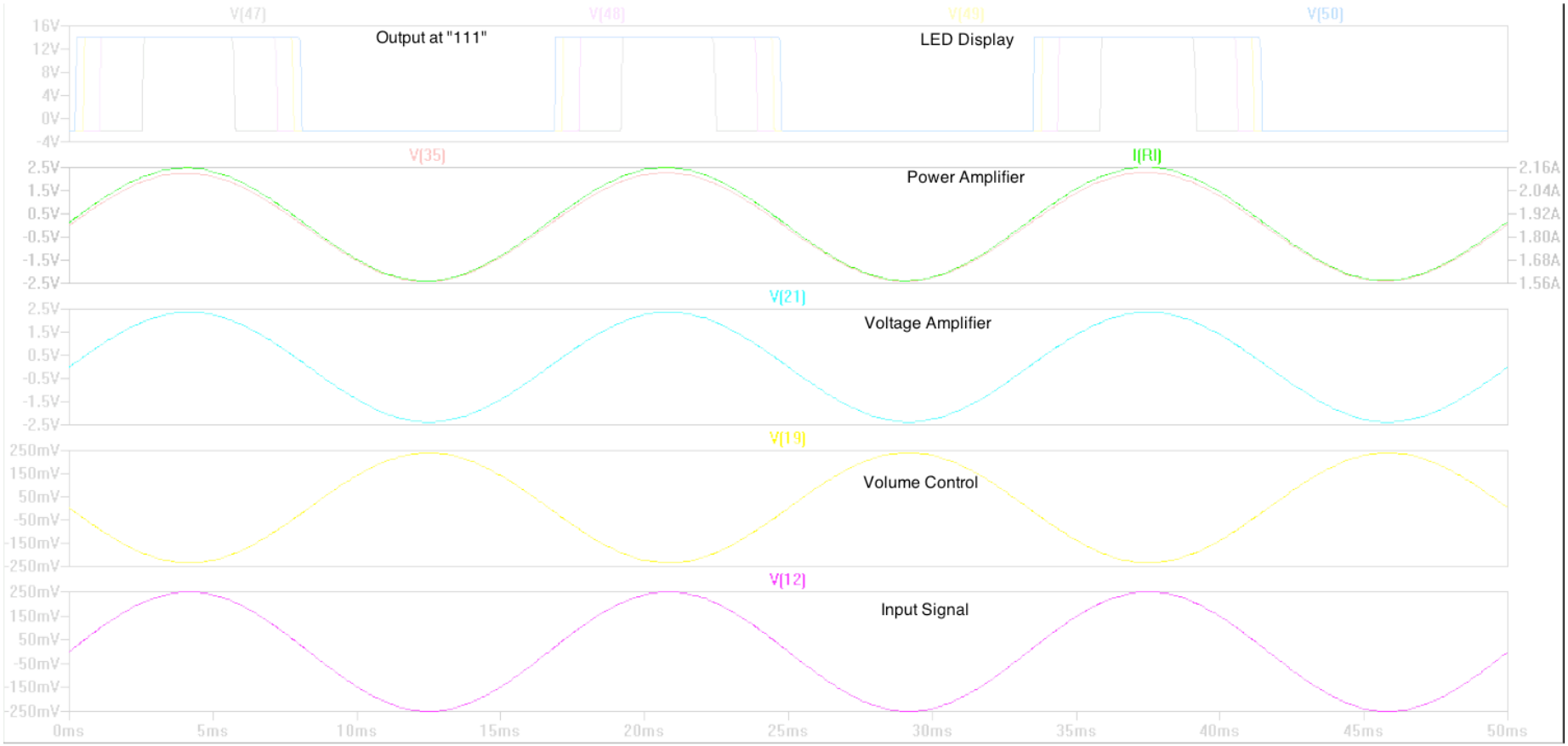
It is clear from the above data that there is no observed error and values are in good accordance with theoretical analysis.

Conclusion: Non-inverting amplifier as a buffer was designed and simulated using HSPICE. Results obtained from these simulations are in good accordance with theoretical analysis. Following conclusions can be drawn from simulation:

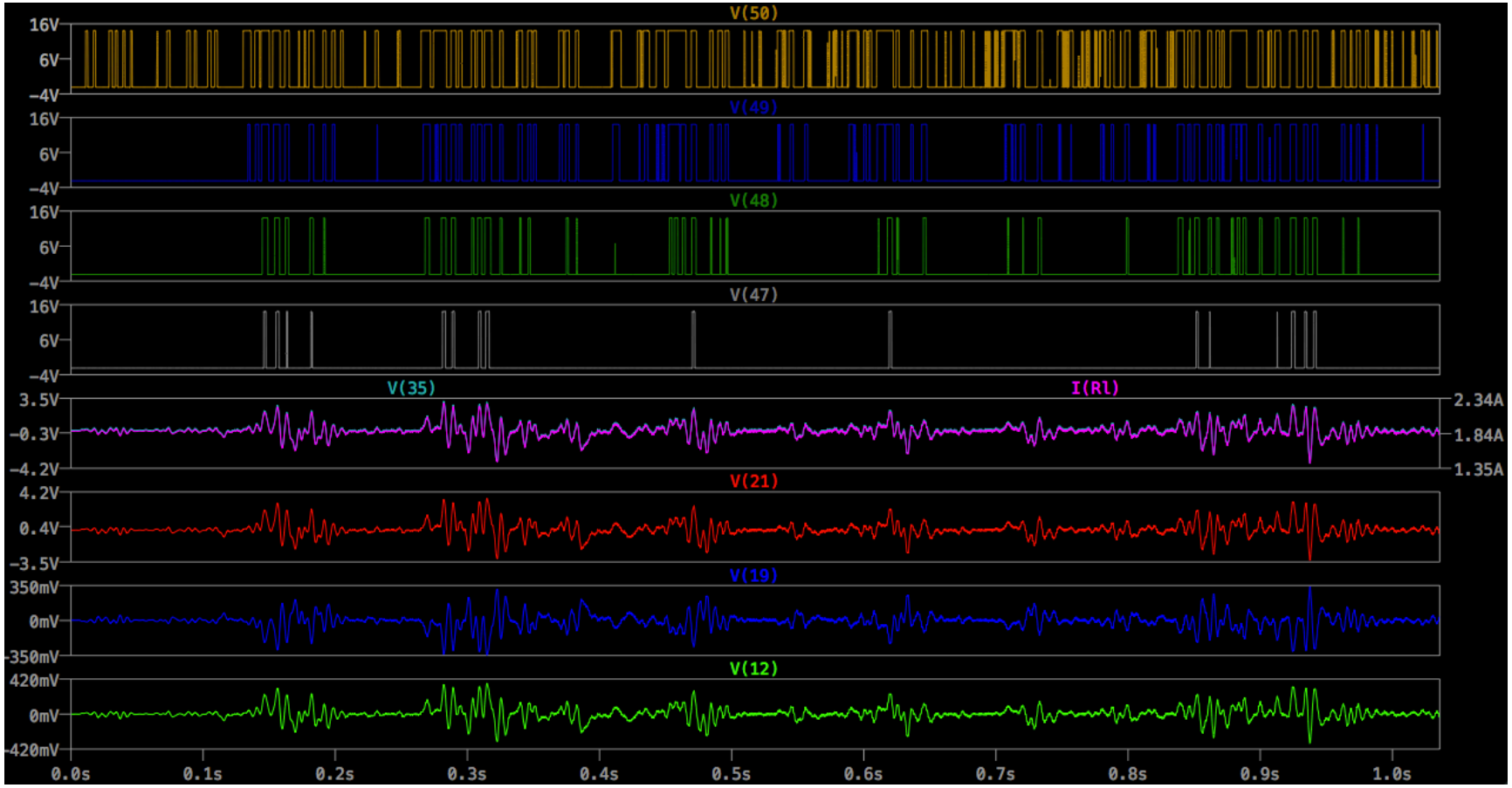
- There is no observed error.
- The output signal is in phase wrt input signal.
- Gain is $A_v = 1$.
- Current drive is good and 4 W of power is delivered to load.


Frequency Responce
20
-3
-18
90°
60°
30°
0°
-30°
-60°
-90°
-120°
-150°
-180°
-210°
1Hz
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz

Overall System Response



Overall System Response



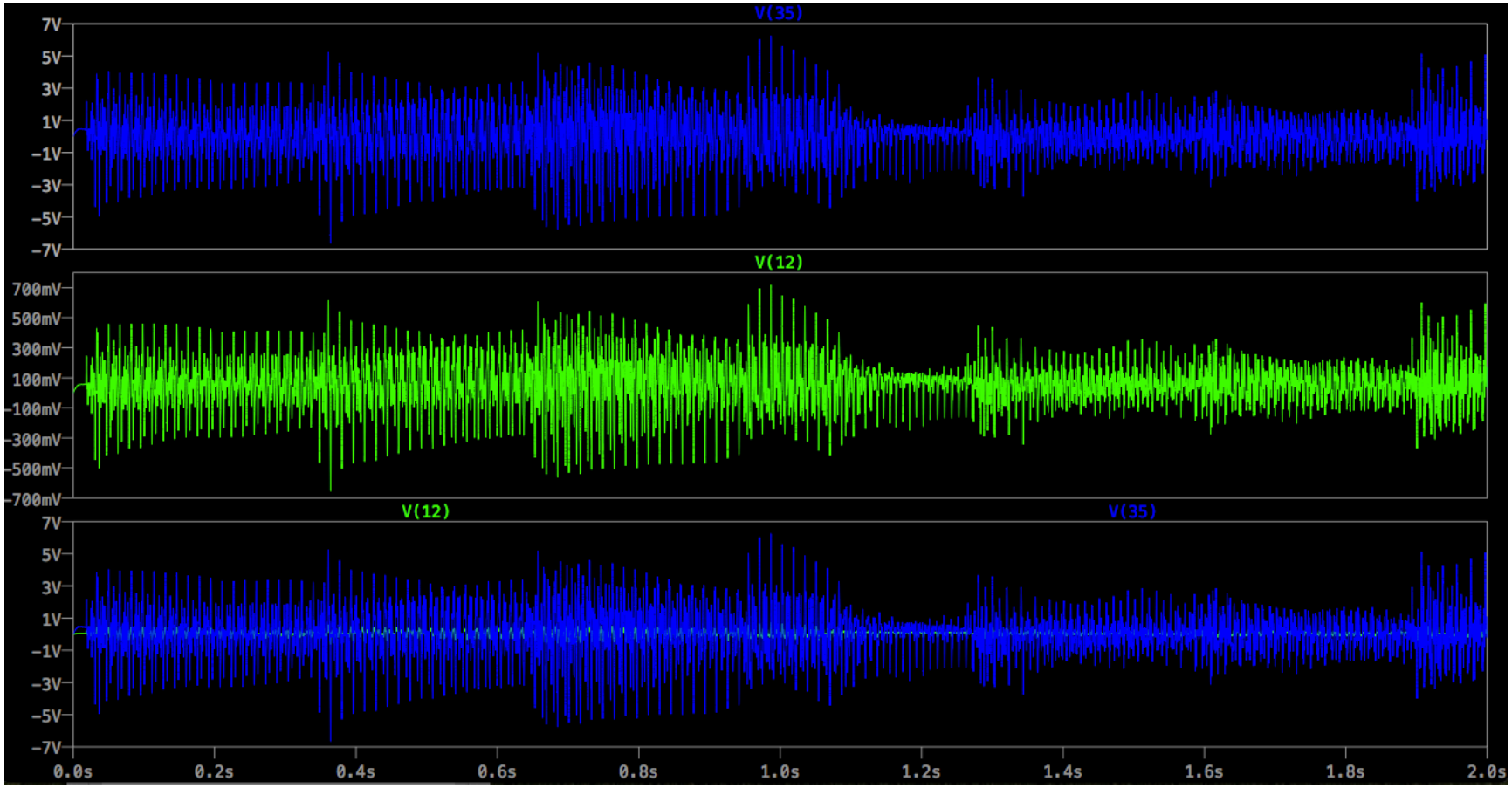
****
*** About Volume Control ***
****
Since Volume Control logic is implemented in PMOS following is volume agin:

I/P	LEVEL	GAIN
000	HHH	0.98
001	HHL	0.85
010	HLH	0.72
011	HLL	0.59
100	LHH	0.46
101	LHL	0.33
110	LLH	0.20
111	LLL	0.07

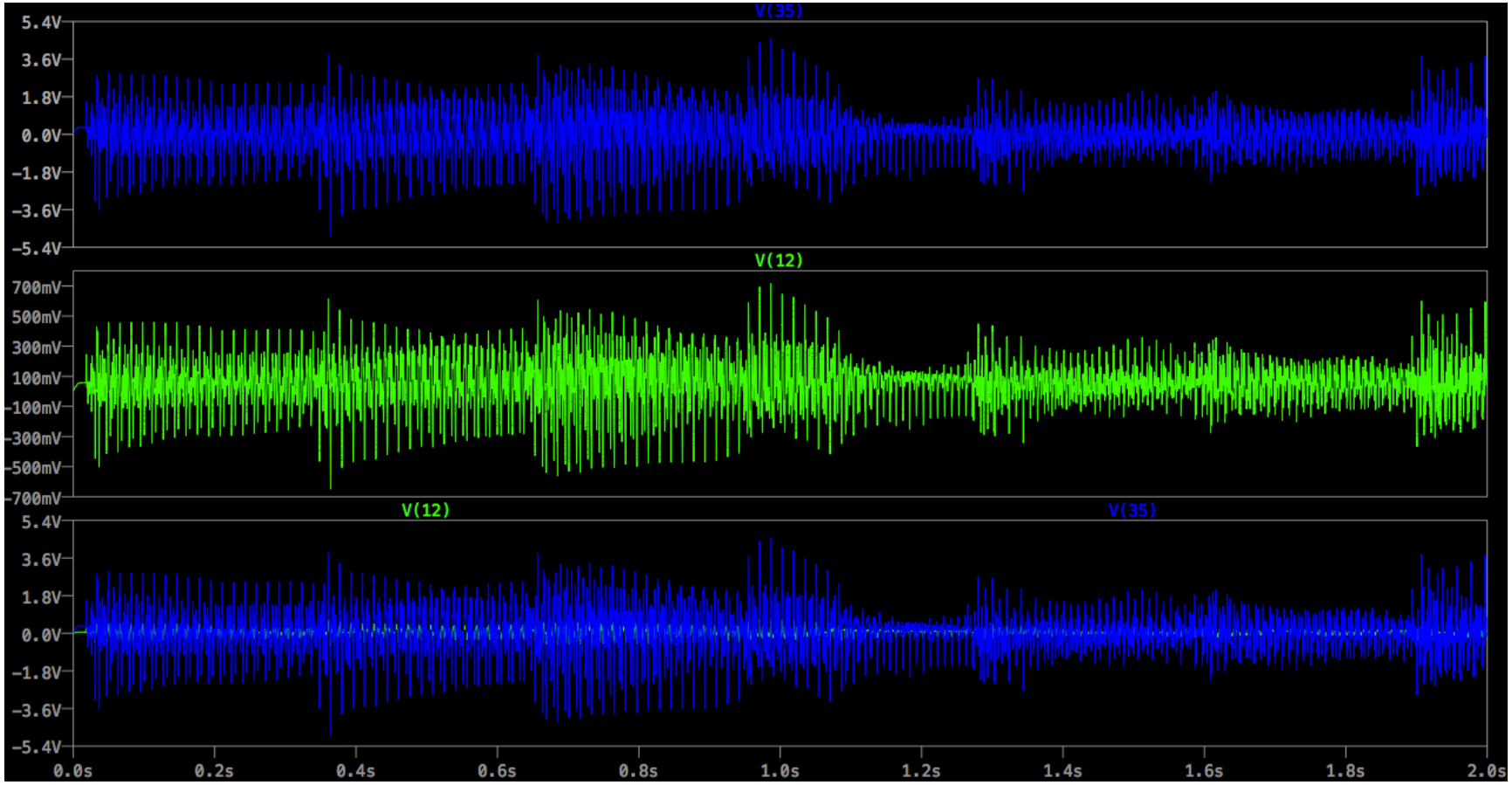
The observed distortion in output signal is due to absence of Pre-Amplification stage.
The Noise in raw signal is not rejected and is amplified accordingly.This can be improved on.

**********EOF**********

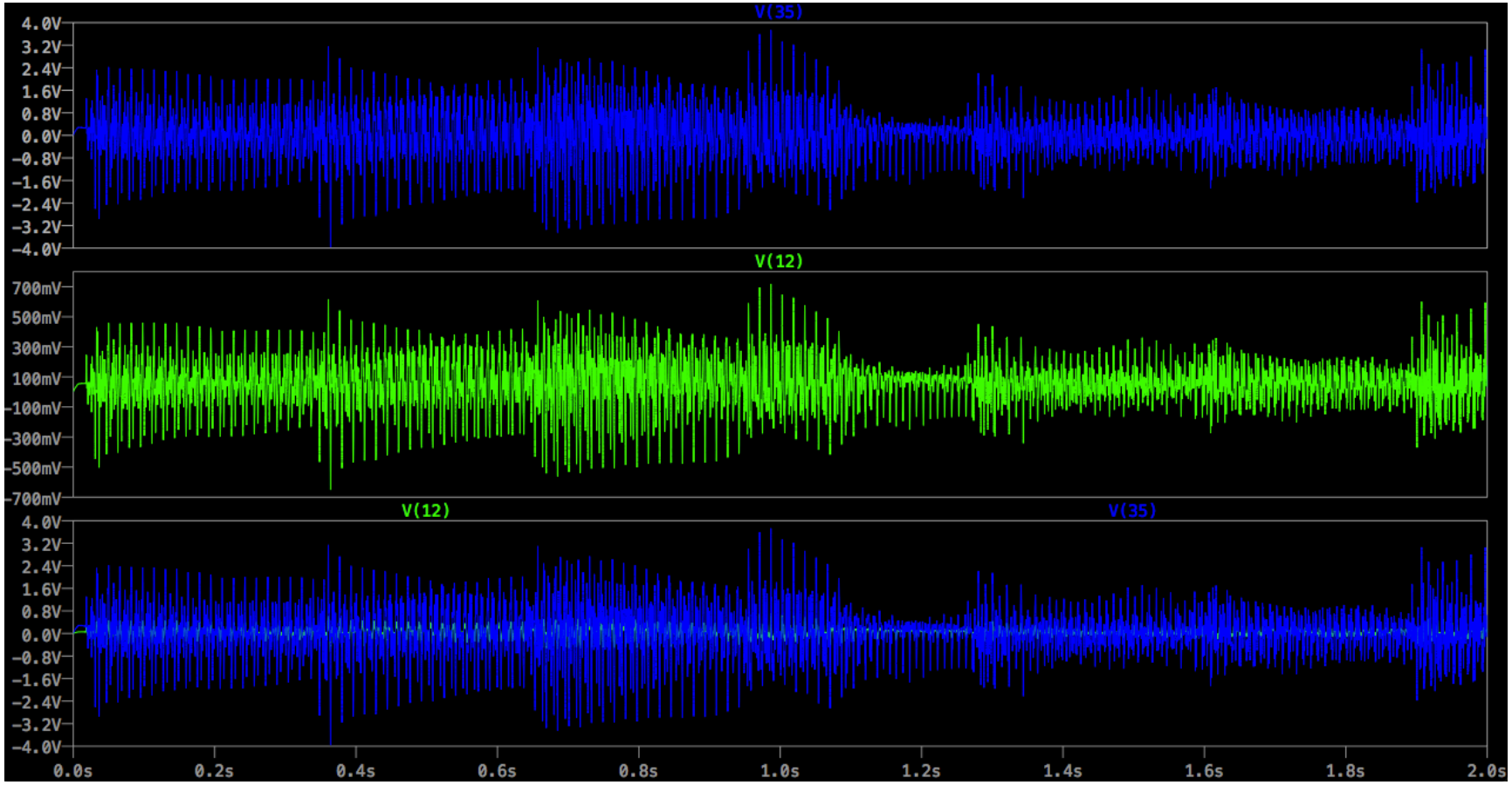
Output at “000”



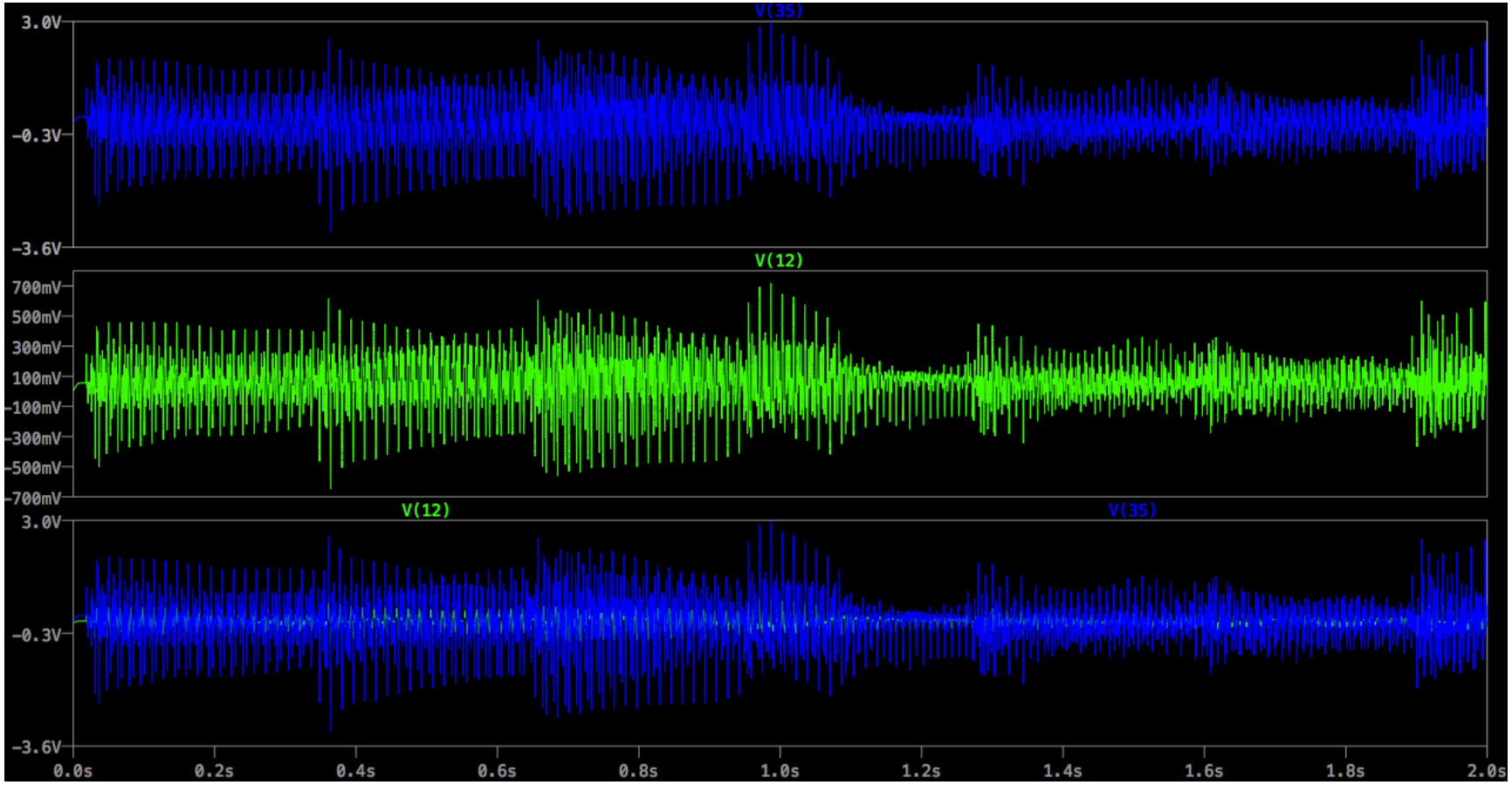
Output at “050”



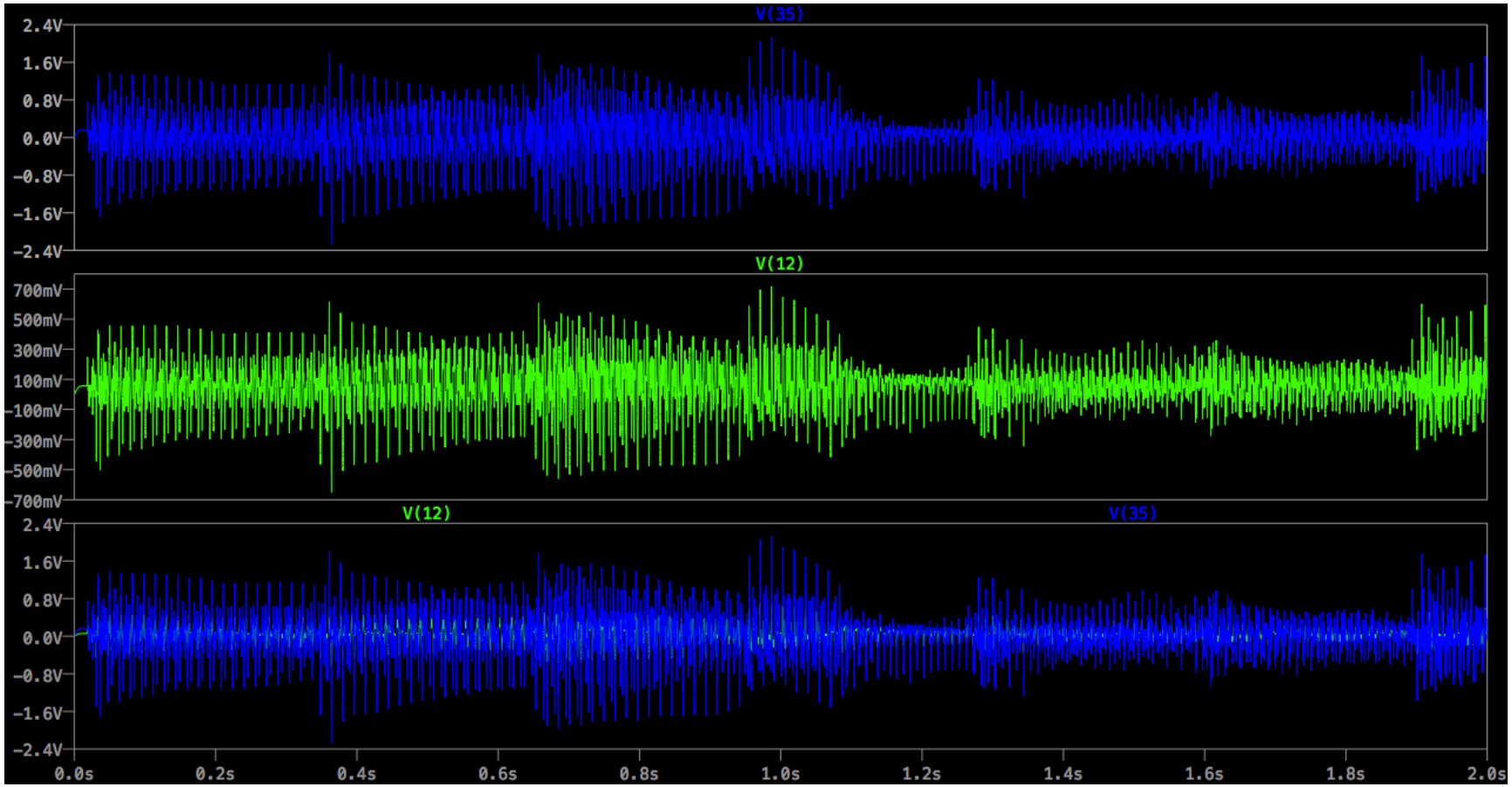
Output at “055”



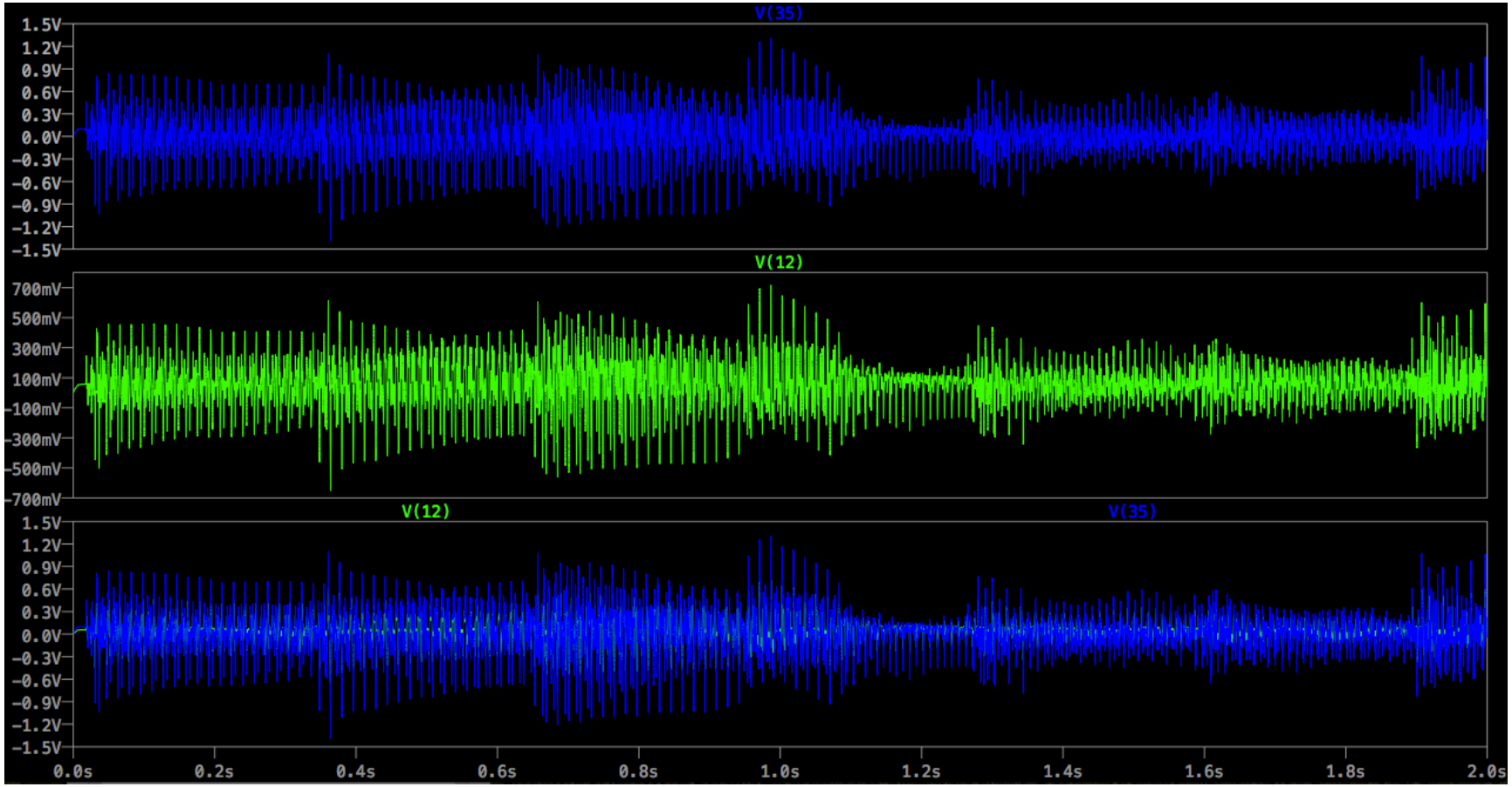
Output at “500”



Output at “505”



Output at “550”



Output at “555”