

IC DESIGN LAB-01

ASSIGNMENT REPORT

Name: Vivek Thakkar

Roll No. : 252VL037

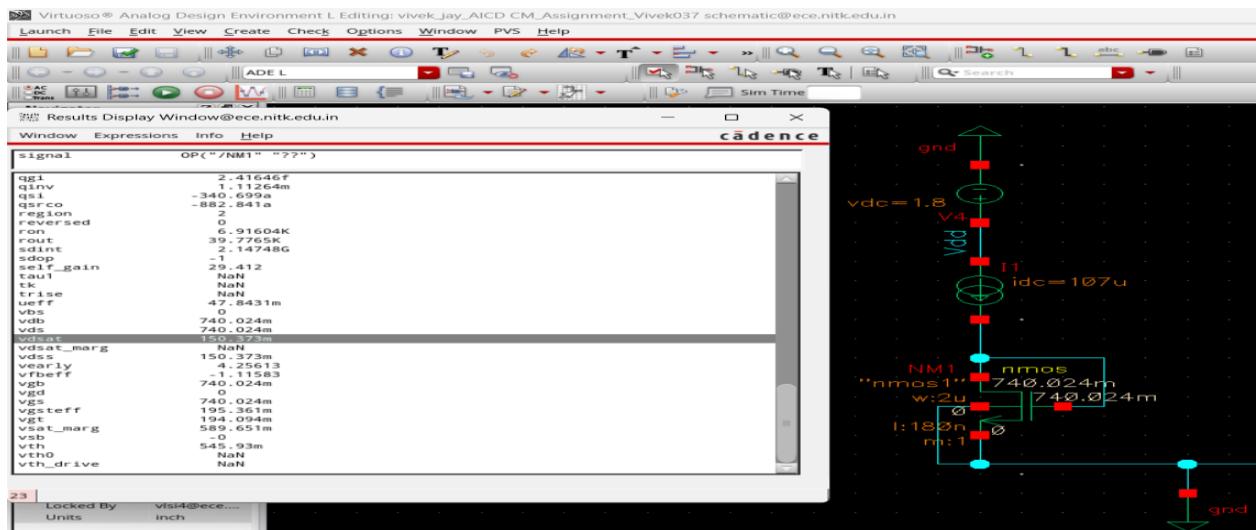
$I_{ref}=107 \mu A$ & Month of birth is November(11). So, $\alpha=2$.

Q.1 Design and simulate a NMOS based basic current mirror to mirror the given reference current I_{REF} and for the specified scaling factor.

→ First of all iterative method was used to find width of NMOS such that $V_{dssat} = 150 \text{ mV}$ with keeping $I_{ref}=109 \mu A$.

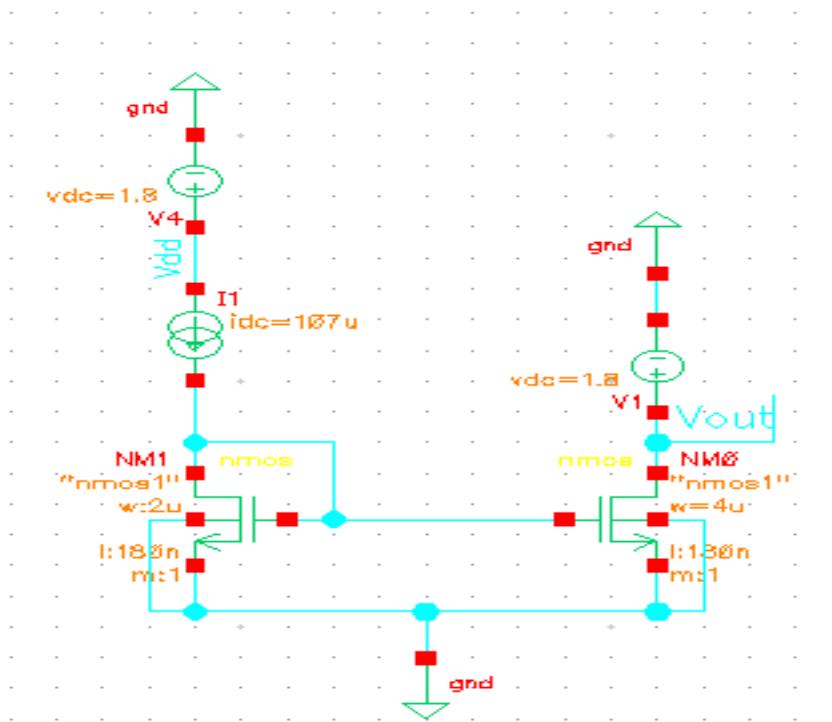
Resultant width for NMOS which satisfied above conditions

= 2 μm .



Here, as an operationg point: $V_{gs}=V_{ds}=740.024 \text{ mV}$.

→ Based on this width and for $\alpha=2$ (width of second NMOS becomes twice, means we use 2 fingers of width $2 \mu\text{m}$), Schematic diagram of NMOS based basic current mirror is:

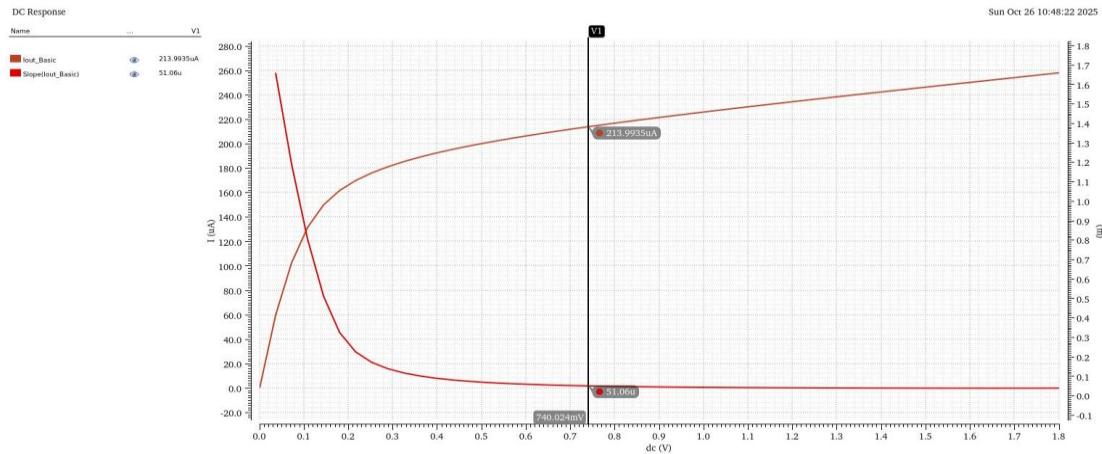


- Plot the static I-V characteristic of the designed current source.
- From the characteristic, find the resistance of the designed current source at the operating point $V_{DS} = V_{GS}$. Compare it with the resistance obtained using DC operating point simulation.

→ Sweeping V_{out1} ($V1$) from 0 to 1.8V and measuring current through drain of NM0 to get the static I-V characteristic of the designed current source.

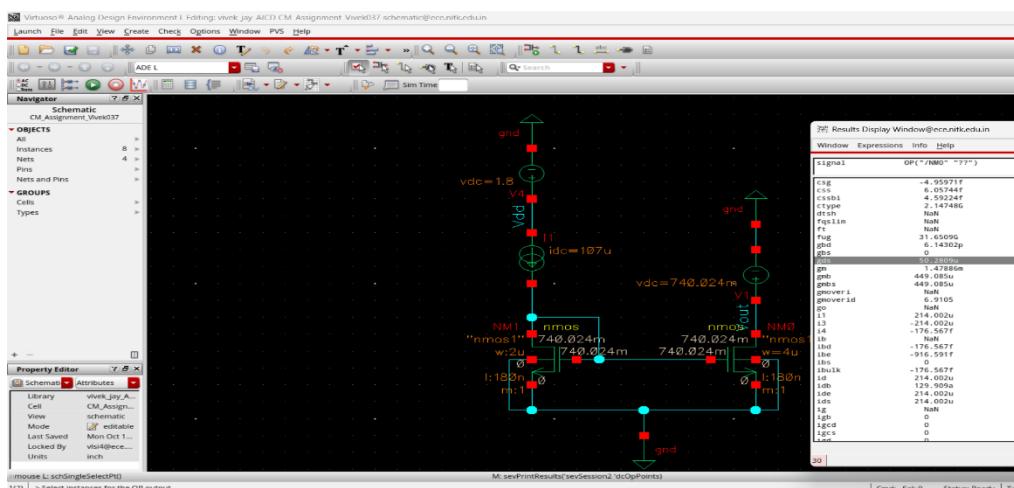
→ Used “deriv” function to differentiate the waveform of the I_{out} with respect to V_{out} to get the waveform which contains values of inverse of output resistance. At $V_{ds}=V_{gs}=740.024$ mV value from that waveform is inverse of the simulated output resistance.

→ Waveform of the static I-V characteristic:



→ At $V_{ds}=V_{gs}=740.024$ mV, got I_{out} very near equal to 214 μ A and $\frac{dI_{out}}{dV_{out}}=51.06 \mu\text{S}$. Inverse of this = **19.584 k Ω** , which is simulated output resistance.

→ Theoretical R_{out} is $\frac{1}{g_{ds}}$ of NM0, which can be seen using DC operating point simulation:



→ Got $g_{ds} = 50.2809 \mu\text{S}$, inverse of this = **19.88 kΩ**, which is theoretical output resistance.

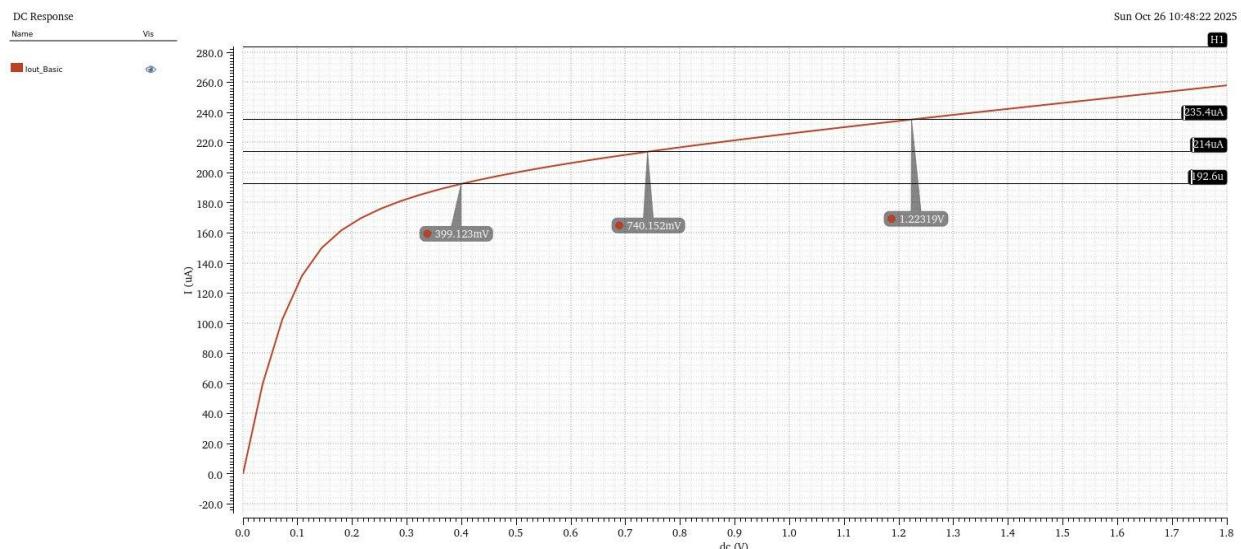
→ Percentage error =

$$\frac{\text{DC operating point output resistance} - \text{simulated output resistance}}{\text{DC operating point output resistance}} \times 100 \%$$

$$= \frac{19.88 \text{ k}\Omega - 19.584 \text{ k}\Omega}{19.88 \text{ k}\Omega} \times 100 \% = \mathbf{1.53\%}$$

- c. Find the voltage swing the current source can accommodate across it without the error deviating beyond $\pm 10\%$.

→ $I_{out} = \alpha * I_{ref}$, $\alpha = 2$ & $I_{ref} = 107 \mu\text{A}$. So, $I_1 = 0.9I_{out} = 192.6 \mu\text{A}$ and $I_2 = 1.1I_{out} = 235.4 \mu\text{A}$. Noted value of V_{out1} in the waveform using horizontal marker:

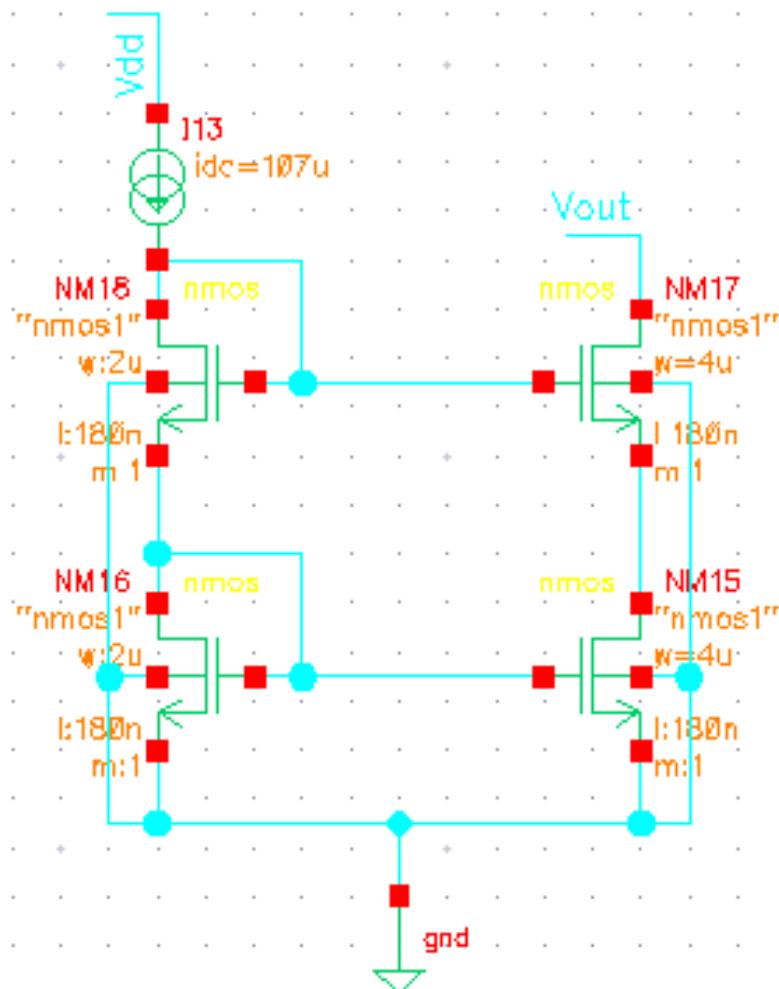


→ Value of V_{out1} at $I_1 = 192.6 \mu\text{A}$ is **399.123 mV** and at $I_2 = 235.4 \mu\text{A}$ is **1.2231 V**.

→ So, the voltage swing the current source can accommodate across it without the error deviating beyond $\pm 10\%$ is 399.123 mV to 1.2231 V.

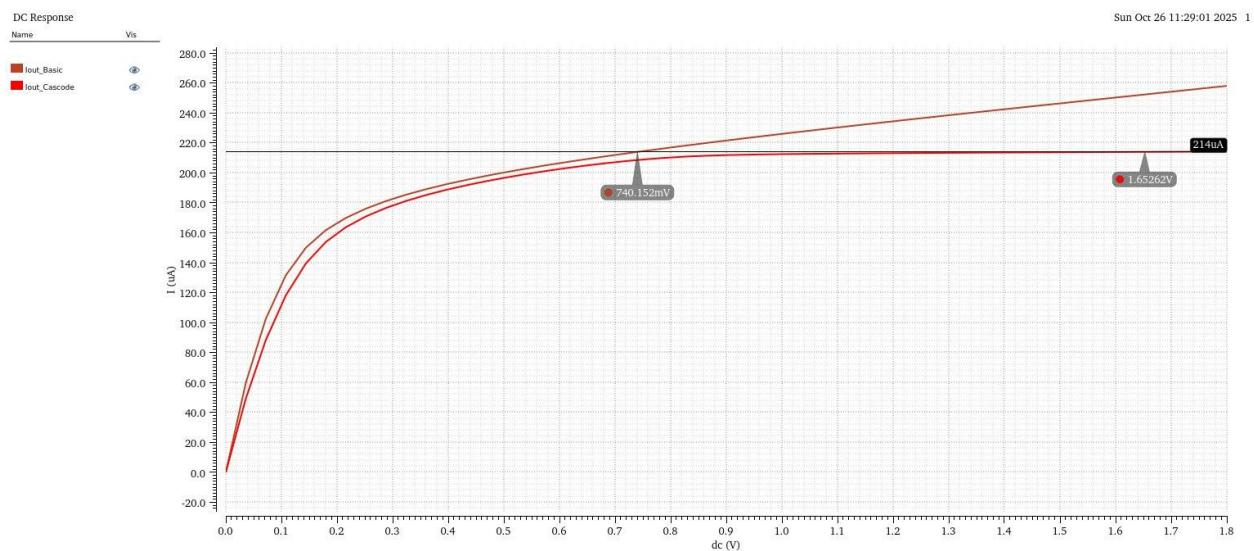
Q.2 Extend the basic current mirror designed above to realize a cascode current source.

→ Since, $I_{out} = 2I_{ref}$. Widths of all transistors of the left part are 2 μm . For right part it is **4 μm** . Schematic diagram of NMOS based cascode current mirror is:



- a) Plot the static I-V characteristic. How does it compare with the basic current mirror? (Plot both the characteristics on the same window for comparison.)

→ Sweeping V_{out1} from 0 to 1.8V and measuring current through drain of NM17 to get the static I-V characteristic of the designed current source and comparing it with basic current mirror's output current:



→ In case of cascode current mirror I_{out} becomes $214 \mu A$, When $V_{out}=1.65262 V$.

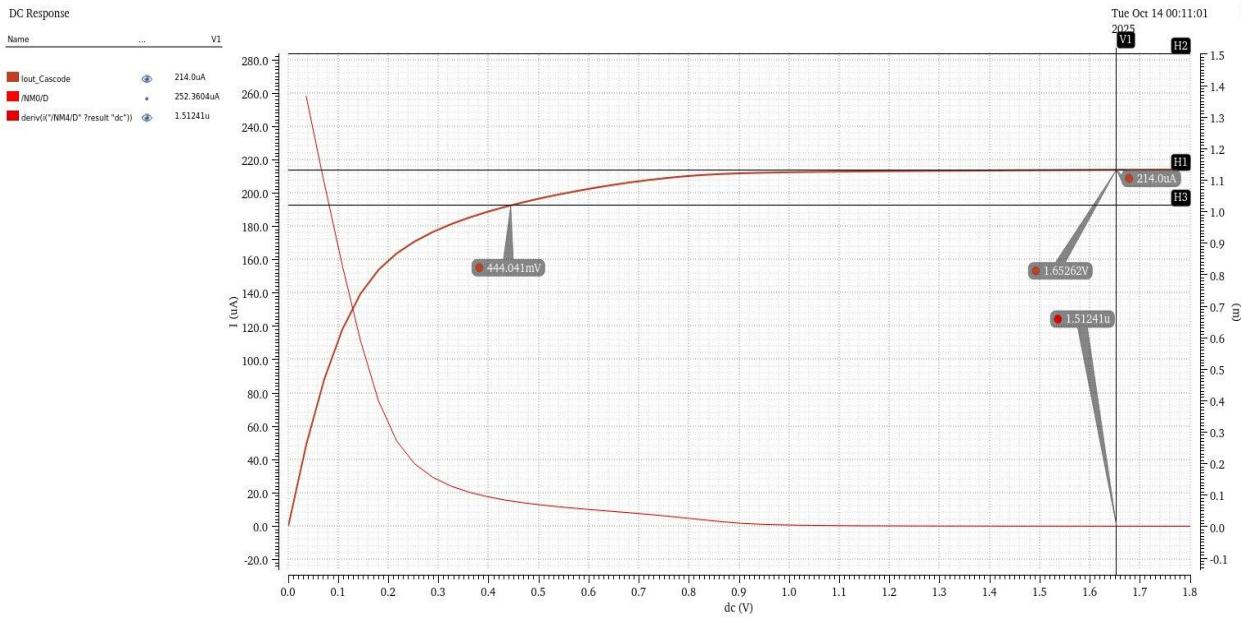
→ Waveform of cascode current mirror is more flatten than basic current mirror. Reason behind this is high output resistance value. In case of basic current mirror single transistor was part of output resistance whose value is r_{o1} only, whereas here casocde structure offers high value of output resistance is $r_{o5}+ r_{o2}+g_{m2}r_{o5}r_{o2}$.

→ The slope of waveform is inverse of output resistance. Since cascode current mirror has high value of output resistance its slope is lesser than basic current mirror's slope, which can be seen from the waveform.

- b) From the characteristic, find the resistance of the designed current source at any one operating point. Compare it with the resistance obtained using DC operating point simulation at the same operating point.

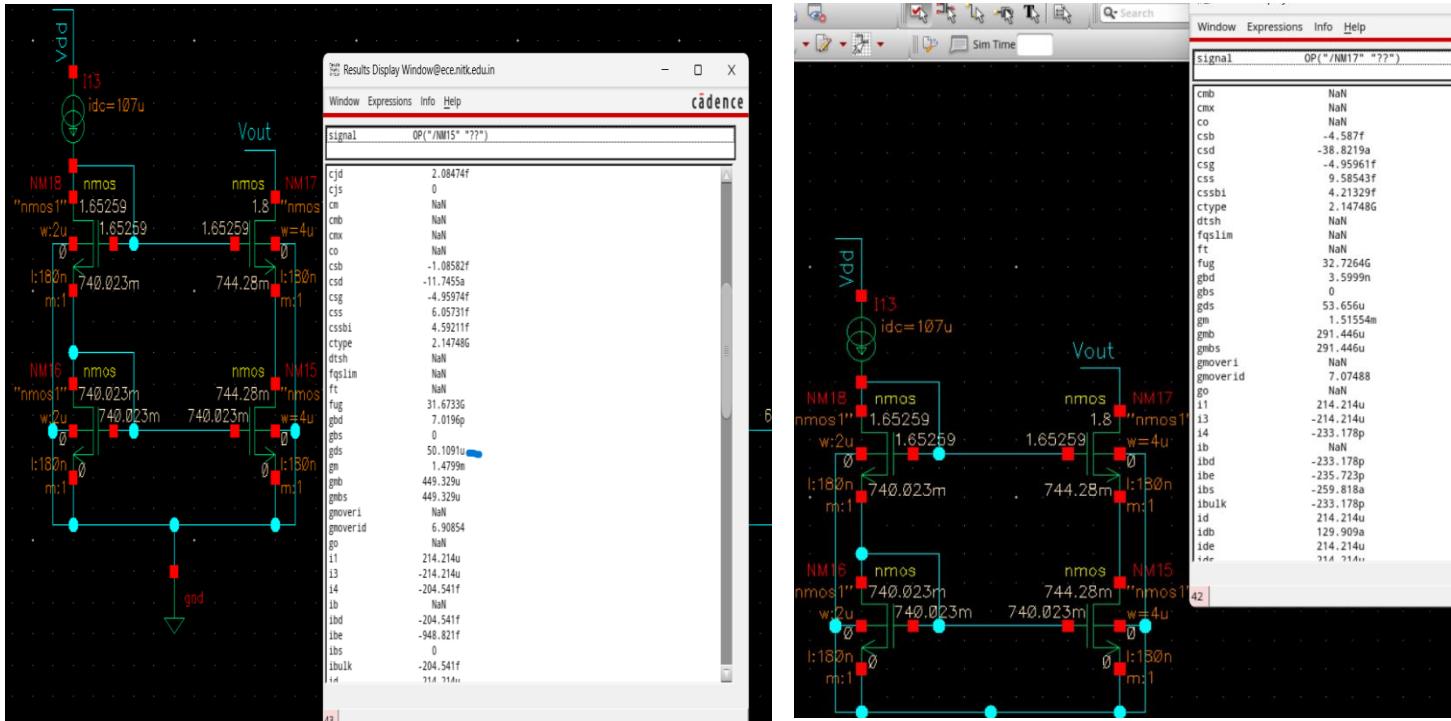
→ Taken $V_{out1}=1.65262$ V as an operating point at that point I_{out} becomes equal to $2I_{ref}=214$ μA .

→ Used “deriv” function to differentiate the waveform of the I_{out} with respect to V_{out1} to get the waveform which contains values of inverse of output resistance. At operating point (**$V_{out}=1.65262$ V**), value from that waveform is inverse of the simulated output resistance.



→ At operating point, $\frac{dI_{out}}{dV_{out}}=1.51241$ μS . Inverse of this = **661.196 kΩ**, which is simulated output resistance.

→ Exact theoretical output resistance of cascode current mirror is $r_{o15} + r_{o17} + (g_{m17} + g_{mb17}) r_{o15} r_{o17}$. Values of these parameters can be found by doing DC operating point analysis, those values are:



→ By putting these values in this equation, will get exact theoretical output resistance: $R_{out} = r_{o15} + r_{o17} + (g_{m17} + g_{mb17}) r_{o17} r_{o15}$. Here, got $R_{out} = 710.615 \text{ k}\Omega$.

→ Percentage error =

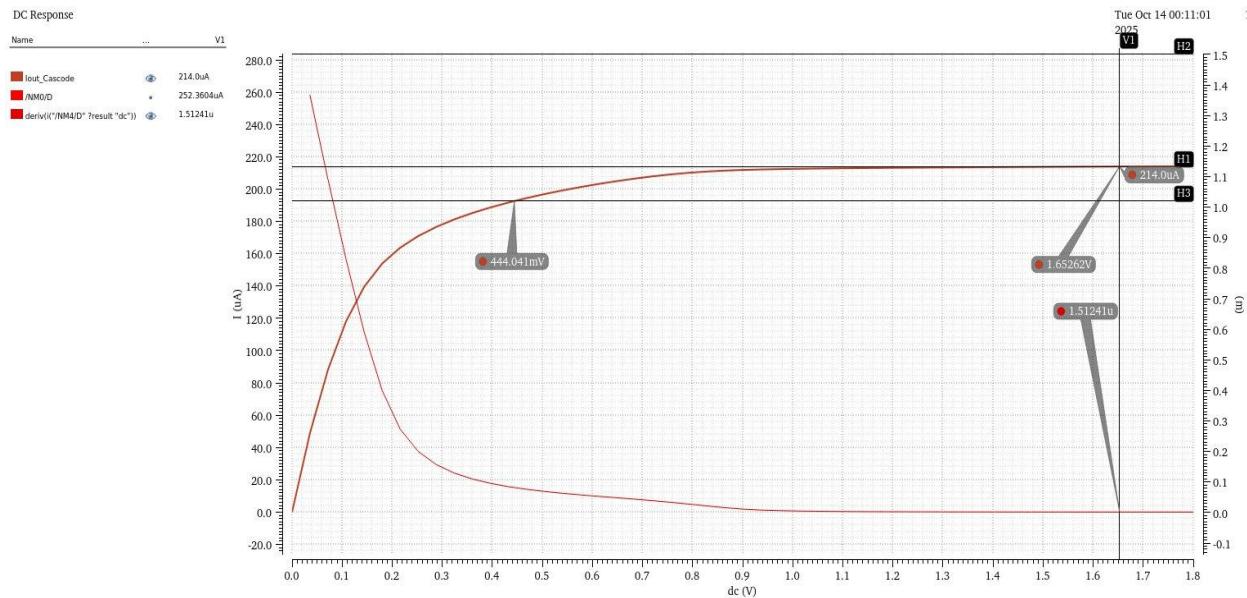
$$\frac{\text{DC operating pt op resistance(theoretical)} - \text{simulated output resistance}}{\text{DC operating pt op resistance(theoretical)}} \times 100 \%$$

$$= \frac{710.615 \text{ k}\Omega - 661.196 \text{ k}\Omega}{710.615 \text{ k}\Omega} \times 100 \% = 6.954 \%$$

→ More percentage error as compare to the basic current mirror.

- c) Find the voltage swing the current source can accommodate across it without the error deviating beyond $\pm 10\%$. How does it compare with the basic current mirror? Comment on your observation and give justifications.

$\rightarrow I_{out} = \alpha * I_{ref}$, $\alpha = 2$ & $I_{ref} = 107 \mu A$. So, $I_1 = 0.9I_{out} = 192.6 \mu A$ and $I_2 = 1.1I_{out} = 235.4 \mu A$. Noted value of V_{out} in the waveform using horizontal marker:

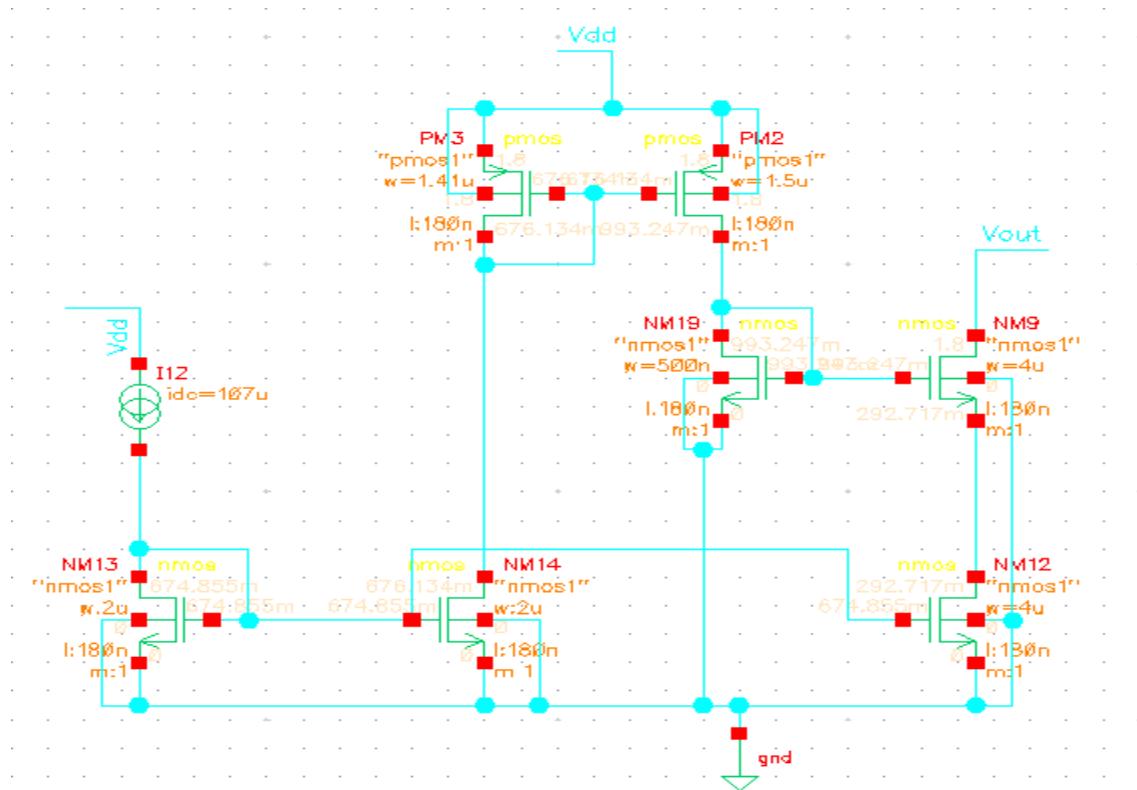


\rightarrow Here, we can observe that there is no much increment in I_{out} beyond $214 \mu A$, whereas in case of basic current mirror V_{out} has some value for $1.1I_{out}$. Reason behind this is increment in output resistance, as output resistance increases slope of I_{out} is getting reduced (almost getting saturates). So, we can't able to get value of V_{out} at $1.1I_{out}$ in this case.

\rightarrow From the above waveform can see the value of V_{out} at $0.9I_{out}$ is equal to **444.041 mV**.

Q.3 Convert the cascode current mirror into a High-swing cascode current mirror. You have only one current source I_{REF} to use.

→ In my case, $a=2$ and width of NMOS of having I_{REF} current = $107 \mu\text{m}$. So, width of NMOS of having I' (which is equal to I_{REF}) current should be equal to $\frac{1}{4} * 2\mu\text{m} = 500 \text{ nm}$.

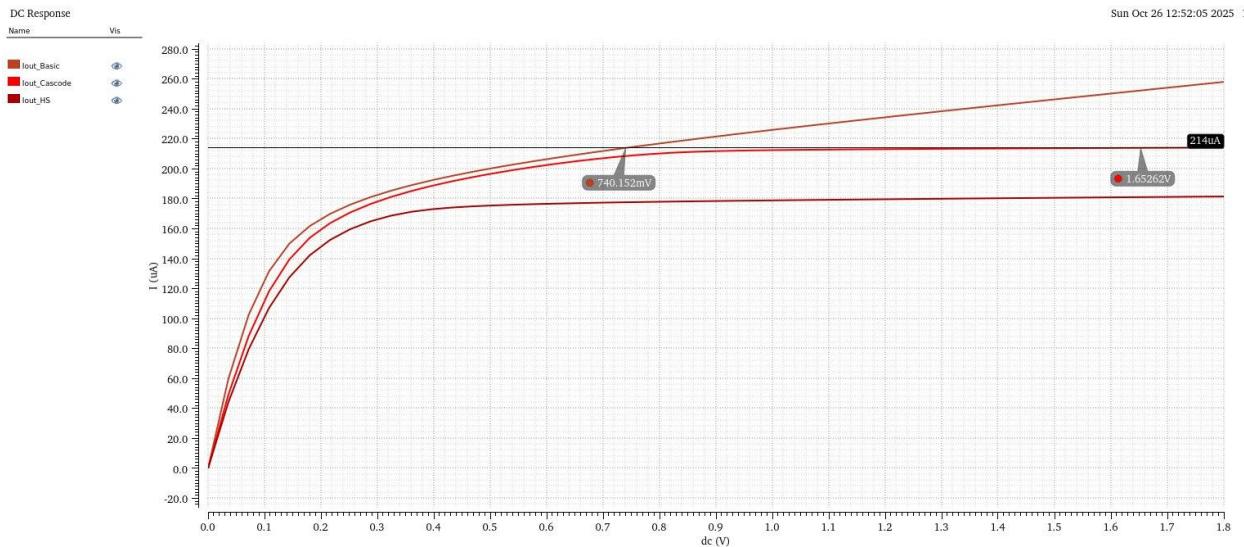


→ Settled transistor sizing of NM9 and NM12 as 4 μm , which are having I_{out} current by taking 8 number of fingers and finger width is 500 nm. Keeping transistor width of NM19 of having I' current as 500 nm.

→ Have done transistor sizing of both PMOS to get I' current equal to the $I_{ref}=107 \mu A$. Widths of both PMOS are **1.41 μm** and **1.5 μm** .

- a) Plot the static I-V characteristic. How does it compare with the basic and cascode current mirror? (Plot all characteristics on the same window for comparison).

→ Sweeping V_{out1} from 0 to 1.8V and measuring current through drain of NM2 to get the static I-V characteristic of the designed current source and comparing it with basic current mirror's and cascode's output current:

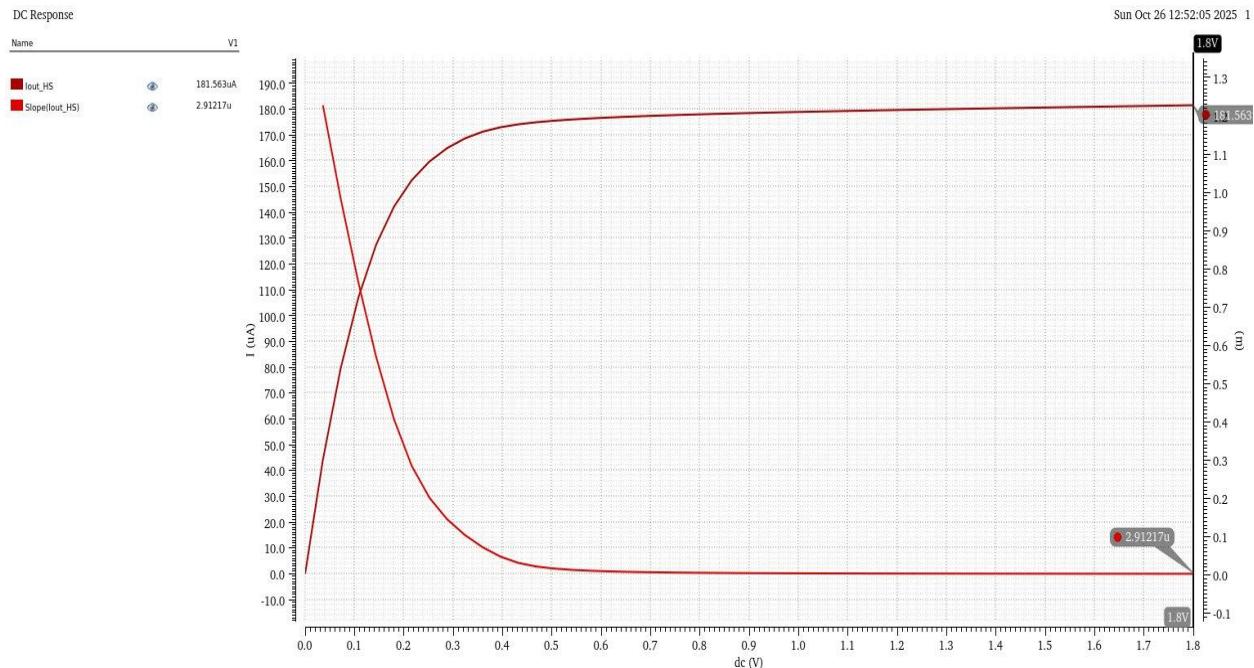


→ From above waveforms can able to see output current of both basic current mirror and cascode current mirror can reach to $2I_{ref}=214 \mu A$ at respective operating point. But, output current of high swing current mirror didn't able to reach to $2I_{ref}=214 \mu A$.

→ For comparatively higher value of V_{out} , output current started getting saturates. Which shows V_{out} has high swing operating region. Final value of output current of high swing current mirror is **181.563 μA** .

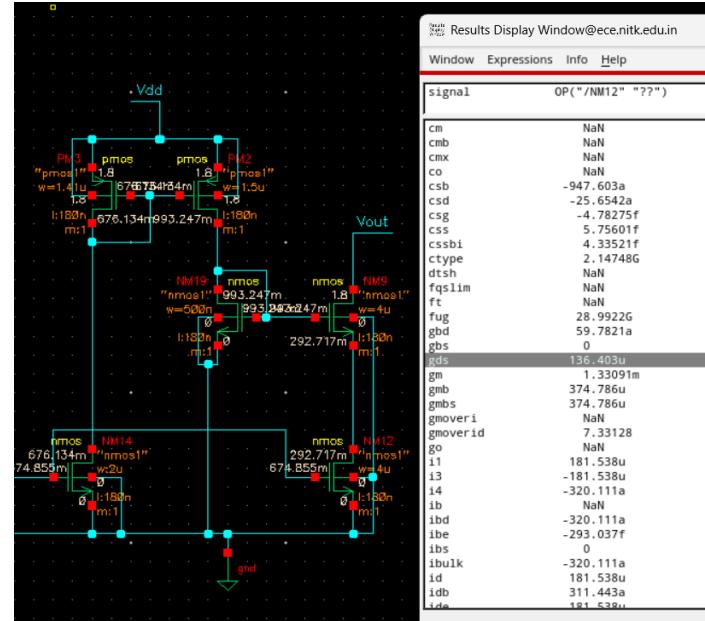
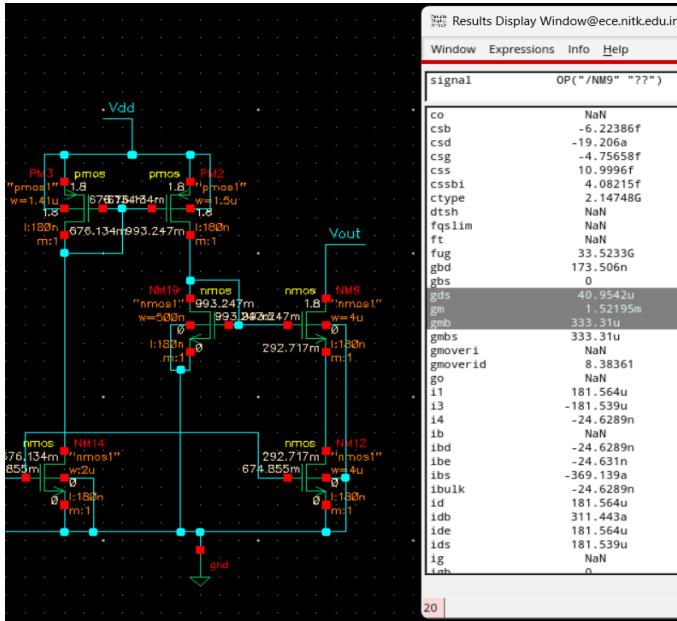
- b) From the characteristic find the resistance of the designed current source at any one operating point. Compare it with the resistance obtained using DC operating point simulation at the same operating point.

→ Used “deriv” function to differentiate the waveform of the I_{out} with respect to V_{out1} to get the waveform which contains values of inverse of output resistance. At operating point ($V_{out1}=1.8V$), value from that waveform is inverse of the simulated output resistance.



→ At operating point, $\frac{dI_{out}}{dV_{out}} = 2.91217 \mu\text{S}$. Inverse of this = **343.386 kΩ**, which is simulated output resistance.

→ Exact theoretical output resistance of cascode current mirror is $r_{o9} + r_{o12} + (g_{m9} + g_{mb9}) r_{o9} r_{o12}$. Values of these parameters can be find by doing DC operating point analysis, those values are:



→ By putting these values in this equation, will get exact theoretical output resistance: $R_{out} = r_{o9} + r_{o12} + (g_{m9} + g_{mb9}) r_{o9} r_{o12}$. Here, got $R_{out} = 363.802 \text{ k}\Omega$.

→ Percentage error =

$$\frac{\text{DC operating pt op resistance(theoretical)} - \text{simulated output resistance}}{\text{DC operating pt op resistance(theoretical)}} \times 100 \%$$

$$= \frac{363.802 \text{ k}\Omega - 343.386 \text{ k}\Omega}{343.386 \text{ k}\Omega} \times 100 \% = 5.945 \%$$

- c) Find the voltage swing the current source can accommodate across it without the error deviating beyond $\pm 10\%$. How does it compare with the basic current mirror? Comment on your observation and give justifications.

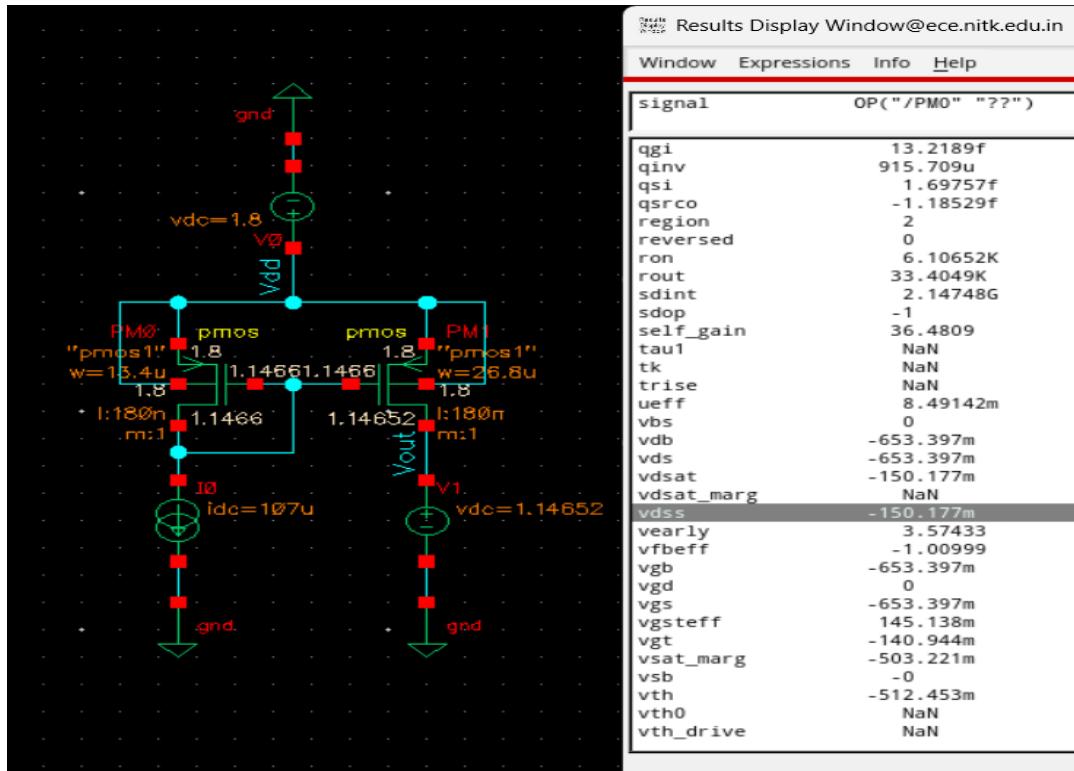
→ Output current itself didn't reach its desired value which is 214 μA , and $0.9I_{out} = 192.6 \mu\text{A}$. Current didn't even reach 10% lower value of $2*I_{ref}$. So, can't determine the voltage swing here. Since, almost constant current is there for high range of V_{out1} . So, voltage swing is high here, that's why this current mirror is called as high swing cascode current mirror.

Q.4 Repeat the above three experiments by designing PMOS based current mirrors.

i) Basic current mirror:

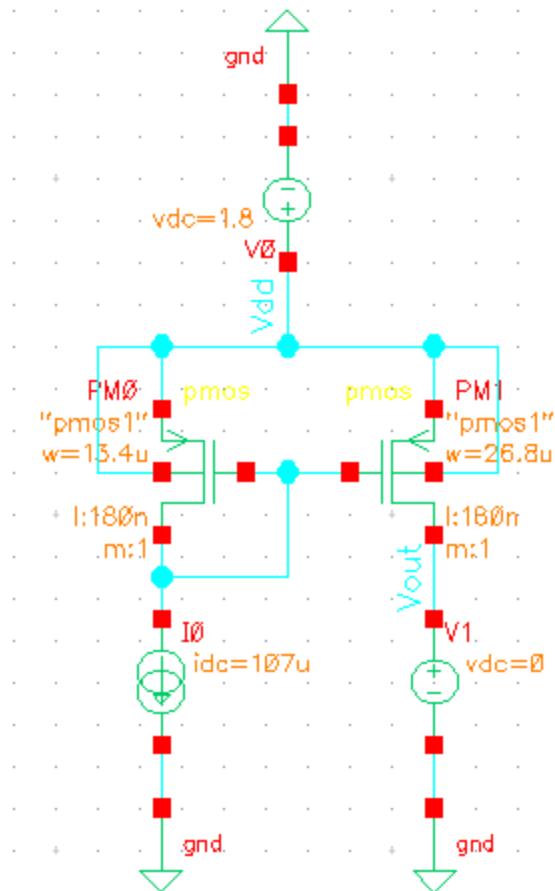
→ First of all iterative method was used to find width of PMOS such that $V_{dssat} = -150\text{mV}$ with keeping $I_{ref} = 107 \mu\text{A}$.

→ For **13.4 μm** width of PMOS $V_{dssat} = -150.177 \text{ mV}$ (evaluated from DC operating point).



→ Here, as an operating point: $V_{gs} = V_{ds} = -653.397 \text{ mV}$ or $V_{sg} = V_{sd} = 653.397 \text{ mV}$.

→ Based on this width and for $a=2$ (width of second PMOS becomes double), Schematic diagram of PMOS based basic current mirror is:



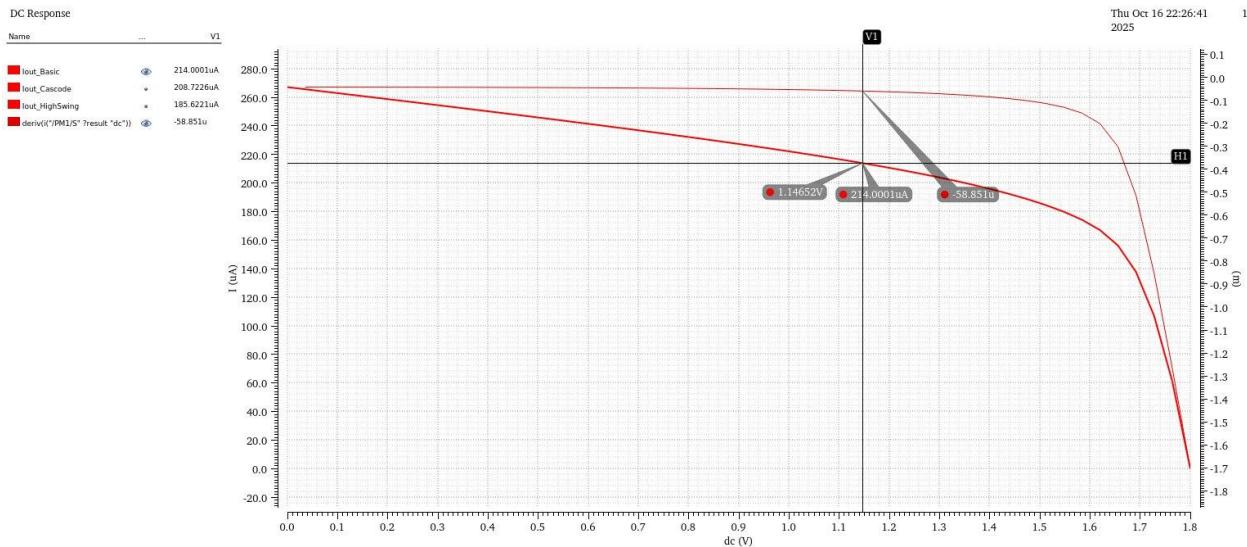
a) & b)

→ Sweeping V_{out} ($V1$) from 0 to 1.8V and measuring current through source of PM1 to get the static I-V characteristic of the designed current source.

→ Used “deriv” function to differentiate the waveform of the I_{out} with respect to V_{out} to get the waveform which contains values of inverse of output resistance. $V_{sd}=V_{sg}=653.397$ mV, here $V_D=V_{out}$

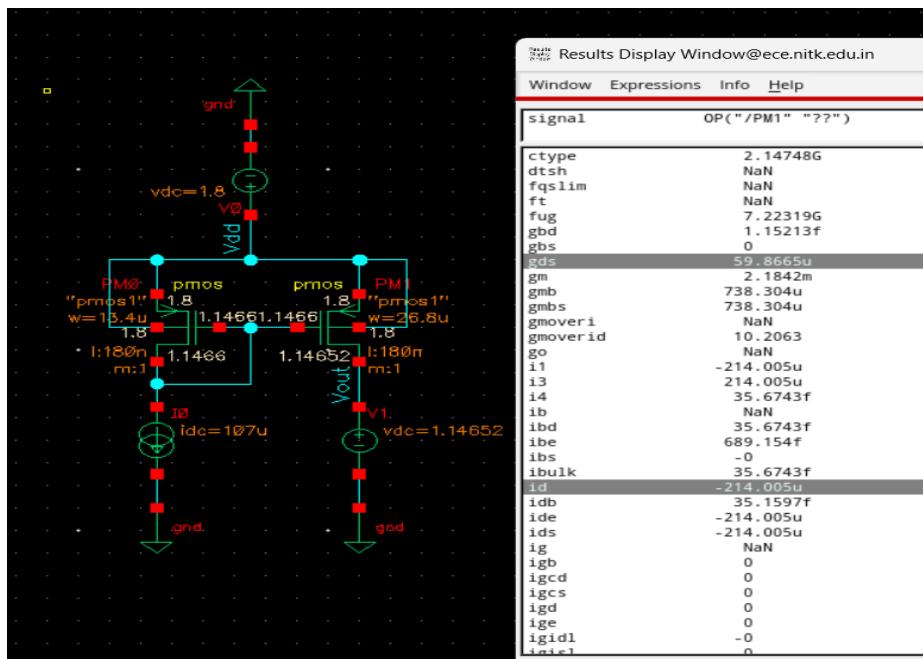
and $V_s=1.8V$. So, operating point $V_{out}=1.8-0.653=1.1465 V$, at this point value from that waveform gives inverse of the simulated output resistance.

→Waveform of the static I-V characteristic:



→At $V_{out}=1.8-0.653=1.1465 V$, got I_{out} very near equal to $214 \mu A$ and $\frac{-dI_{out}}{dV_{out}}=58.815 \mu S$, here, negative sign because of decreasing current at increment in V_{out} . Inverse of this = **$17.002 k\Omega$** , which is simulated output resistance.

→Theoretical R_{out} is $\frac{1}{gds}$ of PM1, which can be seen using DC operating point simulation:



→ Got $g_{ds} = 59.8665 \mu\text{S}$, inverse of this = **16.70 kΩ**, which is DC operating point output resistance.

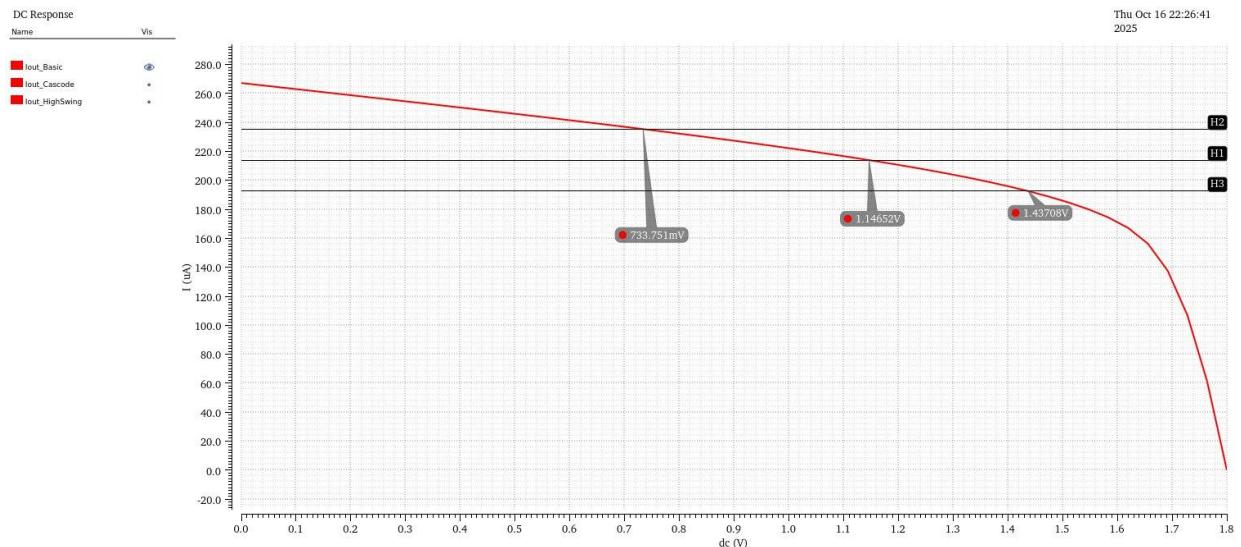
→ Percentage error =

$$\frac{\text{DC operating point output resistance} - \text{simulated output resistance}}{\text{DC operating point output resistance}} \times 100 \%$$

$$= \frac{16.70 \text{ k}\Omega - 17.002 \text{ k}\Omega}{16.70 \text{ k}\Omega} \times 100 \% = -1.8\%$$

c)

→ $I_{out} = \alpha * I_{ref}$, $\alpha = 2$ & $I_{ref} = 107 \mu\text{A}$. So, $I_1 = 0.9I_{out} = 192.6 \mu\text{A}$ and $I_2 = 1.1I_{out} = 235.4 \mu\text{A}$. Noted value of V_{out} in the waveform using horizontal marker:



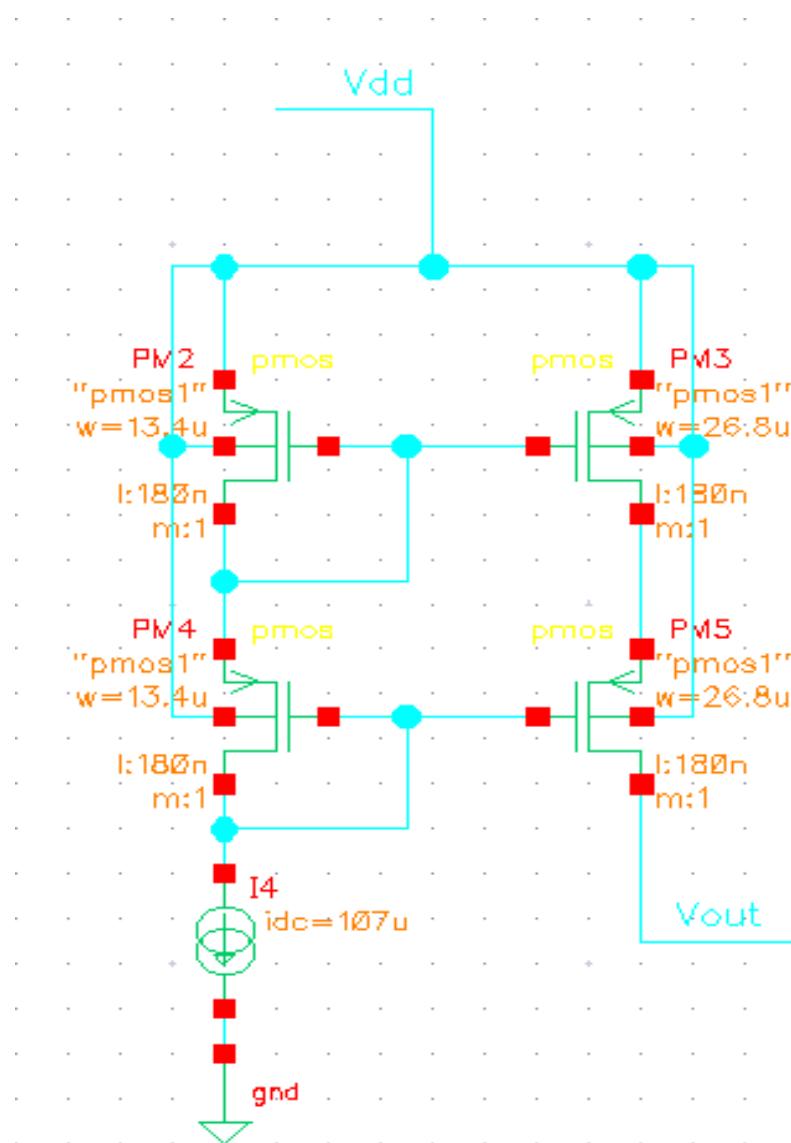
→ Value of V_{out1} at $I_1 = 192.6 \mu\text{A}$ is **1.437 V** and at $I_2 = 235.4 \mu\text{A}$ is **733.751 mV**.

→ So, the voltage swing the current source can accommodate across it without the error deviating beyond ±10% is 733.751 mV to 1.437 V.

ii) Cascode current mirror:

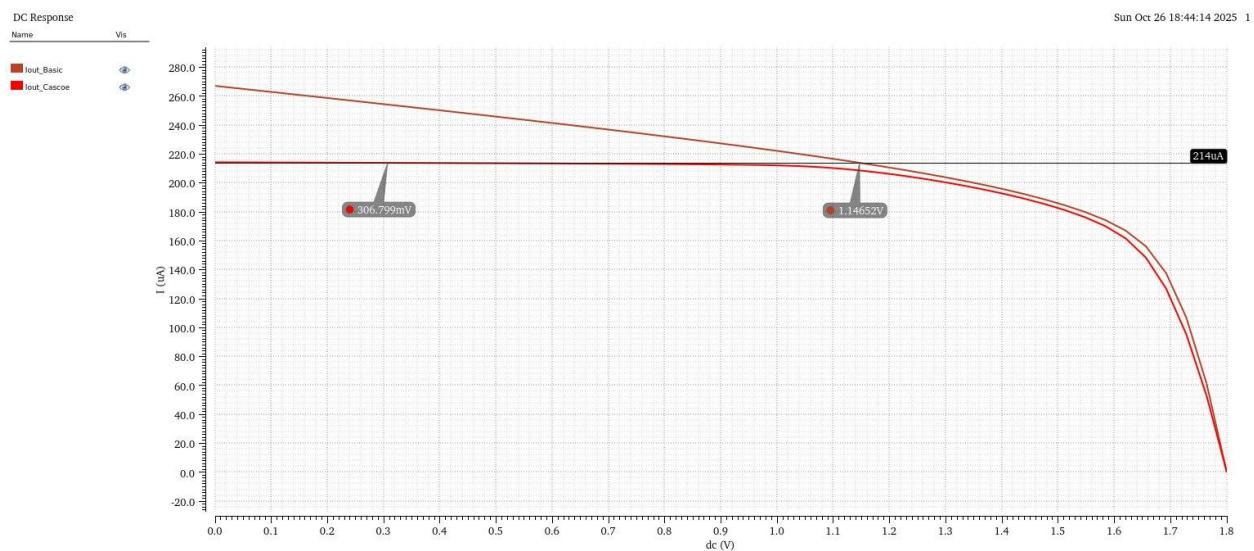
→ Since, $I_{out}=2I_{ref}$. Widths of all left part transistors remains same as previous case which was $13.4 \mu m$ and right part width became twice which is $26.8 \mu m$.

Schematic diagram of PMOS based cascode current mirror is:



a)

→ Sweeping V_{out1} from 0 to 1.8V and measuring current through source of PM5 to get the static I-V characteristic of the designed current source and comparing it with basic current mirror's output current:



→ In case of cascode current mirror I_{out} becomes 214 μ A, When $V_{out}=306.799$ mV.

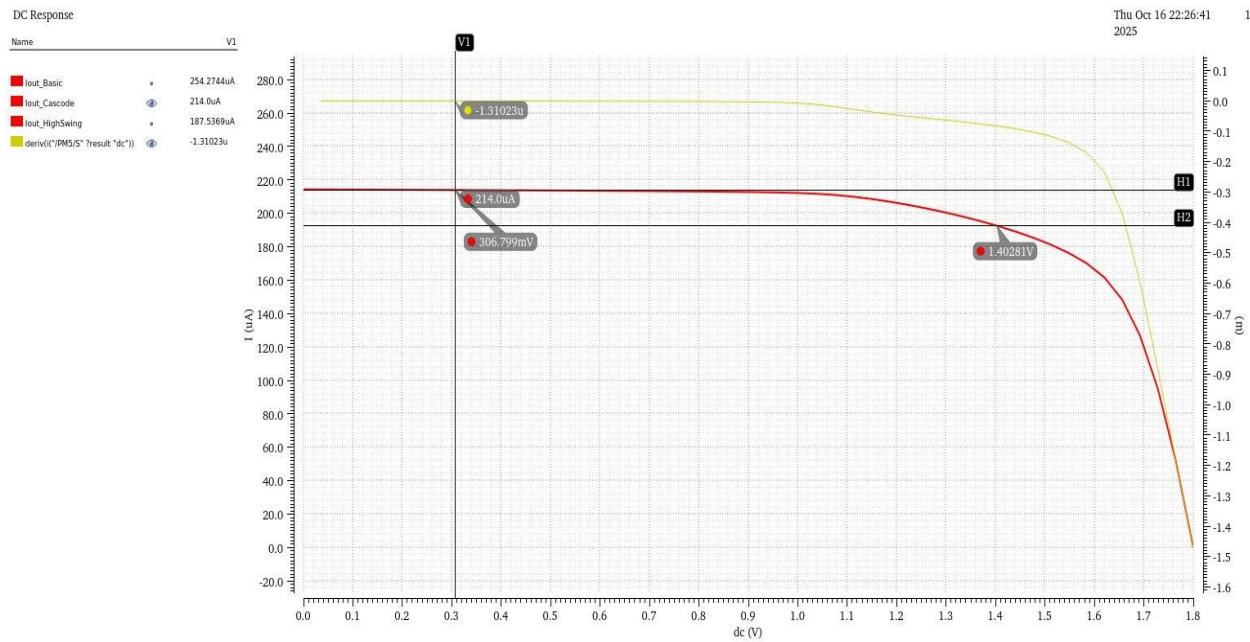
→ Waveform of cascode current mirror is more flatten than basic current mirror. Reason behind this is high output resistance value. In case of basic current mirror single transistor was part of output resistance whose value is r_{o1} only, whereas here casocde structure offers high value of output resistance is $r_{o5}+ r_{o3}+g_m r_{o5} r_{o3}$.

→ The slope of waveform is inverse of output resistance. Since cascode current mirror has high value of output resistance it's slope is lesser than basic current mirror's slope, which can be seen from the waveform.

b)

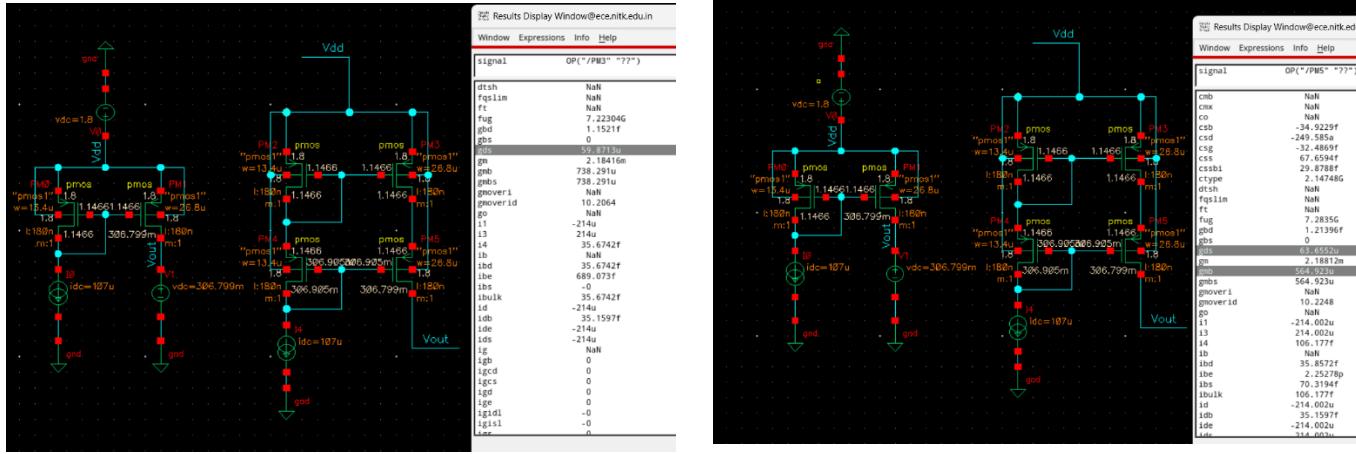
→ Taken $V_{out}=306.799$ mV as an operating point at that point I_{out} becomes equal to $2I_{ref}=214$ μA .

→ Used “deriv” function to differentiate the waveform of the I_{out} with respect to V_{out} to get the waveform which contains values of inverse of output resistance. At operating point ($V_{out}=306.799$ mV), value from that waveform is inverse of the simulated output resistance.



→ At operating point, $-\frac{dI_{out}}{dV_{out}}=1.31023$ μS . Inverse of this = **763.224 kΩ**, which is simulated output resistance.

→ Exact theoretical output resistance of cascode current mirror is $r_{o5} + r_{o3} + (g_{m5} + g_{mb5}) r_{o5} r_{o3}$. Values of these parameters can be find by doing DC operating point analysis, those values are:



→ By putting these values in this equation, will get exact theoretical output resistance: $R_{out} = r_{o5} + r_{o3} + (g_{m5} + g_{mb5}) r_{o5} r_{o3}$. Here, got $R_{out}=754.731 \text{ k}\Omega$.

→ Percentage error =

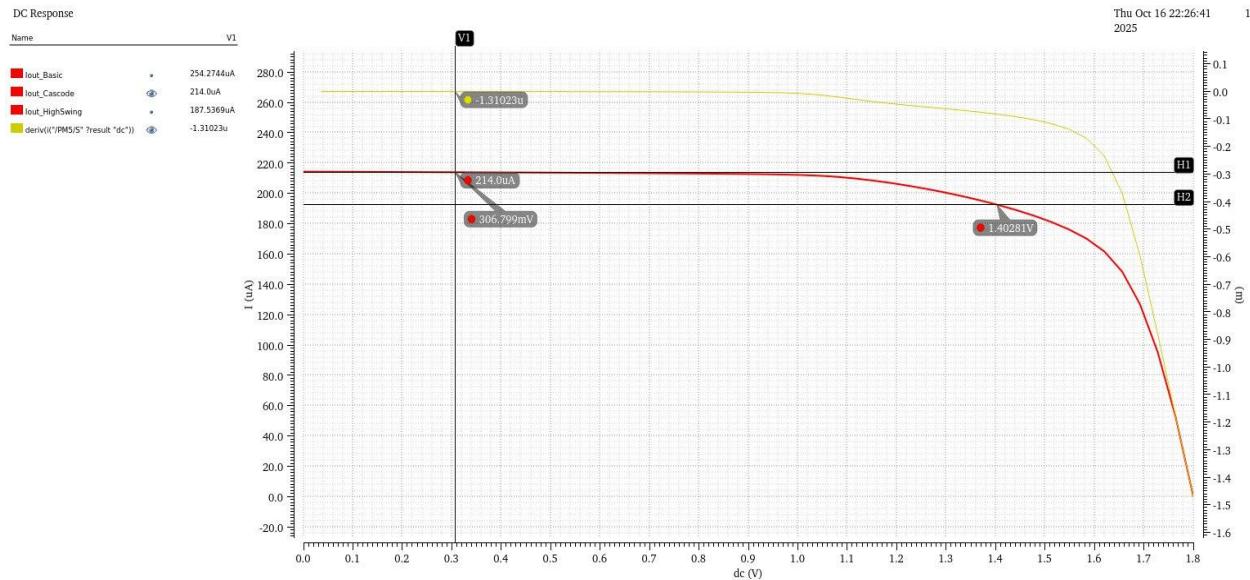
$$\frac{\text{DC operating pt op resistance(theoretical)} - \text{simulated output resistance}}{\text{DC operating pt op resistance(theoretical)}} \times 100 \%$$

$$= \frac{754.731 \text{ k}\Omega - 763.224 \text{ k}\Omega}{754.731 \text{ k}\Omega} \times 100 \% = -1.125 \%$$

→ More percentage error as compare to the basic current mirror.

c)

→ $I_{out} = \alpha * I_{ref}$, $\alpha = 2$ & $I_{ref} = 107 \mu A$. So, $I_1 = 0.9I_{out} = 192.6 \mu A$ and $I_2 = 1.1 I_{out} = 235.4 \mu A$. Noted value of V_{out} in the waveform using horizontal marker:

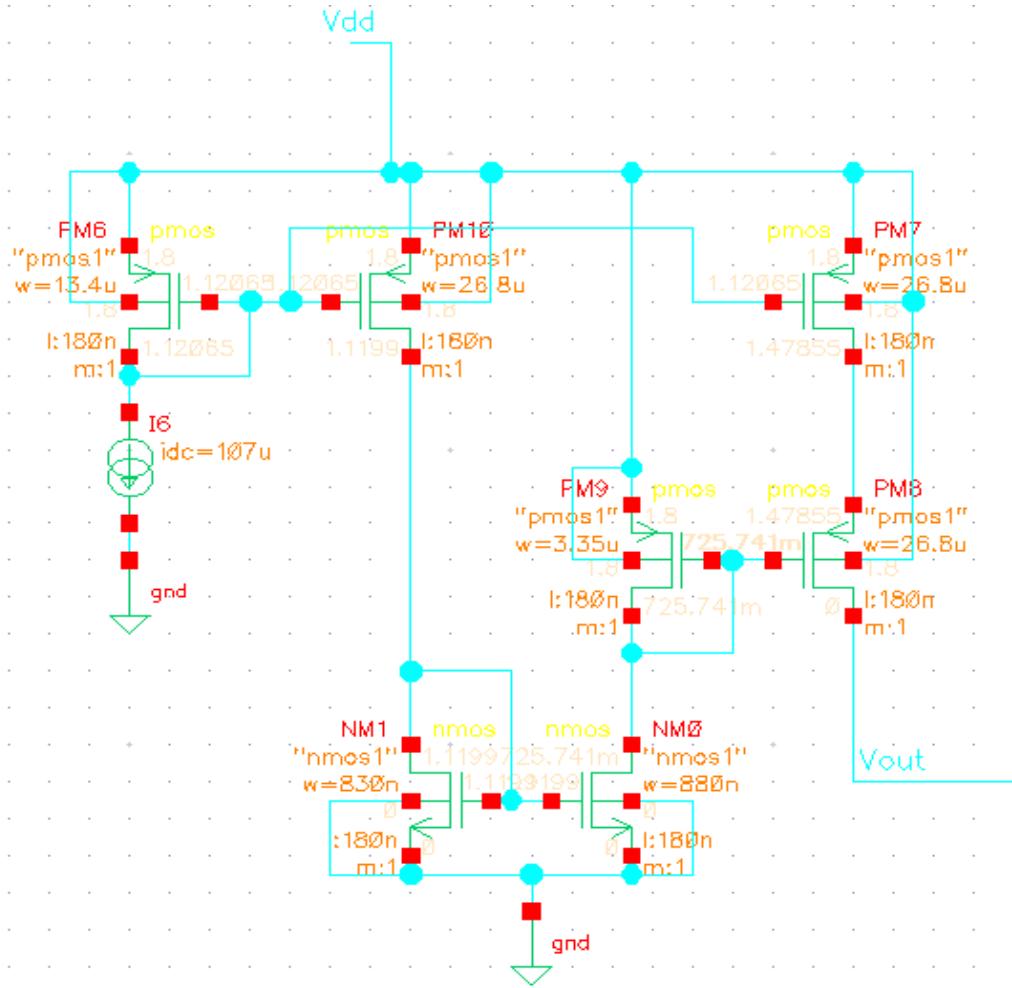


→ Here, we can observe that there is no much increment in I_{out} beyond $214 \mu A$, whereas in case of basic current mirror V_{out} has some value for $1.1I_{out}$. Reason behind this is increment in output resistance, as output resistance increases slope of I_{out} is getting reduced (almost getting saturated). So, we can't able to get value of V_{out} at $1.1I_{out}$ in this case.

→ From the above waveform can see the value of V_{out} at $0.9I_{out}$ is equal to **1.40281 V**.

iii) High swing cascode mirror:

→ Since, $I_{out}=2I_{ref}$. Widths of all left part transistors remains same as previous case which was 13.4 μm and right part width became twice which is 26.8 μm .

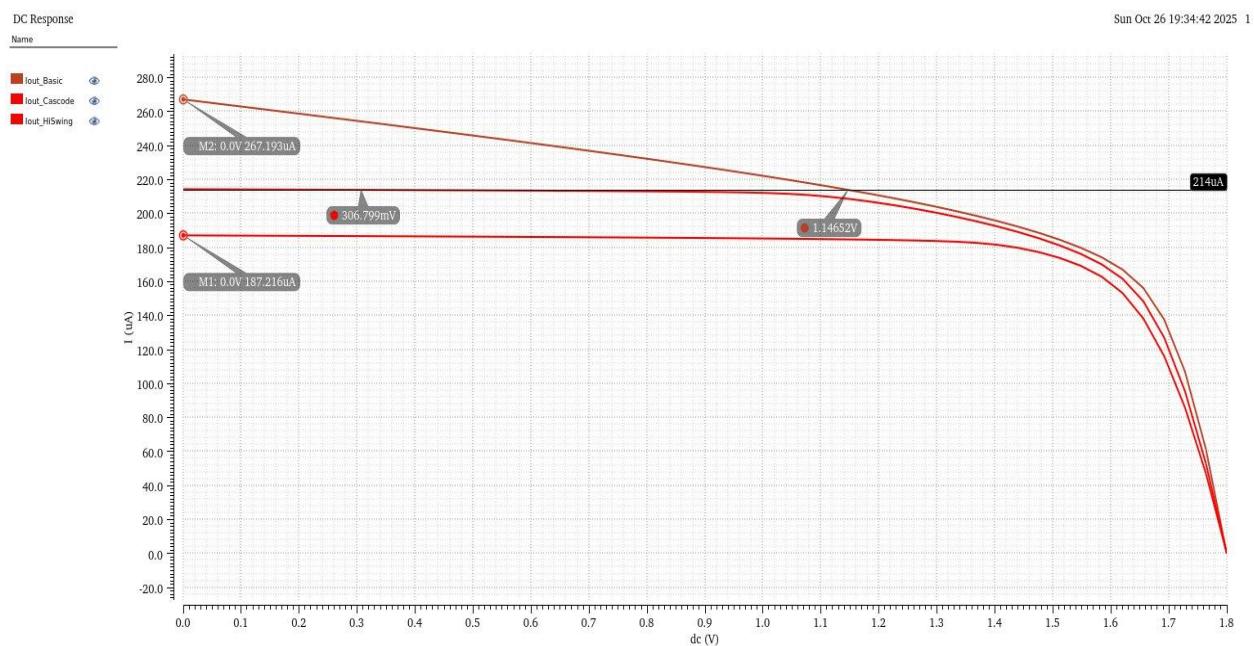


→ Keeping transistor width of $PM9$ of having I' current as $\frac{1}{4} * 13.4 \mu\text{m} = 3.35 \mu\text{m}$. Where $I' = I_{ref} = 107 \mu\text{A}$.

→ Have done transistor sizing of both NMOS to get I' current equal to the $I_{ref} = 107 \mu\text{A}$. Widths of both NMOS are **830 nm** and **880 nm**.

a)

→ Sweeping V_{out} from 0 to 1.8V and measuring current through source of PM8 to get the static I-V characteristic of the designed current source and comparing it with basic current mirror's and cascode's output current:

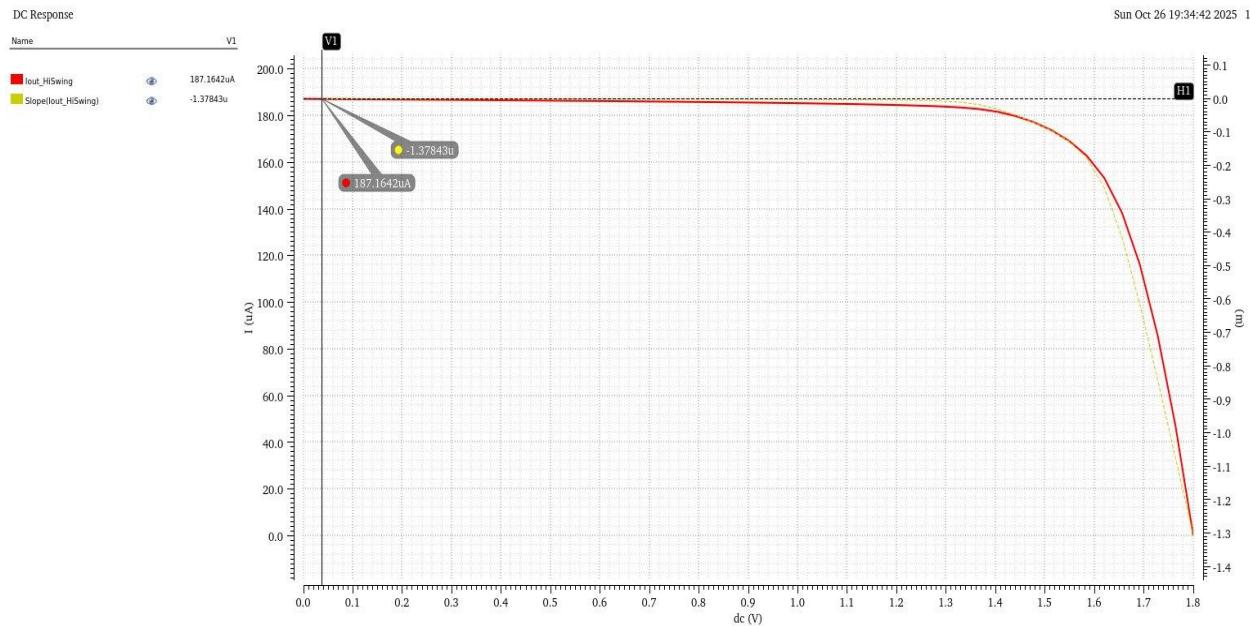


→ From above waveforms can able to see output current of both basic current mirror and cascode current mirror can reach to $I_{out}=214 \mu A$ at some operating point. But, output current of high swing current mirror didn't able to reach to $I_{out}=214 \mu A$.

→ For comparatively higher value of V_{out} , output current started getting saturates. Which shows V_{out} has high swing operating region. Final value of output current of high swing current mirror is **187.216 μA** .

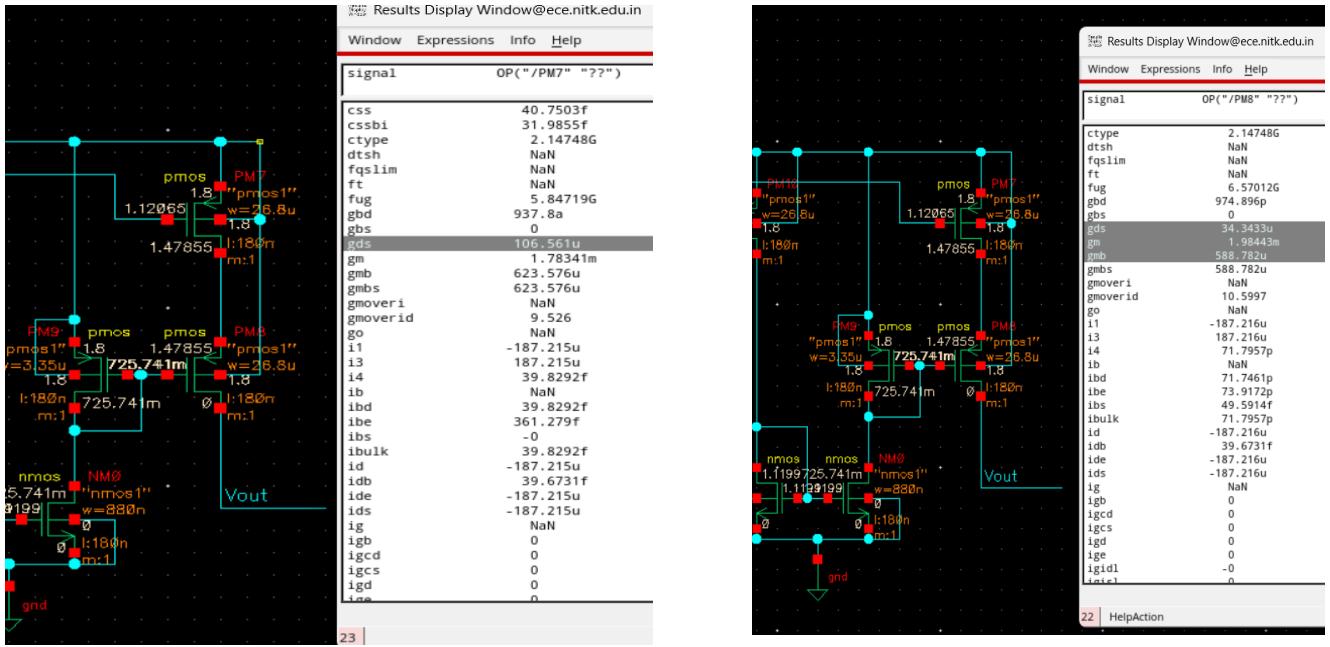
b)

→ Used “deriv” function to differentiate the waveform of the I_{out} with respect to V_{out} to get the waveform which contains values of inverse of output resistance. At operating point ($V_{out}=1.8V$), value from that waveform is inverse of the simulated output resistance.



→ At operating point, $-\frac{dI_{out}}{dV_{out}} = 1.37843 \mu\text{S}$. Inverse of this = **725.463 kΩ**, which is simulated output resistance.

→ Exact theoretical output resistance of cascode current mirror is $r_{o7} + r_{o8} + (g_{m8} + g_{mb8}) r_{o7} r_{o8}$. Values of these parameters can be find by doing DC operating point analysis, those values are:



→ By putting these values in this equation, will get exact theoretical output resistance: $R_{out} = r_{o7} + r_{o8} + (g_{m8} + g_{mb8}) r_{o7} r_{o8}$. Here, got $R_{out} = 741.5865 \text{ k}\Omega$.

→ Percentage error =

$$\frac{\text{DC operating pt op resistance(theoretical)} - \text{simulated output resistance}}{\text{DC operating pt op resistance(theoretical)}} \times 100 \%$$

$$= \frac{741.5865 \text{ k}\Omega - 725.463 \text{ k}\Omega}{741.5865 \text{ k}\Omega} \times 100 \% = 2.174 \%$$

c)

→ Output current itself didn't reach it's desired value which is 214 μA , and $0.9I_{out} = 192.6 \mu\text{A}$. Current didn't even reach 10% lower value of $2I_{ref}$. So, can't determine the voltage swing here. Since, almost constant current is there for high range of V_{out} . So, voltage swing is high here, that's why this current mirror is called as high swing cascode current mirror.