



Prof. Massimo Alioto
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Massimo Alioto is a Professor at the ECE Department of the National University of Singapore, where he leads the Green IC group, and is the Director of the Integrated Circuits and Embedded Systems area and the FD-Fabrics research center on intelligent & connected systems. He held positions at the University of Siena, Intel Labs CRL, University of Michigan Ann Arbor, University of California Berkeley, EPFL - Lausanne.

He is (co)author of 300 publications on journals and conference proceedings, and four books with Springer. His primary research interests include ultra-low power circuits and systems, self-powered integrated systems, near-threshold circuits for green computing, widely energy-scalable integrated systems, circuits for machine intelligence, hardware security, and emerging technologies.

He is the Editor in Chief of the IEEE Transactions on VLSI Systems, Distinguished Lecturer for the IEEE Solid-State Circuits Society, and was Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. Previously, Prof. Alioto was the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society (2010-2012), as well as Distinguished Lecturer (2009-2010) and member of the Board of Governors (2015-2020). He served as Guest Editor of numerous journal special issues, Technical Program Chair of several IEEE conferences (ISCAS 2023, SOCC, PRIME, ICECS, VARI, NEWCAS, ICM), and TPC member (ISSCC, ASSCC). Prof. Alioto is an IEEE Fellow.

▲主辦單位

IEEE SSCS Taipei Chapter
IEEE CASS Taipei Chapter

▲協辦單位

臺大電子所 (NTU GIEE)



Distinguished Lecture

Intelligent Systems with Ultra-Wide Power-Performance Adaptation - Going Well beyond the Diminishing Returns of Voltage Scaling

時間：2021. 4. 30 (五), 3:30 – 5:00PM

地點：台大電機二館103室 (敬請配戴口罩)

報名網址：<https://reurl.cc/Q7xzoO>



線上演講

Abstract: Wide power-performance adaptation has become crucial in always-on nearly real-time and energy-autonomous SoCs that are subject to wide variability in the power availability and the performance target, as required by applications such as AI, vision and audio cognition. Wide adaptation is indeed a prerequisite to assure sustained operation in spite of the widely fluctuating energy/power source, and to grant swift response upon the occurrence of events of interest (e.g., on-chip data analytics), while maintaining extremely low consumption in the common case. These requirements have led to a strong demand for SoCs having an extremely wide performance-power scalability and adaptation, which vastly exceeds the capabilities of conventional wide voltage scaling.

In this talk, recent directions to drastically extend the performance-power scalability of digital, analog and power management circuits and architectures are presented. Silicon demonstrations of better-than-voltage-scaling adaptation to the workload are illustrated for the data path, the clock path and the memory sub-system. Several silicon demonstrations are presented for accelerators, processors and SRAMs with enhanced peak performance above traditionally allowed at nominal voltage, yet at reduced minimum energy. Energy-quality scaling is explored as additional dimension to break the conventional performance-energy tradeoff in error-resilient applications such as AI and vision, from networks on chip to memories and accelerators. Further performance and energy improvements are discussed through uncommonly flexible in-memory broad-purpose computing frameworks for true data locality, from buffering to signal conditioning and neural net workloads. Finally, challenges and opportunities for the decade ahead are discussed to enable a new generation of always-on intelligent systems with divergently high peak performance and low minimum power.