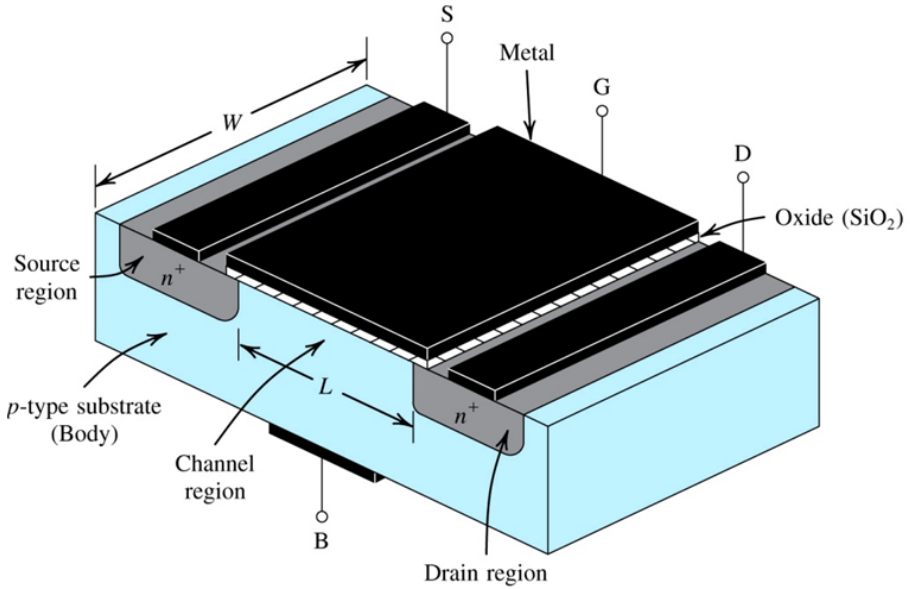
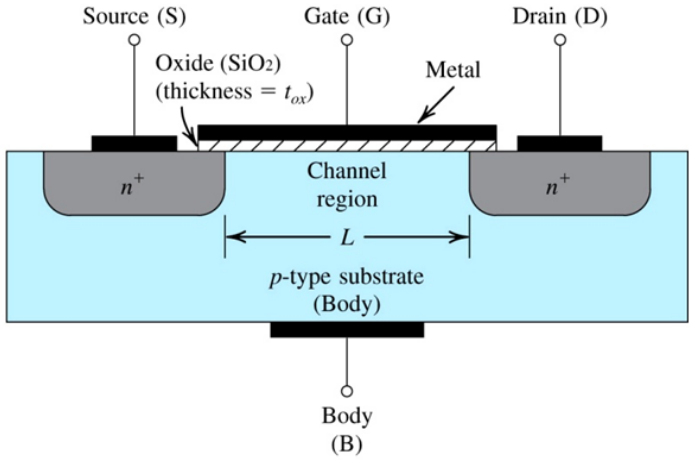
CHAPTER 5 MOS FIELD-EFFECT TRANSISTORS (MOSFETs)

Chapter Outline

5.1 Device Structure and Physical Operation

Device structure of MOSFET





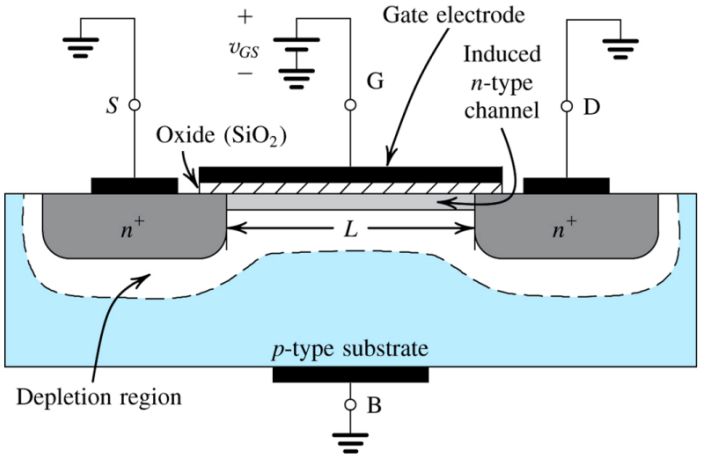
- "MOS" ≡ metal-oxide-semiconductor structure
- MOSFET is a four-terminal device: gate (G), source (S), drain (D) and body (B)
- The device size (channel region) is specified by channel width (W) and channel length (L)
- Two kinds of MOSFETs: n-channel (NMOS) and p-channel (PMOS) devices
- The device structure is basically symmetric in terms of drain and source
- Source and drain terminals are specified by the operation voltage

Operation with zero gate voltage

- The MOS structure form a parallel-plate plate capacitor with gate oxide layer in the middle
- Two *pn* junctions (S-B and D-B) are connected as back to back diodes
- The source and drain terminals are isolated by two depletion regions without conducting current
- The operating principles will be introduced by using the *n*-channel MOSFET as an example

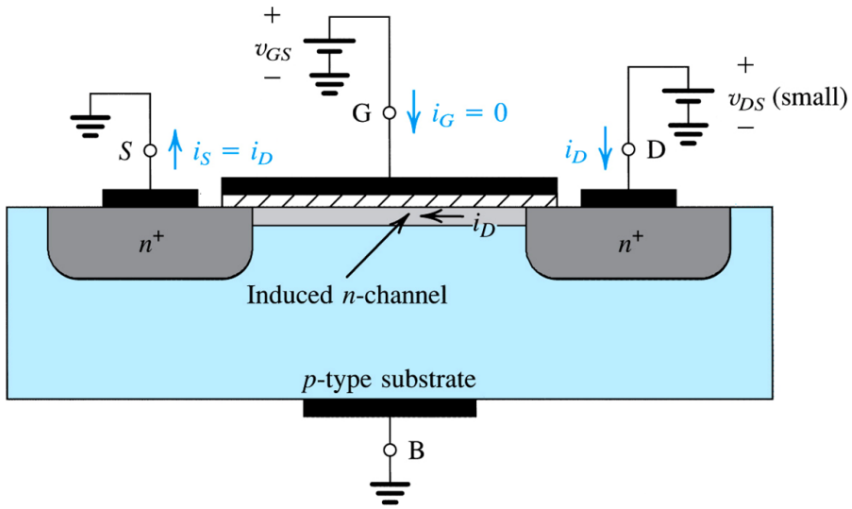
Creating a channel for current flow

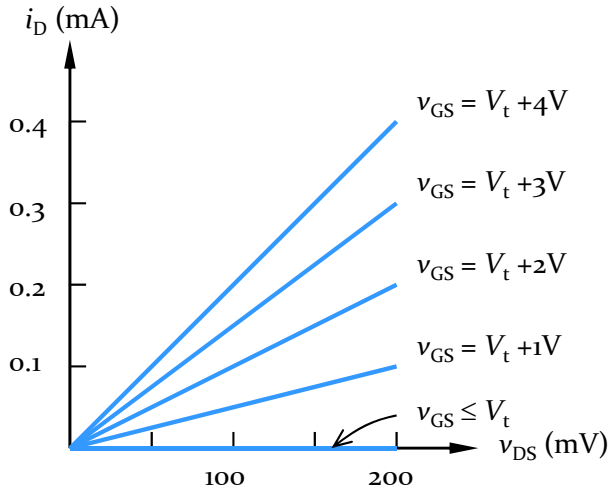
- Positive charges accumulate in gate as a positive voltage applies to gate electrode
- Electric field forms a depletion region by pushing holes in *p*-type substrate away from the surface
- Electrons accumulate on the substrate surface as gate voltage exceeds a **threshold voltage** V_t
- The induced *n* region thus forms a **channel** for current flow from drain to source
- The channel is created by inverting the substrate surface from *p*-type to *n*-type → **inversion layer**
- The field controls the amount of charge in the channel and determines the channel conductivity



Applying a small drain voltage

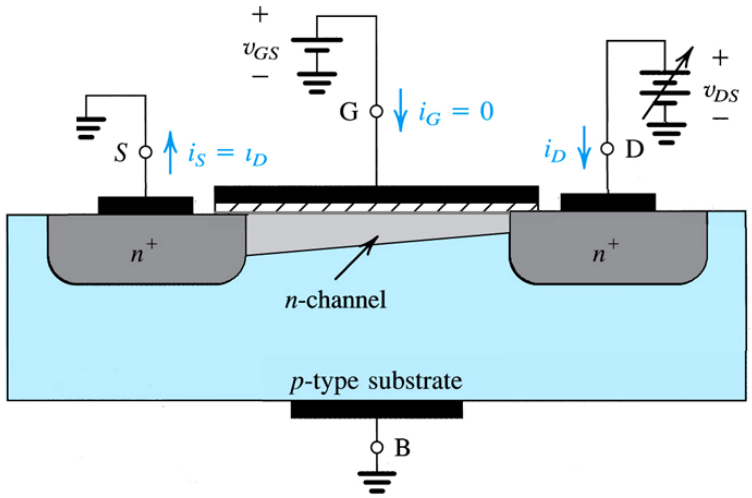
- A positive $v_{GS} > V_t$ is used to induce the channel → n-channel **enhancement-type** MOSFET
- Free electrons travel from source to drain through the induced n-channel due to a small v_{DS}
- The current i_D flows from drain to source (opposite to the direction of the flow of negative charge)
- The current is proportional to the number of carriers in the induced channel
- The channel is controlled by the **effective voltage** or **overdrive voltage**: $v_{OV} \equiv v_{GS} - V_t$
- The electron charge in the channel due to the overdrive voltage: $|Q| = C_{ox}WLv_{OV}$
- **Gate oxide capacitance** C_{ox} is defined as capacitance per unit area
- MOSFET can be approximated as a linear resistor in this region with a resistance value inversely proportional to the excess gate voltage

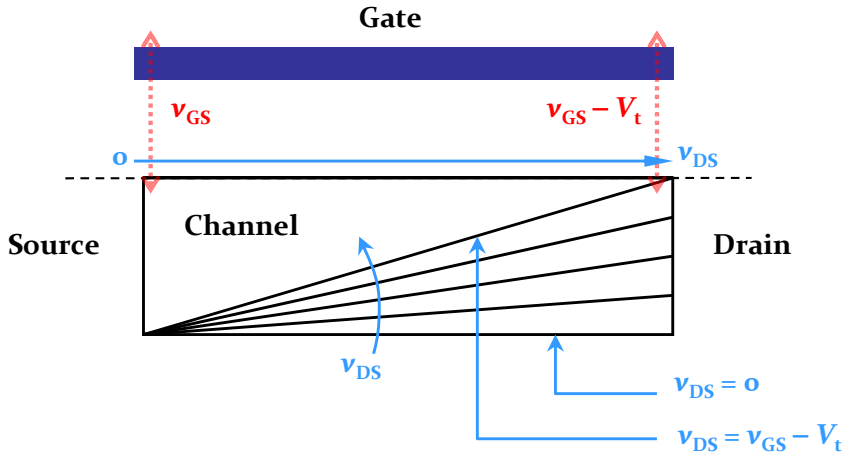




Operation as increasing drain voltage

- As v_{DS} increases, the voltage along the channel increases from o to v_{DS}
- The voltage between the gate and the points along the channel decreases from v_{GS} at the source end to (v_{GS}–v_{DS}) at the drain end
- Since the inversion layer depends on the voltage difference across the MOS structure, increasing v_{DS} will result in a tapered channel
- The resistance increases due to tapered channel and the i_D-v_{DS} curve is no longer a straight line
- At the point $v_{DSsat} = v_{GS}–V_t$, the channel is **pinched off** at the drain side
- Increasing v_{DS} beyond this value has little effect on the channel shape and i_D saturates at this value
- **Triode region**: $v_{DS} < v_{DSsat}$
- **Saturation region**: $v_{DS} \geq v_{DSsat}$





Derivation of the I-V relationship

- Induced charge in the channel due to MOS capacitor:

$$Q_I(x) = -C_{ox}[v_{GS} - V_t - v(x)]$$

- Equivalent resistance dR along the channel:

$$dR = \frac{dx}{qn(x)\mu_n h(x)W} = \frac{dx}{\mu_n W Q_I(x)}$$

- I-V derivations:

$$dv = i_D dR = \frac{i_D dx}{\mu_n W Q_I(x)} = \frac{i_D dx}{\mu_n C_{ox} W[v_{GS} - V_t - v(x)]}$$

$$\int_0^{v_{DS}} \mu_n C_{ox} W[v_{GS} - V_t - v(x)]dv = \int_0^L i_D dx$$

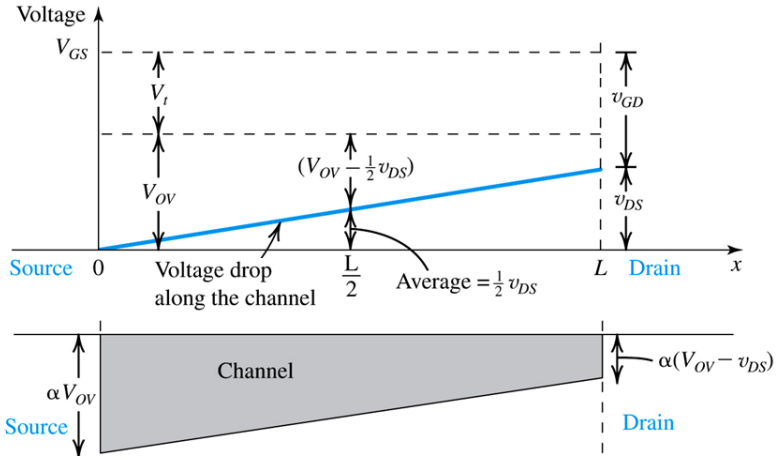
$$i_D = \mu_n C_{ox} \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$$

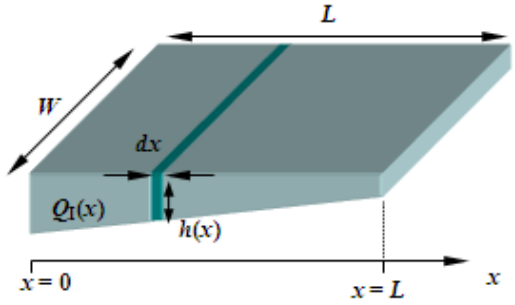
  - Process transconductance parameter (μA/V²): $k'_n = \mu_n C_{ox}$
  - Aspect ratio: W/L
  - Transconductance parameter (μA/V²): $k_n = \mu_n C_{ox}(W/L)$

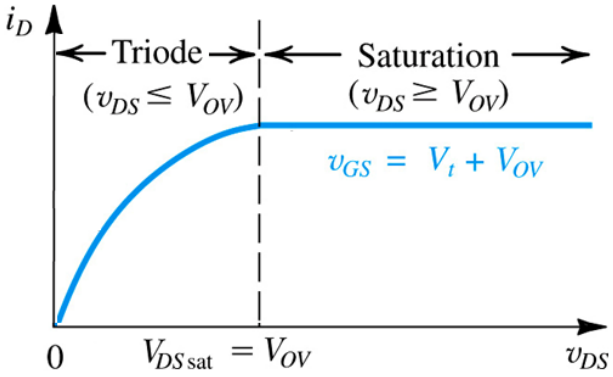
- Drain current of MOSFETs:
  - Triode region: $i_D = k_n[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$
  - Saturation region: $i_{Dsat} = \frac{1}{2}k_n(v_{GS} - V_t)^2$

- On-resistance (channel resistance for small v_{DS}):

$$r_{DS} = 1/k_n(v_{GS} - V_t)$$







The *p*-channel enhancement-type MOSFET

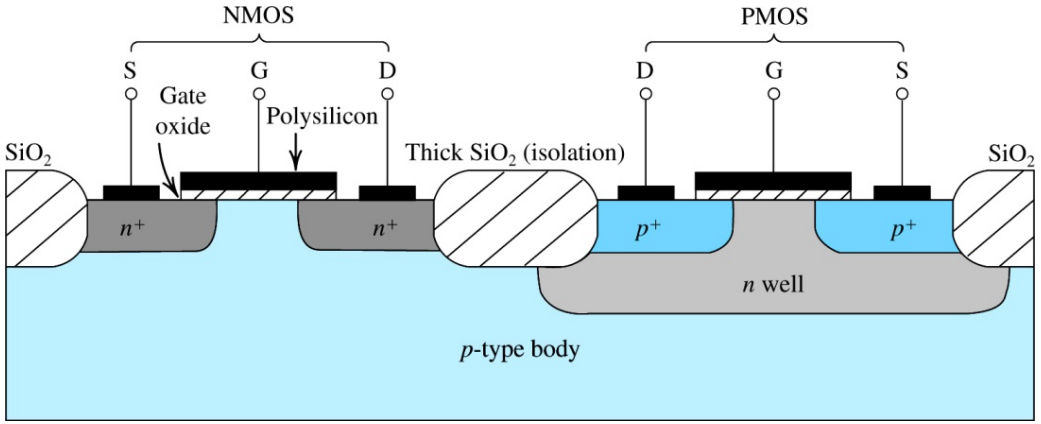
- *p*-channel enhanced-type MOSFETs are fabricated on *n*-type substrate with p^+ source and p^+ drain
- Normally, source is connected to high voltage and drain is connected to low voltage
- As a negative voltage applies to the gate, the resulting field pushes electrons in *n*-type substrate away from the surface, leaving behind a carrier-depletion region
- As gate voltage exceeds a negative **threshold voltage** V_t, holes accumulate on the substrate surface
- A *p*-type channel (**inversion layer**) is induced for current flow from source to drain
- Negative gate voltage is required to induce the channel → **enhancement-type** MOSFET

Complementary MOS (CMOS)

- CMOS technology employs both PMOS and NMOS devices
- If substrate is *p*-type, PMOS transistors are formed in *n* well (*n*-type body needed)
- If substrate is *n*-type, NMOS transistors are formed in *p* well (*p*-type body needed)
- The substrate and well are connected to voltages which reverse bias the junctions for device isolation

Exercise 5.1 (Textbook)

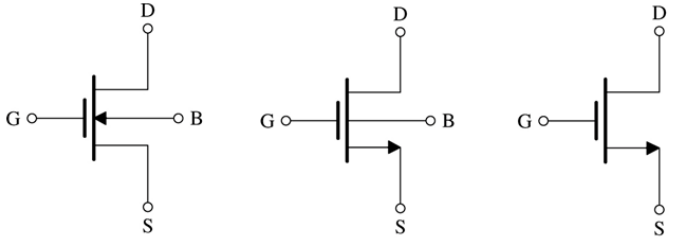
Exercise 5.2 (Textbook)



5.2 Current-Voltage Characteristics

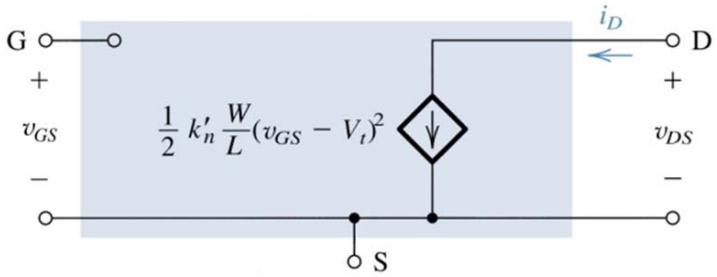
Circuit symbol

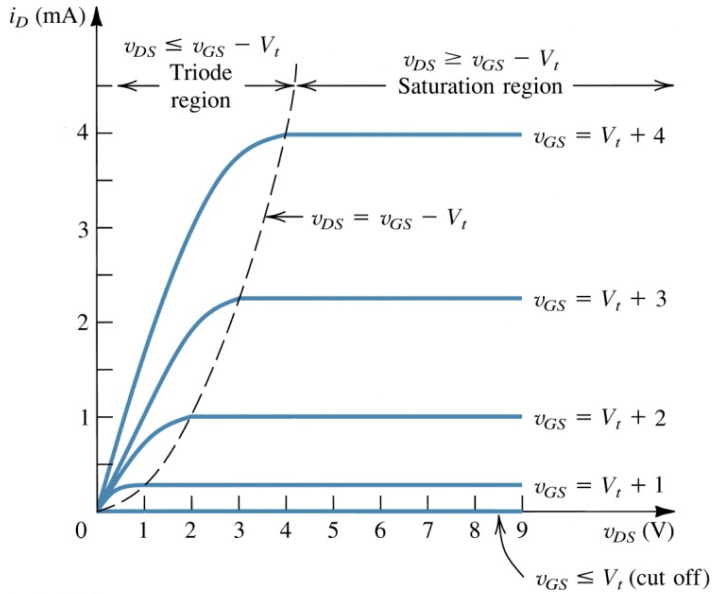
- *n*-channel enhancement-mode MOSFET

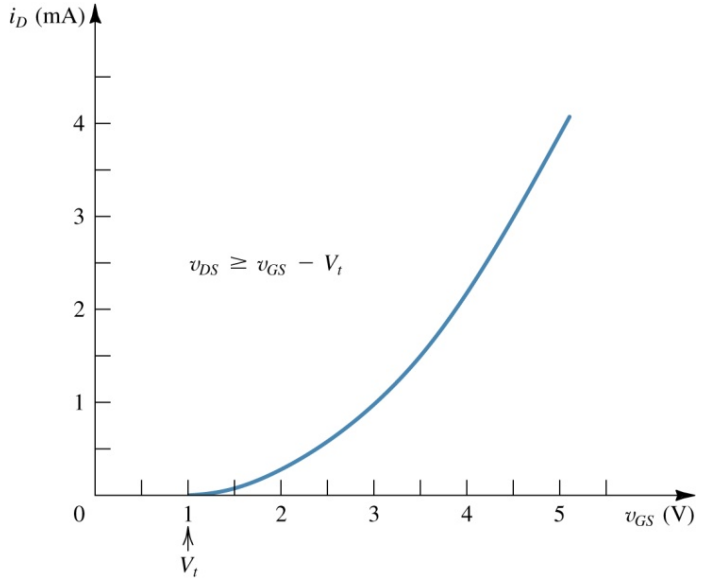


The current-voltage characteristics

- Cut-off region: ($v_{GS} \le V_t$)
  - ➔ $i_D = 0$
- Triode region: ($v_{GS} > V_t$ and $v_{DS} < v_{GS} - V_t$)
  - ➔ $i_D = \mu_n C_{ox} \frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$
- Saturation: ($v_{GS} > V_t$ and $v_{DS} \ge v_{GS} - V_t$)
  - ➔ $i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)^2$
- large-signal model (saturation)







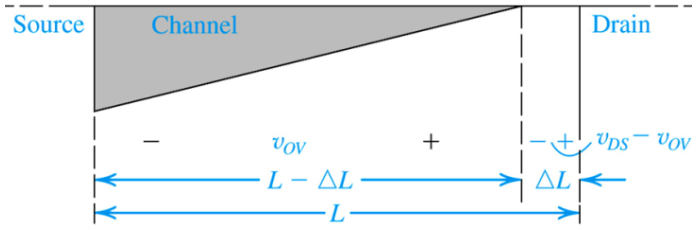
Channel length modulation

- The channel pinch-off point moves slightly away from drain as $v_{DS} > v_{DSsat}$
- The effective channel length (L_{eff}) reduces with v_{DS}
- Electrons travel to pinch-off point will be swept to drain by electric field
- The length accounted for conductance in the channel is replaced by L_{eff}:

$$\int_0^{v_{GS}-V_t} k_n' W[v_{GS}-V_t-v(x)]dv = \int_0^{L_{eff}} i_D dx$$

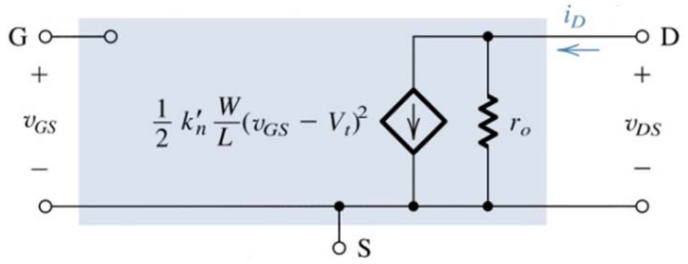
$$i_D = \frac{1}{2}k_n'\frac{W}{L_{eff}}(v_{GS}-V_t)^2 = \frac{1}{2}k_n'\frac{W}{L-\Delta L}(v_{GS}-V_t)^2 \approx \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2\left(1+\frac{\Delta L}{L}\right)$$

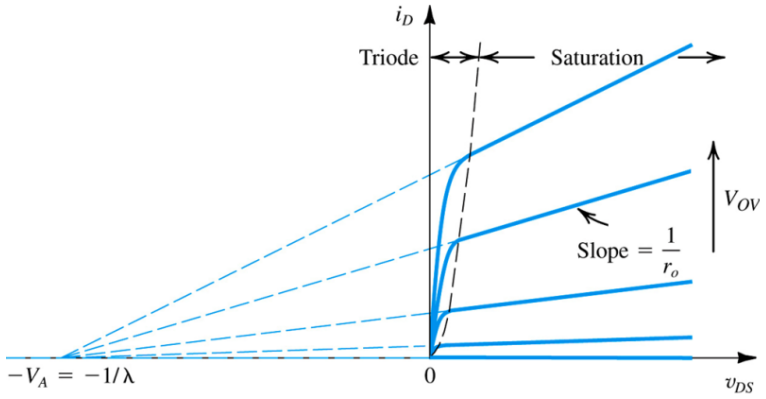
assuming that $\frac{\Delta L}{L} \propto v_{DS} \rightarrow i_D = \frac{1}{2}k_n'\frac{W}{L}(v_{GS}-V_t)^2(1+\lambda v_{DS})$



Finite output resistance

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}=constant} = \left[\lambda\frac{k_n'}{2}\frac{W}{L}(v_{GS}-V_t)^2\right]^{-1} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$





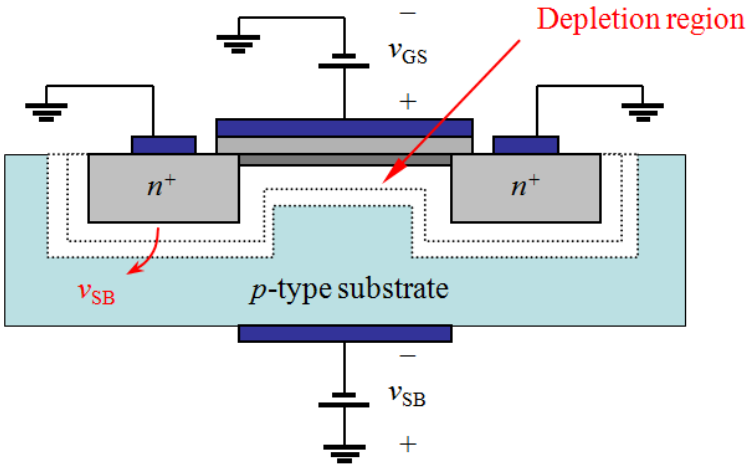
- V_A (**Early voltage**) = $1/\lambda$ is proportional to channel length: $V_A = V'_A L$
- V'_A is process-technology dependent with a typical value from 5 ~ 50 V/μm
- Due to the dependence of i_D on v_{DS}, MOSFET shows **finite output resistance** in saturation region

The body effect

- The BS and BD junction should be reverse biased for the device to function properly
- Normally, the body of a *n*-channel MOSFET is connected to the most negative voltage
- The depletion region widens in BS and BD junctions and under the channel as V_{SB} increases
- **Body effect**: V_t increases due to the excess charge in the depletion region under the channel
- The body effect can cause considerable degradation in circuit performance
- Threshold voltage:

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}]$$

$$\text{where } \gamma = \frac{\sqrt{2qN_A\varepsilon_{Si}}}{C_{ox}} \text{ and } \phi_f = \frac{kT}{q}\ln(\frac{N_A}{n_i})$$



- Current equations:

$$i_D = \mu_n C_{ox}\frac{W}{L}[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2]$$

$$i_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_t)^2$$

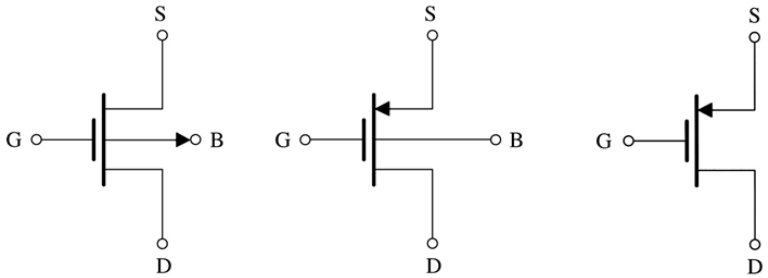
Temperature effect

- V_t decreases by ~2mV for every 1°C rise → i_D increases with temperature
- k'_n decreases with temperature → i_D decreases with increasing temperature
- For a given bias voltage, the overall observed effect of a temperature increase is a decrease in i_D

Breakdown and input protection

- Weak avalanche
  - *pn* junction between the drain and substrate suffers avalanche breakdown as V_{DS} increases
  - Large drain current is observed
  - Typical breakdown voltage 20 ~ 150 V
- Punch-through
  - Occurs at lower voltage (~20 V) for short channel devices
  - Drain current increases rapidly as the drain depletion region extends through the channel
  - Does not result in permanent damage to the device
- Gate-oxide breakdown
  - Gate-oxide breakdown occurs when gate-to-source voltage exceeds 30 V
  - Permanent damage to the device
- Input Protection
  - Protection circuit is needed for the input terminals of MOS integrated circuits
  - Using clamping diode for the input protection

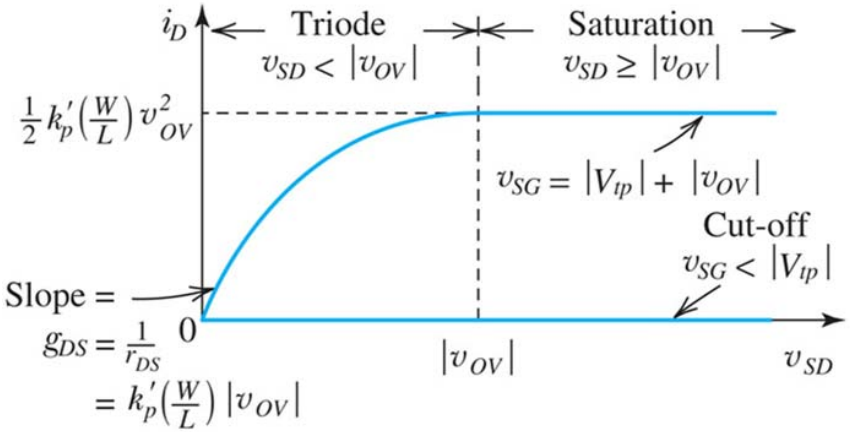
The *p*-channel enhancement-type MOSFET



- For a PMOS, the source is connected to high voltage and the drain is connected to low voltage
- To induce the *p*-channel for the MOSFET, a negative v_{GS} is required → V_t (threshold voltage) < oV
- The body is normally connected to the most positive voltage

The current-voltage characteristics

- Cut-off region: ($v_{GS} \geq V_{tp}$)
  - ➔ $i_D = 0$
- Triode region: ($v_{GS} < V_{tp}$ and $v_{DS} > v_{GS}-V_{tp}$)
  - ➔ $i_D = \mu_p C_{ox} \frac{W}{L}[(v_{GS}-V_{tp})v_{DS} - \frac{1}{2}v_{DS}^2]$
- Saturation: ($v_{GS} < V_{tp}$ and $v_{DS} \leq v_{GS}-V_{tp}$)
  - ➔ $i_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(v_{GS}-V_{tp})^2$



- Transconductance parameter $k'_p = \mu_p C_{ox} \approx 0.4\, k'_n$
- The values of v_{GS}, v_{DS}, V_t and λ for *p*-channel MOSFET operation are all negative
- Drain current i_D is still defined as a positive current

Exercise 5.4 (Textbook)

Exercise 5.5 (Textbook)

Exercise 5.6 (Textbook)

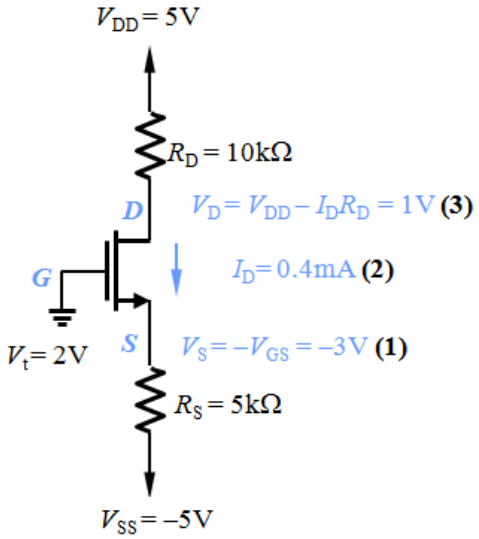
Exercise 5.7 (Textbook)

5.3 MOSFET Circuits at DC

DC analysis for MOSFET circuits

- Assume the operation mode and solve the dc bias utilizing the corresponding current equation
- Verify the assumption with terminal voltages (cutoff, triode and saturation)
- If the solution is invalid, change the assumption of operation mode and analyze again

DC analysis example

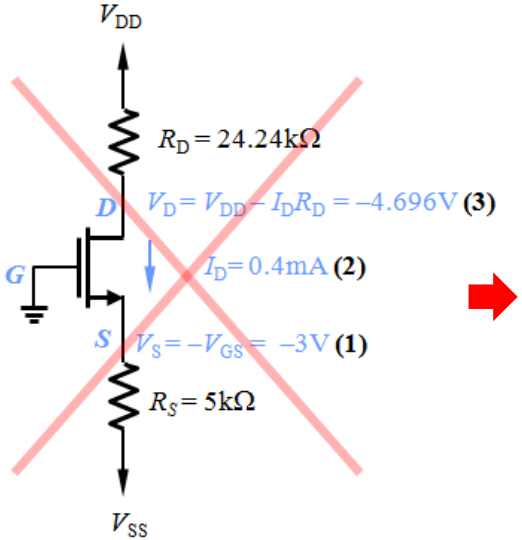


Assuming MOSFET in saturation

$$-V_{SS}=V_{GS}+I_DR_S=V_{GS}+\frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2R_S$$

$$\rightarrow V_{GS}=3V \text{ or } 1V(\text{not a valid solution})$$

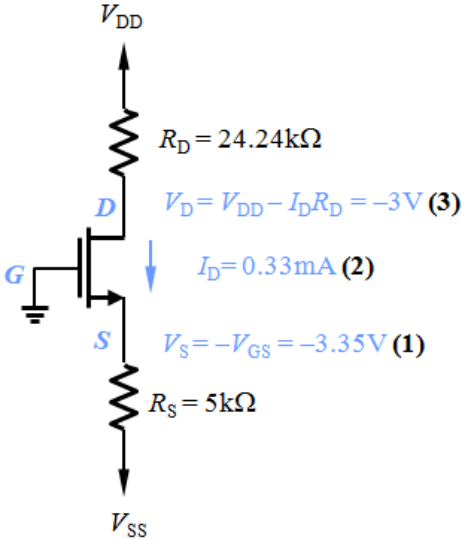
$$(V_{DS}=4\text{V})\geq(V_{GS}-V_t=1\text{V})\rightarrow \text{saturation}$$



Assuming MOSFET in saturation

$$\rightarrow V_{GS}=3V \text{ and } V_{DS}=-1.696V$$

$$V_{DS}<V_{GS}-V_t\rightarrow \text{not in saturation!}$$



Assuming MOSFET in triode

$$I_D=k_n'\frac{W}{L}[(V_{GS}-V_t)V_{DS}-\frac{1}{2}V_{DS}^2]$$

$$V_{GS}+I_DR_S=-V_{SS}$$

$$V_{DS}+I_D(R_D+R_S)=V_{DD}-V_{SS}$$

$$\rightarrow V_{GS}=3.35V, V_{DS}=0.35V \text{ and } I_D=0.33mA$$

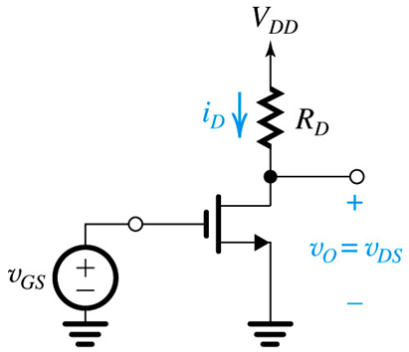
$$V_{DS}<V_{GS}-V_t\rightarrow \text{in triode}$$

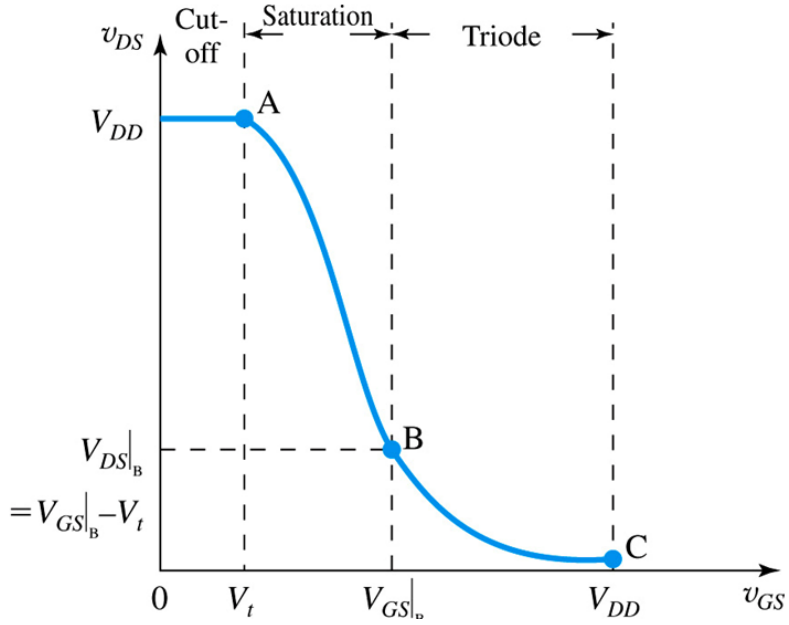
Exercise 5.8 (Textbook)
Exercise 5.9 (Textbook)
Exercise 5.10 (Textbook)
Example 5.5 (Textbook)
Example 5.6 (Textbook)
Exercise 5.12 (Textbook)
Example 5.7 (Textbook)
Example 5.8 (Textbook)

5.4 Applying the MOSFET in Amplifier Design

MOSFET voltage amplifier

- MOSFET with a resistive load R_D can be used as a voltage amplifier
- The voltage transfer characteristic (VTC)
  - The plot of v_I (v_{GS}) versus v_O (v_{DS})
  - DC analysis as v_{GS} increases from o to V_{DD}
  - Cutoff mode: (o V ≤ v_{GS} < V_t)
    - ➔ $i_D = 0$
    - ➔ $v_O = v_{DS} = V_{DD}$
  - Saturation mode: (v_{GS} > V_t)
    - ➔ $i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2$
    - ➔ $v_O = v_{DS} = V_{DD} - \frac{1}{2} k_n (v_{GS} - V_t)^2 R_D$
  - Triode mode: (v_{GS} further increases)
    - ➔ $i_D = k_n [(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2]$
    - ➔ $v_O = v_{DS} = V_{DD} - k_n [(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2] R_D$





Biasing the MOSFET to obtain linear amplification

- The slope in the VTC indicates voltage gain
- MOSFET in saturation can be used as voltage amplification
- Point Q is known as **bias point** or **dc operating point**
  - ➔ $V_{DS} = V_{DD} - \frac{1}{2} k_n (V_{GS} - V_t)^2 R_D$
- The signal to be amplified is superimposed on V_{GS}
  - ➔ $v_{GS}(t) = V_{GS} + v_{gs}(t)$
- The time-varying part in $v_{GS}(t)$ is the amplified signal
- The circuit can be used as a linear amplifier if:
  - A proper bias point is chosen for gain
  - The input signal is small in amplitude

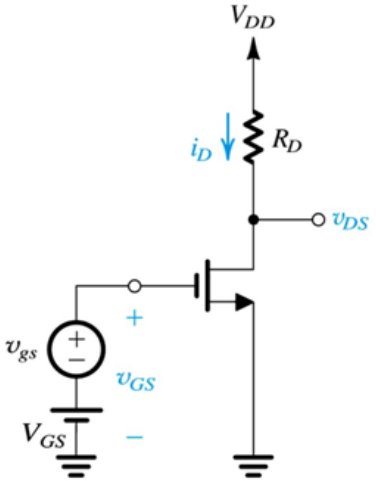
The small-signal voltage gain

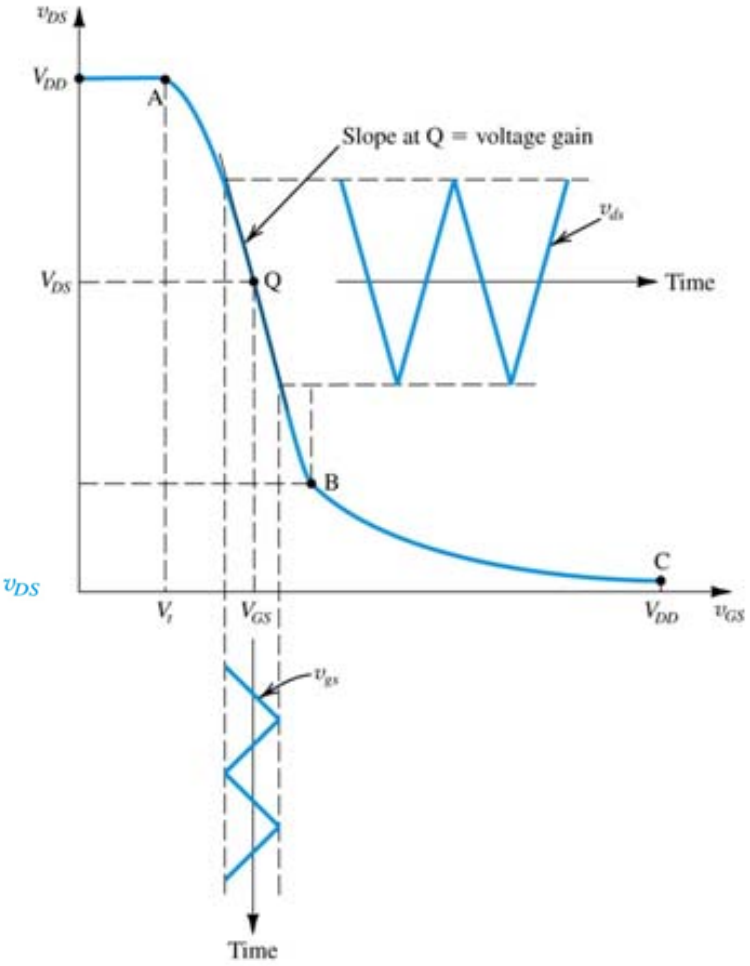
- The amplifier gain is the slope at Q:

$$A_v \equiv \frac{dv_{DS}}{dv_{GS}}\Big|_{v_{GS}=V_{GS}} = -k_n (V_{GS} - V_t) R_D = -k_n V_{OV} R_D$$

- Maximum voltage gain of the amplifier

$$|A_v| = \left| -\frac{I_D R_D}{V_{OV}/2} \right| < \frac{V_{DD}}{V_{OV}/2} = |A_{v\max}|$$



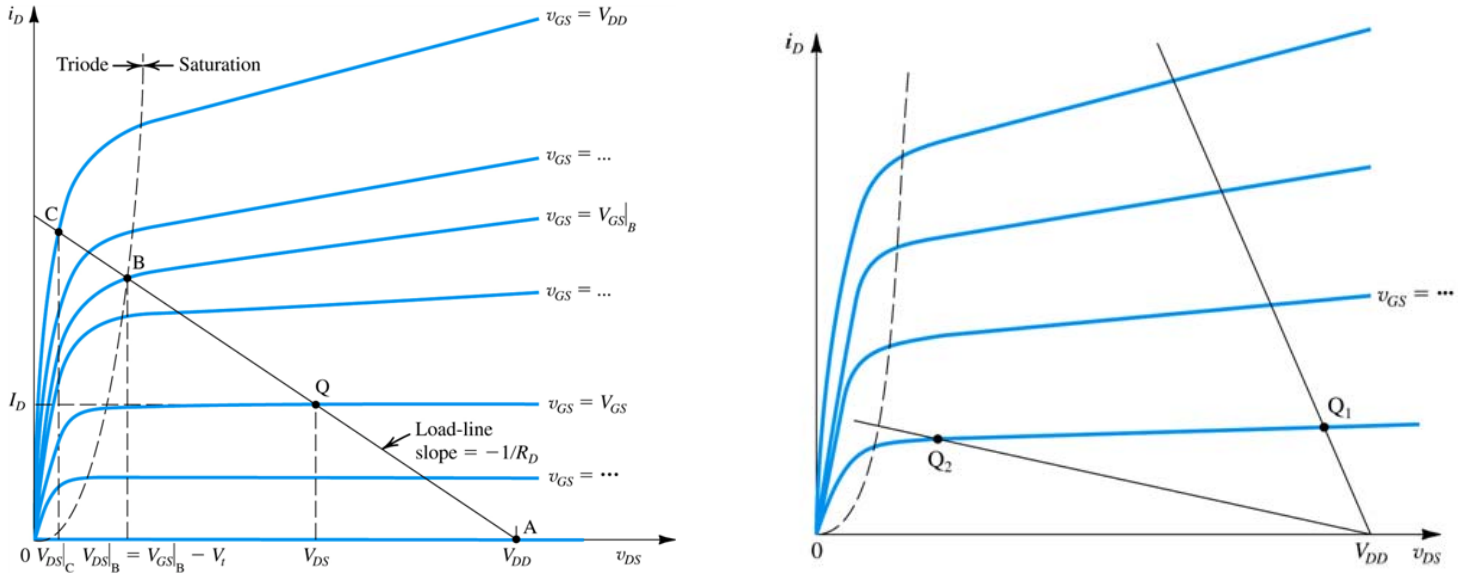


Determining the VTC by graphical analysis

- Provides more insight into the circuit operation
- **Load line**: the straight line represents in effect the load
  - ➔ $i_D = (V_{DD} - v_{DS})/R_D$
- The operating point is the intersection point

Locating the bias point *Q*

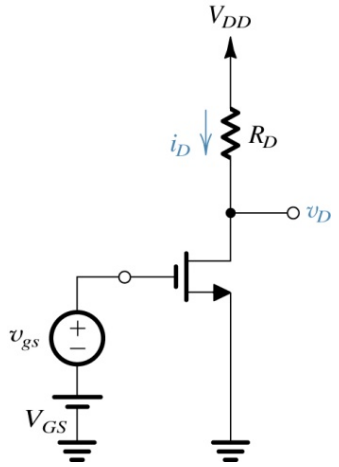
- The bias point (intersection) is determined by properly choosing the load line
- The output voltage is bounded by V_{DD} (upper bound) and V_{OV} (lower bound)
- The load line determines the voltage gain
- The bias point determines the maximum upper/lower voltage swing of the amplifier



5.5 Small-Signal Operation and Models

The DC bias point

- MOSFET in saturation
  - Drain current: $I_D = \frac{1}{2}k_n(V_{GS}-V_t)^2 = \frac{1}{2}k_n V_{OV}^2$
  - Drain voltage: $V_{DS} = V_{DD} - I_D R_D > V_{OV}$
- The small-signal circuit parameters are determined by the bias point



The small-signal operation

- The small-signal drain current:

$$v_{GS} = V_{GS} + v_{gs}$$

$$i_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}+v_{gs}-V_t)^2 = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2 + k_n'\frac{W}{L}(V_{GS}-V_t)v_{gs} + \frac{1}{2}k_n'\frac{W}{L}v_{gs}^2$$

$$\approx \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_t)^2 + k_n'\frac{W}{L}(V_{GS}-V_t)v_{gs} = I_D + i_d$$

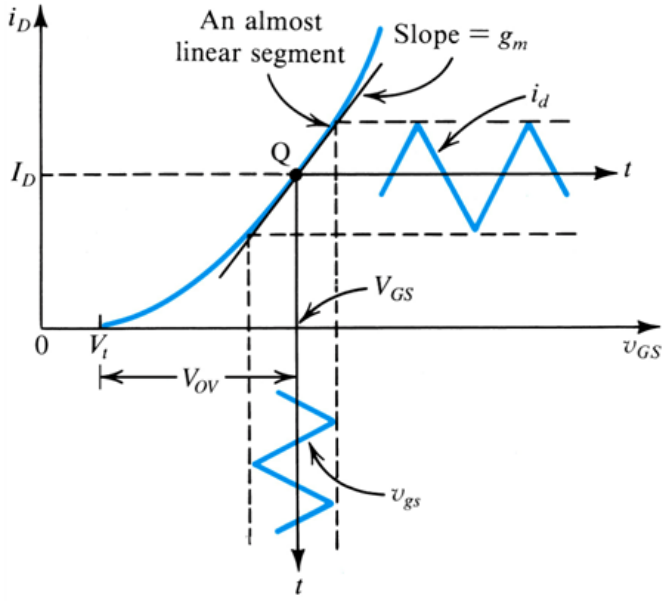
$$\rightarrow i_d = k_n'\frac{W}{L}(V_{GS}-V_t)v_{gs}$$

- The small-signal voltage gain:

$$v_D = V_{DD} - i_D R_D = V_{DD} - (I_D + i_d)R_D = V_D - i_d R_d = V_D + v_d$$

$$\rightarrow v_d = -i_d R_D = -k_n'\frac{W}{L}V_{OV}R_D v_{gs}$$

$$\rightarrow A_v \equiv \frac{v_d}{v_{gs}} = -k_n'\frac{W}{L}V_{OV}R_D$$



The small-signal parameters

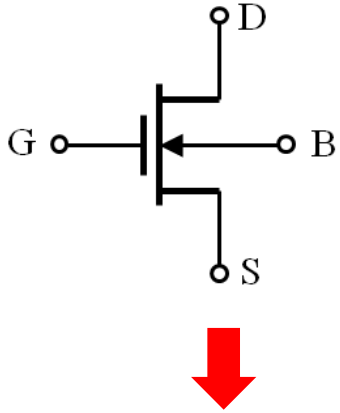
- Transconductance (g_m): describes how i_d change with v_{gs}

$$g_m \equiv \frac{i_d}{v_{gs}} = \frac{\partial i_D}{\partial v_{GS}}\bigg|_{v_{GS}=V_{GS}} = k_n' \frac{W}{L}(V_{GS} - V_t) = \sqrt{2k_n' \frac{W}{L} I_D}$$

- Output resistance (r_o): describes how i_d change with v_{ds}

$$r_o \equiv [\frac{\partial i_D}{\partial v_{DS}}]^{-1}_{v_{GS}=constant} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$$

  - Drain current varies with v_{DS} due to channel length modulation
  - Finite r_o to model the linear dependence of i_D on v_{DS}
  - The effect can be neglected if r_o is sufficiently large



- Body transconductance (g_{mb}): describes how i_d changes with v_{bs}

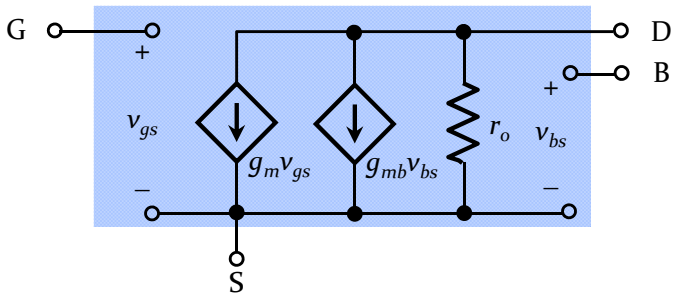
$$i_D = \frac{1}{2} k_n' \frac{W}{L}(v_{GS} - V_t)^2$$

$$\rightarrow g_{mb} \equiv \frac{\partial i_D}{\partial v_{BS}}\bigg|_{\substack{v_{GS}=\text{constant} \\ v_{DS}=\text{constant}}} = \frac{\partial i_D}{\partial V_t}\frac{\partial V_t}{\partial v_{BS}} = -k_n' \frac{W}{L}(v_{GS} - V_t)\frac{\partial V_t}{\partial v_{BS}} = g_m \frac{\partial V_t}{\partial v_{SB}}$$

$$V_t = V_{t0} + \gamma[\sqrt{2\phi_F + v_{SB}} - \sqrt{2\phi_F}] \text{ where } \gamma = \sqrt{2qN_A\varepsilon_{Si}} / C_{ox}$$

$$\rightarrow \frac{\partial V_t}{\partial v_{SB}} \equiv \chi = \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}}$$

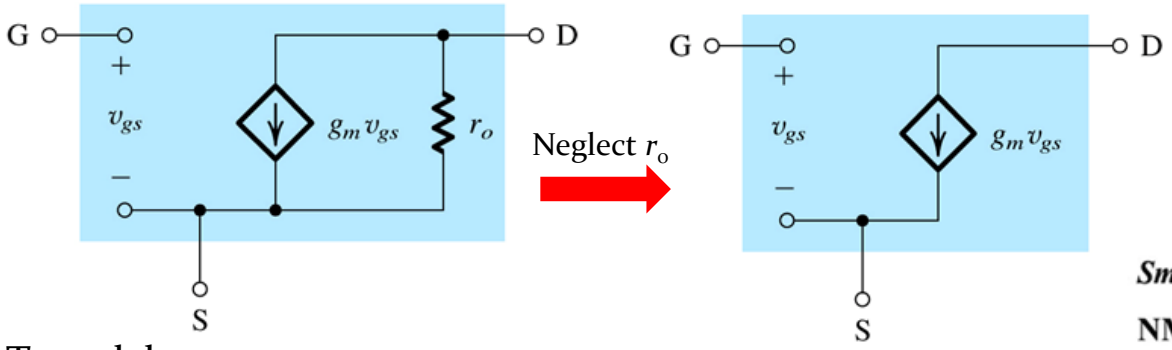
$$g_{mb} = g_m \chi$$



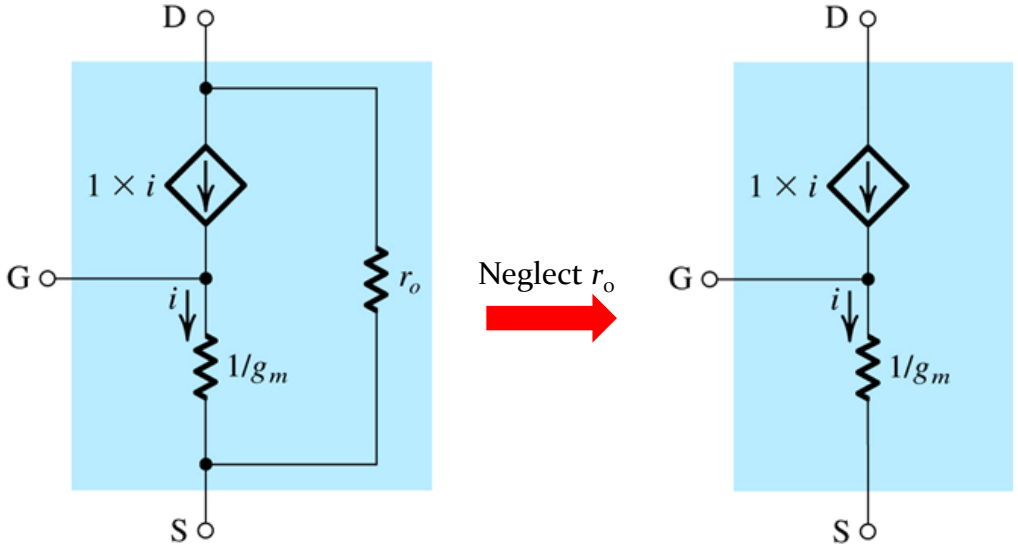
  - The body effect of the MOSFET is modeled by g_{mb}
  - Can be neglected if body and source are connected together

The small-signal equivalent circuit models

❑ Hybrid-π model



❑ T-model



Small-Signal Parameters

NMOS transistors

- Transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

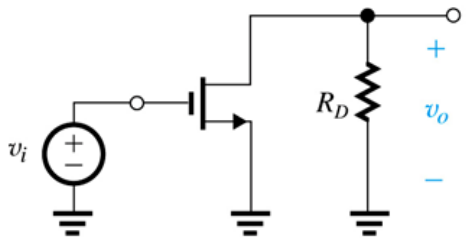
- Output resistance:

$$r_o = V_A / I_D = 1/\lambda I_D$$

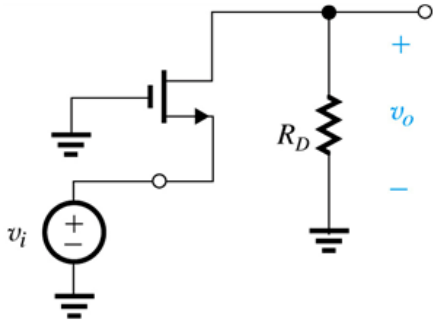
5.6 Basic MOSFET Amplifier Configuration

Three basic configurations

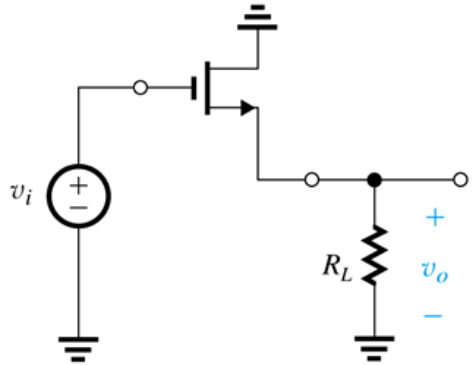
Common-Source (CS)



Common-Gete (CG)

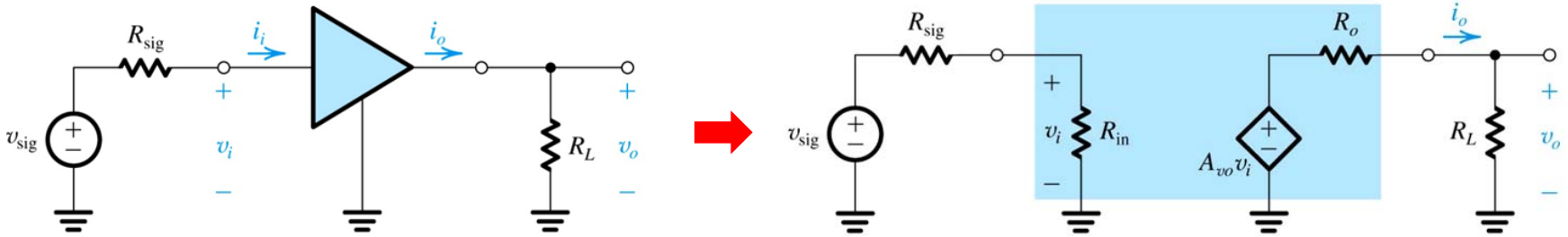


Common-Drain (CD)



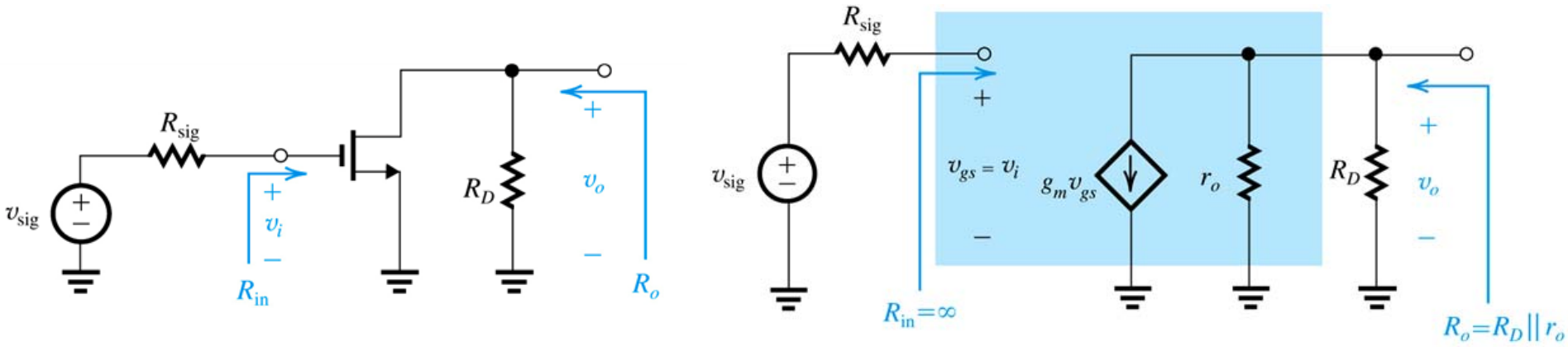
Characterizing amplifiers

- The MOSFET circuits can be characterized by a voltage amplifier model (unilateral model)
- The electrical properties of the amplifier is represented by R_{in}, R_o and A_{vo}
- The analysis is based on the small-signal or linear equivalent circuit (dc components not included)
- Voltage gain: $A_v \equiv \dfrac{v_o}{v_i} = \dfrac{R_L}{R_L + R_o} A_{vo}$
- Overall voltage gain: $G_v \equiv \dfrac{v_o}{v_{sig}} = \dfrac{R_{in}}{R_{in} + R_{sig}} A_v = \dfrac{R_{in}}{R_{in} + R_{sig}} \dfrac{R_L}{R_L + R_{so}} A_{vo}$



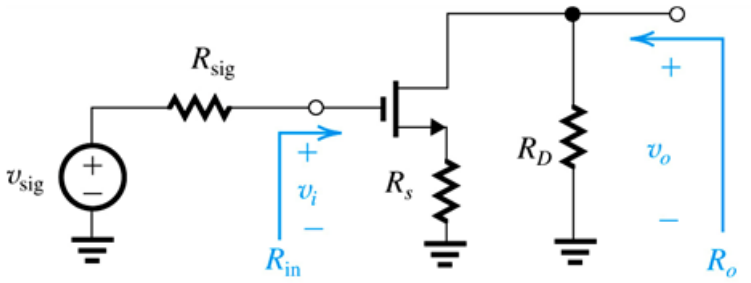
The common-source (CS) amplifier

- Characteristic parameters of the CS amplifier
  - Input resistance: $R_{in} = \infty$
  - Output resistance: $R_o = R_D \,||\, r_o \approx R_D$
  - Open-circuit voltage gain: $A_{vo} = -g_m(R_D \,||\, r_o) \approx -g_m R_D$
  - Voltage gain: $A_v = -g_m(R_D \,||\, R_L \,||\, r_o) \approx -g_m(R_D \,||\, R_L)$
- CS amplifier can provide high voltage gain
- Input and output are out of phase due to negative gain
- Output resistance is moderate to high
- Small R_D reduces R_o at the cost of voltage gain

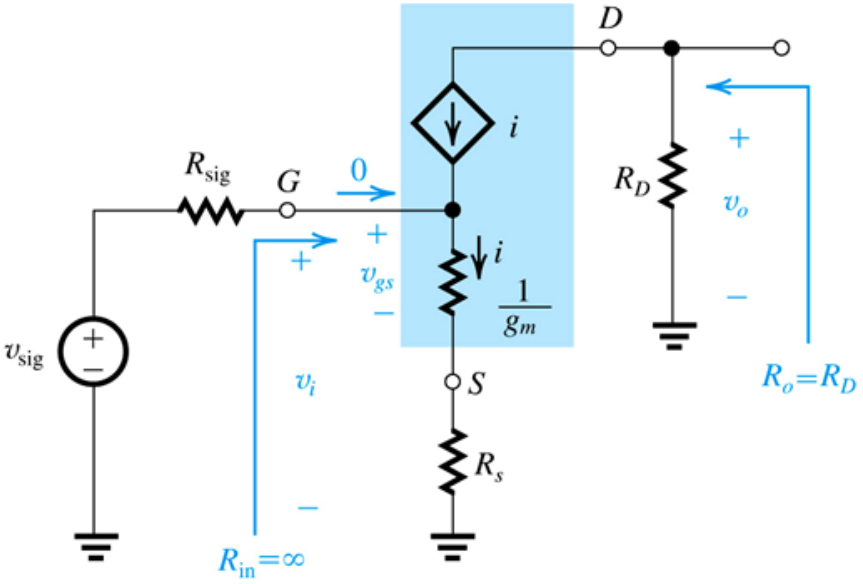


The common-source (CS) with a source resistance

- Characteristic parameters (by neglecting r_o)
  - Input resistance:
    $R_{in} = \infty$
  - Output resistance:
    $R_o = R_D$
  - Open-circuit voltage gain:
    $$A_{vo} = -\frac{g_m R_D}{1 + g_m R_s}$$
  - Voltage gain:
    $$A_v = -\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s}$$
  - Overall voltage gain:
    $$G_v = -\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s}$$

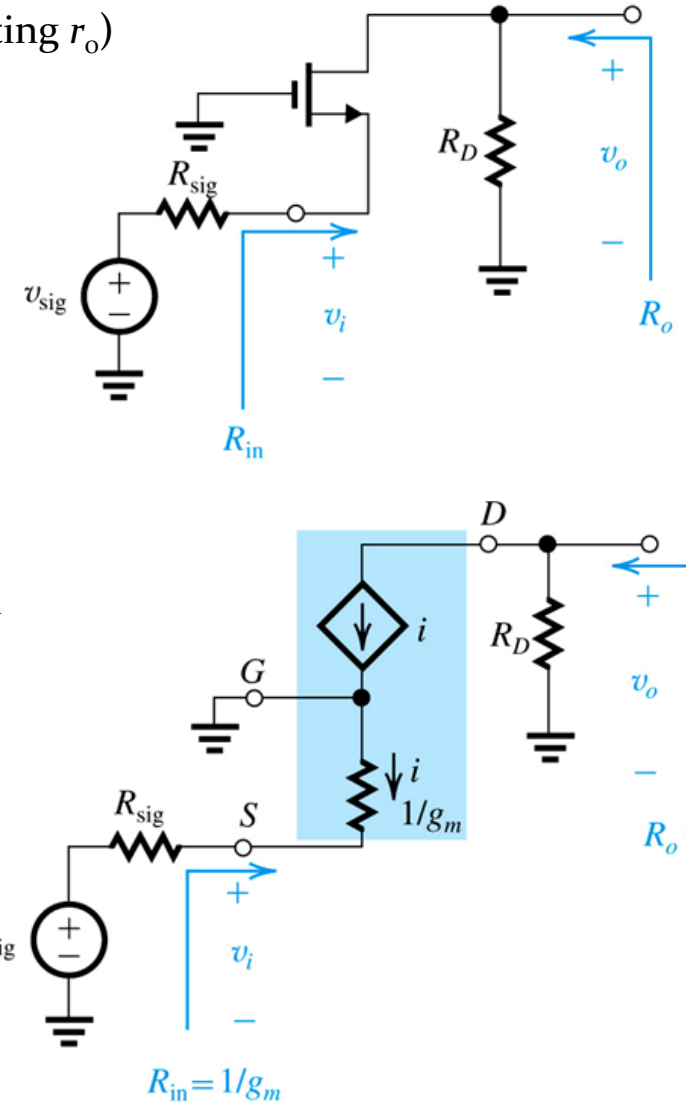


- **Source degeneration resistance** R_s is adopted
- Gain is reduced by the factor $(1+g_m R_s)$
- Considered a negative feedback of the amplifier



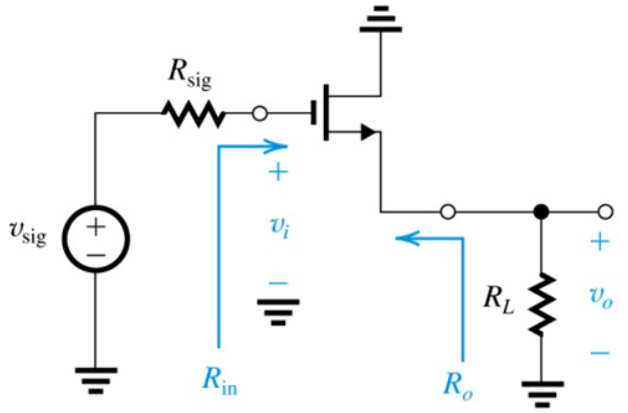
The common-gate (CG) amplifier

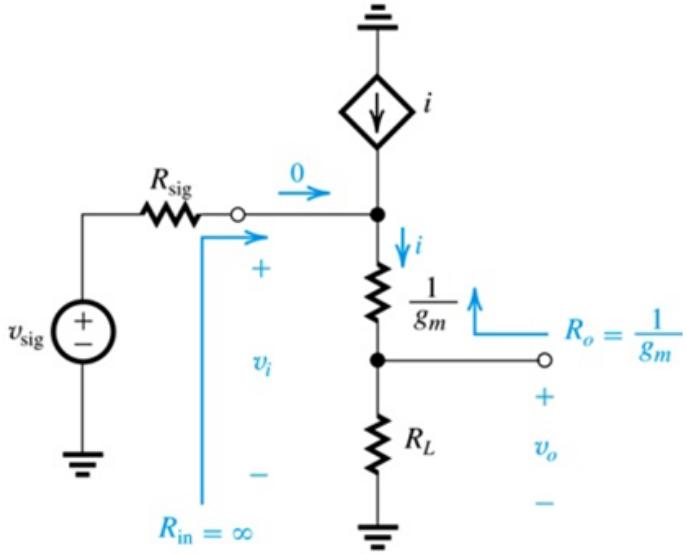
- Characteristic parameters of the CG amplifier (by neglecting r_o)
  - Input resistance: $R_{in} = 1/g_m$
  - Output resistance: $R_o = R_D$
  - Open-circuit voltage gain: $A_{vo} = g_m R_D$
  - Voltage gain: $A_v = g_m(R_D \parallel R_L)$
  - Overall voltage gain: $G_v = \dfrac{1}{1+g_m R_{sig}} g_m(R_D \parallel R_L)$
- CG amplifier can provide high voltage gain
- Input and output are in-phase due to positive gain
- Input resistance is very low
- A single CG stage is not suitable for voltage amplification
- Output resistance is moderate to high
- Small R_D reduces R_o at the cost of voltage gain
- The amplifier is no longer unilateral if r_o is included



The common-collector (CD) amplifier

- Characteristic parameters of the CD amplifier (by neglecting r_o)
  - Input resistance: $R_{in} = \infty$
  - Output resistance: $R_o = 1/g_m$
  - Voltage gain: $A_v = R_L/(R_L + 1/g_m) = g_m R_L/(g_m R_L + 1) \approx 1$
  - Overall voltage gain: $G_v = (R_L)/(R_L + 1/g_m) = g_m R_L/(g_m R_L + 1) \approx 1$
- CD amplifier is also called **source follower**.
- Input resistance is very high
- Output resistance is very low
- The voltage gain is less than but can be close to 1
- CD amplifier can be used as voltage buffer





5.7 Biasing in MOS Amplifier Circuits

DC bias for MOSFET amplifier

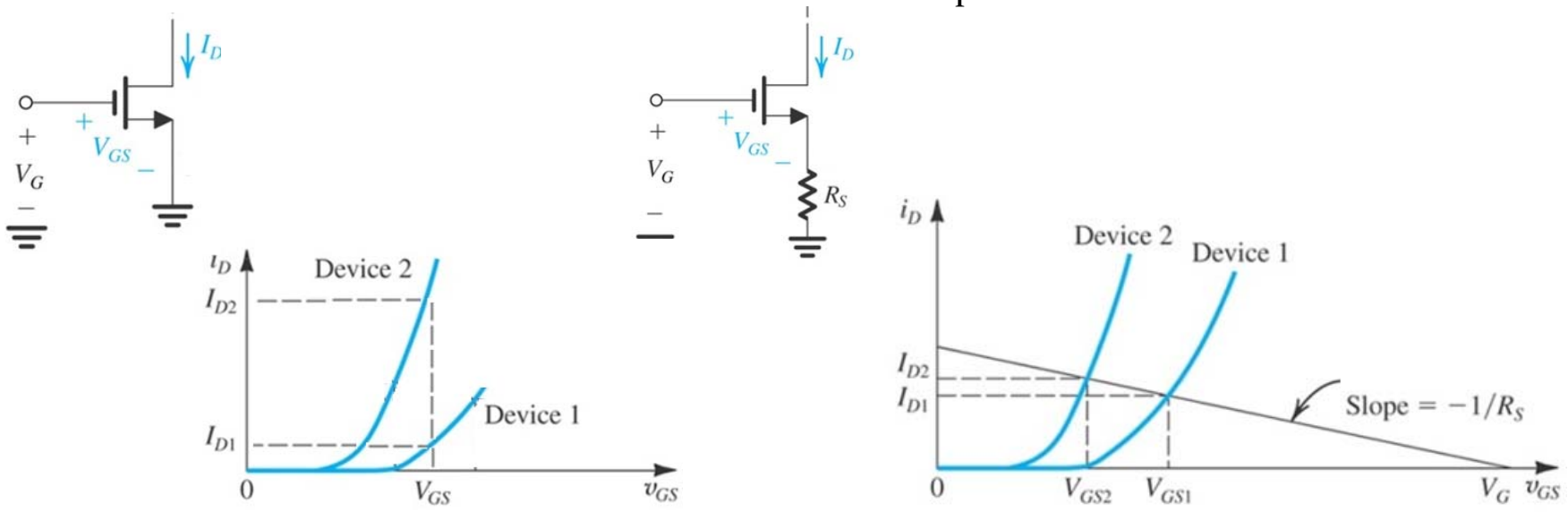
- The amplifiers are operating at a proper dc bias point
- Linear signal amplification is provided based on small-signal circuit operation
- The DC bias circuit is to ensure the MOSFET in **saturation** with a proper collector current I_D

Biasing by fixing gate-to-source voltage

- Fix the dc voltage V_{GS} to specify the saturation current of the MOSFET: $I_D = \frac{1}{2}k_n(V_{GS}-V_t)^2 = \frac{1}{2}k_n(V_G-V_t)^2$
- Bias current deviates from the desirable value due to variations in the device parameters V_t and μ_n

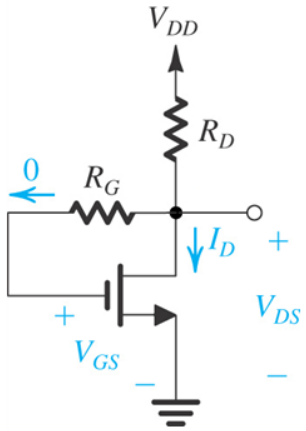
Biasing by fixing gate voltage and connecting a source resistance

- The bias condition is specified by: $V_G = V_{GS} + \frac{1}{2}k_n(V_{GS}-V_t)^2 R_S$ and $I_D = \frac{1}{2}k_n(V_{GS}-V_t)^2$
- Drain current has better tolerance to variations in the device parameters



Biasing using a drain-to-gate feedback resistor

- A single power supply is needed
- R_G ensures the MOSFET in saturation ($V_{GS} = V_{DS}$)
- MOSFET operating point: $\frac{V_{DD} - V_{GS}}{R_D} = \frac{1}{2} k_n (V_{GS} - V_t)^2$
- The value of the feedback resistor R_G affects the small-signal gain



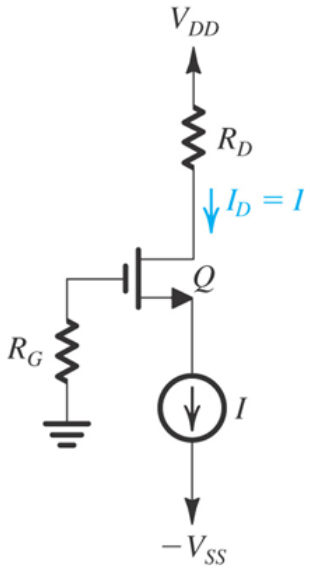
Biasing using a constant-current source

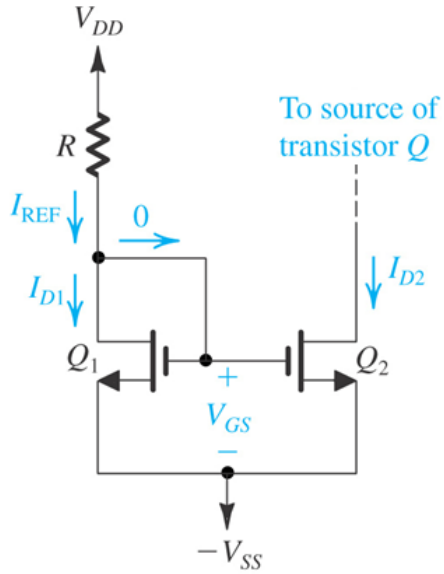
- The MOSFET can be biased with a constant current source I
- The resistor R_D is chosen to operate the MOSFET in active mode
- The current source is typically a current mirror
- Current mirror circuit:
  - MOSFETs Q_1 and Q_2 are in saturation
  - The reference current $I_{REF} = I = I_D$

$$\frac{V_{DD} - V_{GS}}{R} = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

$$I_{REF} = \frac{1}{2} k_n (V_{GS} - V_t)^2$$

  - When applying to the amplifier circuit, the voltage V_{D2} has to be high enough to ensure Q_2 in saturation





Example 6.11 (Textbook)

Exercise 6.31 (Textbook)

Exercise 6.32 (Textbook)

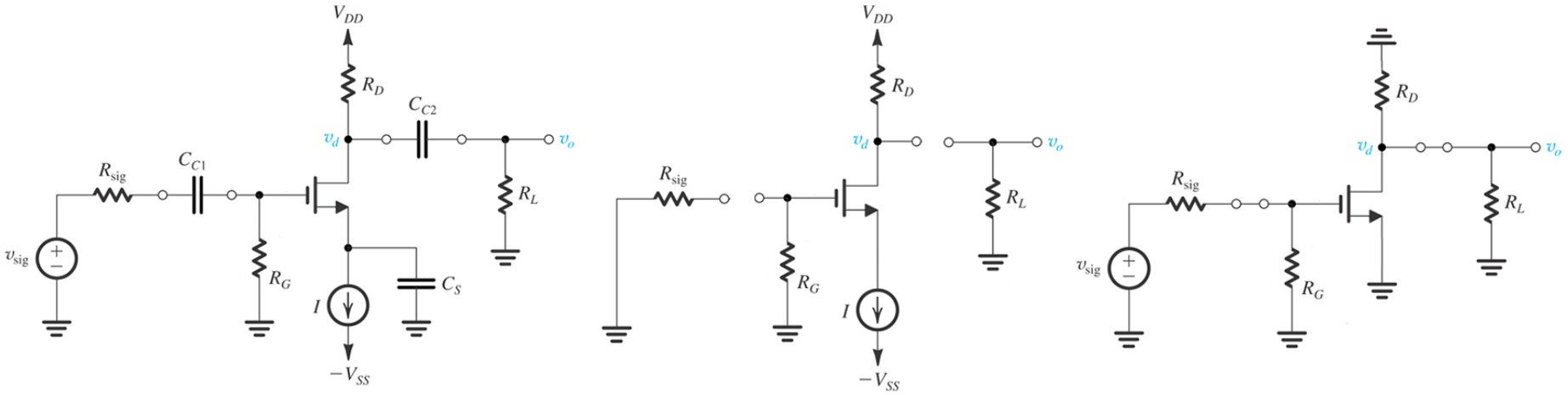
Exercise 6.33 (Textbook)

5.8 Discrete-Circuit MOS Amplifiers

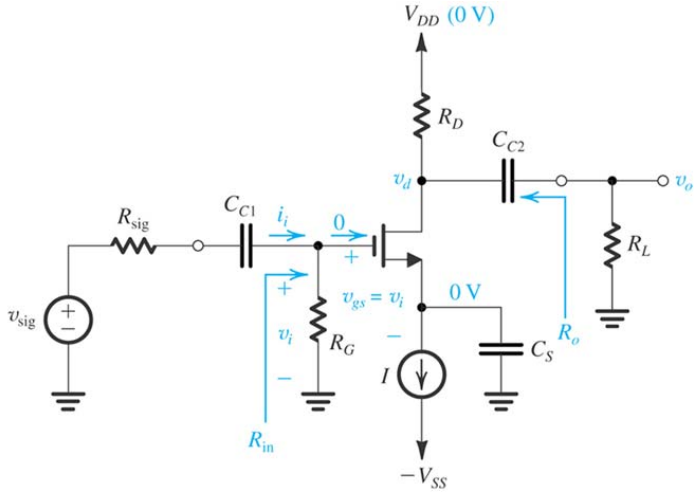
Circuit analysis:

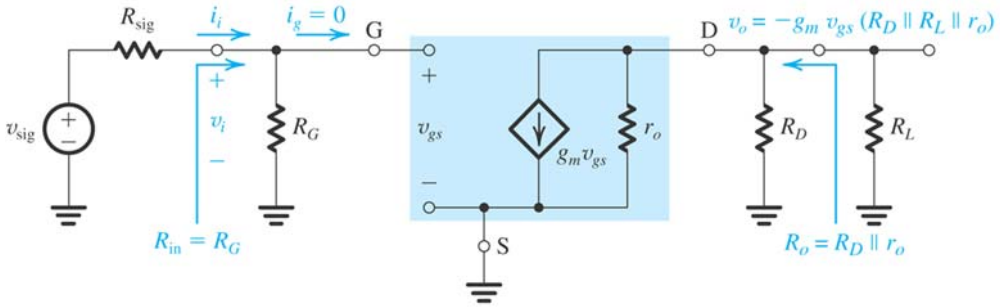
- DC analysis:
  - Remove all ac sources (short for voltage source and open for current source)
  - All capacitors are considered open-circuit
  - DC analysis of MOSFET circuits for all nodal voltages and branch currents
  - Find the dc current I_D and make sure the MOSFET is in saturation
- AC analysis:
  - Remove all dc sources (short for voltage source and open for current source)
  - All **large capacitors** are considered short-circuit
  - Replace the MOSFET with its small-signal model for ac analysis
  - The circuit parameters in the small-signal model are obtained based on the value of I_D

Complete amplifier circuit **DC equivalent circuit** **AC equivalent circuit**

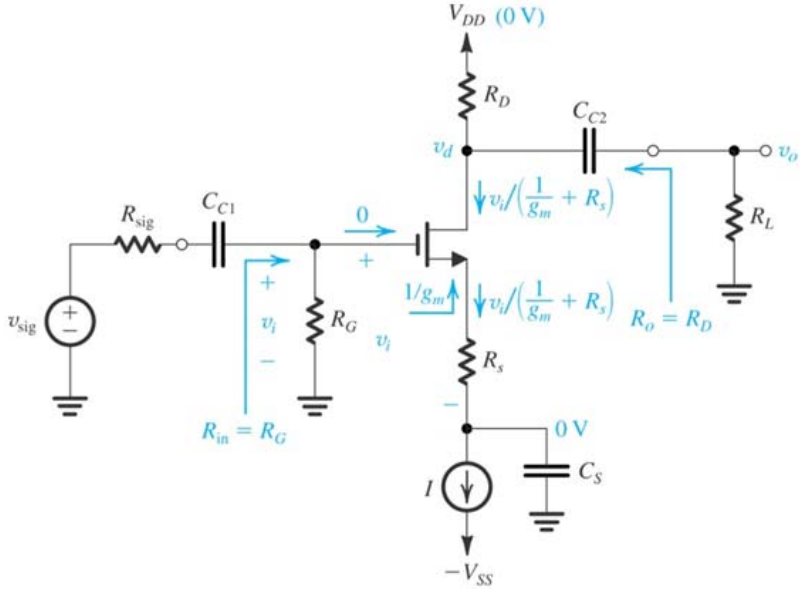


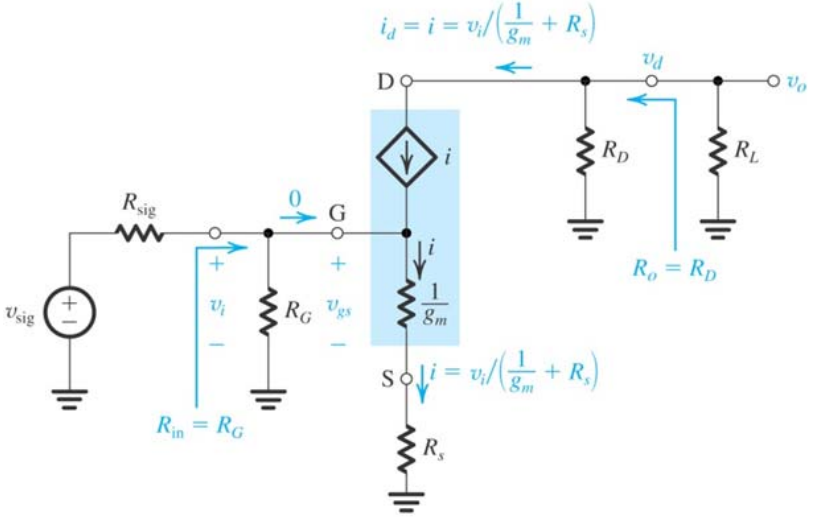
The common-source (CS) amplifier



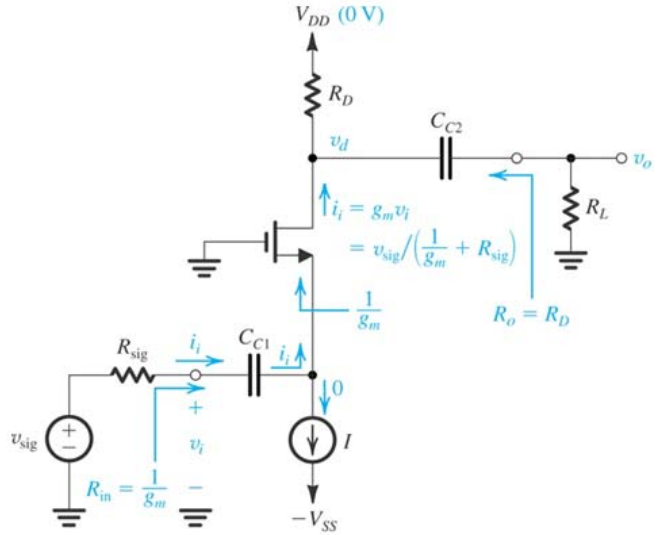


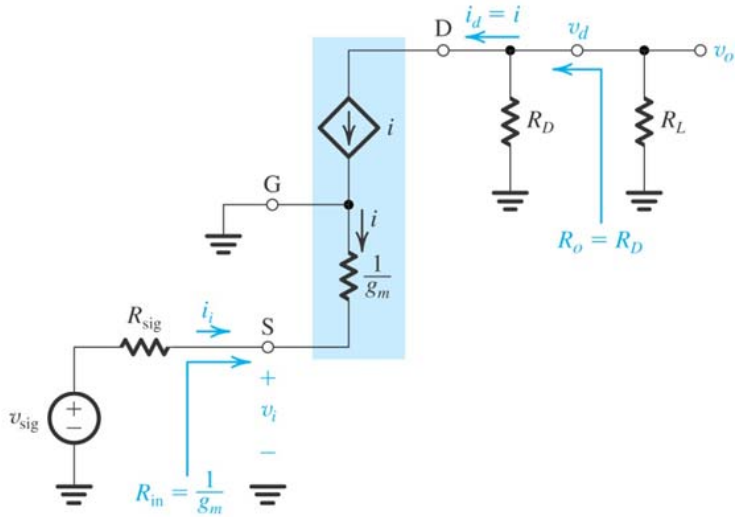
The common-source amplifier with a source resistance



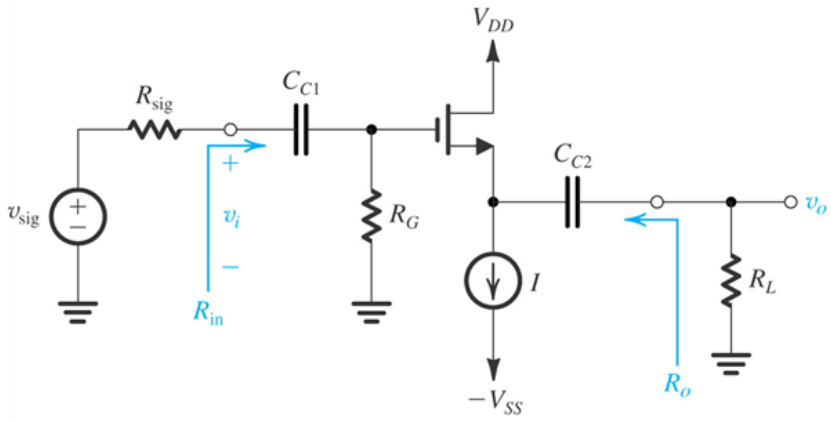


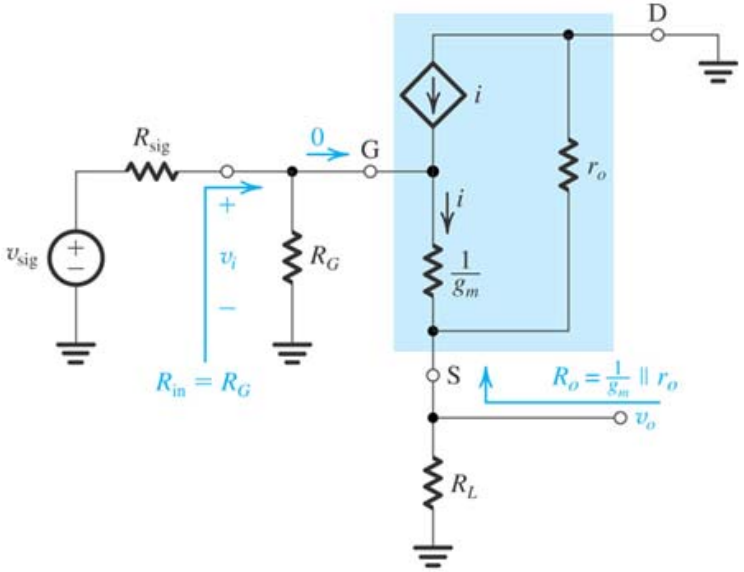
The common-gate (CG) amplifier





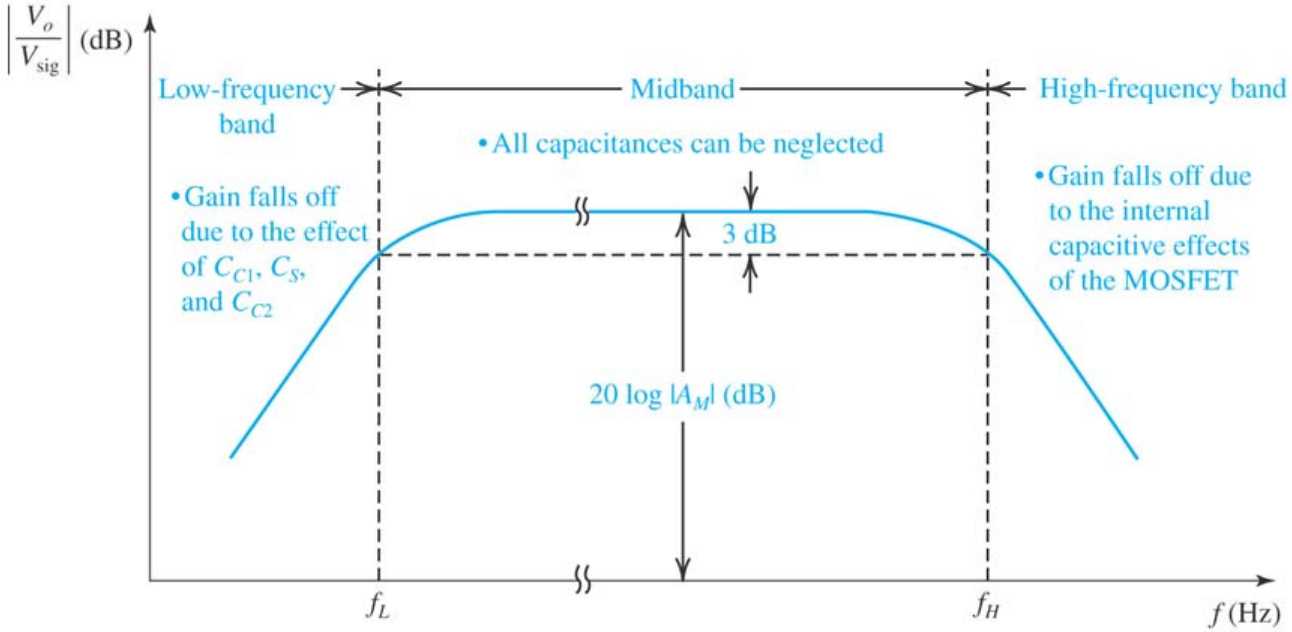
The common-drain (CD) amplifier





The amplifier frequency response

- The gain falls off at low frequency band due to the effects of the coupling and by-pass capacitors
- The gain falls off at high frequency band due to the internal capacitive effects in the MOSFETs
- Midband:
  - All coupling and by-pass capacitors (large capacitance) are considered short-circuit
  - All internal capacitive effects (small capacitance) are considered open-circuit
  - Midband gain is nearly constant and is evaluated by small-signal analysis
  - The bandwidth is defined as $BW = f_H - f_L$
  - A figure-of-merit for the amplifier is **its gain-bandwidth product** defined as $GB = |A_M|BW$



Exercise 6.37 (Textbook)

Exercise 6.38 (Textbook)

Exercise 6.40 (Textbook)

Exercise 6.41 (Textbook)

Exercise 6.42 (Textbook)

Exercise 6.43 (Textbook)

Exercise 6.44 (Textbook)