

Elements of Fabrication Technology

7.1 Introduction

An “*integrated circuit or ICs*” is an electronic network fabricated in a single piece of semiconductor material. In IC fabrication, the semiconductor surface is subjected to various processing steps in which impurities and other materials are added or removed in specific geometrical patterns.

There has been a revolution in the electronics industry after the invention of the transistor which was closely followed by the invention of the monolithic integrated circuit. Since 1960s, new industries have been created to manufacture semiconductor devices ranging from small diodes to complex microprocessor chips. The fabrication of devices with microscopic features demand new and improved lithographic methods, technology and equipment. Billions of dollars have been spent on tools, equipment, and plant facilities, and millions of new jobs have been created around the world in fabricating and packaging these devices. Simultaneous advancements in computer technology and applications software merged with this improved process technology making it possible to integrate billions of transistors in a single chip, with device dimensions below 0.1 micrometre.

In 1964, Gordon Moore, a founder of Intel Corporation, predicted that the number of transistors in an integrated circuit would double every 18 months—this prediction, known as “*Moore’s law*” has turned out to be accurate. Increases in circuit density have been accompanied by reductions in feature size.

The steady downscaling of transistor dimensions over the past two decades has been the main stimulus to the growth of integrated circuits and the information industry. The more the device dimension gets smaller, the higher become its packing density, the higher its circuit speed and the lower its power dissipation. Integrated-circuit prices continue to fall. The fortunes of manufacturers have risen and fallen according to their ability to keep up with this ferocious pace. These have been key to the evolutionary progress leading to today’s

computers and communication system that offer superior performance, dramatically reduced cost per function, and much reduced physical size compared to their predecessors.

Silicon remains the predominate material from which semiconductors are made. Germanium was used in the manufacture of early transistors but it was later superseded by silicon. However, gallium-arsenide (GaAs) offers certain advantages like speed, frequency, and radiation resistance over comparable silicon devices. Therefore, certain kinds of specialised commercial and military analog, digital, and interface devices, have been made from GaAs. Now, GaAs technology is being challenged by another technology using silicon-germanium (SiGe) for radio frequency and microwave applications.

An IC is built sequentially in steps. The process steps work together to add layers to the IC. The chip gets thicker as the fabrication continues. Each step in the process has its own representative drawing. All these drawings relate to each other, forming three-dimensional components that operate together to form a working IC chip. IC layout is the process of creating the two-dimensional representations of the fabrication layers, which are then used to manufacture an IC chip.

Today we use "computer aided drafting (CAD)" tools to draw each layer of our IC. The layers have to line up extremely accurate. This chapter presents a simplified approach to the understanding of the fundamentals of IC development, and IC chip fabrication.

Regardless of the type, size, or complexity of semiconductor devices, their manufacturing processes exhibit more similarities than differences. IC fabrication starts with polished semiconductor wafers cut from large crystals which undergo a series of layering, patterning, doping, and heat-treating processes. Surviving devices must pass rigorous testing procedures before they end up as packaged products suitable for sale.

In IC fabrication, starting with our substrate wafer, one can do three things: change it, add to it, or remove material from it. To learn IC fabrication, it is necessary to understand how to make these changes, i.e., how to change, add or remove material from some specific areas.

Various steps in IC fabrication

The IC fabrication consists of the following steps (Figure 7.1).

1. Wafer preparation

- (a) Crystal growth of the wafer
- (b) Wafer slice and polish

2. Wafer processing

- (a) Epitaxial growth
- (b) Oxidation
- (c) Etching
- (d) Photolithography
- (e) Diffusion
- (f) Ion implantation
- (g) Metallisation

3. Testing & packaging

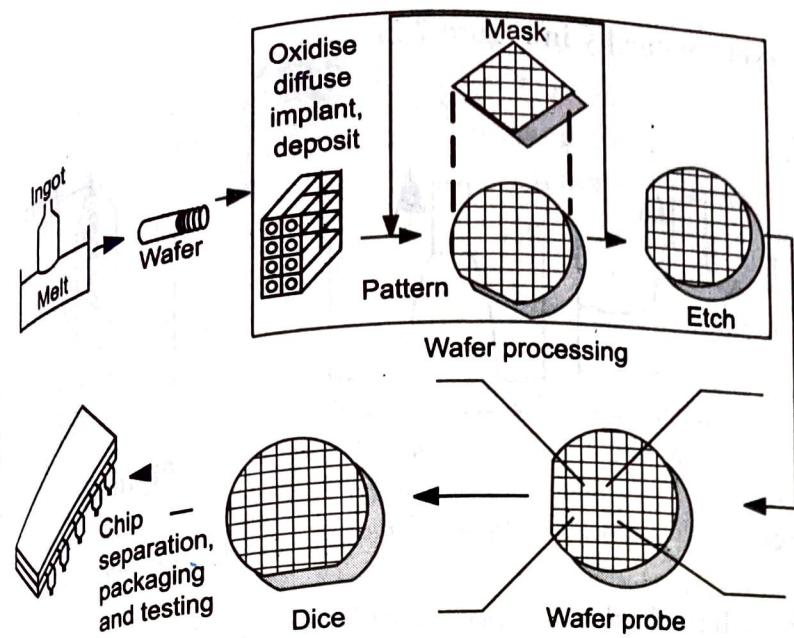


Figure 7.1 Pixels in a CCD chip

7.2 Making a Wafer Base: From Crystal Growth to Wafer Preparation

A **crystal** is a solid material whose atomic skeleton forms a definite geometric pattern (*lattice*). To make our chips, we need a single large crystal of silicon. If one dangles a piece of cotton in a large vat of sugar syrup, a single crystal of sugar eventually grows. Silicon wafers are prepared in the same way.

Small chunks of polycrystalline silicon are placed in a quartz (silica) crucible with small amounts of the chemical dopant elements needed to produce either n- or p-type silicon.

This crucible of silicon is heated, until it is completely molten to form a liquid, called the melt. A seed, or small crystal of doped silicon, is required to start the process. It is clamped into a rotating block above the crucible. Slowly this seed crystal is lowered into the vat, until it touches the surface of the molten silicon. Once the seed crystal touches the surface of the silicon, the vat temperature is reduced. Gradually, the cooling silicon atoms start to attach themselves to the seed crystal in the same way as the crystal of sugar. The seed crystal and molten silicon cling together as they cool. Once the crystal starts to grow, the rotating block that holds the seed crystal is raised out of the silicon melt very slowly. The seed is rotated in one direction, and the crucible in its holder is rotated in the opposite direction. Crystal growth begins as the seed is slowly raised above the melt. Eventually, the single seed crystal becomes a huge ingot. All the melted silicon in our crucible has finally attached to it. It is like a hanging cylinder now. This method of crystal growth is known as the *Czochralski* method of crystal growth. The machine required is commonly known as a crystal puller. The temperature, the pulling rate, and the inside dimensions of the crucible are important parameters, controlled by a close loop, computer to obtain a uniform, dislocation free crystal of desired diameter.

The whole process is illustrated schematically in Figure 7.2.

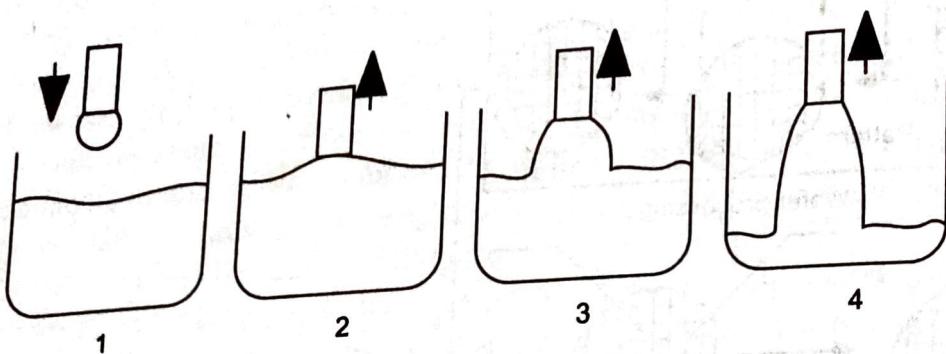


Figure 7.2 The seed crystal of silicon grows into a very large crystal of silicon

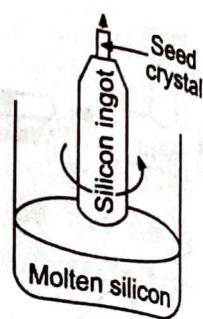


Figure 7.3
Czochralski crystal growth system

The Czochralski (CZ) crystal growth method is the most popular process for growing large, single crystals for manufacturing semiconductor devices. A cross-section diagram of the process is illustrated in Figure 7.3.

The long crystal of silicon is then sliced into thin round crystals known as "wafers", like slicing a loaf of bread as shown in Figure 7.4. Each slice is called a *wafer*. The wafers are sawed off from the crystal with the inside edge of a thin, ring-shaped circular saw blade. The wafers then undergo a two-step polishing process to ensure that the surface is free of irregularities and is absolutely flat.

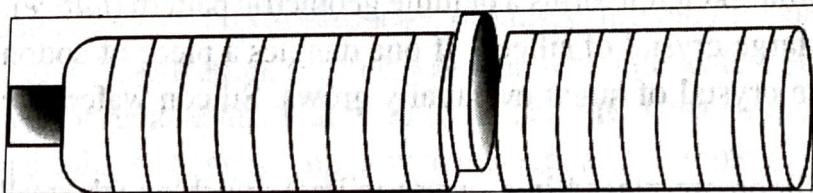


Figure 7.4 The large crystal is sliced into wafers

Just like diamonds, silicon crystals cut along certain planes. The chips must be oriented in the same direction as the crystal lattice of the wafer to make the wafer easier to cut. Some processing steps are dependent on crystal orientation. For example, there are some chemical etches that will etch preferentially faster on one edge of the crystal lattice than they will on another edge. Flat edges are ground along one or two sides of the wafer to know which way around it is. The flat side of the circle gives us a reference plane to align chips so that preferential etching can be controlled.

The wafer is then cleaned, polished and checked for flatness and defects before we can use it. Our entire IC chip is then built on this thin wafer which is also known as the substrate material.

Rather than placing just one chip in the centre, it is possible to build more next to it at the same time. Therefore, many chips next to each other are placed all across the wafer. One wafer could have hundreds of chips built on it.

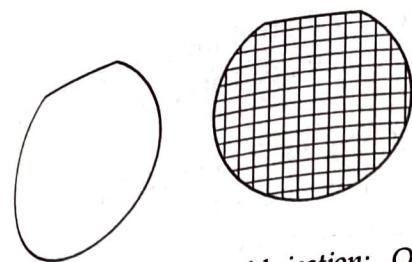


Figure 7.5 Batch fabrication: One wafer is used to make many chips

chips as possible on a big wafer.

The IC chips, which are configured on the wafer in a stop-and-repeat pattern, are formed in a batch process. The width of separation is equal to the thickness of the saw used in singulation. The economics of chip fabrication dictate that as many chips as possible be processed at the same time on a given wafer. Thus, reducing the size of the chips by decreasing their feature dimensions and using larger-diameter wafers are the most cost-effective ways of fabricating ICs. This is known as "batch fabrication".

When the processing is done, the chips are cut apart, with the wafer's crystal lattice orientation as shown in Figure 7.5. Each one of these little rectangles will be an individual silicon chip.

More chips at the same time can be built with a bigger wafer. It takes the same effort to process a 1" wafer as it does an 8" wafer, so there is an economy of scale for larger wafers. The goal is to build as many silicon

7.3 Changing Layer Composition or Doping Methods

As discussed earlier, processing steps fall into three main categories: changing the existing surface material, adding extra material, or removing material. Let us begin by learning how to change the composition of the silicon base wafer. *Doping* is the process of introducing specified amounts of dopants into the surface of the wafer. It occurs when the crystal is doped during the growth process by adding donor or acceptor elements to the melt. However, doping during wafer fabrication is achieved by thermal *diffusion* or *ion implantation*.

7.3.1 Ion implantation

The p-n junctions are made by introducing impurities into the substrate. These impurities should jump in the right place. Placing the impurity atoms into the wafer surface one at a time with a tweezers is not a good solution. So, modern engineers use a sophisticated approach: implantation which is nothing but a shotgun blast technique.

A source of the chosen impurity is placed above the wafer surface. Depending on the type of desired semiconductor, one could use boron, arsenic, phosphorus or other atoms. These impurities are generated as ions. An ion is an atom with some electrons removed, and is therefore positively charged, or with extra electrons and therefore negatively charged. The ions used for implantation have positive charge.

Many wafers, maybe 25 or so, are placed in a big chamber. The air is sucked out using large vacuum pumps. Once generated, the ions are accelerated toward the wafer by putting an extremely high negative voltage across the wafer and the ion source. With this very high negative voltage, the ions starts moving.

The positive ions are attracted to the wafer by the negative voltage. Magnets are used to focus and steer or guide the ions to strike at the right place. The surface of the wafer is totally

Annealing
In ion implantation, we have brutally forced atoms to strike into our silicon crystal, damaging the crystal lattice. Since a good crystal lattice structure is needed for the next steps of fabrication, there is a need to repair and get back the nice crystal lattice structure. To repair the crystal lattice, the wafer is annealed, which means it is heated. This helps all the atoms to loosen and settle with each other, forming a more consistent structure. This is rather like shaking a badly packed box of balls to make them settle down evenly.

A very shallow implant, after "annealing", makes the atoms diffuse outward. The implanted atoms spread themselves throughout the material in all directions. Therefore, annealing is a kind of diffusion process. Thus to have a good crystal lattice structure, ion implantation must be followed by a drive-in step (heat treatment or annealing), which redistributes the ions and increases the depth of penetration as shown in Figure 7.8.

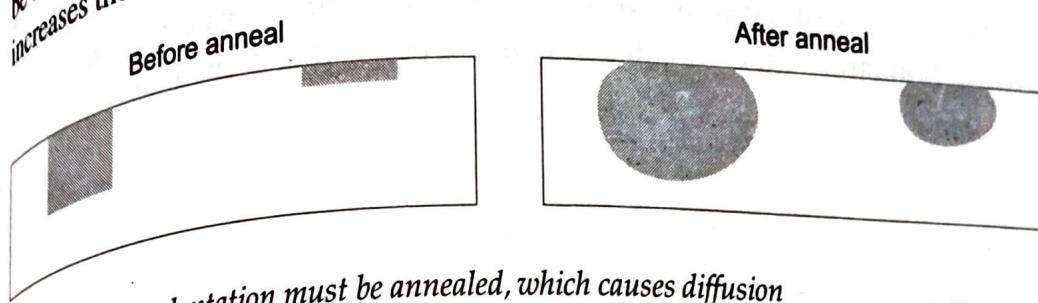


Figure 7.8 Implantation must be annealed, which causes diffusion

7.4 Adding a Layer or Deposition

Besides changing the surface properties by implantation, there may be a need to add an entirely new layer of some other material. Let us look at various ways to add a new layer to the wafer.

7.4.1 Epitaxial deposition

Some semiconductor devices need very good, thin layers of silicon, one on top of the other, in order to function correctly. Therefore, new layers of silicon need to match the substrate crystal lattice. We cannot just use any method to do this, since some methods do not maintain the crystal lattice alignment. Growing another layer of silicon very slowly, though, keeps the necessary crystal lattice orientation. This is called *epitaxial* deposition. There are several ways to do it.

7.4.2 Chemical vapour deposition (CVD)

Layers of silicon dioxide, silicon nitride or polysilicon can be deposited on the wafer surface using the CVD technique at a high temperature.

Certain gases mixed at high temperature will react with each other to produce silicon. If the wafers are kept nearby, they will catch a few of these silicon atoms generated by the reaction of the gases. The rate of condensation of the atoms on the wafer is controlled by changing the temperature. Growing a new layer using a mixture of gases in this way is called "chemical vapour deposition", or CVD. For example, if silane gas and oxygen are allowed to react above

a silicon substrate, the end product, silicon dioxide, will be deposited as a solid film on the silicon wafer substrate.

If silane gas alone is used, then a silicon layer will be deposited on the wafer. If the reaction temperature is high enough (above 1000 °C), the layer deposited will be a crystalline layer. Such a layer called epitaxial layer, and the deposition process is referred as an "epitaxy" rather than CVD.

The basic CVD process consists of the following steps. First the wafer is placed in a quartz tube that can withstand very high temperatures as shown in Figure 7.9. At one end of the tube, highly reactive gases are pumped in. The mixture of gases react with each other, encouraged by the high temperature. The reacted gases travel through the tube until they encounter the wafer. The temperature of the wafer is cooler than the gases, so the silicon in the mixture condenses onto the surface. This gives us a nice epitaxial layer across the surface that aligns perfectly with the crystal lattice of the wafer. If we vary the mixture of gases, we can vary the type of silicon grown. Sometimes, the silicon layer might be p-type, sometimes it might be n-type.

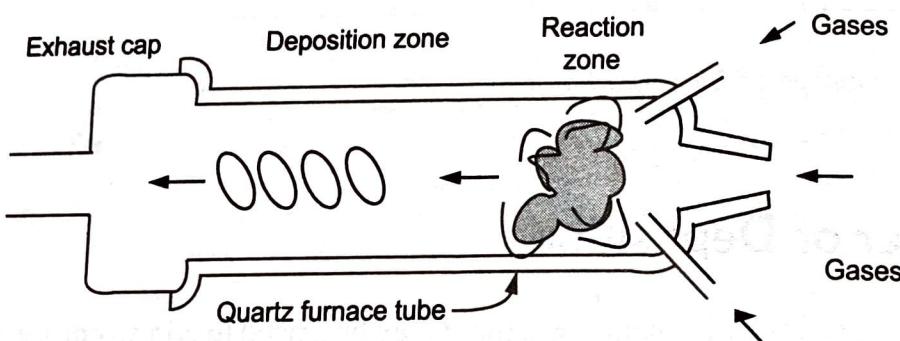


Figure 7.9 Vapourised silicon condenses on many wafers at one time

Epitaxial layer such as silicon on silicon are grown slowly to maintain the good quality of the crystal lattice. Silicon that is grown quickly using CVD does not have a very good crystal structure. It is like frost on a windowpane, and is made up of many different crystals that eventually join, rather than one large crystal. This type of silicon is known as a "polycrystalline silicon" (meaning many crystals). Polycrystalline silicon is usually referred to simply as poly.

Poly is used extensively in ICs to make FET gates and resistors. Like our silicon, it, too, can be doped. The doping is usually done to change its resistivity, whereas doping regular silicon is done to set energy levels and transistor characteristics.

A variation of CVD is *plasma enhanced chemical vapour deposition*, or PECVD. PECVD is very similar to CVD, but instead of using high temperatures to start the chemical reaction, plasma is used instead. "Plasma" is a state of matter formed when gases at very low pressures are subjected to high frequency and high voltage. For example, a fluorescent lighting tube contains plasma.

There is another variation of the CVD technique known as *LPCVD* (low-pressure) where the deposition is carried out under reduced gas pressure for better uniformity.

4. Crystal orientation
5. Time

7.4.4 Metallisation by "sputtering"

The deposition of a conductive material, to form the interconnective leads between the circuit component parts and the bonding pads on the surface of the chip, is referred to as the metallisation process. As chip density increases, the interconnection can no longer be accomplished on a single level of metal but requires multilevel metallisation with contact holes interconnecting the various levels.

Materials such as aluminum, aluminum alloys, platinum, titanium, tungsten, molybdenum, and gold are used for various metallisation processes. Of these, aluminum is the most commonly used metallisation material, because it adheres well to both silicon and silicon dioxide (low contact resistance), it can be easily vacuum deposited (it has a low boiling point), it has a relative high conductivity, and it patterns easily with photo-resist processes.

High-energy plasma can also be used to help deposit materials that cannot be deposited using CVD. Plasma made from inert gas, such as argon, can be used to knock atoms into submission, using a machine called a "sputterer". It is used to deposit a layer of metal. A chamber containing a large block of the desired metal is suspended above the wafers. The metal is blasted onto the wafer to form the new surface. The air is sucked out, and a small amount of argon pumped into the chamber. Argon turns into high-energy plasma at very low pressures and when subjected to high frequency and high voltage. As the high-energy argon atoms smash into the metal, they force metal atoms to dislodge or sputter off from the block, flying out into the plasma. This is kind of like sandblasting the metal with argon atoms.

The metal atoms become ionised by their ordeal and stick to the wafers kept below. As the process continues, more and more metal atoms get blasted away, attaching themselves to the wafer surface. Eventually, the wafers are coated with metal of correct and well controlled thickness.

7.4.5 "Metallisation" by evaporation

Another way of depositing metal is "evaporation". The wafers are loaded into a large chamber that has all the air sucked out of it. This chamber contains a large tungsten filament, like the coils of a light bulb. The coils have small chunks of the desired metal placed inside them.

As current is passed through the filament, it starts to glow. The coil gets so hot that the metal inside melts. As the filament gets even hotter, the metal finally starts to evaporate. The evaporated metal atoms fly around in the hot gas. They eventually hit cooler surfaces and form a layer of condensation. They condense onto everything inside the chamber, including our chip.

This process has the disadvantage of non-uniform metal coverage. *Sputtering* offers better control of the metallisation quality than the vacuum deposition method. It is currently being used in the majority of IC metallisation processes.

7.5 Removing a Layer or Etching

"Etching" is a process of removing unprotected material. There are certain chemicals which, when poured onto the wafer, cause a reaction with certain materials on the surface of the wafer. This chemical dissolves or eats the materials. Once dissolved, wafers can be washed leaving underlying layers. Metals, oxides, silicon can be removed by etching. Etching can be classified into two types.

1. *Dry or plasma etching* : uses ionised gases rendered chemically active by a radio-frequency generated plasma. Ideally this kind of etching should result in anisotropic etching as shown in Figure 7.11(a).
2. *Wet etching*: uses chemicals to remove the unprotected materials. It occurs in all directions resulting in an isotropic etching as shown in Figure 7.11(b). Horizontal etching causes an *under cut* as shown in the figure.

RIE (reactive ion etching) is a type of dry etching and is almost the opposite of sputtering. Instead of a block of metal being bombarded by argon atoms, we reverse the polarity of the chamber voltage and sandblast our wafer instead. If we use a mixture of gases that happen to react chemically with our new surface material, then the surface will be removed even faster.

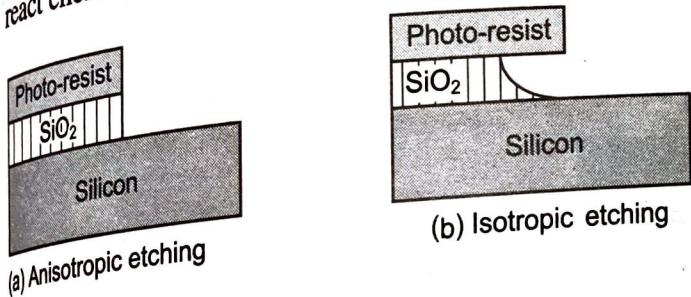


Figure 7.11 Different types of etching

7.6 Photolithography or Pattern Transfer

"Photolithography" is a patterning process whereby the elements representing the IC circuit are transferred onto the wafer by photomasking and etching. Some specific small areas, strips, rectangles or other areas of the wafer are subjected to this process.

Photolithography has similarities to photographic processes. The images of the various semiconductor element layers are formed on masks made of glass, which are then transferred to the wafer. Therefore, it is a process by which some patterns drawn on a glass mask are transferred to the wafer.

The surface to be patterned is coated with photo-resist. "Photo-resist" is a light sensitive material that changes its structure and properties when exposed to UV light. Resist that is not exposed to light remains intact, hard, firm and protective. However, where light does hit the resist, a change occurs to its chemical structure. Resist that is exposed to light becomes dissolvable. Those areas of the surface exposed to light can then be washed away using the appropriate solvent.

In the photolithography process, the light is passed through a sheet of glass known as mask onto the surface of the wafer. The mask contains an image of the regions that we want to protect from processing. Therefore some portion of the mask is transparent to UV light and the remaining portion is non-transparent. Light that shines through the mask will expose the resist and becomes dissolvable. On all other portions of the wafer surface, the mask blocks the light and the resist remains hard. This is why the protective material is named resist. It resists the process that is about to be done to the chip. For example, if the chip is dipped in a strong acid, the regions protected by resist will remain untouched by the acid. Or, if the chip is bombarded with ions, the regions protected by resist will remain untouched by the ions.

There is no need to keep this layer of protection any longer than one step in the process. Each step needs a new protective layer of resist. Each layer has a different design. For each layer we draw will have its own mask. The image on the mask is usually drawn in chrome, so that no light will be able to shine through.

Basic sequence of photolithography

1. The wafer is placed on a rotating spin coater. Resist material is dripped onto the wafer. Because the wafer is spinning, the resist spreads out resulting in a nice, even, thin film as shown in Figure 7.12.

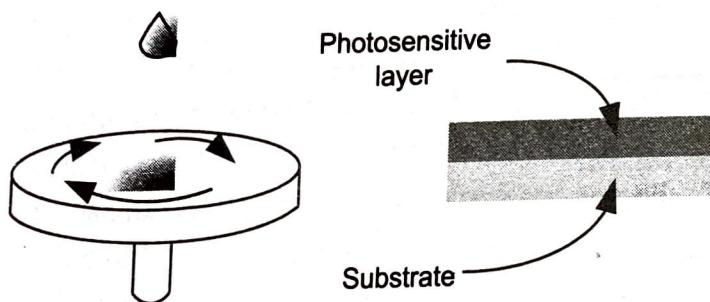


Figure 7.12 Photo-resist coating substrate is coated evenly with photosensitive resist by dropping the chemical onto the spinning wafer.

2. The photo-resist is dehydrated in an oven (the photo-resist, as we know, is made of a light-sensitive organic polymer) or baked hard.
3. It is exposed to ultra violet light.
4. The photo-resist exposed areas become soluble and non-exposed areas remain hard.
5. The soluble photo-resist is chemically removed (development). It resist means washing it in a special dissolving solution. It dissolves areas that were chemically changed by exposure to light. Only the shaded areas of resist remain.
6. The patterned photo-resist will now serve as an etching mask for SiO₂. These areas of hardened resist now protect specific sections of the chip from the next step of processing.
7. The areas no longer covered with resist will be attacked and eaten away by wet acid etching. The SiO₂ is etched away leaving the substrate exposed.
8. After finishing acid etching, the remaining resist is removed by using other chemicals.

9. The selected areas of the wafer can now be doped with techniques like ion implantation or diffusion. The whole sequence is shown in Figure 7.13. Thus the pattern on the mask is transferred onto the wafer by photolithography.

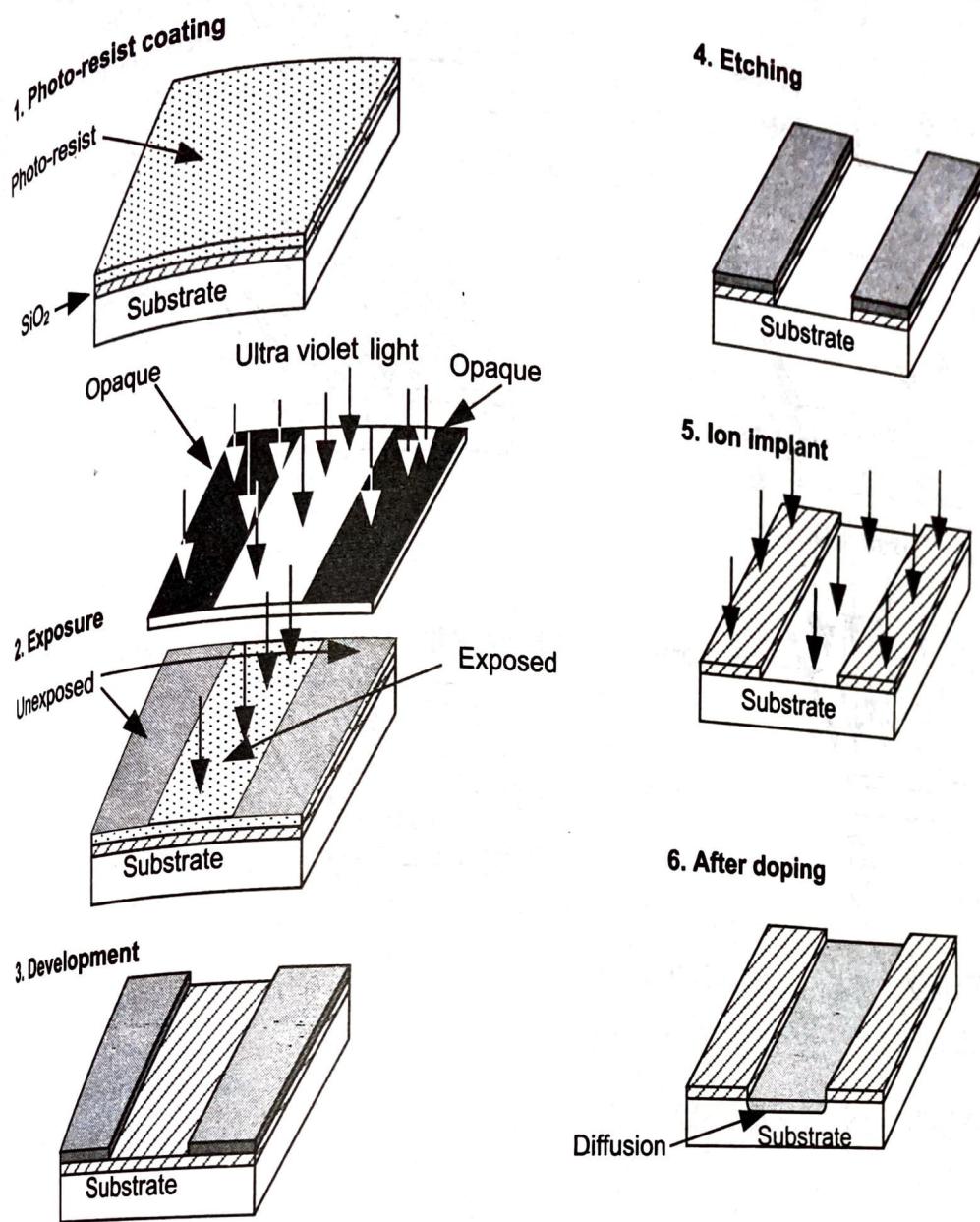


Figure 7.13 Pattern transfer

Figure 7.14 shows the sequence of steps for generating a polysilicon gate.

There are two types of photo-resist. One becomes removable when exposed to light. This type of resist is called "*positive resist*" and is the most common type of resist used. We will assume we are using positive resist in this book.

The other type acts exactly opposite. The exposed regions do not dissolve. Instead they harden. They cannot be removed by the developer. The shaded regions dissolve. This type of resist is known as "*negative resist*". Negative resist is not as good at producing high quality image and is harder to work with.

A mask that is mainly covered with chrome is known as a "*dark field mask*". Light will not pass through the majority of the mask. A mask which is primarily clear with only small areas of chrome is known as a "*light field mask*". The majority of the mask is see-through.

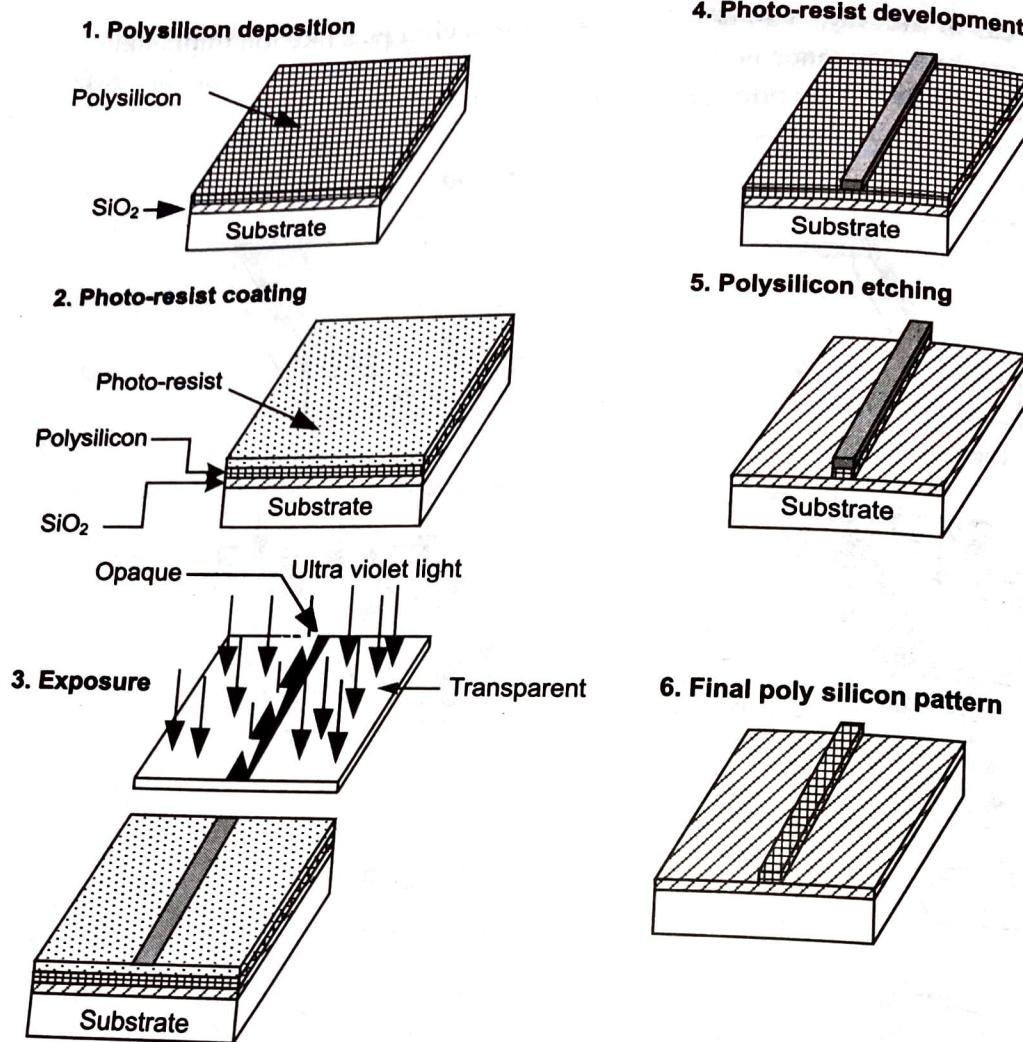


Figure 7.14 Polysilicon gate formation

Photolithography is a fundamental part of every step in the IC fabrication process, whether for implantation, doping, formation of the epitaxial layer or any other surface changes.

Every step requires coating with resist. Every step requires a mask. Every step requires exposure to light. Every step requires removal of exposed resist. Every step requires processing and every step requires removal of the remaining resist in preparation for the next step. And all these steps is only one step in processing one layer. You might have 20 or 30 layers in a chip.

The increasing need for ICs to be smaller and operate at higher speeds has forced the industry to develop ICs with ever small features. As feature sizes decrease, the patterning technology has to advance to a situation where the requirements of high resolution, tight pattern registration (alignment), and highly accurate dimensional control are met. Photomasking is the most critical element of the IC fabrication process in that alignment of the different photomask overlays and mask contamination have an overwhelming effect on fabrication yield.