CMOS FABRICATION

The CMOS can be fabricated using different processes such as:

- N-well process for CMOS fabrication
- P-well process
- Twin tub-CMOS-fabrication process

The fabrication of CMOS can be done by following the below shown twenty steps, by which CMOS can be obtained by integrating both the NMOS and PMOS transistors on the same chip substrate. For integrating these NMOS and PMOS devices on the same chip, special regions called as wells or tubs are required in which semiconductor type and substrate type are opposite to each other.

A P-well has to be created on a N-substrate or N-well has to be created on a P-substrate. In this article, the fabrication of CMOS is described using the P-substrate, in which the NMOS transistor is fabricated on a P-type substrate and the PMOS transistor is fabricated in N-well.

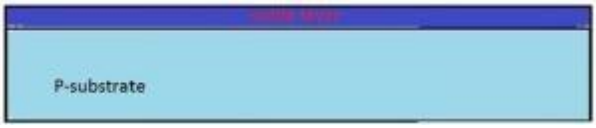
The fabrication process involves twenty steps, which are as follows:

Step1: Substrate

Primarily, start the process with a P-substrate.

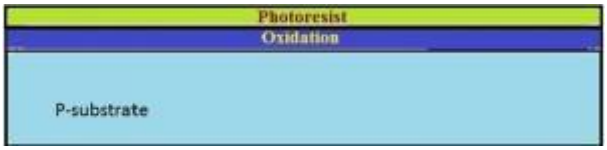
Step2: Oxidation

The oxidation process is done by using high-purity oxygen and hydrogen, which are exposed in an oxidation furnace approximately at 1000 degree centigrade.



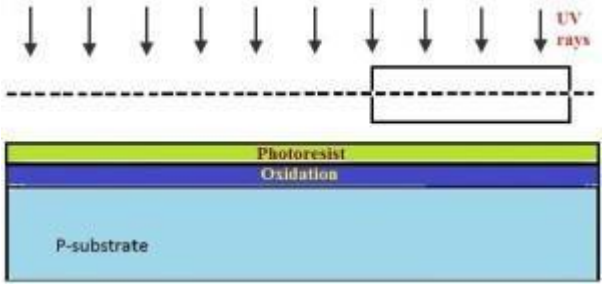
Step3: Photoresist

A light-sensitive polymer that softens whenever exposed to light is called as Photoresist layer. It is formed.

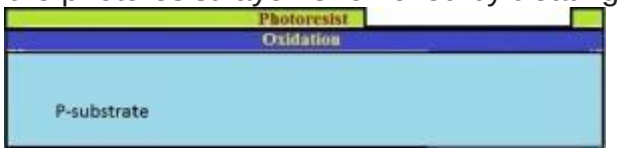


Step4: Masking

The photoresist is exposed to UV rays through the N-well mask

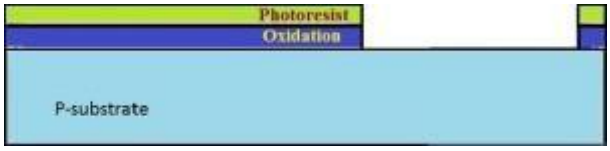


Step5: Photoresist removal

A part of the photoresist layer is removed by treating the wafer with the basic or acidic solution. 

Step6: Removal of SiO2 using acid etching

The SiO2 oxidation layer is removed through the open area made by the removal of photoresist using hydrofluoric acid.

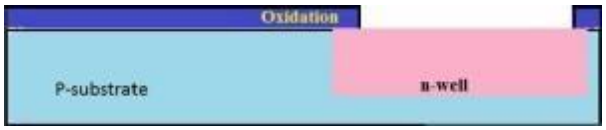


Step7: Removal of photoresist

The entire photoresist layer is stripped off, as shown in the below figure.

Step8: Formation of the N-well

By using ion implantation or diffusion process N-well is formed.

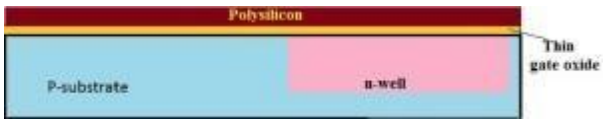


Step9: Removal of SiO2

Using the hydrofluoric acid, the remaining SiO2 is removed.

Step10: Deposition of polysilicon

Chemical Vapor Deposition (CVD) process is used to deposit a very thin layer of gate oxide.

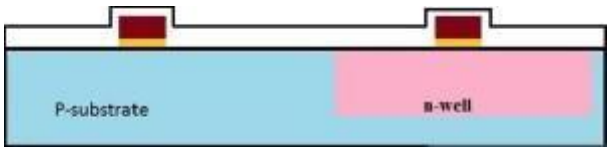


Step11: Removing the layer barring a small area for the Gates

Except the two small regions required for forming the Gates of NMOS and PMOS, the remaining layer is stripped off.

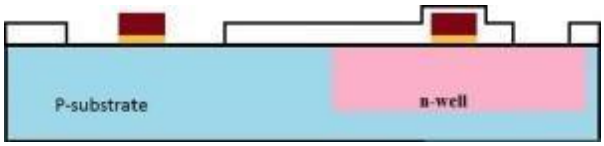
Step12: Oxidation process

Next, an oxidation layer is formed on this layer with two small regions for the formation of the gate terminals of NMOS and PMOS.



Step13: Masking and N-diffusion

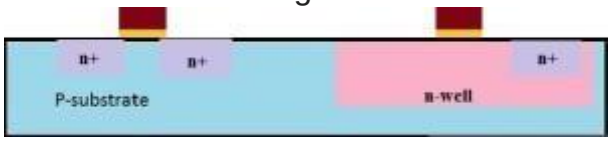
By using the masking process small gaps are made for the purpose of N-diffusion.



The n-type (n+) dopants are diffused or ion implanted, and the three n+ are formed for the formation of the terminals of NMOS.

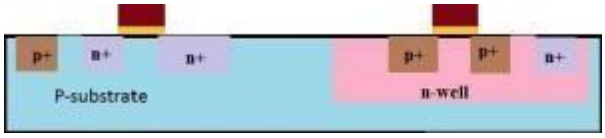
Step14: Oxide stripping

The remaining oxidation layer is stripped off.



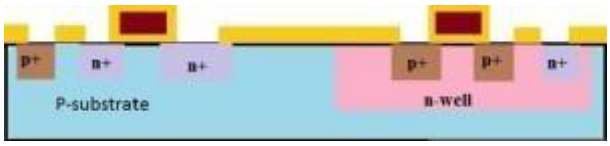
Step15: P-diffusion

Similar to the above N-diffusion process, the P-diffusion regions are diffused to form the terminals of the PMOS.



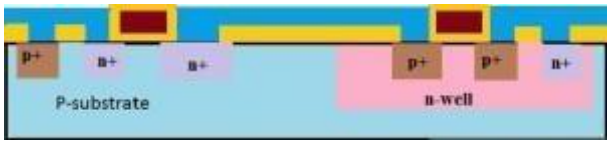
Step16: Thick field oxide

A thick-field oxide is formed in all regions except the terminals of the PMOS and NMOS.



Step17: Metallization

Aluminum is sputtered on the whole wafer.

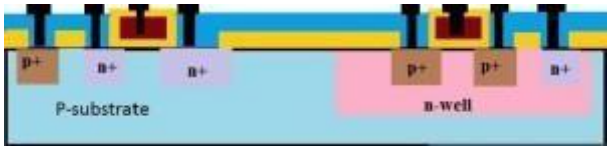


Step18: Removal of excess metal

The excess metal is removed from the wafer layer.

Step19: Terminals

The terminals of the PMOS and NMOS are made from respective gaps.



Step20: Assigning the names of the terminals of the NMOS and PMOS