

Block diagram of a sequential circuit.

- Special type of circuit
- It consists of a combinational circuit to which memory elements are connected to form a feedback path.
- 2 main types of Sequential circuits.
  - Synchronous ✓
  - Asynchronous . ✓
- 'N' number of i/p & o/p
- Here o/p depends on a combination of both the present i/p as well as the previous o/p. Previous o/p gets treated as the former & the present state.

3 State :

- ① present i/p
- ② Past i/p and/or
- ③ Past o/p

# Difference b/w Synch And Asynch Sequential circuit.

## Synchronous

- > These circuits are easy > These circuit are difficult to design.
- > A clocked flip flop acts as memory
- > they are slower
- > The status of memory element is affected only at the active edge of clk if i/o is changed

eg: FF

## A Synchronous

- > An unlocked ff or time delay element is used as memory element.
- > Faster as clock is not present.
- > The status of memory element will change any time as soon as i/o is changed.

eg: Latches

## Latch

- It is structured based on logic gates blocks
- It does not have clk signal in its internal circuit
- Latch is sensitive to input signal only
- It is level trigger
- It can not be used as register
- It is a Async. circuit

## FF

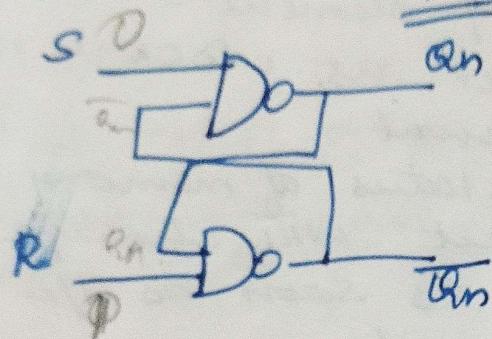
- It is structured based on blocks of latches + logic gates.
- It has a clock with internal circuit.
- FF is sensitive to i/o and clock signal.
- It is edge trigger.
- It can be used as register.
- It is synchronous circuit.

## SR Latch using NAND

NAND 77

A	B	$\overline{\text{NAND}(AB)}$
0	0	1
0	1	0
1	0	0
1	1	0

### Logic Diagram



$$\frac{\text{P.S}}{Q_n} \quad \frac{\text{N.S}}{Q_{n+1}}$$

$$\overline{Q_{n+1}} = \overline{Q_n \cdot \overline{Q_n}} = \overline{0} = 1$$

### Truth table.

	S	R	$Q_n$	$Q_{n+1}$
(i)	0	0	X	<span style="border: 1px solid black; padding: 2px;">ID</span>
(ii)	0	1	X 0 1	<u>Set</u>
(iii)	1	0	X 0 1	<u>Reset</u>
(iv)	1	1	X	$Q_n$ (No change)

$$\overline{Q_{n+1}} = \overline{0 \cdot Q_n} = \overline{0} = 1$$

Case 3:-

$$S=1 \quad R=0$$

$$Q_{n+1} = \overline{1 \cdot \overline{Q_n}} = \overline{Q_n} = 0$$

$$\overline{Q_{n+1}} = \overline{0 \cdot \overline{Q_n}} = \overline{0} = 1$$

### Case 4:

$$S=1 \quad R=1$$

$$Q_{n+1} = \overline{1 \cdot \overline{Q_n}} = \overline{Q_n} = 0$$

$$\overline{Q_{n+1}} = \overline{0 \cdot \overline{Q_n}} = \overline{Q_n} = 0$$

No value

### Case 1:- $S=0 \quad R=0$

$$Q_{n+1} = \overline{0 \cdot \overline{Q_n}} = \overline{0} = 1$$

$$\overline{Q_{n+1}} = \overline{0 \cdot \overline{Q_n}} = \overline{0} = 0$$

### Case 2: $S=0 \quad R=1$

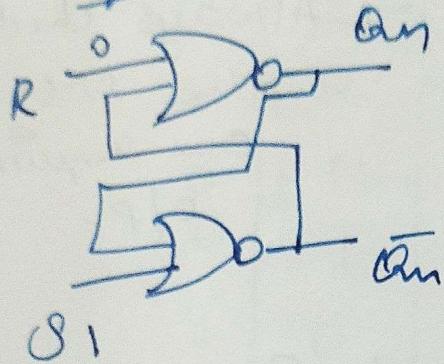
$$Q_{n+1} = \overline{0 \cdot \overline{Q_n}} = \overline{0} = 1$$

$$\overline{Q_{n+1}} = \overline{0 \cdot \overline{Q_n}} = \overline{0} = 0$$

If you get value no need to find the complement

## SR Latch using NOR

Logic circuit



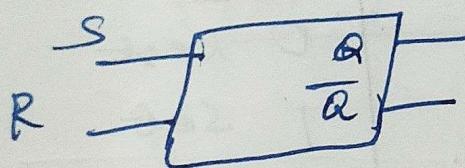
$Q_n$

$Q_{n+1}$

$\bar{Q}_{n+1}$

$S_1$

Logic symbol



Case 3 =

$$Q_{n+1} = \overline{0 + \overline{Q}_n} = \overline{0 + 0} = 0$$

(i)  $S=0 \quad R=0$

$$Q_{n+1} = 0 + \overline{Q}_n = Q_n$$

(ii)  $S=0 \quad R=1$

$$Q_{n+1} = \overline{1 + \overline{Q}_n} = 0$$

(iii)  $S=1 \quad R=0$

$$Q_{n+1} = \overline{0 + \overline{Q}_n} = Q_n$$

$$Q_{n+1} = \overline{1 + \overline{Q}_n} = 0$$

(iv)  $S=1 \quad R=1$

$$Q_{n+1} = \overline{1 + \overline{Q}_n} = 0$$

NOR TT

A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

→ while  
using NOR  
gate R.S.

TT

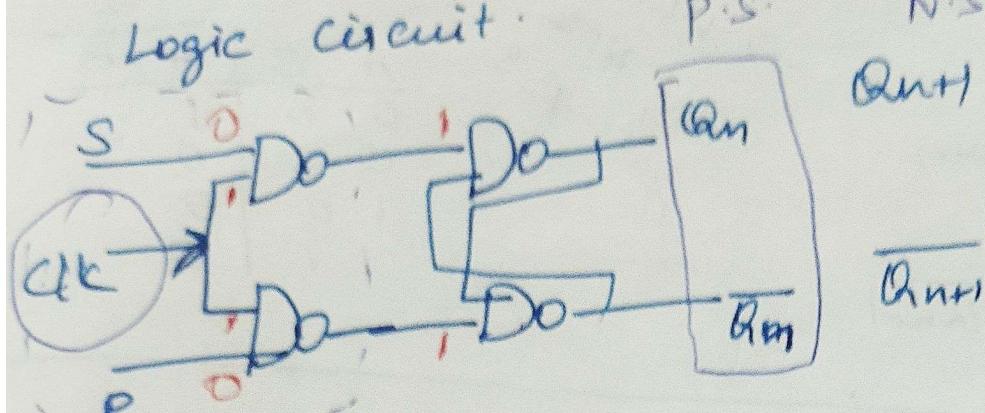
S	$\overline{R}$	$Q_n$	$Q_{n+1}$
0	0	0	0 [no change]
0	0	1	1
0	1	0	0 [Re Set]
0	1	1	1 [Set]
1	0	0	1
1	0	1	1
1	1	1	0 [I.D]
1	1	1	1

TT

S	R	$Q_n$	$Q_{n+1}$
0	0	x	$Q_n$ (no change)
0	1	x	0 Reset
1	0	x	1 Set
1	1	x	I.D

SR      FF     $\rightarrow$  Single bit  
Storage dev.

Logic circuit.



$Q_{n+1}$      $\rightarrow$  Always the  
the N.S.  
Our requi-  
o/p.

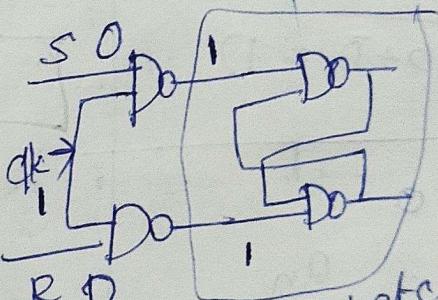
clk i/p

Truth Table.

CLK	S	R	$Q_n$	$Q_{n+1}$
↑	0	0	x	<u><math>Q_n</math></u>
↑	0	1	x	0 Rest
↑	1	0	x	1 Set
↑	1	1	x	I.D.

(i)  $S=0 \quad R=0$

$$Q_{n+1} = \overline{1 \cdot Q_n} = Q_n$$



(ii)  $S=0 \quad R=1$

$$Q_{n+1} = \overline{1 \cdot Q_n} = Q_n \Rightarrow 0$$

$$\overline{Q_{n+1}} = \overline{0 \cdot Q_n} = 1$$

S.R Latch.  
 $S=1, R=0$

(iii)  $S=1 \quad R=0$

$$Q_{n+1} = \overline{0 \cdot \overline{Q_n}} = \overline{0} = 1$$

$$Q_{n+1} =$$

(iv)  $S=1 \quad R=1$

$$Q_{n+1} = \overline{0 \cdot \overline{Q_n}} = 1 \quad \left. \begin{array}{l} \text{Not possible.} \\ \overline{Q_{n+1}} = \overline{0 \cdot Q_n} = 1 \end{array} \right\} \text{I.D.}$$

Char -

S	R	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X $\leq^0$
1	1	1	X $\geq^0$

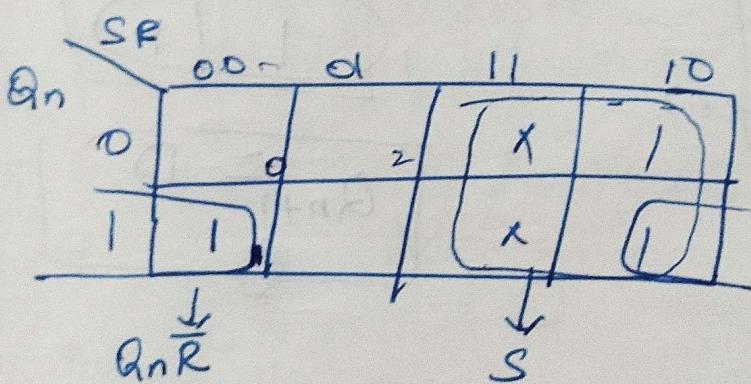
Flip Flop are basically the circuits that maintain a certain state unless and until directed by the input for changing that state.

Types of FF

SR, T, JK

D.

Toggle,  
Data / delay.



$$Q_{n+1} = S + Q_n \bar{R}$$

### Applications of FF:

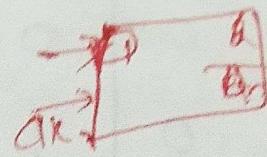
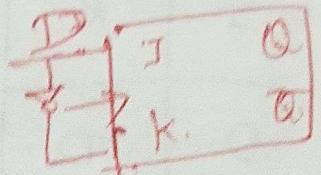
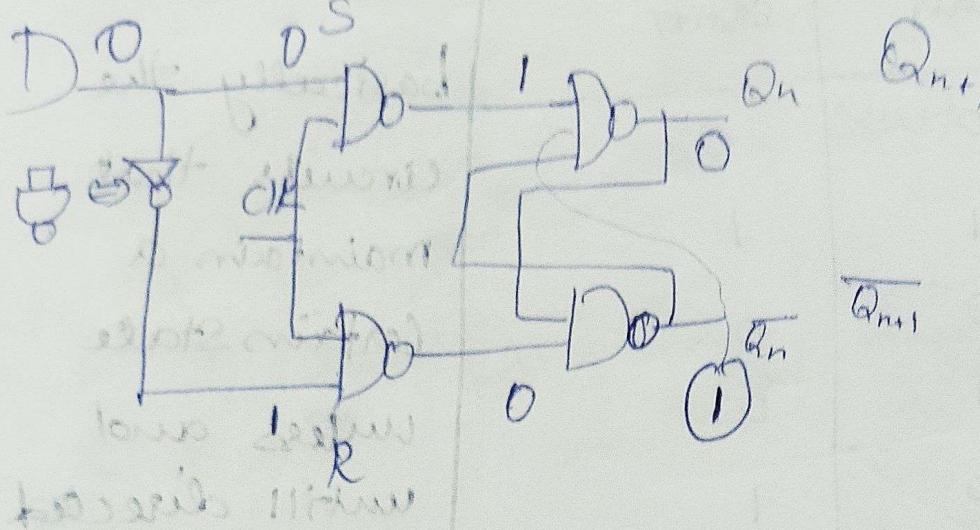
#### 1. Shift registers

- Parallel to serial conversion
- Serial to parallel conversion.
- Data storage  $\leftarrow$  serial parallel.

#### 2. Counter

- Count the number of pulse
- Frequency division

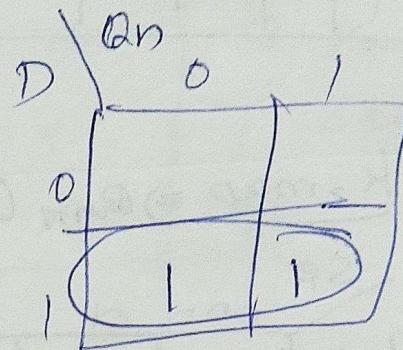
D FF - Data line / Delay



2 var k-m.

Truth Table

	i/p	o/p
clk ↑	D	Qn+1
R ↑	0	X → 0
R ↑	1	X → 1
		0 (Reset)
		1 (Set)



$$Q_{n+1} = D$$

Characteristic table.

$$(i) D = 0$$

$$Q_{n+1} = \overline{1 \cdot \overline{Q_n}} = Q_n \rightarrow 0$$

$$\overline{Q_{n+1}} = \overline{1 \cdot Q_n} = 1$$

$$(ii) D = 1$$

$$Q_{n+1} = 0 \cdot \overline{Q_n} = 1$$

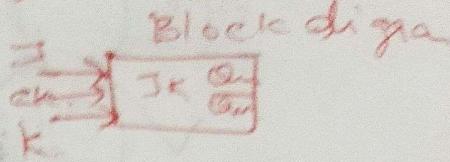
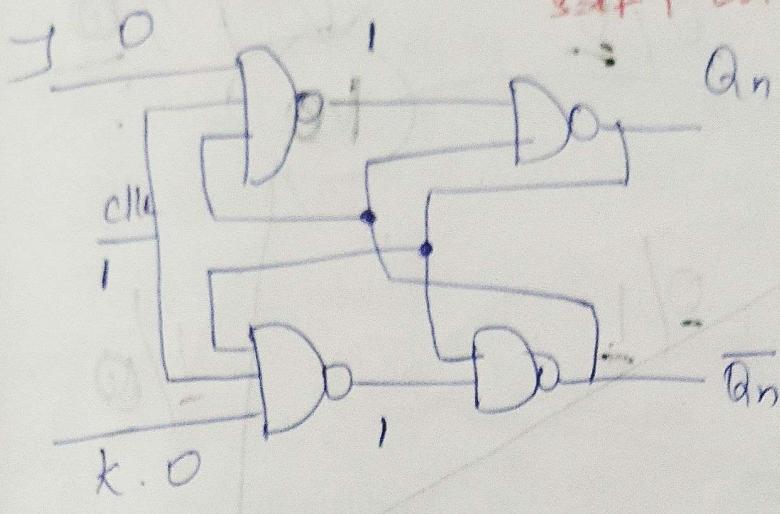
PS	NS	D
0	0	0
0	1	1
1	0	0
1	1	1

JK FF (Condu.)  
Excitation Table

PS	NS	T INPUT
0	0	0, X
0	1	1, X
1	0	X, 1
1	1	X, 0

## JK FF

→ To overcome the SR FF  
problem in FF goes to JK



Truth Table.

J	K	Qn	Qn+1
0	0	X; 0	0 Qn Previous state
0	1	X; 0	0 Reset
1	0	X; 1	1 Set
1	1	X; 0	Qn Toggle complement of Qn

(i)  $J=0 \quad K=0$

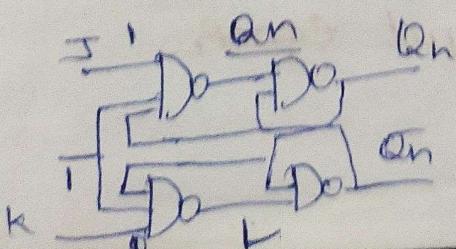
$$Q_{n+1} = \overline{1 \cdot Q_n} = Q_n.$$

$$\overline{Q_{n+1}} = \overline{1 \cdot Q_n} = \overline{Q_n}.$$

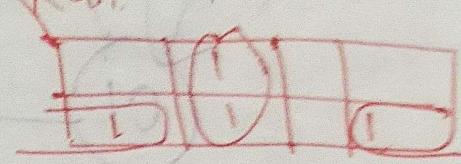
(ii)

$$J=1 \quad K=0$$

$$Q_{n+1} = \overline{Q_n \cdot \overline{Q_n}} = \overline{0} = 1$$

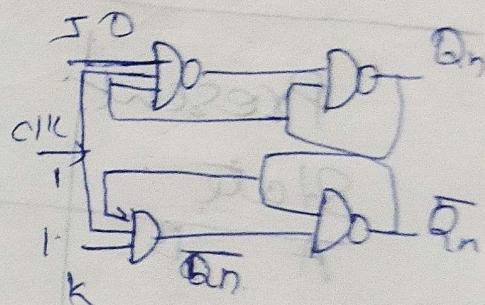


I.



$$Q_{n+1} = \overline{Q_n} J + \overline{Q_n} K$$

$$Q_{n+1} = J \overline{Q_n} + Q_n K$$



(ii)

$$J=0 \quad K=1$$

$$Q_{n+1} = \overline{1 \cdot \overline{Q_n}} = Q_n \rightarrow 0$$

$$\overline{Q_{n+1}} = \overline{\overline{Q_n} \cdot Q_n} = \overline{0} = 1$$

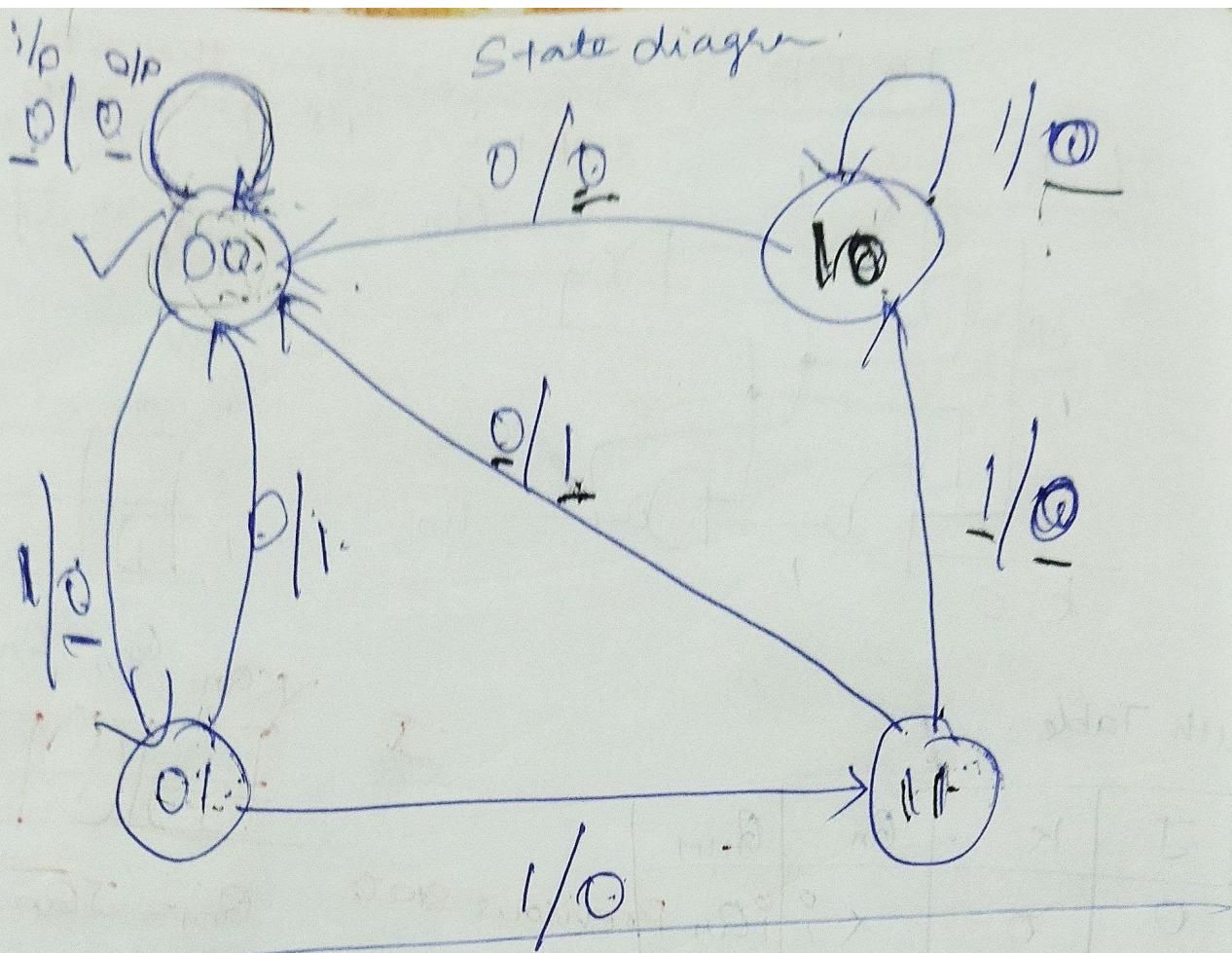
(iv)

$$J=1 \quad K=1$$

$$Q_{n+1} = \overline{Q_n \cdot \overline{Q_n}} = \overline{0} = 1$$

$$\overline{Q_{n+1}} =$$

$$Q_{n+1} = \overline{Q_n \cdot 1} = \overline{Q_n}$$



Present State A B	Next State		Output $X = 0 \quad X = 1$
	$X = 0$	$X = 1$	
0 0	0 0	0 1	0 0
0 1	0 0	1 1	1 0
1 0	1 0	1 0	0 0
1 1	0 0	1 0	1 0

Analysis of Clocked Sequential circuit  
 State equation, output equation.

Step 1:- translate this specification.  
into a state ~~state~~ of table.

State diagram

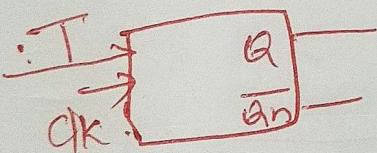
a circle : a state

a directed lines connecting the  
circle : the transition b/w the states

Each directed line is labeled I/P/O/P

T - Flip Flop

Toggle. I/P '0' ~~is~~ output  
will be P/S



Truth table.

T	$Q_{n+1}$
0	$Q_n$
1	$\bar{Q}_n$

Excitation.

Excitation table.

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1

Characteristic table.

T	$Q_{n+1}$	$Q_{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

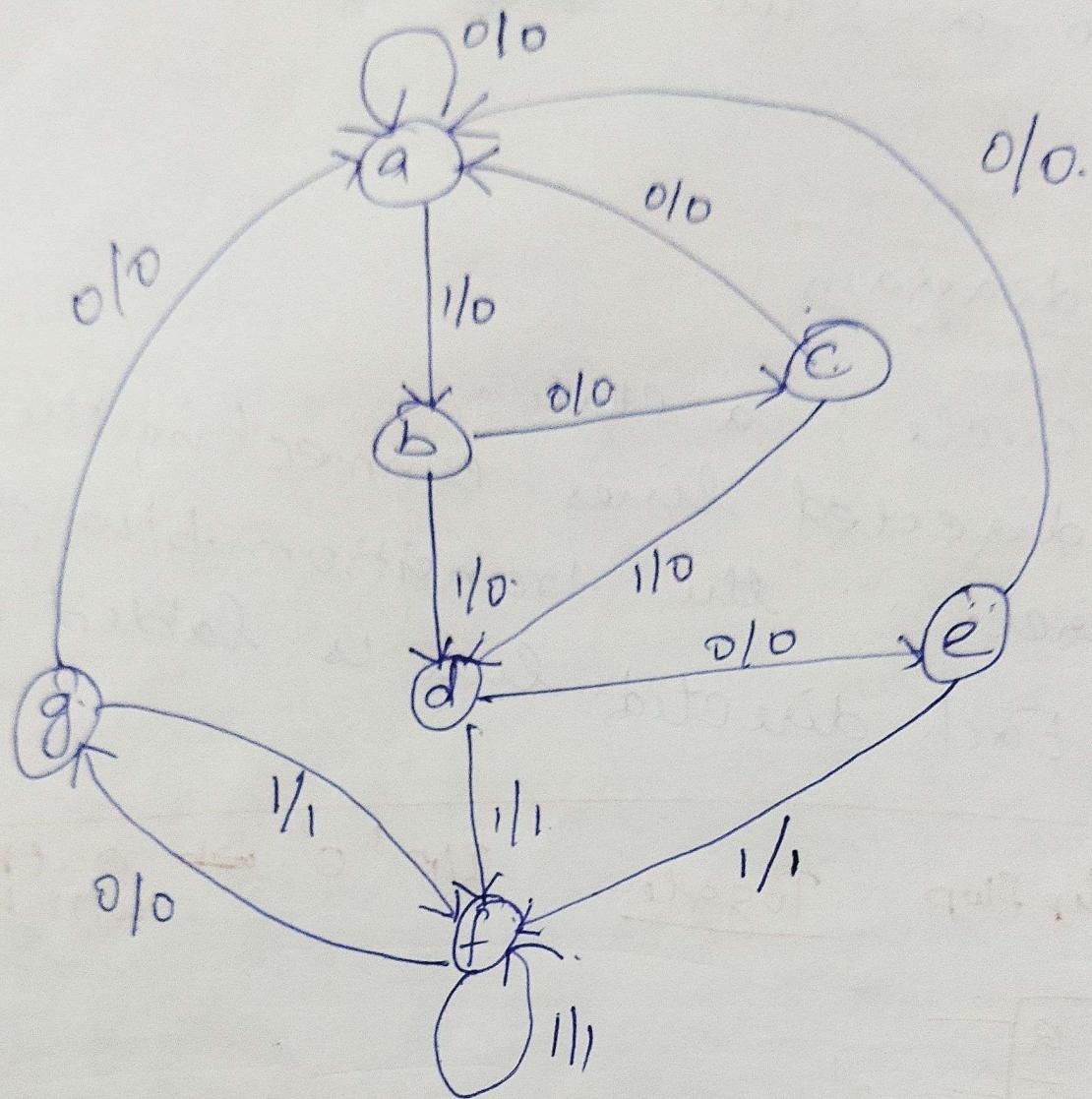
equation.

T	$Q_n$	1
0	0	1
1	1	0

$$Q_{n+1} = \overline{T} Q_n + T \bar{Q}_n$$

$$(Q_{n+1}) = T \oplus Q_n$$

## State Reduction & Assignment



Step 1:- State diagram is given, which describes the behaviour of the circuit that is to be designed.

Step 2:- Obtain the state table

Step 3:- The no. of states can be reduced by state reduction method.

Step 4:- Do state assignment of required.

Step 5:- obtain the expression from circuit o/p & f/p. & Implement the circuit.

## Registers & Counters

### Module - 4

Shift Register,  
Ripple counter,  
Synchronous counter  
other counter, HDL for  
Reg

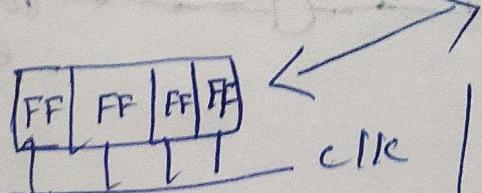
- Counter is a digital device used to count number of pulses & also used for frequency divider.
- Counter can count in 2 ways ie
- 1 up count. ( $0, 1, 2, \dots, N$ ) used EVM, shopping mode
  - 2 down count ( $N, N-1, \dots, 1, 0$ ) - Space related app
- Present count of the counter & represent state of counter x.
- Counter contains set of FFs, A n-bit counter will FFs &  $2^n$  states.
- 4 bit. to count. 4 FF  
 $\frac{\text{total } f_3}{2^n}$
- Each state frequency = total f<sub>3</sub> /  $2^n$ .

$$3 \text{ bit counter} = 2^3 \text{ state} \cdot 8 \text{ state.}$$

State frequency.  $\frac{\text{total}}{2^n}$

### Classification

A Synchro, Synchronous.



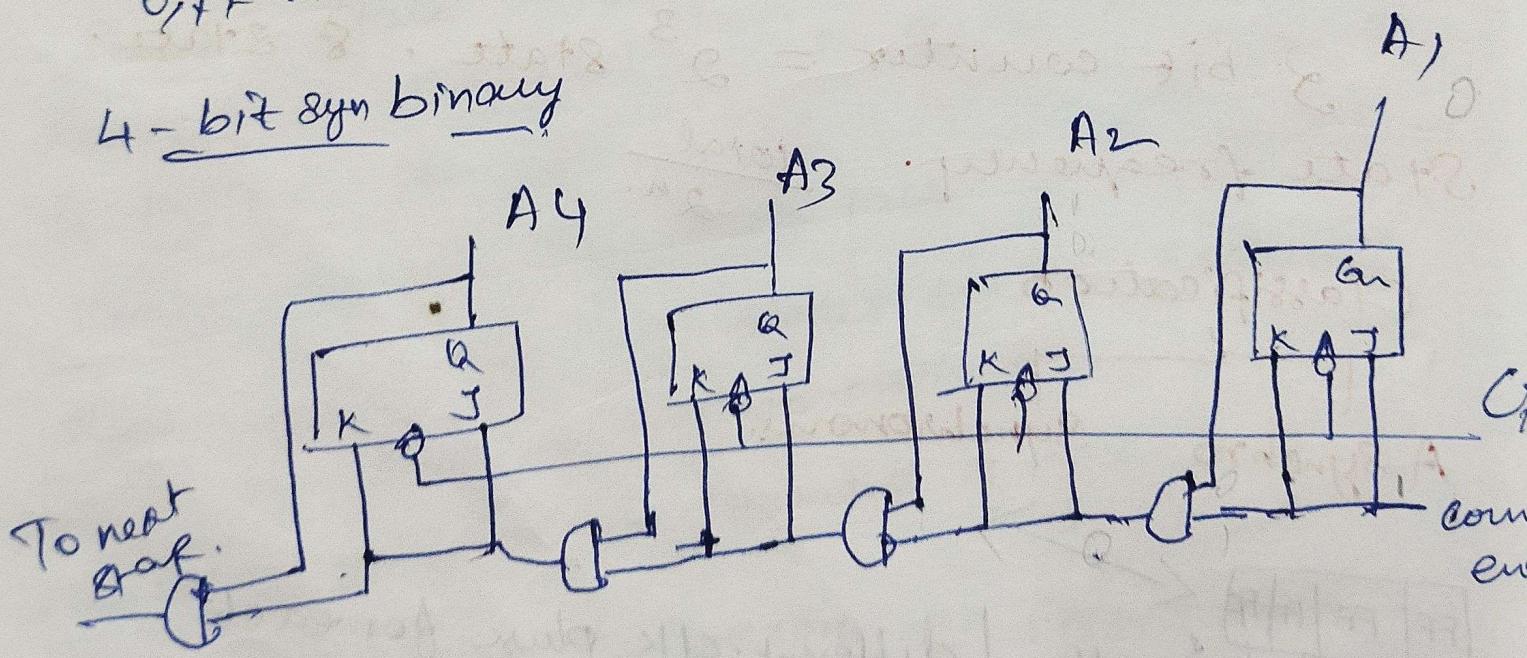
different clk pulse for each FF in the counter.

- Asynchronous
- Async refers to states that doesn't have a fixed time relationship with each other.
  - In. Asyn counter ff doesn't have similar clock ~~phase~~ pulse. So their states change exactly at same time.
  - First FF has clk, output of each FF will acts clock to next FF.
  - Ex:- Ripple counter, up, down.

### Synchronous counters

up counter, Down counter, up/down.  
0, 1, ..., N, N ..., 0.

### 4-bit syn binary



'fixed edge trigger clk'

" coat "

pr JK N +

x 1 1 \*

x 0 0 \*

77-P

Q<sub>3</sub> Q<sub>2</sub> Q<sub>1</sub> Q<sub>0</sub>

0 0 0 0 0

0 0 1 0 1

0 0 1 1 2 77

0 1 0 0 3 T

24

1100

0

1

0

1

0

1

0

1

+ progress after unit 18

units left

progress toward

000

111

110

B & this can

not be

8 5 6

000

100

110

(1)

110

### 3-bit Synchronous UP counter

Step 1: Determine no. of FFs = 3. So 3 FF  
Decide type of FF using T-FF

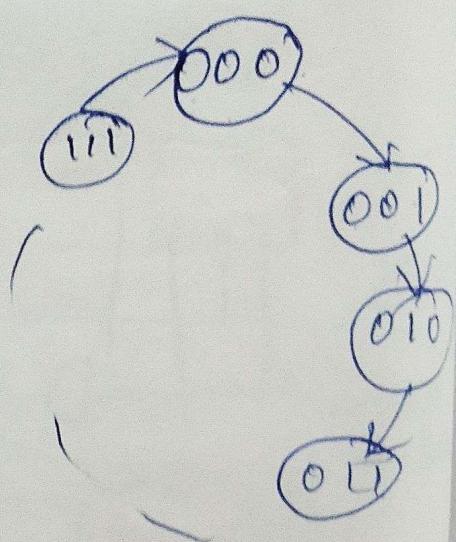
Step 2:- make the Excitation table for the FF.

$P_s$	$Q_n$	$Q_{n+1}$	T
0	0	0	0
0	0	1	1
1	0	0	1
1	1	1	0

$$2^3 = 8$$

Step 3:- find the state diagram & circuit diagram.

$2^3 = 8$  states. Max count is 7.  
 000 ...  
 001  
 010  
 011  
 111



### Circuit Table

<u>PS.</u>	N.S.			FF II/P		
	<u>Q<sub>C</sub></u>	<u>Q<sub>B</sub></u>	<u>Q<sub>A</sub></u>	<u>T<sub>C</sub></u>	<u>T<sub>B</sub></u>	<u>T<sub>A</sub></u>
0	0	0	0	0	0	1
0	0	1	0	0	1	1
0	1	0	0	1	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	0
1	0	1	1	1	0	1
1	1	0	1	1	0	1
1	1	1	0	0	0	1

from the state diagram Step 4 :- Obtain Simplified equation using k-map  
Boolean expression

$Q_C + \bar{Q}_C^+$   $\Rightarrow$  check in exci table.

<u>Q<sub>C</sub></u>	<u>Q<sub>B</sub></u>	<u>Q<sub>A</sub></u>	<u>T<sub>C</sub></u>
0	0	0	0
0	1	0	1

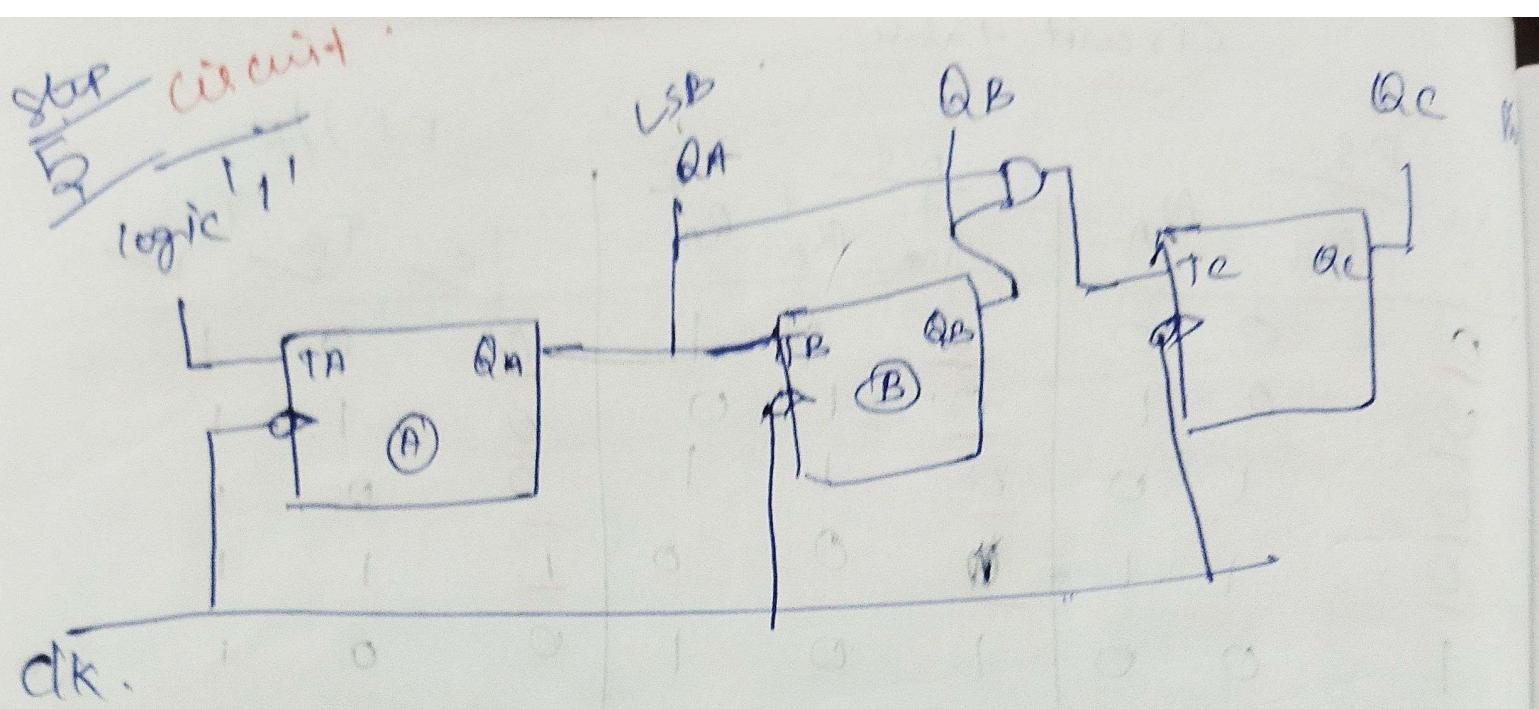
$T_C = Q_B Q_A$

<u>Q<sub>C</sub></u>	<u>Q<sub>B</sub></u>	<u>Q<sub>A</sub></u>	<u>T<sub>B</sub></u>
0	0	0	0
0	1	1	0

$T_B = Q_A$

<u>Q<sub>C</sub></u>	<u>Q<sub>B</sub></u>	<u>Q<sub>A</sub></u>	<u>T<sub>A</sub></u>
0	0	0	1
1	1	1	1

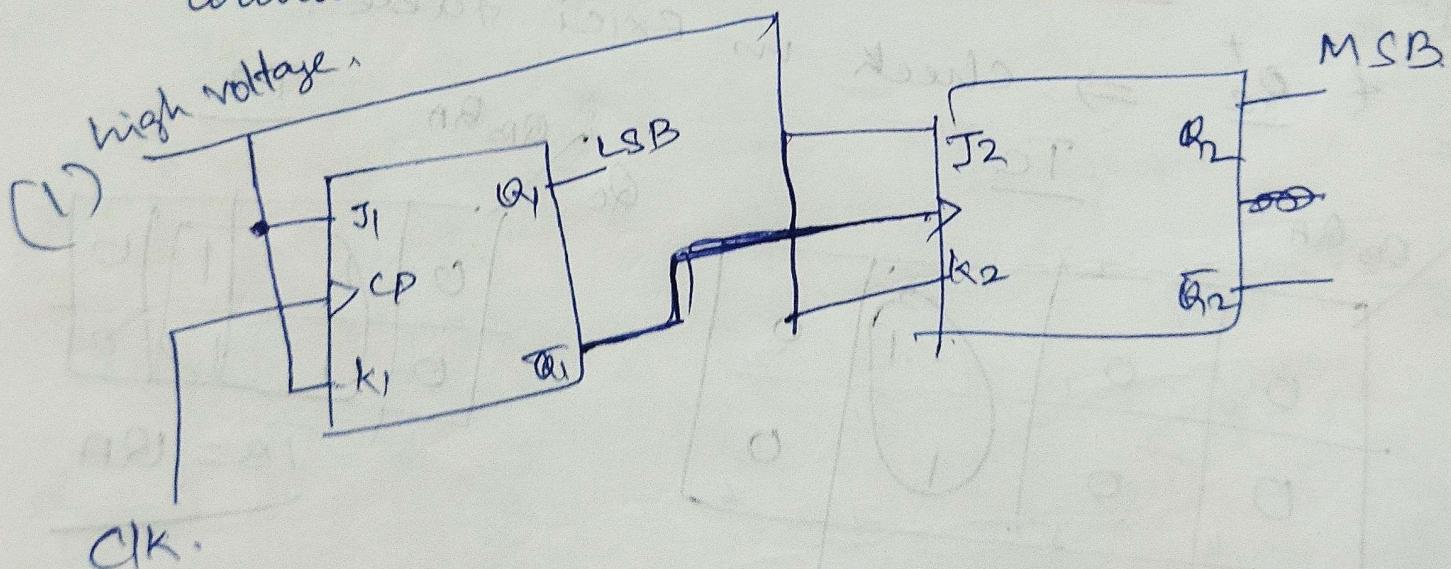
$T_A = 1$



$$TA = \frac{1}{T_B} \quad QC = QA \cdot QB.$$

2-bit Asynchronous Up counter - Ripple.

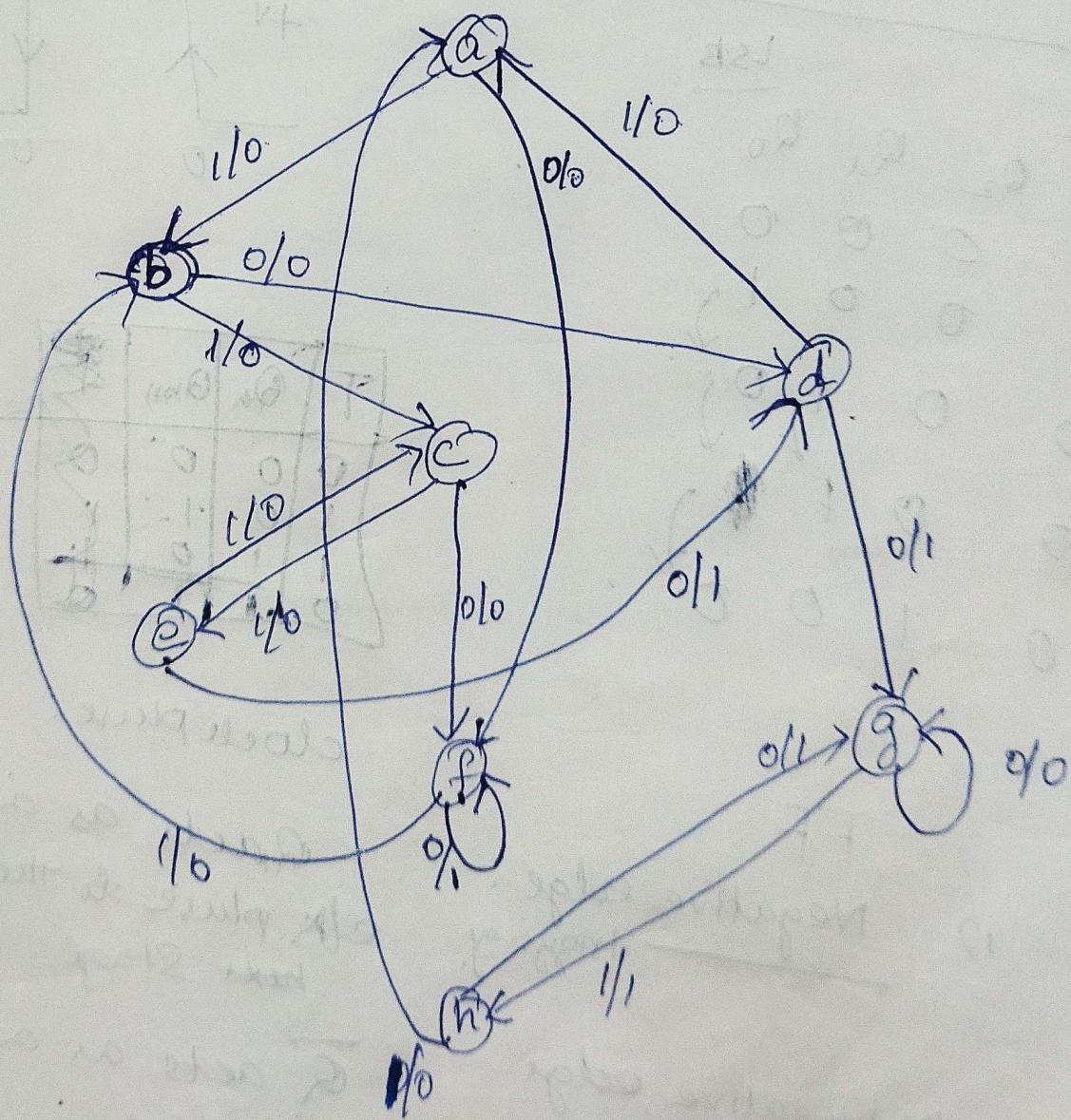
→ clk is not simultaneously to all the counter.



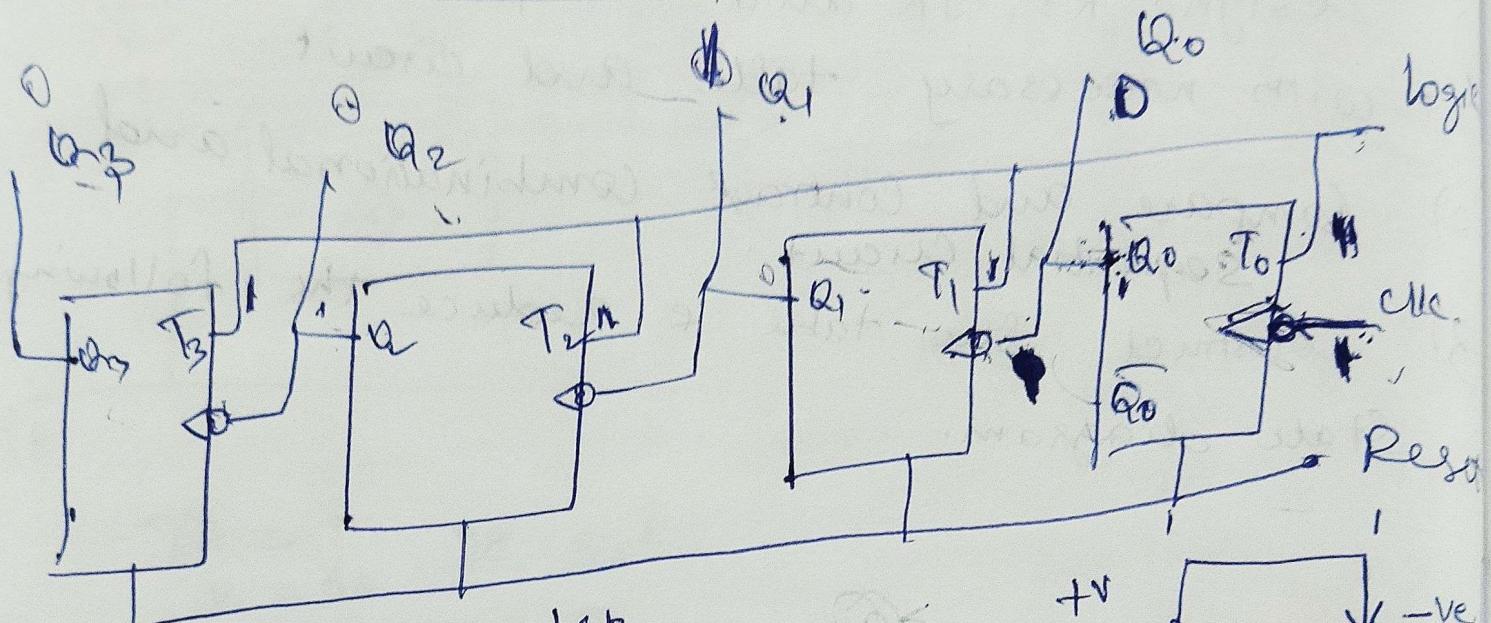
every time the JK = 1, toggle state.

### Assignment - 3

- 1) Design RS, JK and T- Flip flop with necessary table and circuit.
- 2) Compare and contrast combinational and sequential circuit.
- 3) Construct the table & reduce the following State diagram.



Ripple counter  
Asynchronous counter is not having similar pulse.



	MSB	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	LSB
0.	0.	0	0	0	0	0
1	0	0	0	1	0	1
2	0	0	1	0	0	0
3	0	0	0	1	0	1
4	0	1	0	0	0	0

T	Q <sub>n</sub>	Q <sub>(n+1)</sub>	
0	0	0	0
1	0	1	1
1	1	0	1
0	1	1	0

clock phase.

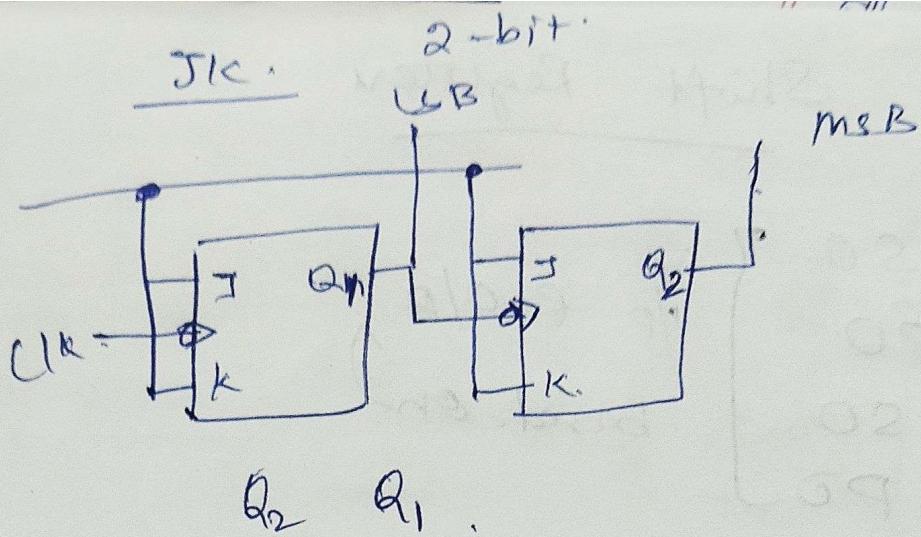
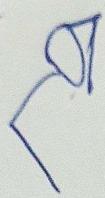
1) FF  
Negative edge triggering.

acts as a  
clk phase to the  
next stage. up

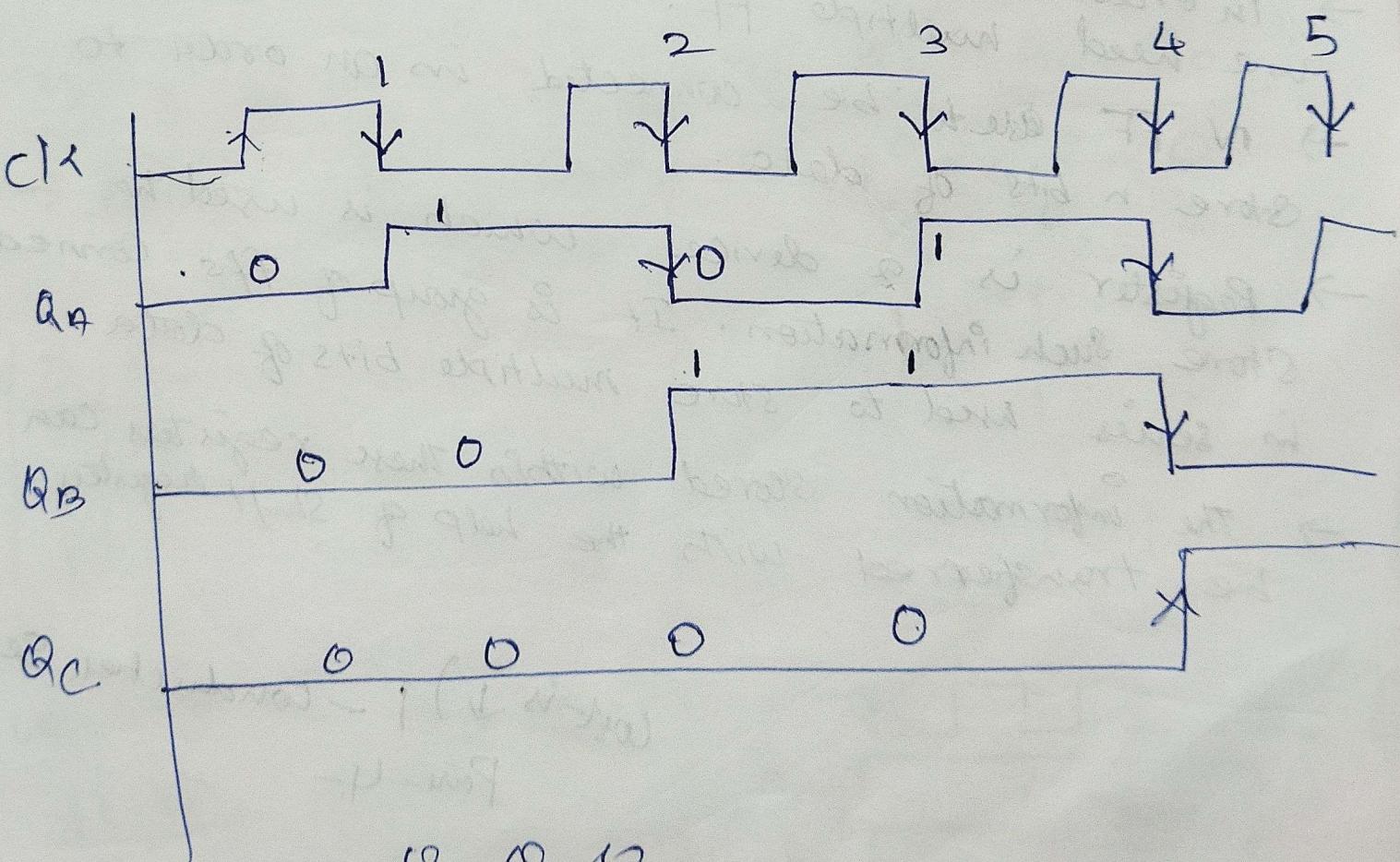
- 2) Negative edge
- 3) +ve edge
- 4) +ve edge triggering

1) Q acts as a  
clk phase;  
2) acts as a clk phase  
3) acts as a clk phase  
4) acts as

7



- Asynchronous counter
- Different FF are used with a diff clk phase.
- All the FF are used in toggle mode.



0	0	0
0	0	1
0	1	0
0	1	1

## Shift Registers

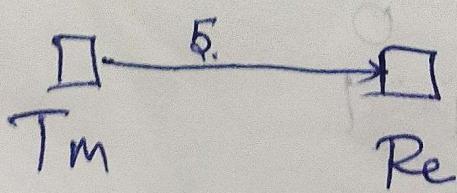
✓ SISO      ]  
✓ SIPO      ] I/P & O/P  
✓ PISO      ] based. on  
✓ PIPO

- Flip flops can be used to store a single bit of binary data (0 or 1)
- In order to store multiple bits of data, we need multiple FF.
- N FF are to be connected in an order to store n bits of data.
- Register is a device which is used to store such information. It is group of FFs connected in series used to store multiple bits of data.
- The information stored within these registers can be transferred with the help of Shift registers.

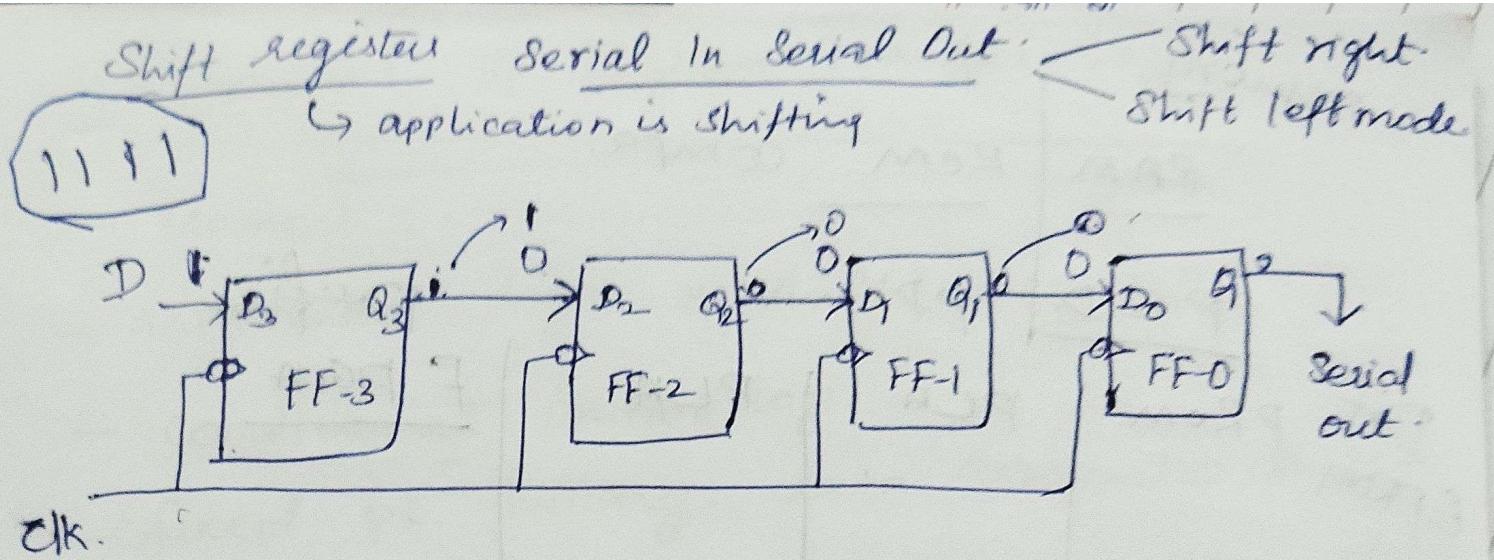
(cost is ↓) ; - conducted.

Part 4:-

use of Shift Register.      4 CLK.



4 bit numbers.



→ It is a sequential circuit which is used to data storage & data transfer.

→ 4 - D FF

→ Initial '0'

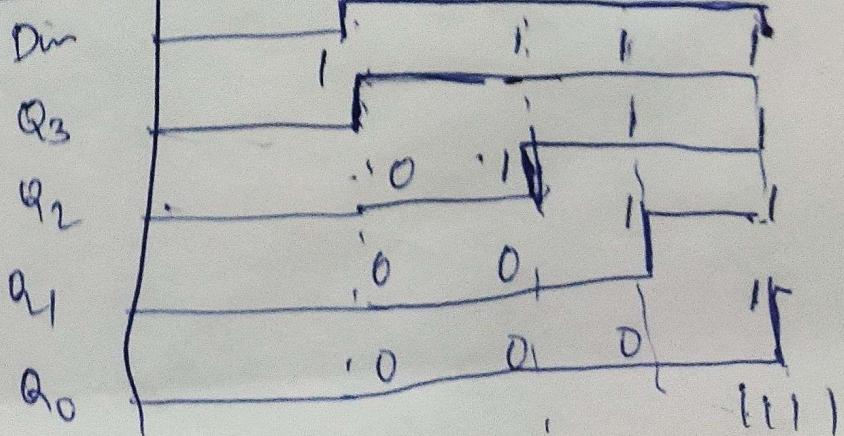
Clk	D	$Q_{n+1}$
0	X	$Q_n$
1	0	0
1	1	1

Clk.	$Q_3$	$Q_2$	$Q_1$	$Q_0$
Init	0	0	0	0
↓	0	0	0	0
↓	1	0	0	0
↓	1	1	0	0
↓	1	1	1	0
↓	1	1	1	1

we want to store:

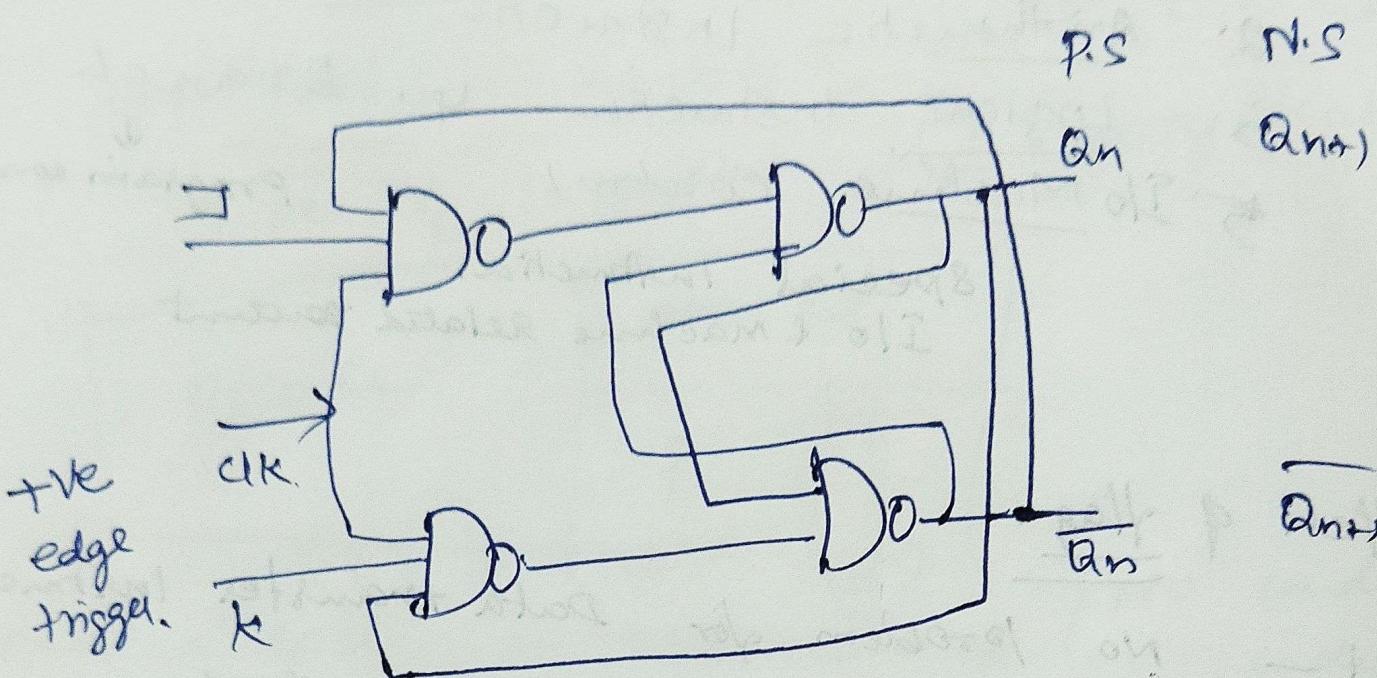
1111

wave form of Clk



# JK flip flop

~~clock~~  $J = 1, K = 0$



Clk	J	K	Qn	Qn <sub>prev</sub>	Previous State <u>Qn</u>
↑	0	0	X	X	reset <u>0</u>
↑	0	1	X	X	Set <u>1</u>
↑	1	1	X	X	<u>Qn</u>

$$Clk = 1 \quad J=0, \quad K=1 \quad Q_n = 0$$

$$1 \cdot \overline{Q_n} = Q_n \cdot 0 \quad \checkmark$$

$$\begin{matrix} 0 \\ 1 \end{matrix} \rightarrow \begin{matrix} 0 \\ 1 \end{matrix}$$

$$\begin{matrix} 0 \\ 1 \end{matrix} \quad \begin{matrix} 0 \\ 1 \end{matrix} \quad \begin{matrix} 0 \\ 1 \end{matrix}$$

$$1 \rightarrow \overline{1 \cdot Q_n} = \overline{Q_n} \cdot 1$$

$$\begin{matrix} 0 \\ 1 \end{matrix}$$

$$\begin{matrix} 1 \\ 0 \end{matrix} \quad \begin{matrix} 1 \\ 0 \end{matrix} \quad \begin{matrix} 1 \\ 0 \end{matrix}$$

$$Clk = 1 \quad J=1, \quad K=0 \quad Q_n = 1$$

$$1 \rightarrow \overline{1 \cdot \overline{Q_n}} = Q_n = 1 \quad \checkmark$$

$$0$$

3ilp NAND

3ilp AND

$$000 \quad 0$$

$$001 \quad 0$$

$$010 \quad 0$$

$$011 \quad 0$$

$$100 \quad 0$$

$$101 \quad 0$$

$$110 \quad 0$$

~~add A + B = C~~

$$000 \quad 1$$

$$001 \quad 1$$

$$010 \quad 1$$

$$011 \quad 1$$

$$100 \quad 1$$

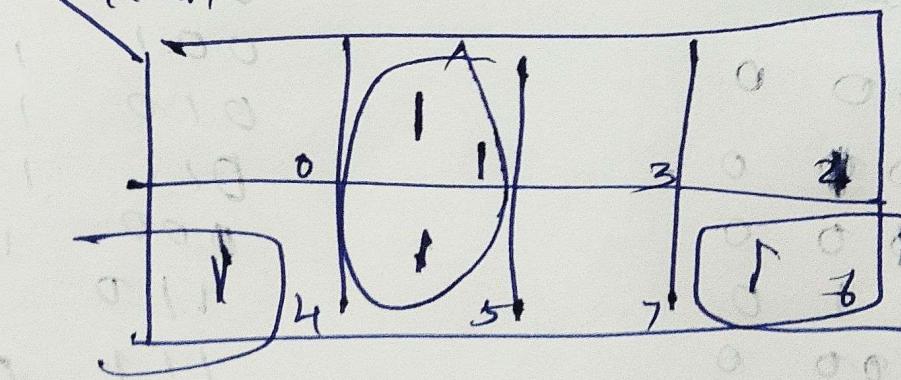
$$110 \quad 1$$

$$111 \quad 0$$

chara table

J	K	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$Q_{n+1} = J Q_n + K Q_n$$



$$Q_{n+1} = \overline{J} Q_n + \overline{K} Q_n$$

## Excitation table.

$Q_m$	$Q_{m+1}$	J. K.	
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0.