

## 8.8 Intrinsic Semiconductor

A semiconductor in an extremely pure form is known as an **intrinsic semiconductor**.

In an intrinsic semiconductor, even at room temperature, hole-electron pairs are created. When electric field is applied across an intrinsic semiconductor, the current conduction takes place by two processes, namely ; by *free electrons* and *holes* as shown in Fig. 8.10. The free electrons are produced due to the breaking up of some covalent bonds by thermal energy. At the same time, holes are created in the covalent bonds. Under the influence of electric field, conduction through the semiconductor is by both free electrons and holes. Therefore, the total current inside the semiconductor is the sum of currents due to free electrons and holes.

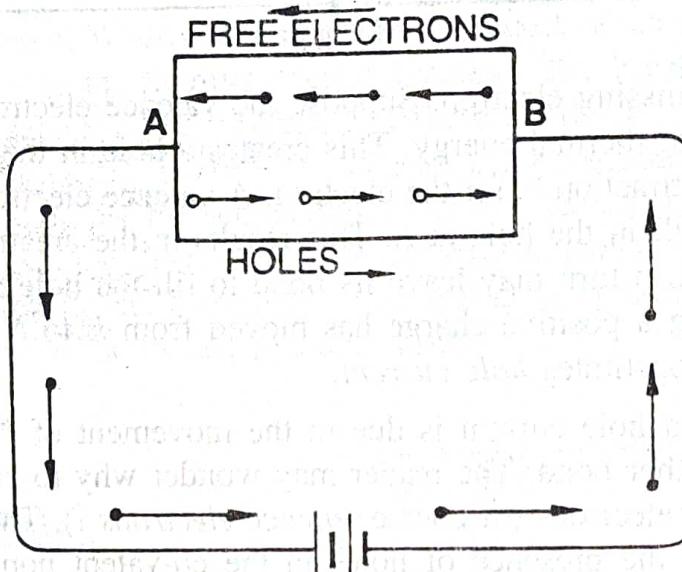


Fig. 8.10

It may be noted that current in the external wires is fully electronic *i.e.* by electrons. What about the holes? Referring to Fig. 8.10, holes being positively charged move towards the negative terminal of supply. As the holes reach the negative terminal *B*, electrons enter the semiconductor crystal near the terminal and combine with holes, thus cancelling them. At the same time, the loosely held electrons near the positive terminal are attracted away from their atoms into the positive terminal. This creates new holes near the positive terminal which again drift towards the negative terminal.

## 8.9 Extrinsic Semiconductor

The intrinsic semiconductor has little current conduction capability at room temperature. To be useful in electronic devices, the pure semiconductor must be altered so as to significantly increase its conducting properties. This is achieved by adding a small amount of suitable impurity to a semiconductor. It is then called *impurity or extrinsic semiconductor*. The process of adding impurities to a semiconductor is known as *doping*. The amount and type of such impurities have to be closely controlled during the preparation of extrinsic semiconductor. Generally, for  $10^8$  atoms of semiconductor, one impurity atom is added.

The purpose of adding impurity is to increase either the number of free electrons or holes in the semiconductor crystal. As we shall see, if a pentavalent impurity (having 5 valence electrons) is added to the semiconductor, a large number of free electrons are produced in the semiconductor. On the other hand, addition of trivalent impurity (having 3 valence electrons) creates a large

number of holes in the semiconductor crystal. Depending upon the type of impurity added, extrinsic semiconductors are classified into :

(i) *n*-type semiconductor

(ii) *p*-type semiconductor

### 8.10 *n*-type Semiconductor

When a small amount of pentavalent impurity is added to a pure semiconductor, it is known as *n*-type semiconductor.

The addition of pentavalent impurity provides a large number of free electrons in the semiconductor crystal. Typical examples of pentavalent impurities are arsenic (At. No. 33), and antimony (At. No. 51). Such impurities which produce *n*-type semiconductor are known as donor impurities because they donate or provide free electrons to the semiconductor crystal.

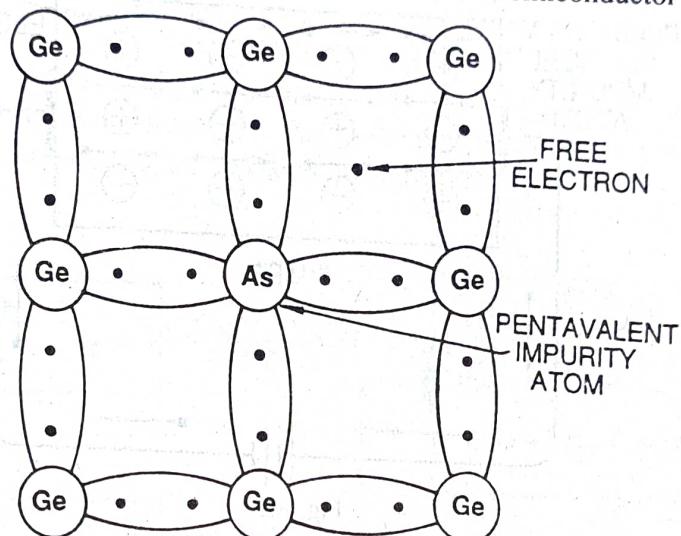


Fig. 8.11

To explain the formation of *n*-type semiconductor, consider a pure germanium crystal. We know that germanium atom has four valence electrons. When a small amount of pentavalent impurity like arsenic is added to germanium crystal, a large number of free electrons become available in the crystal. The reason is simple. Arsenic is pentavalent *i.e.* its atom has five valence electrons. An arsenic atom fits in the germanium crystal in such a way that its four valence electrons form covalent bonds with four germanium atoms. The fifth valence electron of arsenic atom finds no place in co-valent bonds and is thus free as shown in Fig. 8.11. Therefore, for each arsenic atom added, one free electron will be available in the germanium crystal. Though each arsenic atom provides one free electron, yet an extremely small amount of arsenic impurity provides enough atoms to supply millions of free electrons.

Fig. 8.12 shows the energy band description of *n*-type semi-conductor. The addition of pentavalent impurity has produced a number of conduction band electrons *i.e.*, free electrons. The four valence electrons of pentavalent atom form covalent bonds with four neighbouring germanium atoms. The fifth left over valence electron of the pentavalent atom cannot be accommodated in the valence band and travels to the conduction band. The following points may be noted carefully :

- (i) Many new free electrons are produced by the addition of pentavalent impurity.

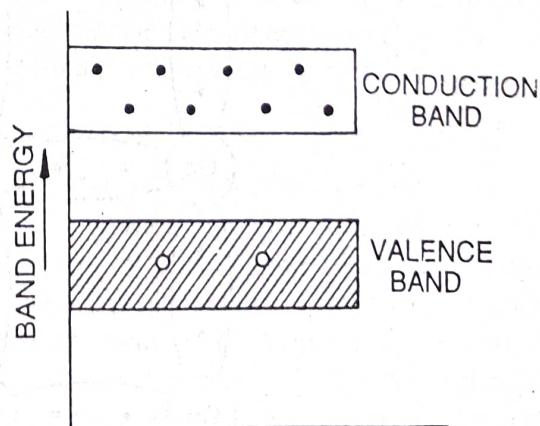


Fig. 8.12

(ii) Thermal energy of room temperature still generates a few hole-electron pairs. However, the number of free electrons provided by the pentavalent impurity far exceeds the number of holes. It is due to this predominance of electrons over holes that it is called *n-type semiconductor* (*n* stands for negative).

**n-type conductivity.** The current conduction in an *n-type semiconductor* is predominantly by free electrons *i.e.* negative charges and is called *n-type or electron type conductivity*. To understand *n-type conductivity*, refer to Fig. 8.13. When p.d. is applied across the *n-type semiconductor*, the free electrons (donated by impurity) in the crystal will be directed towards the positive terminal, constituting electric current. As the current flow through the crystal is by free electrons which are carriers of negative charge, therefore, this type of conductivity is called negative or *n-type conductivity*. It may be noted that conduction is just as in ordinary metals like copper.

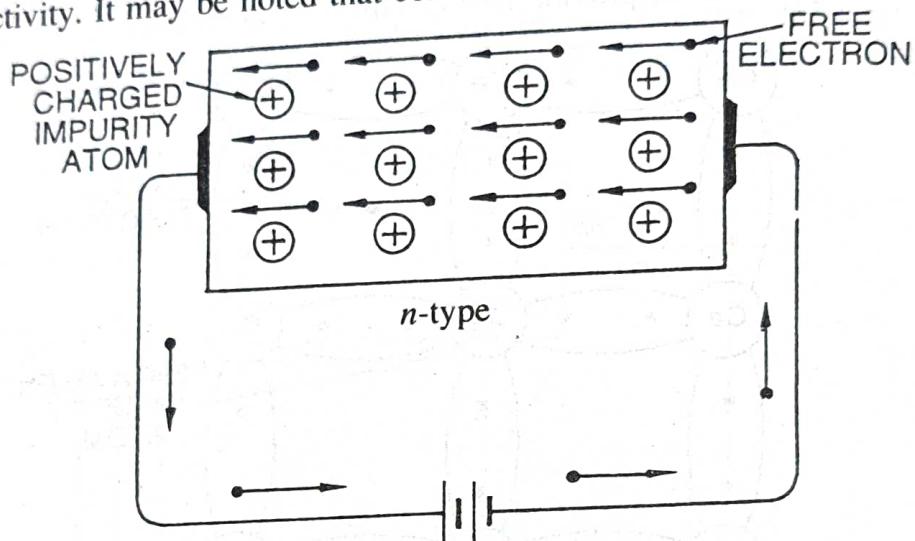


Fig. 8.13

## 8.11 p-type Semiconductor

When a small amount of trivalent impurity is added to a pure semiconductor, it is called *p-type semiconductor*.

The addition of trivalent impurity provides a large number of holes in the semiconductor. Typical examples of trivalent impurities are gallium (At. No. 31) and indium (At. No. 49). Such impurities which produce *p-type semiconductor* are known as acceptor impurities because the holes created can accept the electrons.

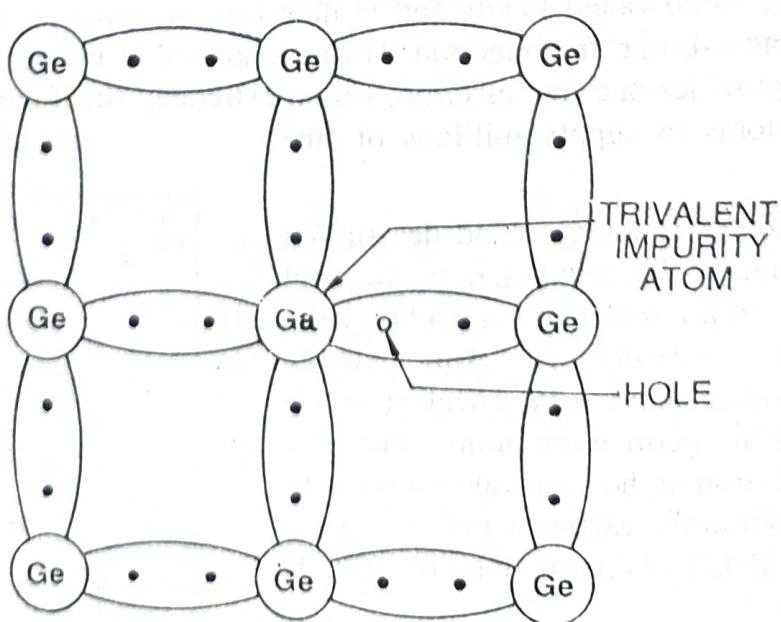


Fig. 8.14

To explain the formation of *p*-type semiconductor, consider a pure germanium crystal. When a small amount of trivalent impurity like gallium is added to germanium crystal, there exists a large number of holes in the crystal. The reason is simple. Gallium is trivalent *i.e.* its atom has three valence electrons. Each atom of gallium fits into the germanium crystal but now can form only three single co-valent bonds with three germanium atoms as shown in Fig. 8.14. In the fourth co-valent bond, only germanium atom contributes one valence electron while gallium has no valence electron to contribute as all its three valence electrons are already engaged in the co-valent bonds with neighbouring germanium atoms. In other words, fourth bond is incomplete; being short of one electron. This missing electron is called a *hole*. Therefore, for each gallium atom added, one hole is created. A small amount of gallium provides millions of holes.

Fig. 8.15 shows the energy band description of the *p*-type semiconductor. The addition of trivalent impurity has produced a large number of holes. However, there are a few conduction band electrons due to thermal energy associated with room temperature. But the holes far outnumber the conduction band electrons. It is due to the predominance of holes over free electrons that it is called *p*-type semiconductor (*p* stands for positive).

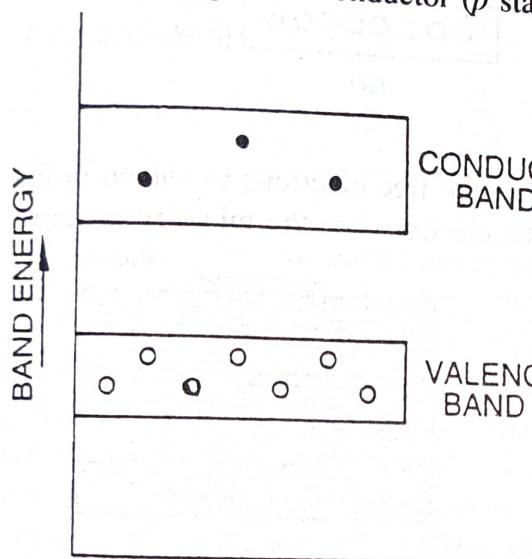


Fig. 8.15

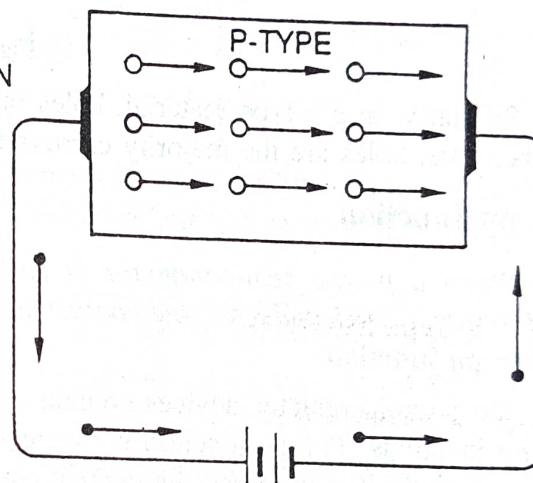


Fig. 8.16

**p-type conductivity.** The current conduction in *p*-type semiconductor is predominantly by holes *i.e.* positive charges and is called *p*-type or *hole-type* conductivity. To understand *p*-type conductivity, refer to Fig. 8.16. When *p.d.* is applied to the *p*-type semiconductor, the holes (donated by the impurity) are shifted from one co-valent bond to another. As the holes are positively charged, therefore, they are directed towards the negative terminal, constituting what is known as hole current. It may be noted that in *p*-type conductivity, the valence electrons move from one co-valent bond to another unlike the *n*-type where current conduction is by free electrons.

## 8.12 Charge on *n*-type and *p*-type Semiconductors

As discussed before, in *n*-type semiconductor, current conduction is due to excess of electrons whereas in a *p*-type semiconductor, conduction is by holes. The reader may think that *n*-type material has a net negative charge and *p*-type a net positive charge. But this conclusion is wrong. It is true that *n*-type semiconductor has excess of electrons but these extra electrons were supplied by the atoms of donor impurity and each atom of donor impurity is electrically neutral. When the impurity atom is added, the term "excess electrons" refers to an excess with regard to the number of electrons needed to fill the co-valent bonds in the semiconductor crystal. The extra electrons are free electrons and increase the conductivity of the semiconductor. The situation with regard to *p*-type semiconductor is also similar. *It follows, therefore, that n-type as well as p-type semiconductor is electrically neutral.*

### 8.13 Majority and Minority Carriers

It has already been discussed that due to the effect of impurity, *n*-type material has a large number of free electrons whereas *p*-type material has a large number of holes. However, it may be recalled that even at room temperature, some of the co-valent bonds break, thus releasing an equal number of free electrons and holes. An *n*-type material has its share of electron-hole pairs (released due to breaking of bonds at room temperature) but in addition has a much larger quantity of free electrons due to the effect of impurity. These impurity-caused free electrons are not associated with holes. Consequently, an *n*-type material has a large number of free electrons and a small number of holes as shown in Fig. 8.17(i). The free electrons in this case are considered *majority carriers*—since the *majority portion of current in n-type material is by the flow of free electrons* — and the holes are the *minority carriers*.

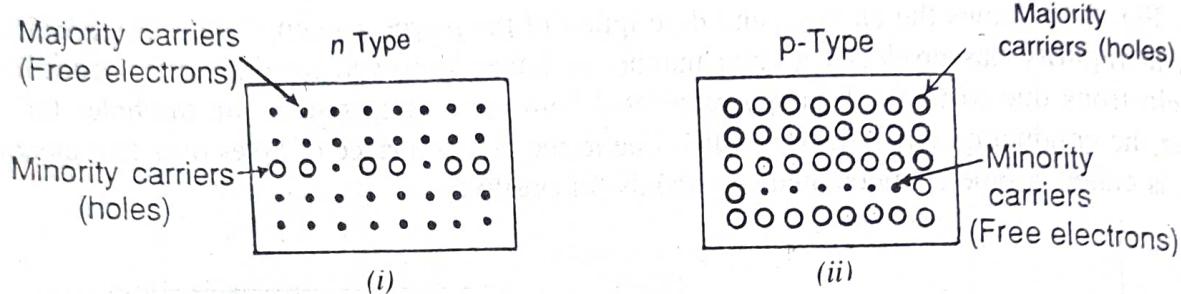


Fig. 8.17

Similarly, in a *p*-type material, holes outnumber the free electrons as shown in Fig. 8.17(ii). Therefore, holes are the majority carriers and free electrons are the minority carriers:

### 8.14 pn Junction

*When a p-type semiconductor is suitably joined to n-type semiconductor, the contact surface is called pn junction.*

Most semiconductor devices contain one or more *pn* junctions. The *pn* junction is of great importance because it is in effect, the *control element* for semiconductor devices. A thorough knowledge of the formation and properties of *pn* junction can enable the reader to understand the semiconductor devices.

**Formation of pn junction.** In actual practice, the characteristic properties of *pn* junction will not be apparent if a *p*-type block is just brought in contact with *n*-type block. In fact, *pn* junction is fabricated by special techniques. One common method of making *pn* junction is called *alloying*. In this method, a small block of indium (trivalent impurity) is placed on an *n*-type germanium slab as shown in Fig. 8.18 (i). The system is then heated to a temperature of about  $500^{\circ}\text{C}$ . The indium and some of the germanium melt to form a small puddle of molten germanium-indium mixture as shown in Fig. 8.18 (ii). The temperature is then lowered and puddle begins to solidify. Under proper conditions, the atoms of indium impurity will be suitably ad-

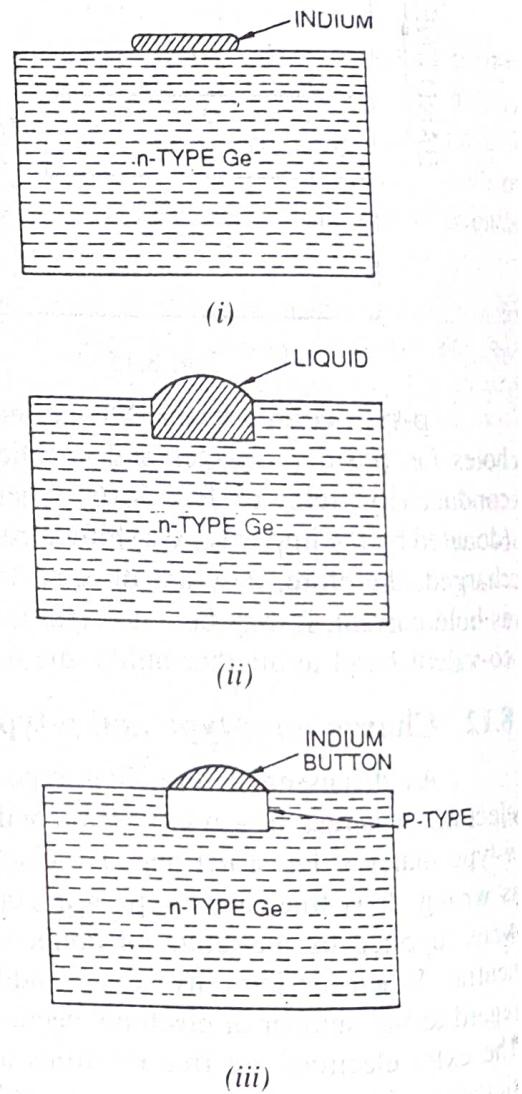


Fig. 8.18

justed in the germanium slab to form a single crystal. The addition of indium overcomes the excess of electrons in the *n*-type germanium to such an extent that it creates a *p*-type region.

As the process goes on, the remaining molten mixture becomes increasingly rich in indium. When all germanium has been redeposited, the remaining material appears as indium button which is frozen on to the outer surface of the crystallised portion as shown in Fig. 8.18 (iii). This button serves as a suitable base for soldering on leads.

### 8.15 Properties of *pn* Junction

To explain the properties of an *pn* junction, consider two types of materials; one *p*-type having \*negative acceptor ions and positively charged holes. The right side material is *n*-type semiconductor having \*\*positive donor ions and free electrons.

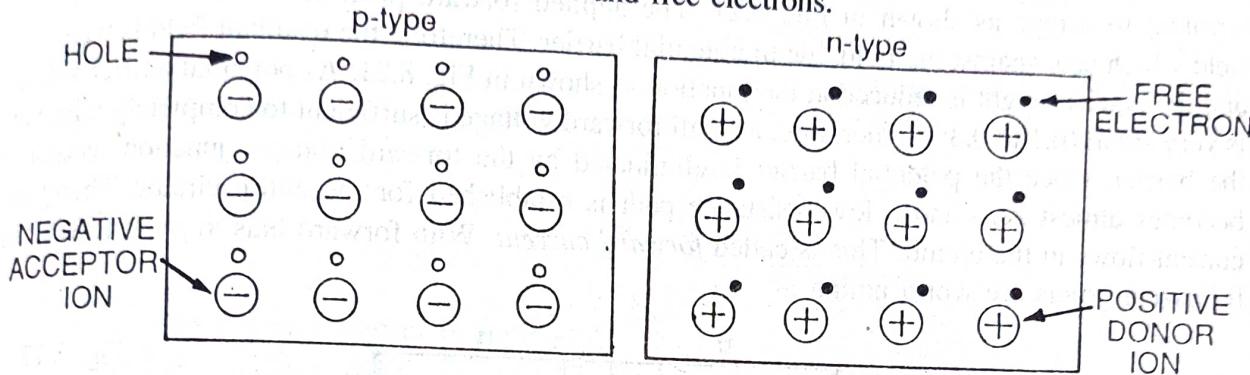


Fig 8.19

Now, suppose the two pieces are suitably treated to form *pn* junction. Keep in mind that *n*-type material has a high concentration of free electrons while *p*-type material has a high concentration of holes. Therefore, at the junction, there is a tendency for the free electrons to diffuse over to the *p*-side and holes to the *n*-side. This process is called diffusion. As the free electrons move across the junction from *n*-type to *p*-type, positive donor ions are uncovered i.e. they are robbed of free electrons. Hence, a positive charge is built on the *n*-side of the junction. At the same time, the free electrons cross the junction and uncover the negative acceptor ions by filling in the holes. Therefore, a net negative charge is established on *p*-side of the junction. When a sufficient number of donor and acceptor ions is uncovered, further diffusion is prevented. It is because now positive charge on *n*-side repels holes to cross from *p*-type to *n*-type and negative charge on *p*-side repels free electrons to enter from *n*-type to *p*-type. Thus, a barrier is set up against further movement of charge carriers i.e. holes and electrons. This is called potential barrier or junction barrier  $V_o$ . The potential barrier is of the order of 0.1 to 0.3 volt. The potential distribution diagram is shown in Fig. 8.20. It is clear from the diagram that a potential barrier  $V_o$  is set up which gives rise to electric field. This field prevents the respective majority carriers from crossing the barrier region.

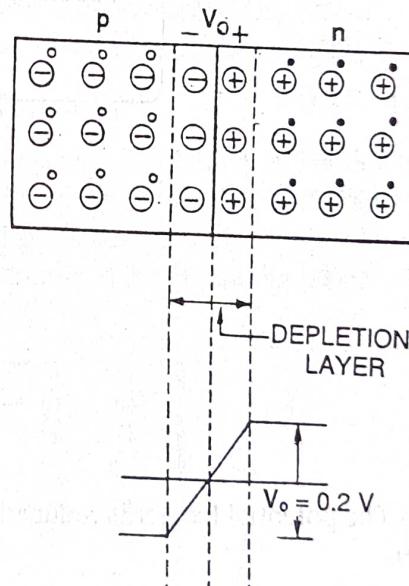


Fig. 8.20

\* The acceptor impurity atom is short of one electron. Therefore, it becomes a negative ion.

\*\* The donor impurity atom donates one electron to the crystal and becomes a positive ion.

It should be noted that outside this barrier on each side of the junction, the material is still neutral. Only inside the barrier, there is positive charge on *n*-side and negative charge on *p*-side. This region is called *depletion layer*. It is called so because the mobile charge carriers (*i.e.* free electrons and holes) have been depleted (*i.e.* emptied) in this region.

### 8.16 Applying Voltage Across pn Junction

The potential difference across a *pn* junction can be applied in two ways, namely; *forward biasing* and *reverse biasing*.

**1. Forward biasing.** When external voltage applied to the junction is in such a direction that it cancels the potential barrier, thus permitting current flow, it is called **forward biasing**.

To apply forward bias, connect positive terminal of the battery to *p*-type and negative terminal to *n*-type as shown in Fig. 8.21. The applied forward potential establishes an electric field which acts against the field due to potential barrier. Therefore, the resultant field is weakened and the barrier height is reduced at the junction as shown in Fig. 8.21. As potential barrier voltage is very small (0.1 to 0.3 V), therefore, a small forward voltage is sufficient to completely eliminate the barrier. Once the potential barrier is eliminated by the forward voltage, junction resistance becomes almost zero and a low resistance path is established for the entire circuit. Therefore, current flows in the circuit. This is called *forward current*. With forward bias to *pn* junction, the following points are worth noting :-

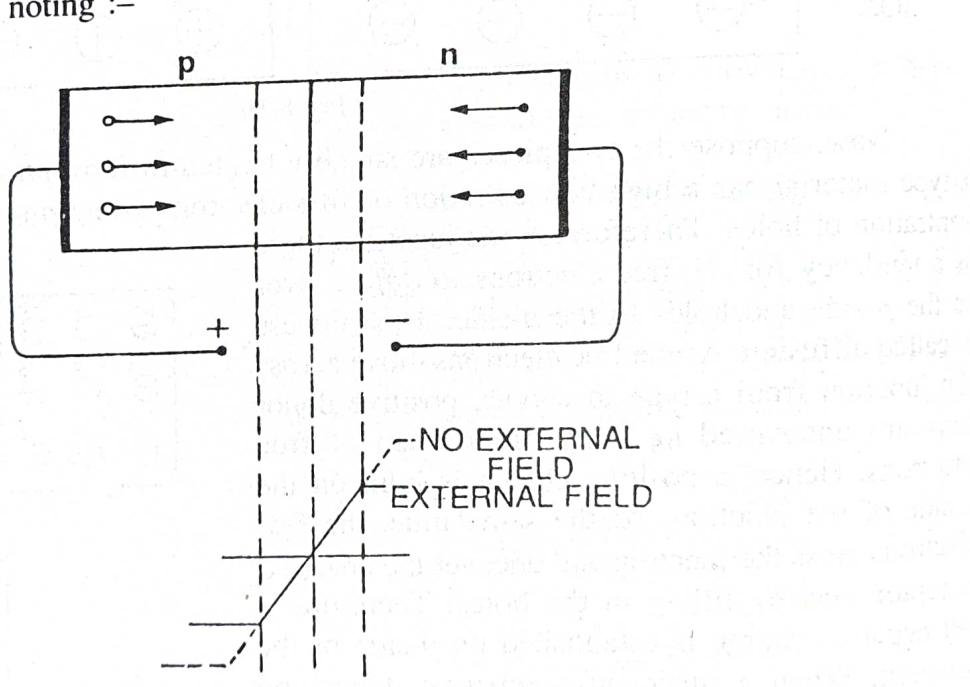


Fig. 8.21

(i) The potential barrier is reduced and at some forward voltage (0.1 to 0.3V), it is eliminated altogether.

(ii) The junction offers low resistance (called *forward resistance*,  $R_f$ ) to current flow.

(iii) Current flows in the circuit due to the establishment of low resistance path. The magnitude of current depends upon the applied forward voltage.

**2. Reverse biasing.** When the external voltage applied to the junction is in such a direction that potential barrier is increased, it is called **reverse biasing**.

To apply reverse bias, connect negative terminal of the battery to *p*-type and positive terminal to *n*-type as shown in Fig. 8.22. It is clear that applied reverse voltage establishes an electric field which acts in the same direction as the field due to potential barrier. Therefore, the resultant field at the junction is strengthened and the barrier height is increased as shown in Fig.

8.22. The increased potential barrier prevents the flow of charge carriers across the junction. Thus, a high resistance path is established for the entire circuit and hence the current does not flow. With reverse bias to  $pn$  junction, the following points are worth noting :-

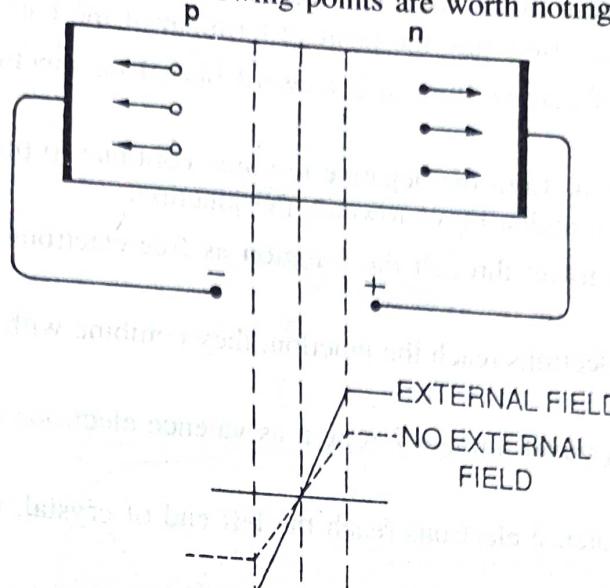


Fig. 8.22

- (i) The potential barrier is increased.
- (ii) The junction offers very high resistance (called *reverse resistance*  $R_r$ ) to current flow.
- (iii) No current flows in the circuit due to the establishment of high resistance path.

**Conclusion.** From the above discussion, it follows that with reverse bias to the junction, a high resistance path is established and hence no current flow occurs. On the other hand, with forward bias to the junction, a low resistance path is set up and hence current flows in the circuit.

### 8.17 Current Flow in a Forward Biased $pn$ Junction

We shall now see how current flows across  $pn$  junction when it is forward biased. Fig. 8.23 shows a forward biased  $pn$  junction. Under the influence of forward voltage, the free electrons in  $n$ -type move \*towards the junction, leaving behind positively charged atoms. However, more electrons arrive from the negative battery terminal and enter the  $n$ -region to take up their places.

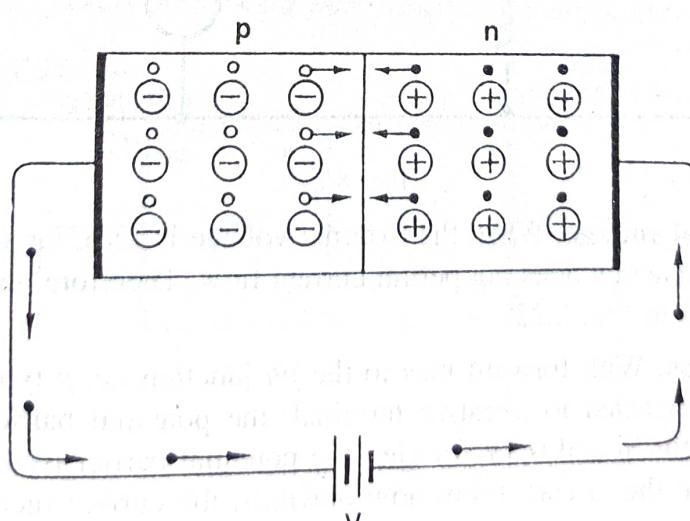


Fig. 8.23

\* Note that negative terminal of battery is connected to  $n$ -type. It repels the free electrons in  $n$ -type towards the junction.

As the free electrons reach the junction, they become \*valence electrons. As valence electrons, they move through the holes in the *p*-region. The valence electrons move towards left in the *p*-region which is equivalent to the holes moving to right. When the valence electrons reach the left end of the crystal, they flow into the positive terminal of the battery.

The mechanism of current flow in a forward biased *pn* junction can be summed up as under :

(i) The free electrons from the negative terminal continue to pour into the *n*-region while the free electrons in the *n*-region move towards the junction.

(ii) The electrons travel through the *n*-region as free-electrons i.e. current in *n*-region is by free electrons.

(iii) When these electrons reach the junction, they combine with holes and become valence electrons.

(iv) The electrons travel through *p*-region as valence electrons i.e. current in the *p*-region is by holes.

(v) When these valence electrons reach the left end of crystal, they flow into the positive terminal of the battery.

From the above discussion, it is concluded that in *n*-type region, current is carried by free electrons whereas in *p*-type region, it is carried by holes. However, in the external connecting wires, the current is carried by free electrons

### 8.18 Volt-Ampere Characteristics of *pn* Junction

 Volt-ampere or *V-I* characteristic of a *pn* junction (also called a *crystal or semiconductor diode*) is the curve between voltage across the junction and the circuit current. Usually, voltage is taken along *x*-axis and current along *y*-axis. Fig. 8.24 shows the \*\*circuit arrangement for determining the *V-I* characteristics of a *pn* junction. The characteristics can be studied under three heads, namely; zero external voltage, forward bias and reverse bias.

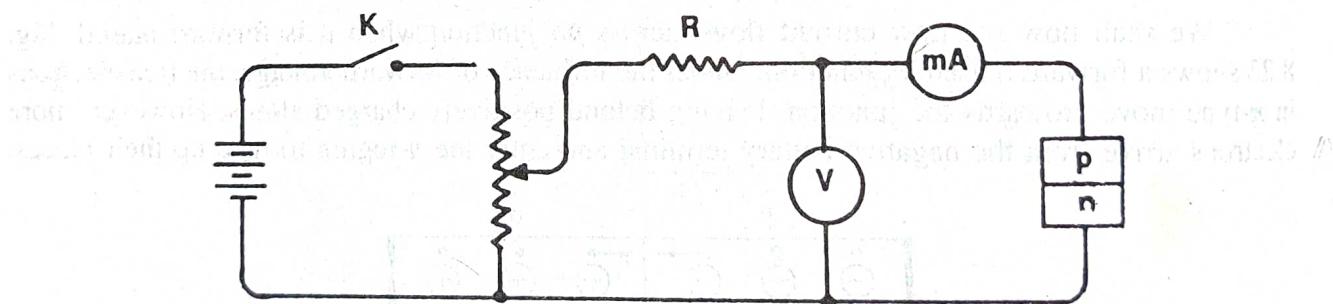


Fig. 8.24

(i) **Zero external voltage.** When the external voltage is zero, i.e. circuit is open at *K*, the potential barrier at the junction does not permit current flow. Therefore, the circuit current is zero as indicated by point *O* in Fig. 8.25.

(ii) **Forward bias.** With forward bias to the *pn* junction i.e. *p*-type connected to positive terminal and *n*-type connected to negative terminal, the potential barrier is reduced. At some forward voltage (0.7V for Si and 0.3V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage. Thus, a rising curve *OB* is obtained with forward bias as shown in Fig. 8.25. From the forward characteristic, it is seen that at first (*region OA*), the current increases very

\* A hole is in the co-valent bond. When a free electron combines with a hole, it becomes a valence electron.

\*\* *R* is the current limiting resistance. It prevents the forward current from exceeding the permitted value.

slowly and the curve is non-linear. It is because the external applied voltage is used up in overcoming the potential barrier. However, once the external voltage exceeds the potential barrier sharply with increase in external voltage (*region AB on the curve*). The curve is almost linear.

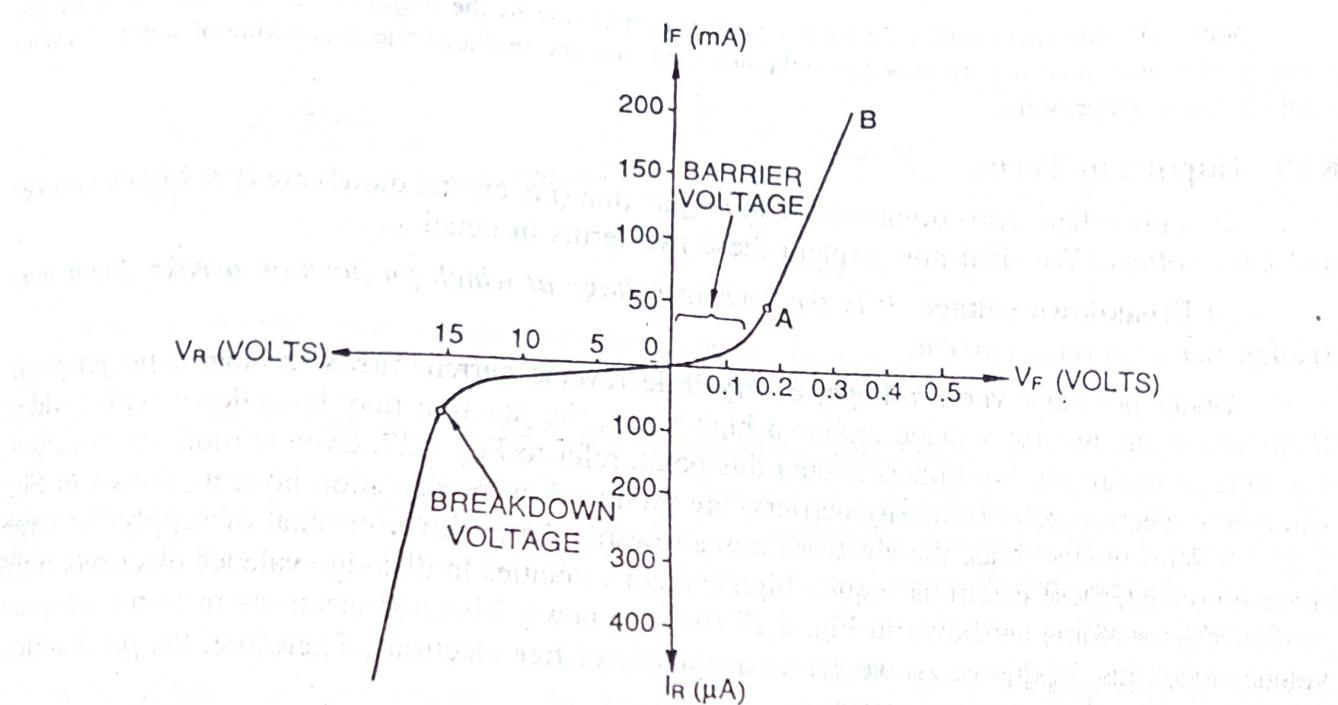


Fig. 8.25

(iii) **Reverse bias.** With reverse bias to the *pn* junction i.e. *p*-type connected to negative terminal and *n*-type connected to positive terminal, potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit. However, in practice, a very small current (of the order of  $\mu\text{A}$ ) flows in the circuit with reverse bias as shown in the reverse characteristic. This is called *reverse saturation current* ( $I_s$ ) and is due to the minority carriers. It may be recalled that there are a few free electrons in *p*-type material and a few holes in *n*-type material. These undesirable free electrons in *p*-type and holes in *n*-type are called *minority carriers*. As shown in Fig. 8.26, to these minority carriers, the applied reverse bias appears as forward bias. Therefore, a small current flows in the reverse direction.

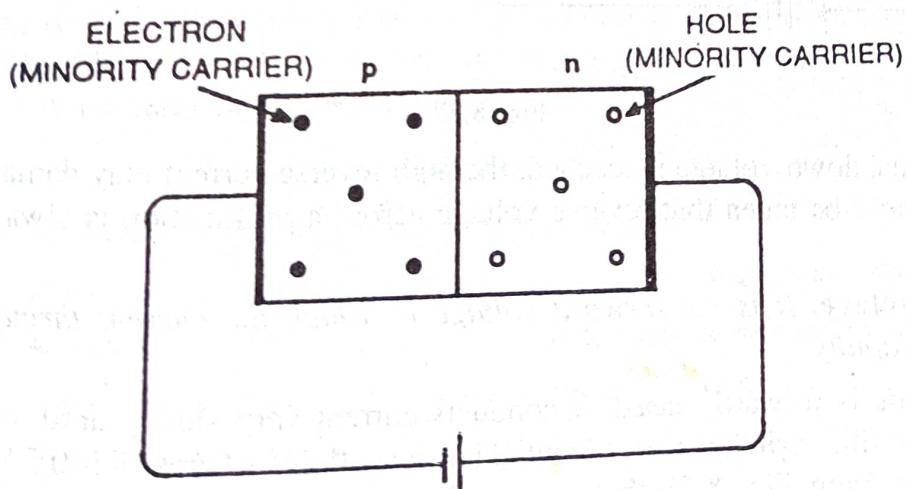


Fig. 8.26

- \* The term saturation comes from the fact that it reaches its maximum level quickly and does not significantly change with the increase in reverse voltage.
- \*\* Reverse current increases with reverse voltage but can generally be regarded as negligible over the working range of voltages.

If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms. At this stage *breakdown* of the junction occurs, characterised by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

**Note.** The forward current through a *pn* junction is due to the *majority carriers* produced by the impurity. However, reverse current is due to the *minority carriers* produced due to breaking of some co-valent bonds at room temperature.

### 8.19 Important Terms

✓ Two important terms often used with *pn* junction (*i.e.* crystal diode) are *breakdown voltage* and *knee voltage*. We shall now explain these two terms in detail.

✓(i) **Breakdown voltage.** *It is the reverse voltage at which *pn* junction breaks down with sudden rise in reverse current.*

Under normal reverse voltage, a very little reverse current flows through a *pn* junction. However, if the reverse voltage attains a high value, the junction may breakdown with sudden rise in reverse current. For understanding this point, refer to Fig. 8.27. Even at room temperature, some hole-electron pairs (minority carriers) are produced in the depletion layer as shown in Fig. 8.27 (i). With reverse bias, the electrons move towards the positive terminal of supply. At large reverse voltage, these electrons acquire high enough velocities to dislodge valence electrons from semiconductor atoms as shown in Fig. 8.27 (ii). The newly liberated electrons in turn free other valence electrons. In this way, we get an *avalanche* of free electrons. Therefore, the *pn* junction conducts a very large reverse current.

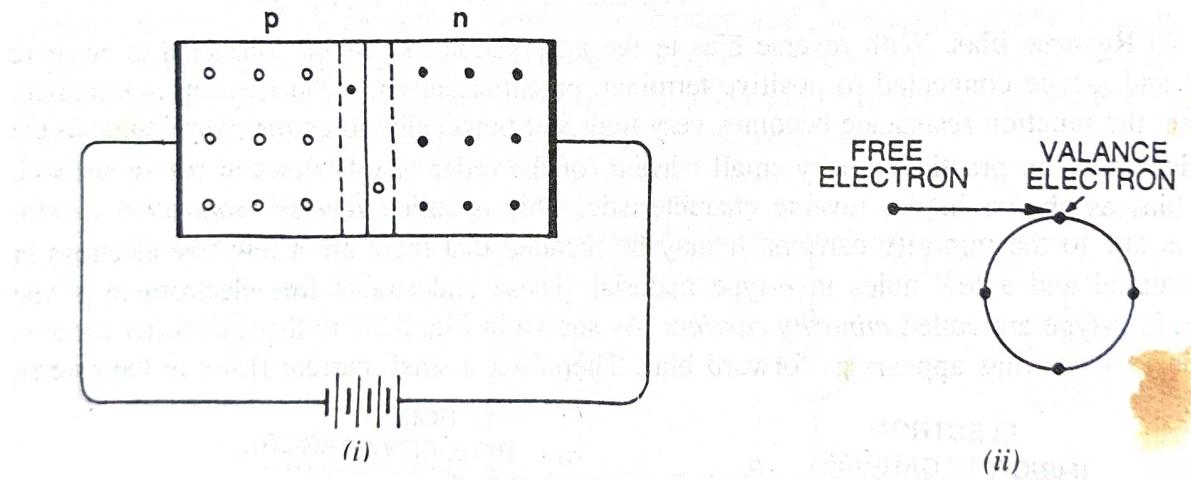


Fig. 8.27

Once the breakdown voltage is reached, the high reverse current may damage the junction. Therefore, care should be taken that reverse voltage across a *pn* function is always less than the breakdown voltage.

✓(ii) **Knee voltage.** *It is the forward voltage at which the current through the junction starts to increase rapidly.*

When a diode is forward biased, it conducts current very slowly until we overcome the potential barrier. For silicon *pn* junction, potential barrier is 0.7 V whereas it is 0.3 V for germanium junction. It is clear from Fig. 8.28 that knee voltage for silicon diode is 0.7V and 0.3V for germanium diode.

Once the applied forward voltage exceeds the knee voltage, the current starts increasing rapidly. It may be added here that in order to get useful current through a *pn* junction, the applied voltage must be more than the knee voltage.

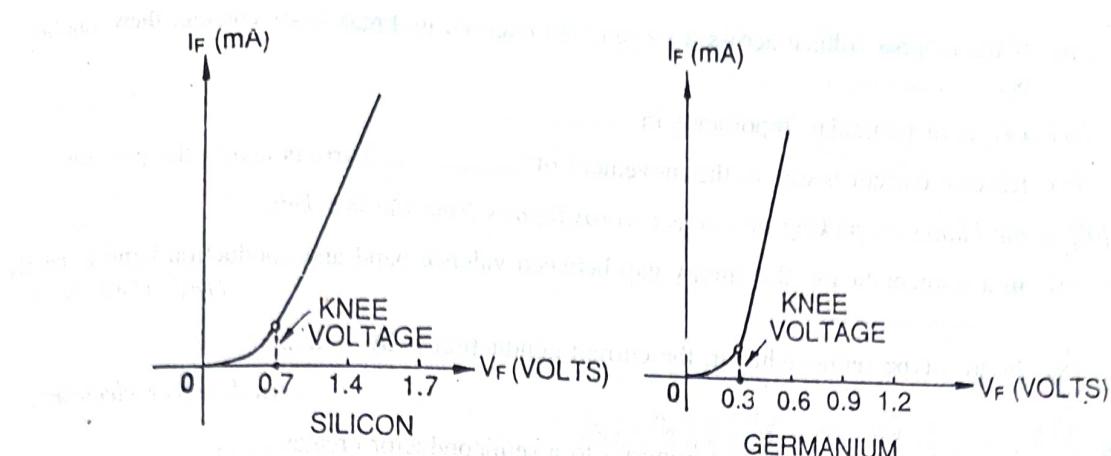


Fig. 8.28

**Note.** The potential barrier voltage is also known as *turn-on voltage*. This is obtained by taking the straight line portion of the forward characteristic and extending it back to the horizontal axis.

### 8.20 Limitations in the Operating Conditions of pn Junction

Every *pn* junction has limiting values of *maximum forward current*, *peak inverse voltage* and *maximum power rating*. The *pn* junction will give satisfactory performance if it is operated within these limiting values. However, if these values are exceeded, the *pn* junction may be destroyed due to excessive heat.

(i) *Maximum forward current*. It is the highest instantaneous forward current that a *pn* junction can conduct without damage to the junction. Manufacturers' data sheet usually specifies this rating. If the forward current in a *pn* junction is more than this rating, the junction will be destroyed due to overheating.

(ii) *Peak inverse voltage (PIV)*. It is the maximum reverse voltage that can be applied to the *pn* junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service. A *pn* junction *i.e.* a crystal diode is used as a rectifier to change alternating current into direct current. In such applications, care should be taken that reverse voltage across the diode during negative half-cycle of a.c. does not exceed the PIV of diode.

(iii) *Maximum power rating*. It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction. This is a very important consideration and is invariably specified by the manufacturer in the data sheet.

#### Self-Test

- Fill in the blanks by inserting appropriate words/figures.

- Resistivity of a semiconductor lies .....conductors and insulators.
- A semiconductor has .....temperature co-efficient of resistance.
- A *p*-type as well as *n*-type semiconductor is electrically .....
- With the addition of pentavalent impurity to a semiconductor, .....semiconductor is obtained.
- If a *pn* junction is forward biased, its resistance is.....
- The knee voltage for silicon *pn* junction is .....
- In *n*-type semiconductor, .....are the minority carriers.