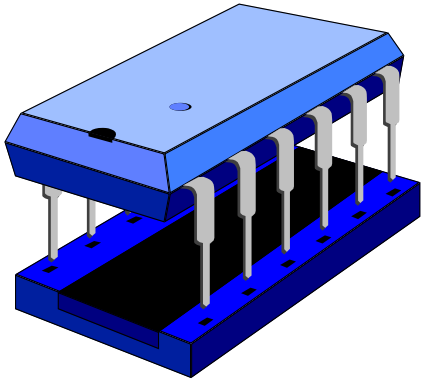

CHIP DESIGN AND USE

Anandha Gopalan (with thanks to **N. Dulay and E. Edwards**)
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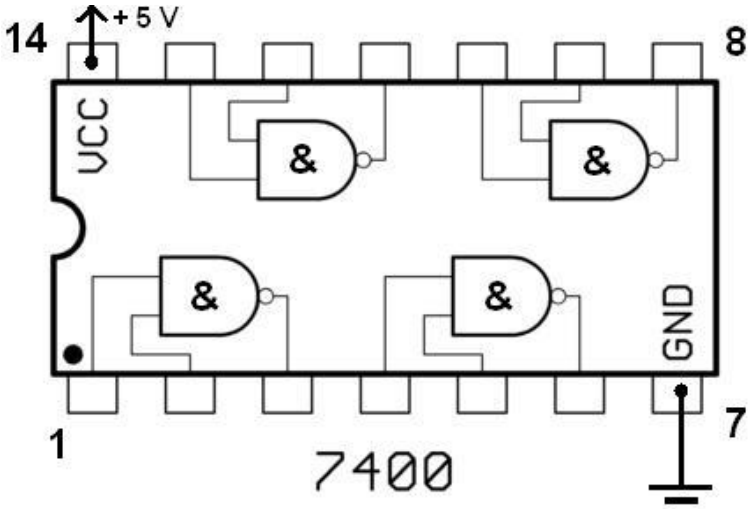
Integrated Circuits

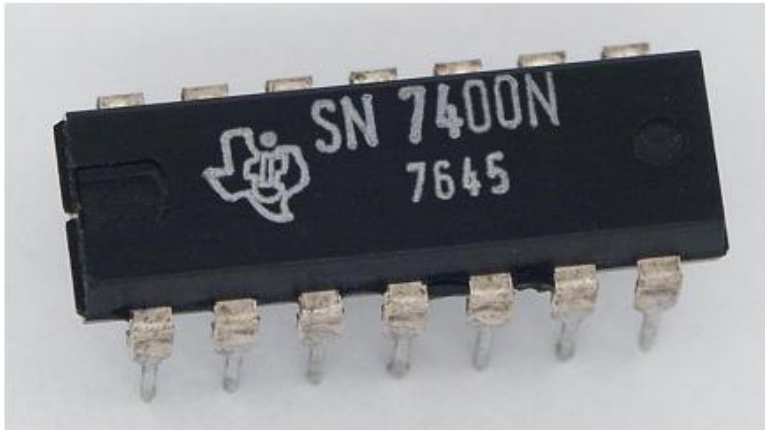
- All ICs (chips) are made up of logic gates
- Are square pieces of silicon onto which logic gates have been deposited
- Generally two rows of pins enable connection onto a larger circuit

IC – Sizes

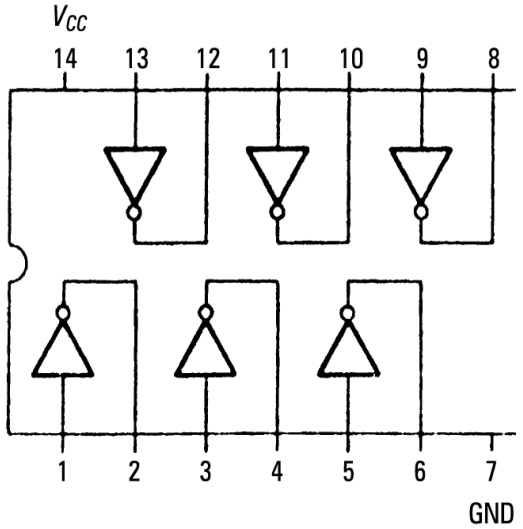
Name	Abbreviation	Number of Gates
Small Scale Integrated	SSI	1-10
Medium Scale Integrated	MSI	10-100
Large Scale Integrated	LSI	100-100,000
Very Large Scale Integrated	VLSI	>100,000

Example SSI Chips





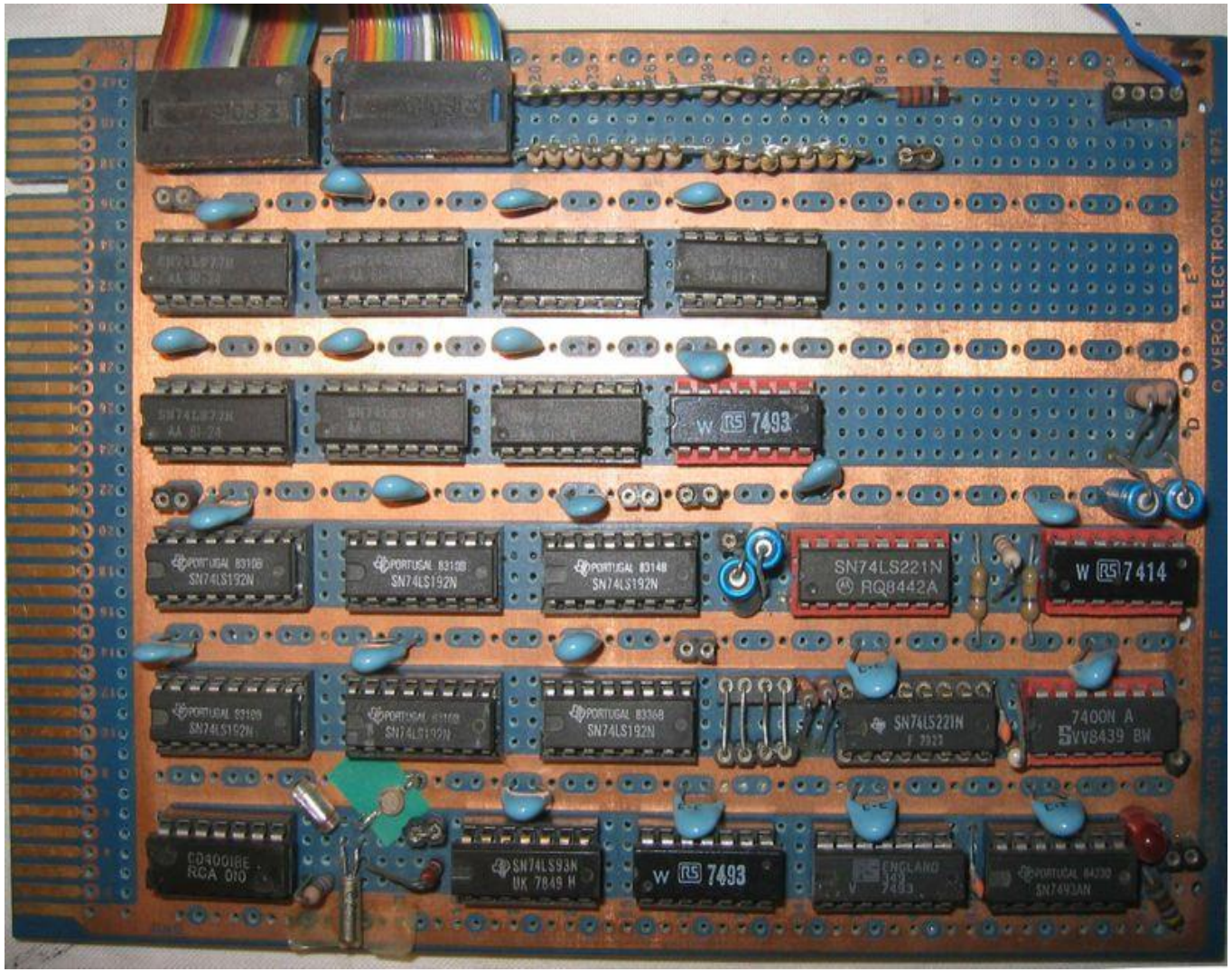
7400 - Nand Gates



7404 – hex inverter

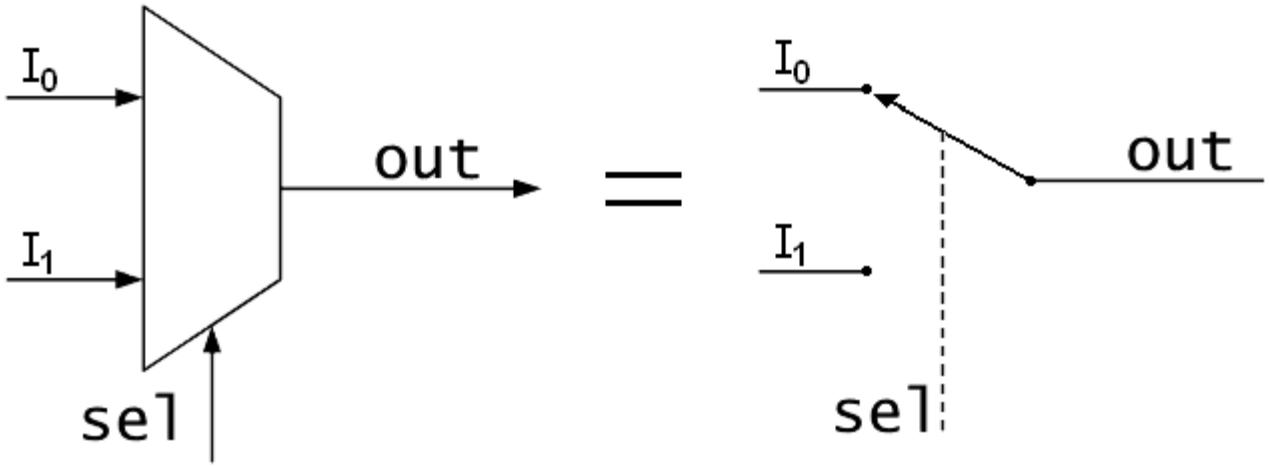
The 7400 TTL series

Example Circuit with SSI/MSI Chips



MSI Chips – Multiplexer

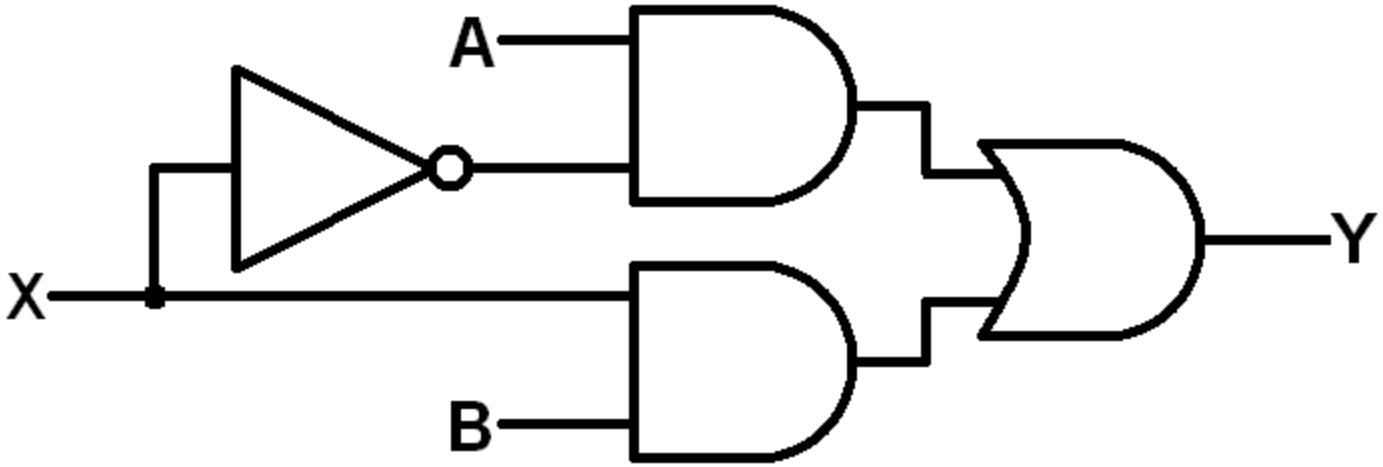
- A multiple-input, single-output switch
- Also called MUX for short ☺



- **sel** selects which of I_0 or I_1 is mapped to the output
- For example, **sel** = 0 selects I_0 and **sel** = 1 selects I_1
- Example is called a 2-to-1 MUX
- With n *selects*/control lines, we can have 2^n input lines

MSI Chips – Multiplexer

- 2-to-1 Multiplexer



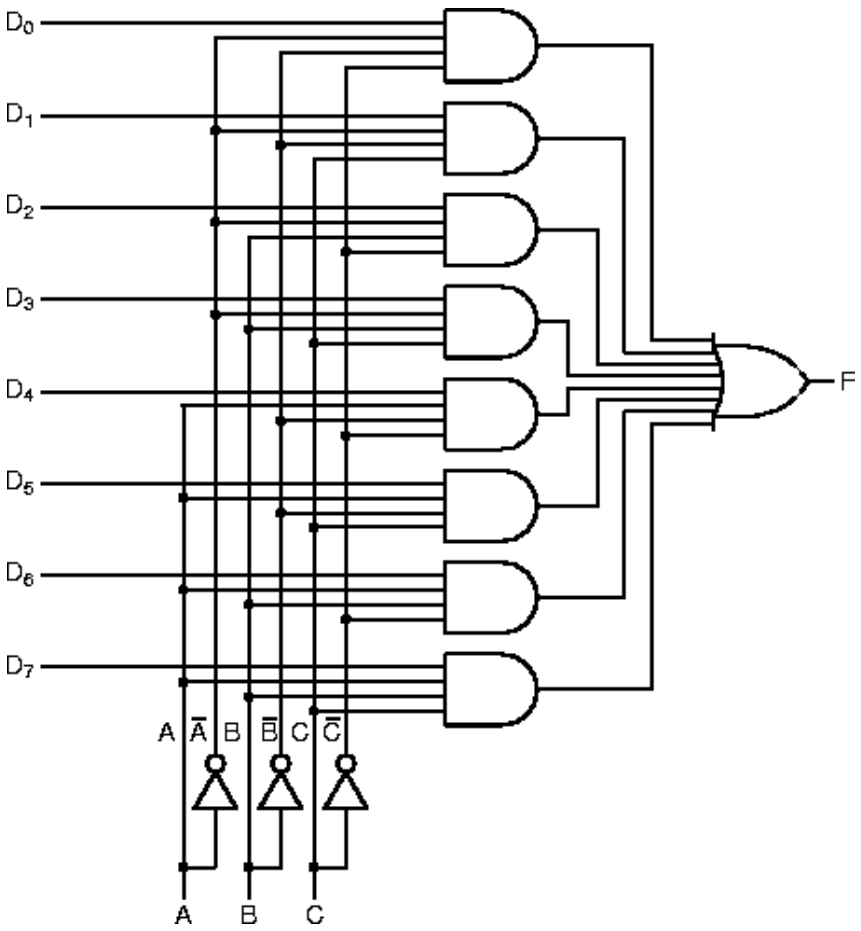
Source: http://www.sparkfun.com/tutorials/371

MSI Chips – Multiplexer

- Truth Table

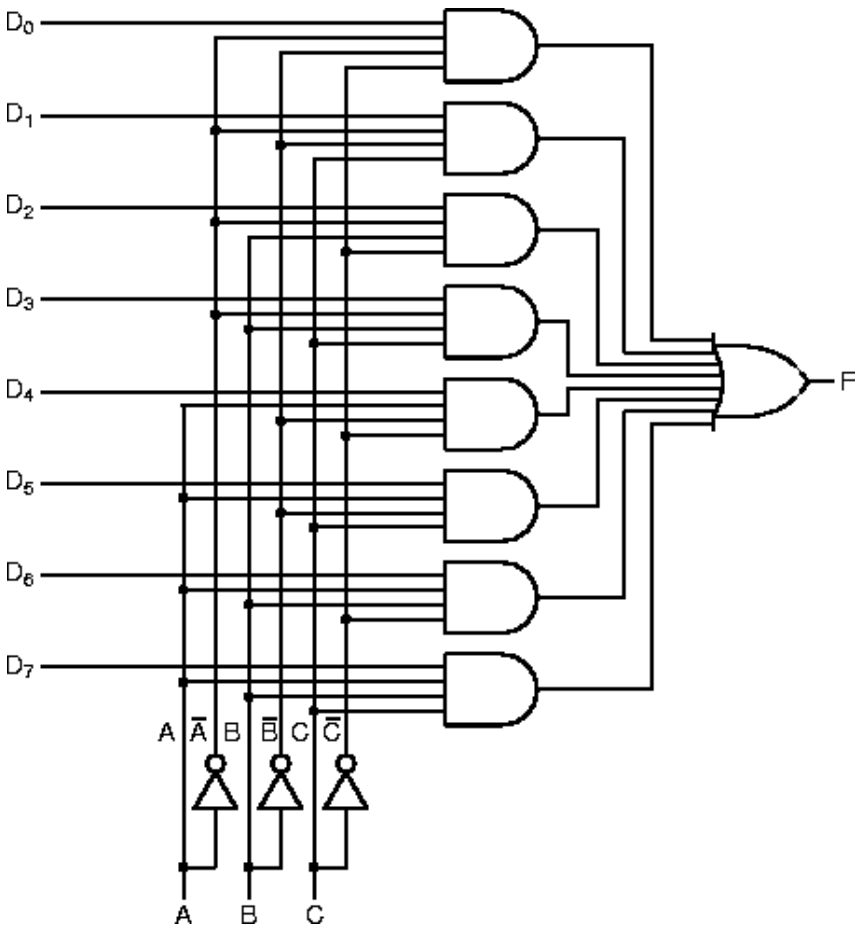
A	B	X	A • X'	B • X	Y
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	1	1
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	1	0	1
1	1	1	0	1	1

MSI Chips – Multiplexer



- The 3 inputs **A**, **B**, **C** select which of the input lines (D_0-D_7) is copied through to the output **F**
- In general, a multiplexer has 2^n inputs and n control lines and one output

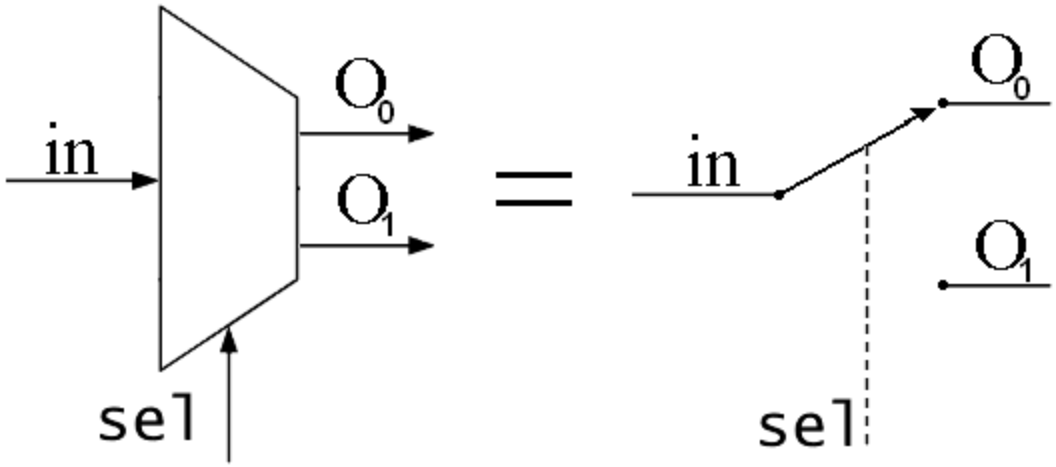
MSI Chips – Multiplexer



- Fits nicely into a 14-pin package (with ground and +5V)

MSI Chips – Demultiplexer

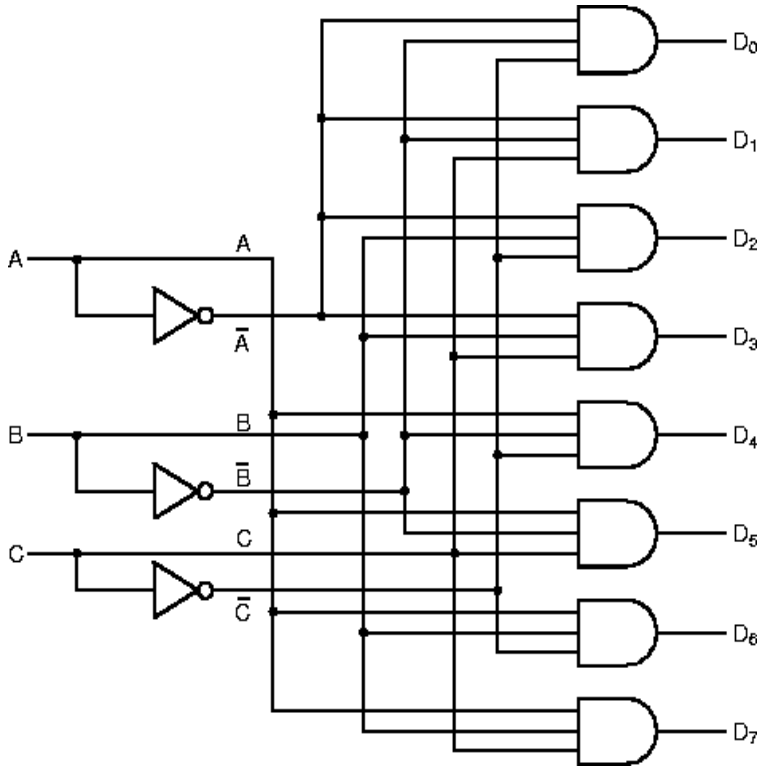
- A single-input, multiple-output switch
  - Opposite of a MUX
- Also called DEMUX ☺
- Usually used in conjunction with a MUX



MSI Chips – Decoder

- A multiple-input, multiple-output logic circuit
  - Converts coded inputs into coded outputs
  - Binary Decoder has n inputs and 2^n outputs
  - Necessary in applications such as data multiplexing and memory address decoding

MSI Chips – Decoder



- Only one output is 1 – the one selected by the n-bit binary input number – the rest are zero
- Useful in transmitting line selection with fewer wires (e.g. selecting a memory chip)

MSI Chips – Decoder

- Truth Table

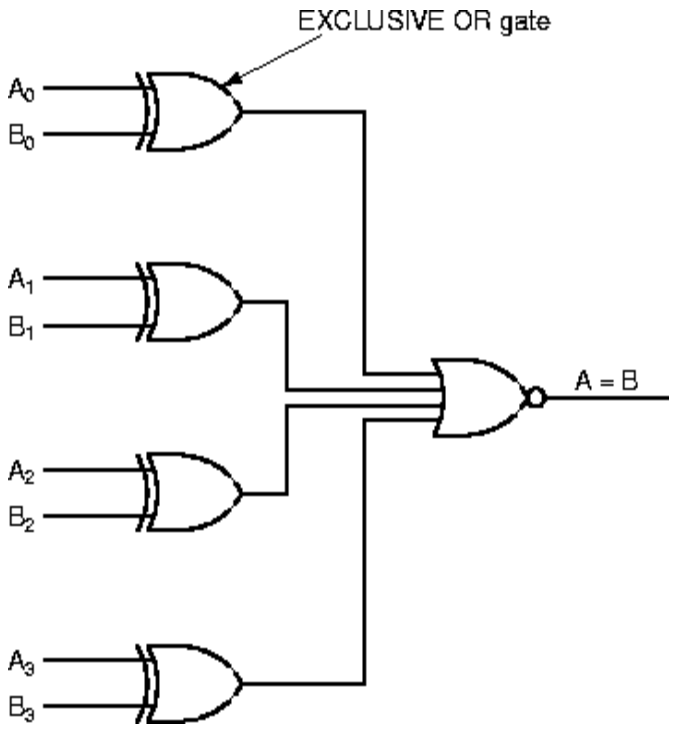
A	B	C	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

MSI Chips – Calculations – Comparator

- To compare two numbers
- Example: 1-bit comparison
  - Which gate to use?
  - Recall:

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

MSI Chips – Calculations – Comparator



- The comparator returns 1 if the two n-bit inputs A and B are equal, 0 otherwise

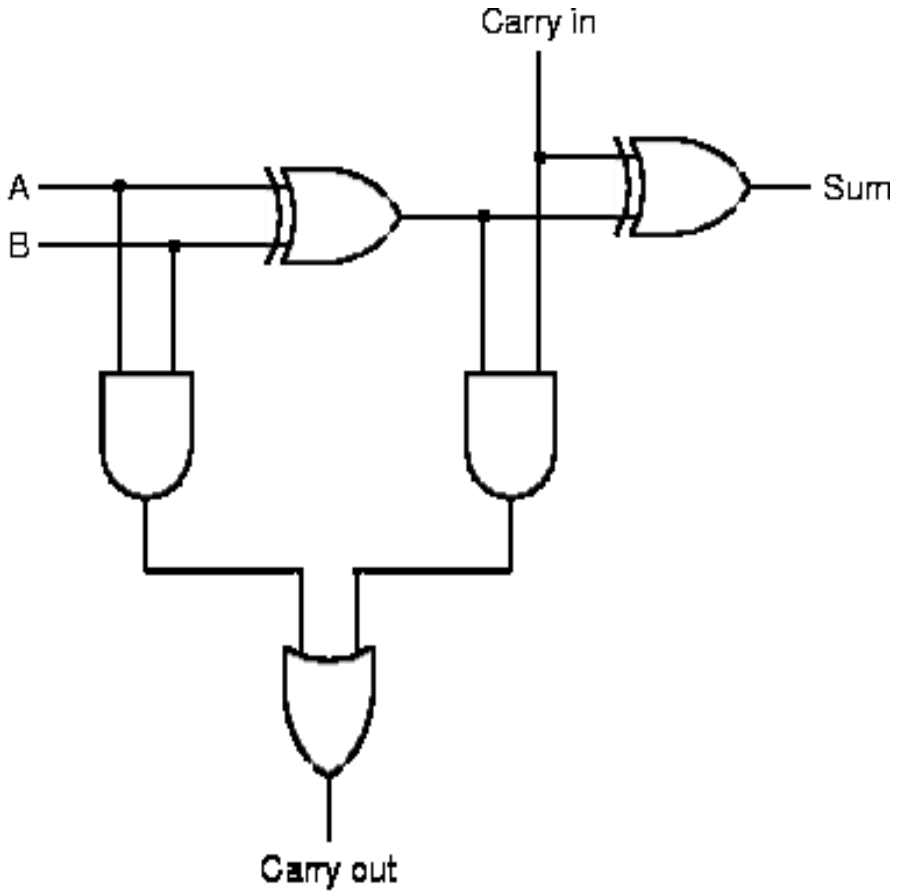
The Arithmetic Logic Unit (ALU)

- Digital circuit that performs arithmetic and logical operations
- Fundamental building block of the central processing unit (CPU) of a computer
  - Even the simplest microprocessors contain one for purposes such as maintaining timers
  - Processors found inside modern CPUs and graphics processing units (GPUs) accommodate very powerful and very complex ALUs
- Concept proposed in 1945 by Mathematician John von Neumann
- Research into ALUs remains an important part of computer science

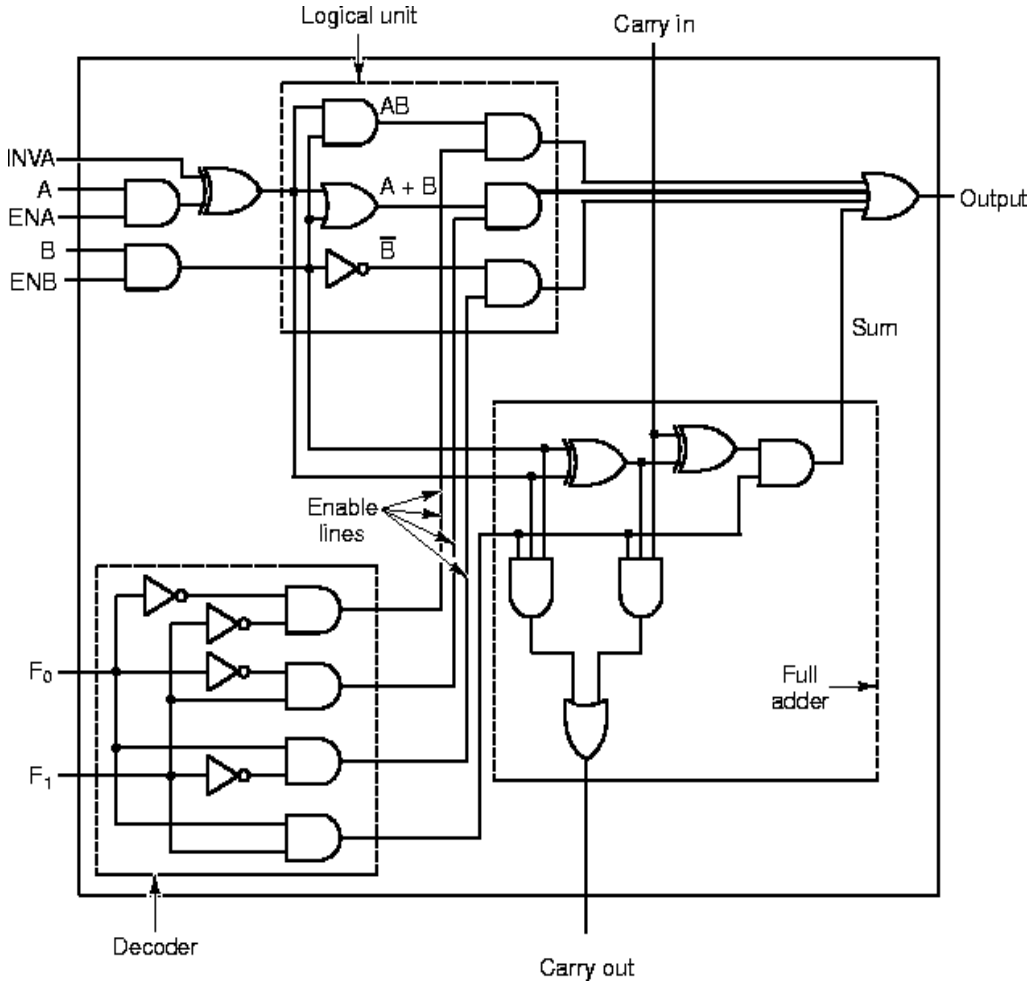
ALU

- Recall: Full Adder

A	B	Carry In	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



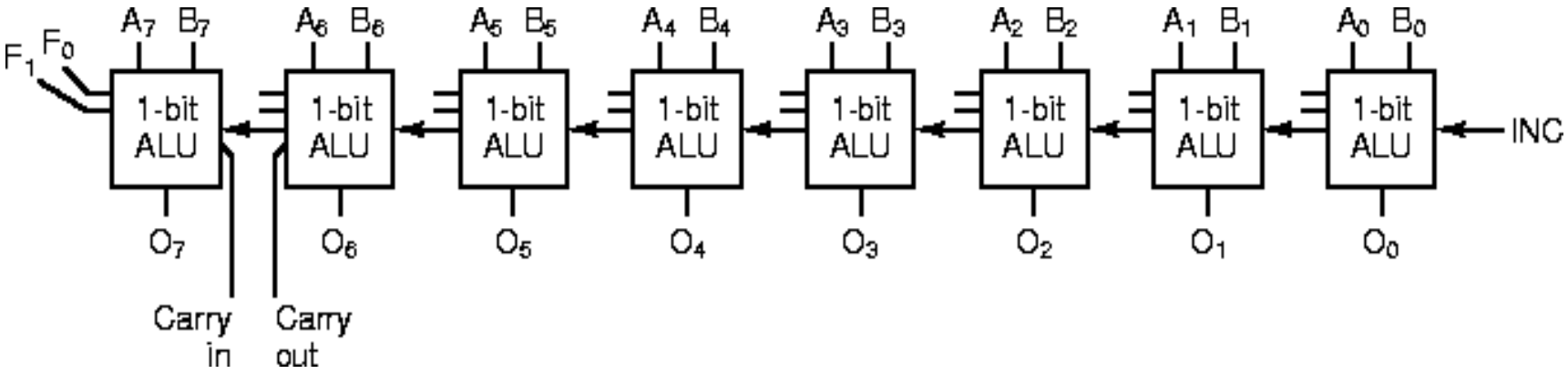
The Arithmetic Logic Unit (ALU)



- The ALU is able to perform multiple functions
- Depending on the input to the decoder (F_0,F_1) one of four functions is selected – A and B, A or B, not B, arithmetic A+B

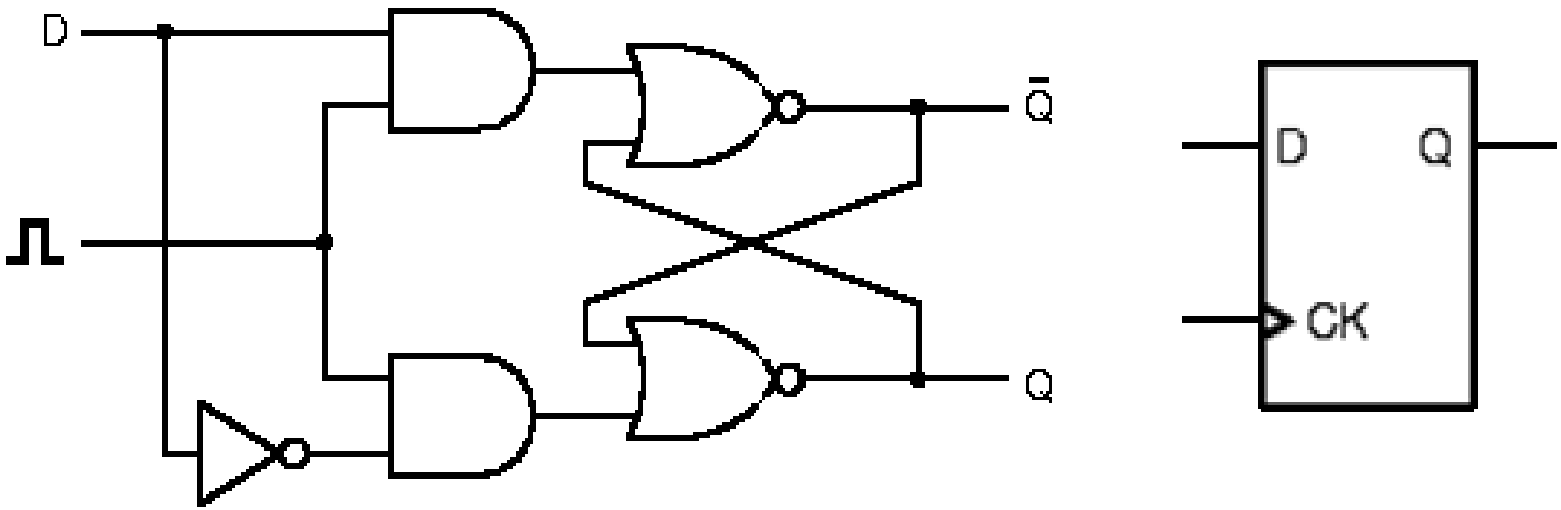
8-bit ALU

- Can link together 1-bit ALUs to form a multi-bit ALU
  - Sometimes known as bit-slice circuits

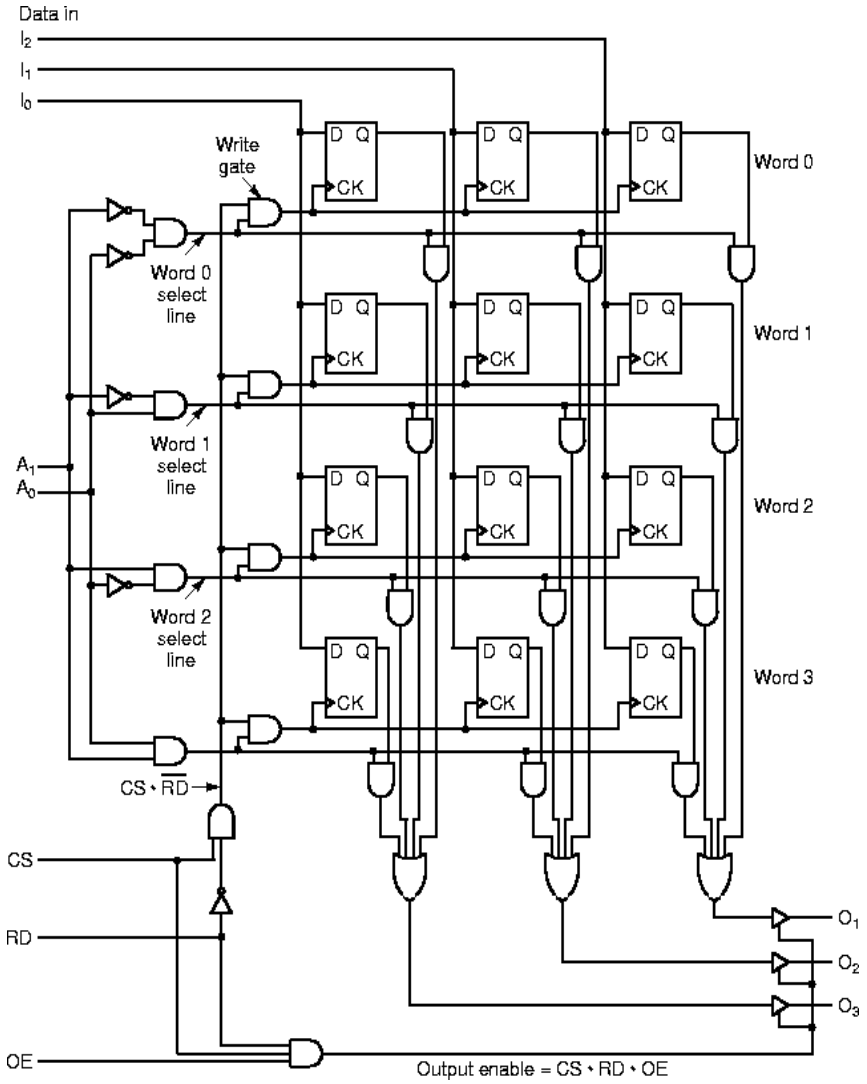


Memory

- Useful variation on the SR latch circuit is the Data latch, or D latch
- Constructed by using the inverted S input as the R input signal
  - Allows for a single input → No race condition as input is inverted

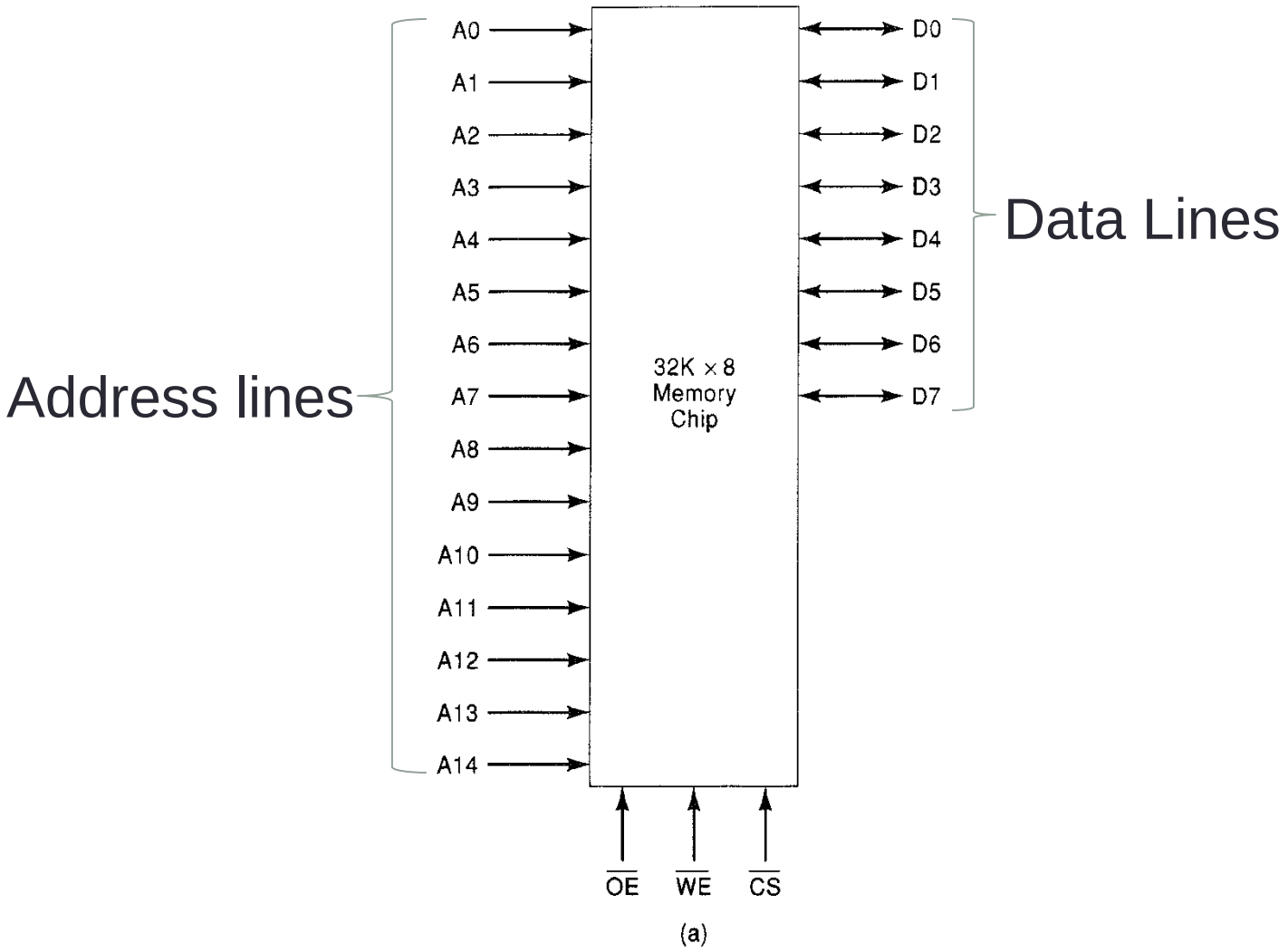


Memory Chips



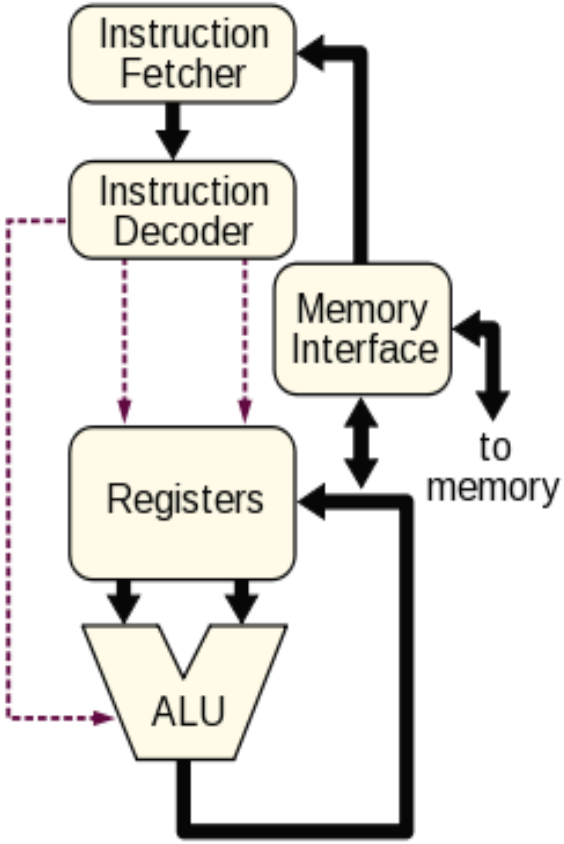
- The memory chip shown here comprises 12 D-latches in a 4x3 configuration
- The 3 bit data will be read or written to one of the four words selected by the input lines A_0/A_1
- A_0/A_1 are the address lines and I_n/O_n are the input/output data lines
- In fact, input and output are never used at the same time
  - Chips use the same pins for input and output

Memory Chips – Potential Layout



CPU Design – VLSI

- Contains millions of gates – same structure as below



CPU Design – VLSI