Analog front-end design

HIGH-FREQUENCY ANALOG CIRCUITS

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Contents

1. Introduction

This project's goal is to design an analog front-end for a sensor composed of a 3rd order low-pass filter and a programmable gain amplifier. Initial design will be done in LtSpice and later implemented on a breadboard and analyzed using Analog Devices' Adalm2000.

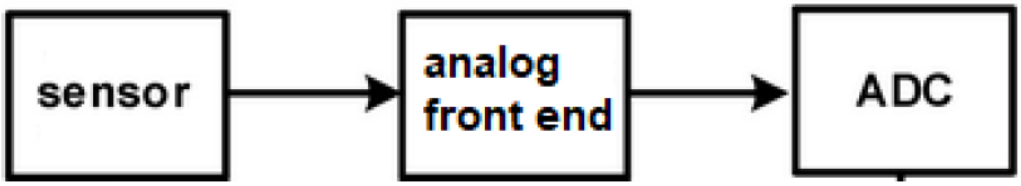


Figure 1: Block diagram of a data acquisition system

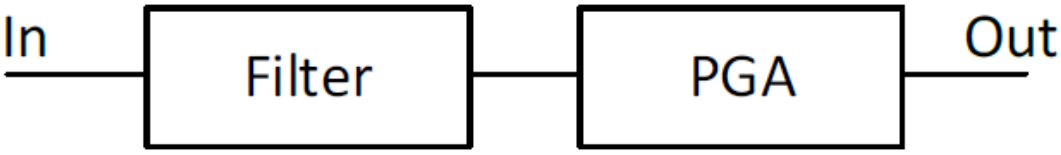


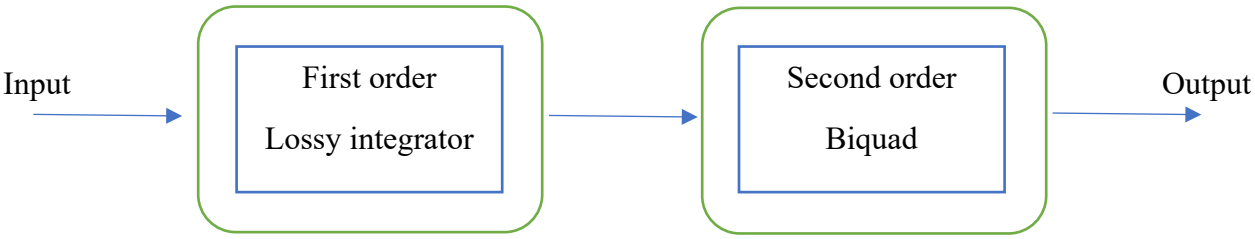
Figure 2: Block diagram of the analog front-end

1.1. Requirements

LPF	Implementation	OA-RC
	Biquad topology	SallenKey
	Filter order	3
	Pass-band gain	1[V/V]
	Bandwidth	6.7kHz
	Approximation type	Butterworth
	Input resistance	>1kΩ
PGA	Active cell	OpAmp
	Implementation	Parallel, switches in signal's path
	Gain domain	0dB ÷ 18dB
	Resolution	6dB
	Input resistance	>1kΩ
	Bandwidth	> 6.7kHz
OA	GBW	>20*6.7kHz
	Phase-margin	>60°
	Open-loop gain	>60dB

2. Filter Design

Filters of higher orders are usually built by cascading blocks of biquads and integrators in order to reduce the complexity of the mathematical calculations and to enhance the simplicity of the design process. Therefore, a 3rd order low-pass filter can be implemented using the structure presented in the figure below:



$$H(s) = H_0 \cdot \frac{c_1}{s + c_1} \cdot \frac{d_2}{s^2 + c_2 s + d_2}$$

TABLE 12.1 Butterworth Normalized and Factored Polynomials

n	Butterworth Polynomials
1	$s + 1$
2	$s^2 + 1.41421s + 1$
3	$(s + 1)(s^2 + s + 1)$
4	$(s^2 + 0.76537s + 1)(s^2 + 1.84776s + 1)$

Figure 3: Butterworth approximation coefficients

c1	c2	d2
1	1	1

These are the normalized values of the filter as given in the Excel spreadsheet “Analog filter design”. This will then be used to compute the denormalized values as well.

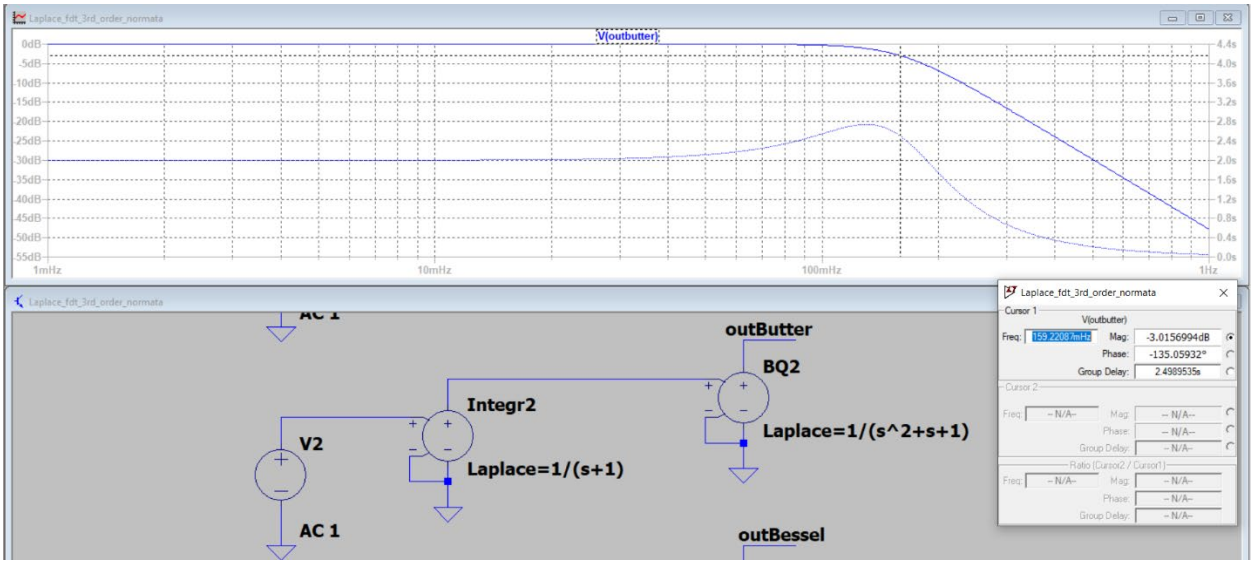


Figure 4: Frequency characteristic of normalized transfer function (wc = 1 rad/sec)

$$H(s) = H_0 \cdot \frac{c_{1d}}{s + c_{1d}} \cdot \frac{d_{2d}}{s^2 + c_{2d}s + d_{2d}}$$

$$f_c = 6.7kHz \Rightarrow w_c = 2*\pi*f_c = 42.1\text{k rad/sec}$$

c1d	c2d	d2d
4.21E+04	4.21E+04	1.77E+09

2.1. Lossy integrator

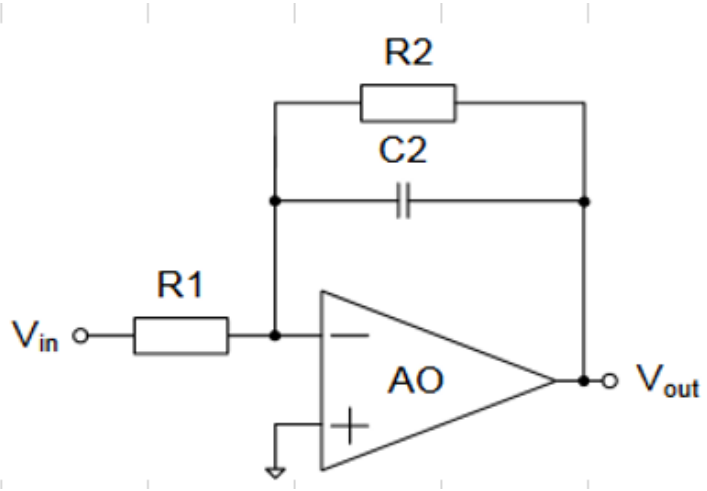


Figure 5:Lossy integrator - OA-RC implementation

2.1.1. Sizing strategy

$$H_{\text{Cu pierderi}}(s) = \frac{\frac{R_2}{R_1}}{1 + sR_2C_2}\ ;\ H(s) = H_0 \cdot \frac{\omega_0}{s + \omega_0}.$$

$$H_0 = \frac{R_2}{R_1}; \omega_0 = \frac{1}{R_2C_2}.$$

$R_{in} = R_1 > 1\text{k}\Omega$ => choose $R_1 = 1.5\text{k}\Omega$

$$R_2 = R_1 = 1.5\text{k}\Omega$$

$$C_2 = 15.8\text{nF} \approx 15\text{nF}$$

2.1.2. LtSpice Simulation

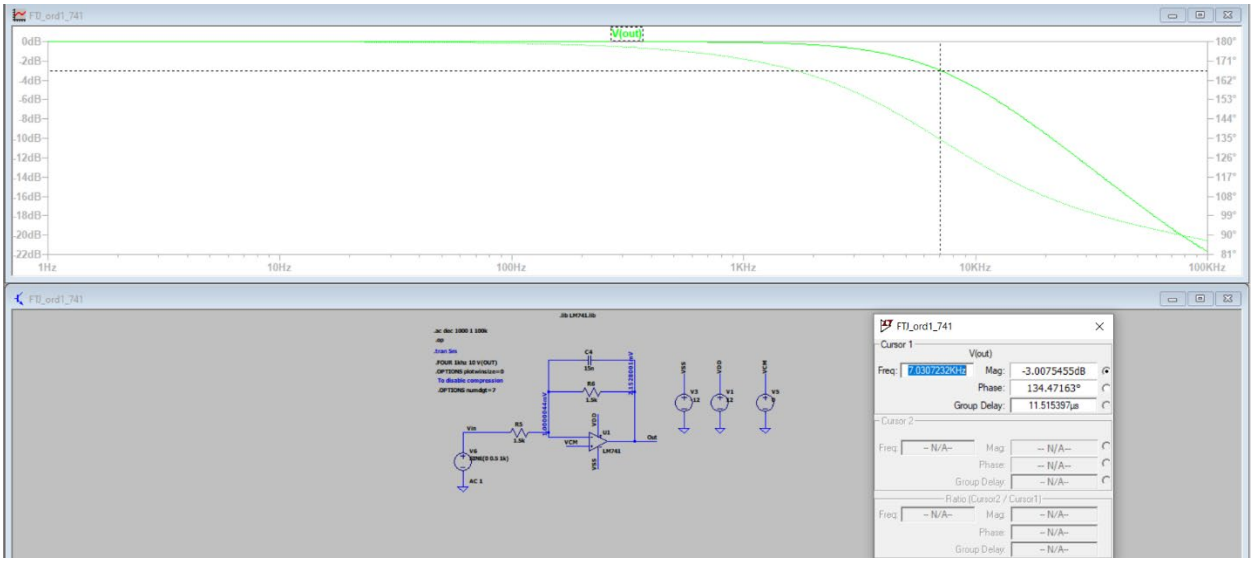


Figure 6: Frequency characteristic of denormalized transfer function

Because of the rounded value of the capacitor to a real-world value the bandwidth is a little higher than 6.7kHz, namely 7kHz.

2.2. SallenKey Biquad

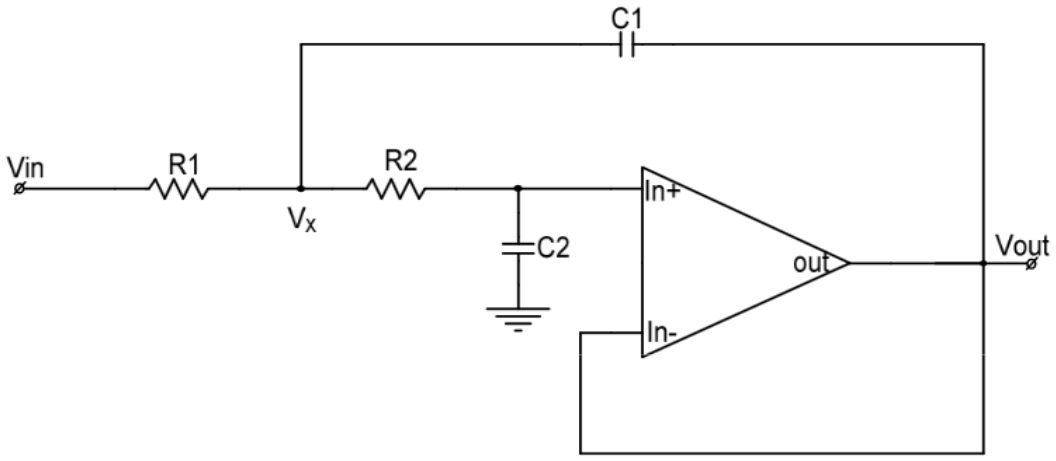


Figure 7: SallenKey biquad - OA-RC implementation

2.2.1. Sizing strategy

$$H(s)=\frac{V_{out}}{V_{in}}=\frac{\frac{1}{R_1R_2C_1C_2}}{s^2+\frac{1}{C_1}\left(\frac{1}{R_1}+\frac{1}{R_2}\right)s+\frac{1}{R_1R_2C_1C_2}};H_0=1;\omega_c=\frac{1}{\sqrt{R_1R_2C_1C_2}};Q=\frac{\sqrt{R_1R_2}}{R_1+R_2}\sqrt{\frac{C_1}{C_2}}$$

choose $R_1 = R_2 = 10\text{k}\Omega$

$$C_1=\frac{2Q}{\omega_0 R};C_2=\frac{C_1}{4Q^2}=\frac{1}{2Q\omega_0 R}$$

$C_1 = 4.75\text{nF} \approx 2\ 10\text{nF in series}$

$C_2 = 1.19\text{nF} \approx 1\text{nF}$

2.2.2. LTSpice Simulation

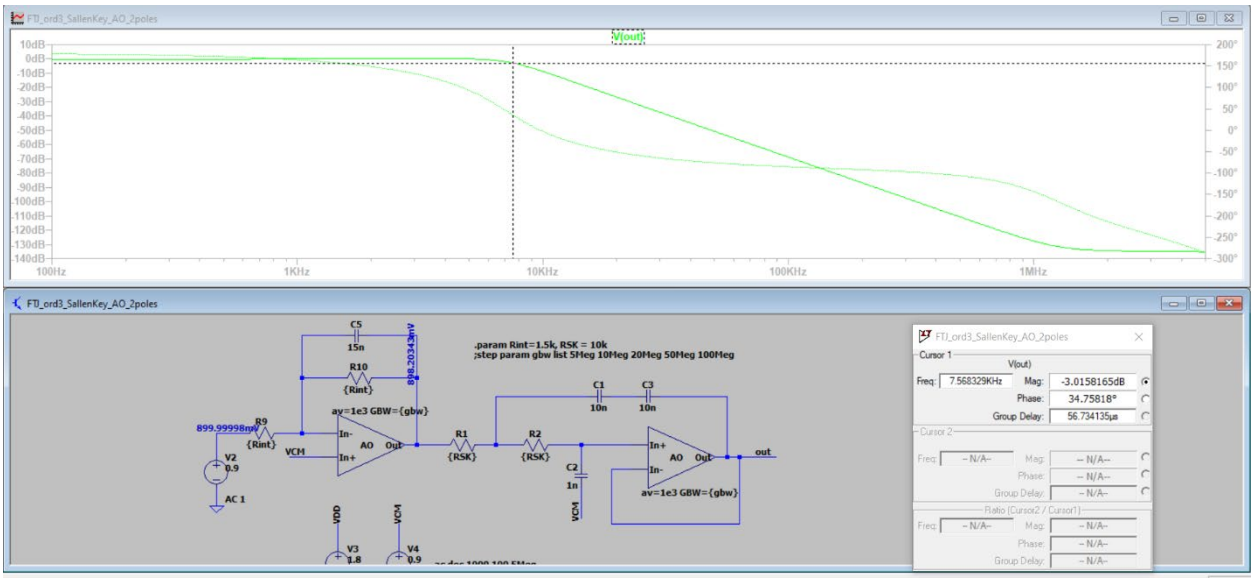


Figure 8: Frequency characteristic of denormalized transfer function

This simulation shows that a circuit with the above computed values for the passive components results in a bandwidth of 7.56kHz, which is close to the target value of 6.7kHz.

3. PGA Design

The next stage of the analog front-end consists of a programmable gain amplifier with an input resistance higher than 1kΩ, a bandwidth higher than 6.7kHz and voltage gain steps of 0, 6, 12 and 18dB. The required architecture is parallel feedback resistors with the switches in the signal's path presented in the figure below:

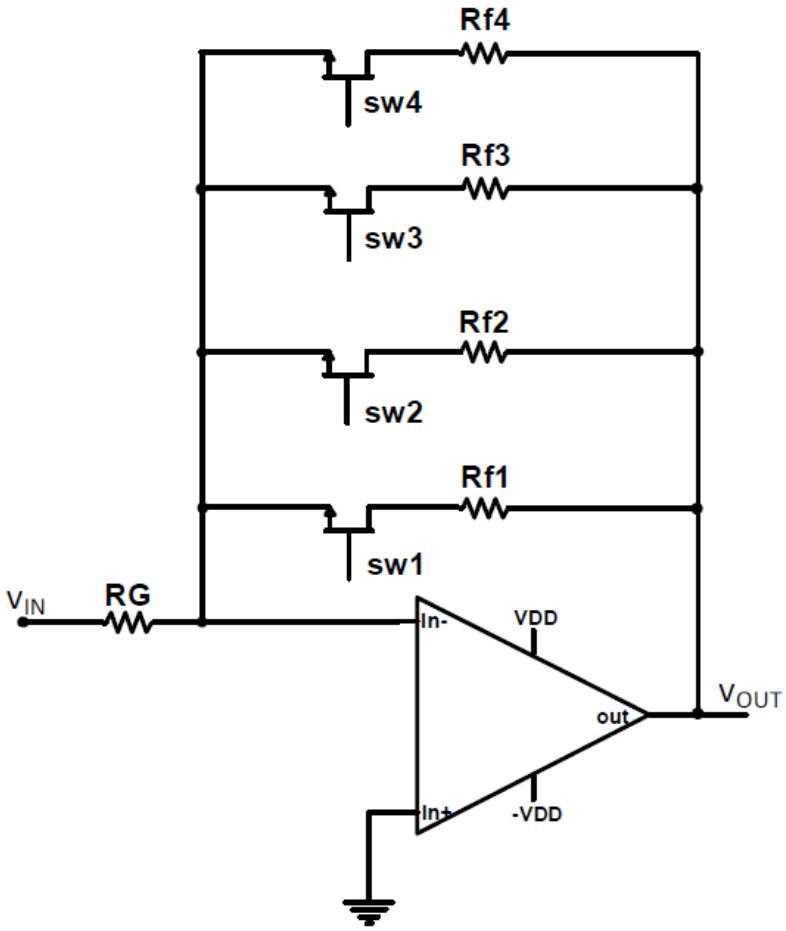


Figure 9: PGA architecture

3.1. Sizing strategy

First step is to convert to linear scale:

$$|A_V| = \{0dB, 6dB, 12dB, 18dB\} = \left\{1\frac{V}{V}, 2\frac{V}{V}, 4\frac{V}{V}, 8\frac{V}{V}\right\}$$

$$|A_V| = \frac{R_{f\_echivalent}}{R_g} \Rightarrow \begin{cases} R_{f4} = 8 \cdot R_G \\ R_{f3} = 4 \cdot R_G \\ R_{f2} = 2 \cdot R_G \\ R_{f1} = R_G \end{cases}$$

$R_{IN} = R_G \geq 1k\Omega$ => choose $R_G = 1k\Omega$

=> $R_{f1} = 1k\Omega$; $R_{f2} = 2k\Omega$; $R_{f3} = 4k\Omega$; $R_{f4} = 8k\Omega$

Since these are not all standard resistor values some of them will be formed from series and parallel connections of multiple resistors that are available.

R_{f2} <= 1kΩ in series with 1kΩ = 2kΩ

R_{f3} <= 1.5kΩ in series with 2.2kΩ = 3.7kΩ ≈ 4kΩ

R_{f4} <= 10kΩ in parallel with 39kΩ = 7.95kΩ ≈ 8kΩ

We need to make sure the bandwidth of the PGA is wider than the one of the filter from the previous stage so we will calculate it in the worst case scenario, i.e. when the gain is the highest. If the active cell of the PGA is the LM741 with a GBW of 1.5MHz we get the following value:

$$BW_{PGA\_min} = \frac{GBW}{1+|A_{vmax}|} = \frac{1.5M}{1+8} = 166.66kHz > 6.7kHz$$

3.2. Switches

Instead of using transistors to control the gain of the amplifier we will use a CD4051BE 8-Channel Analog Multiplexer with the following pinout:

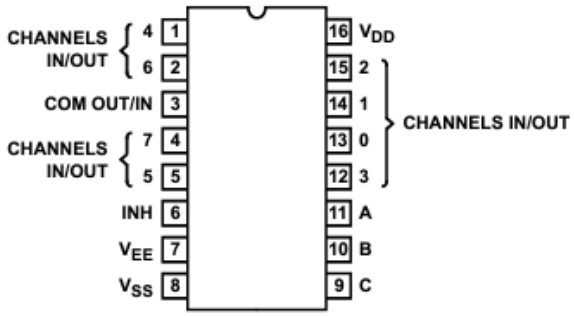


Figure 10: CD4051B 3:8 MUX

4. Final Circuit

Since we only need to control 4 branches we only need channels 0-3, together with A and B inputs for addressing, controlled by 2 switches provided by the HelpKit . The final schematic is represented in the figure below, composed of a TL082 with 2 OpAmps, LM741, CD4051BE and all the passive components we sized above.

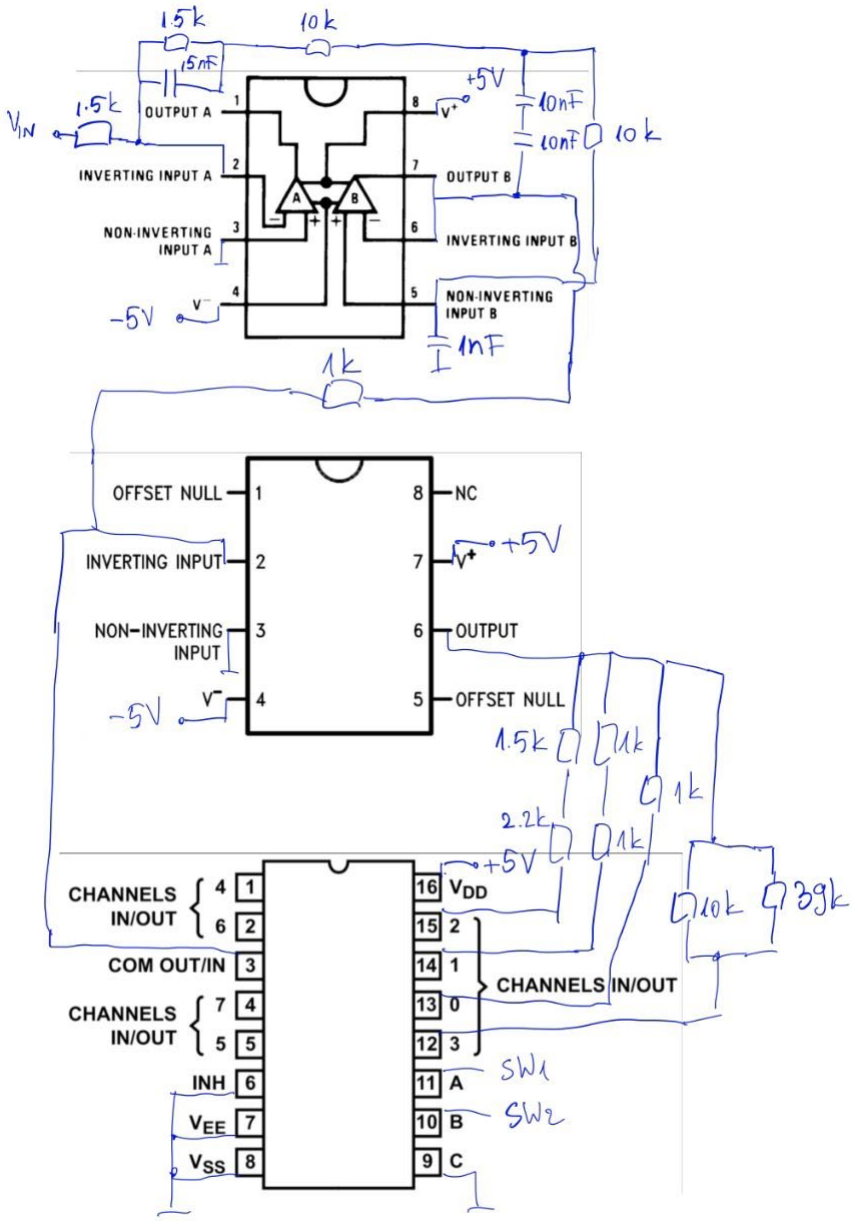


Figure 11: Final Circuit Schematic

5. Circuit Analysis

After wiring all the components on a breadboard according to Figure 11., we can test the behavior of the analog front-end using Scopy via the ADALM2000 device with the following pinout:

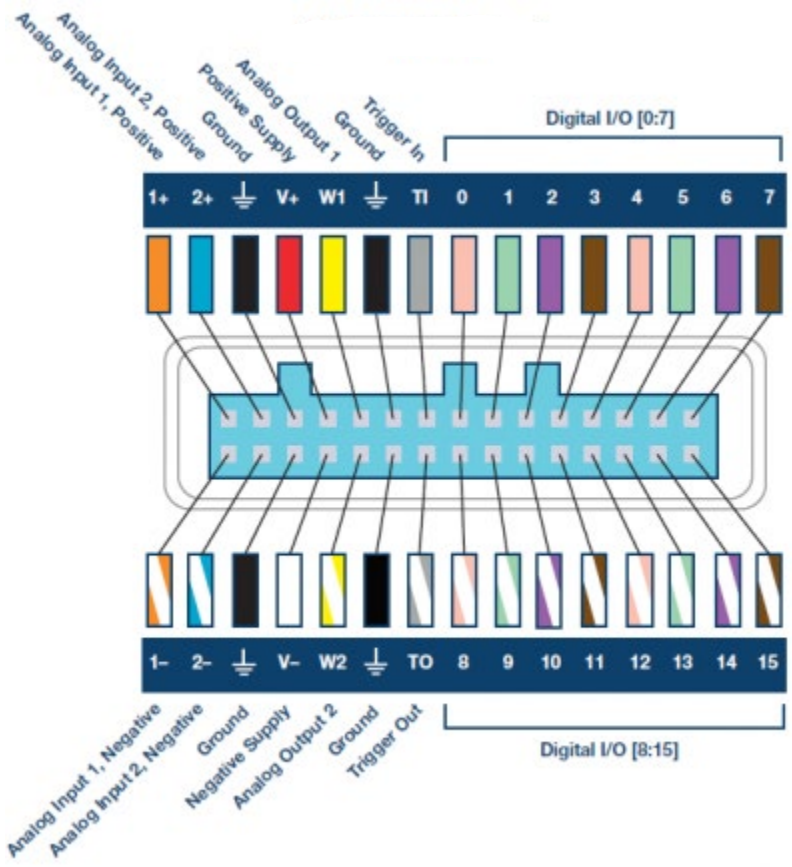


Figure 12: ADALM2000 pinout

We will connect analog input 1+ and analog output W1 to the input of the filter in order to generate the input signal and visualize it in Scopy, analog input 2+ and analog output W2 to the output of the PGA, positive and negative supply V+ and V- to the +5V and -5V power line respectively, and ground and 1-, 2- to the ground line on the breadboard.

We will use the Network Analyzer function to characterize our circuit for each combination of the 2 switches and measure the errors created by the non-idealities of the components and the rounding of the values compared to the target values of 0, 6, 12 and 18dB with a 6.7kHz bandwidth.

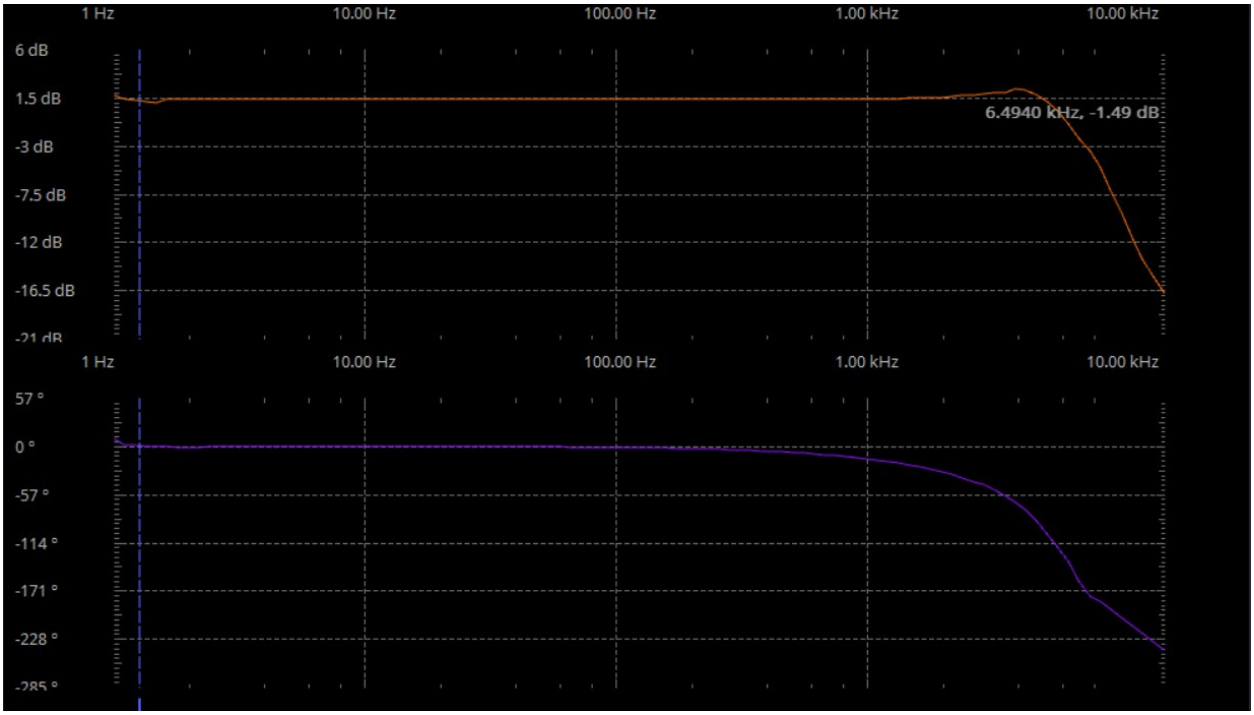


Figure 13: 0dB Bode plots

We can see here that the low frequency gain is 1.5dB instead of 0dB, with a cutoff frequency of 6.5kHz.

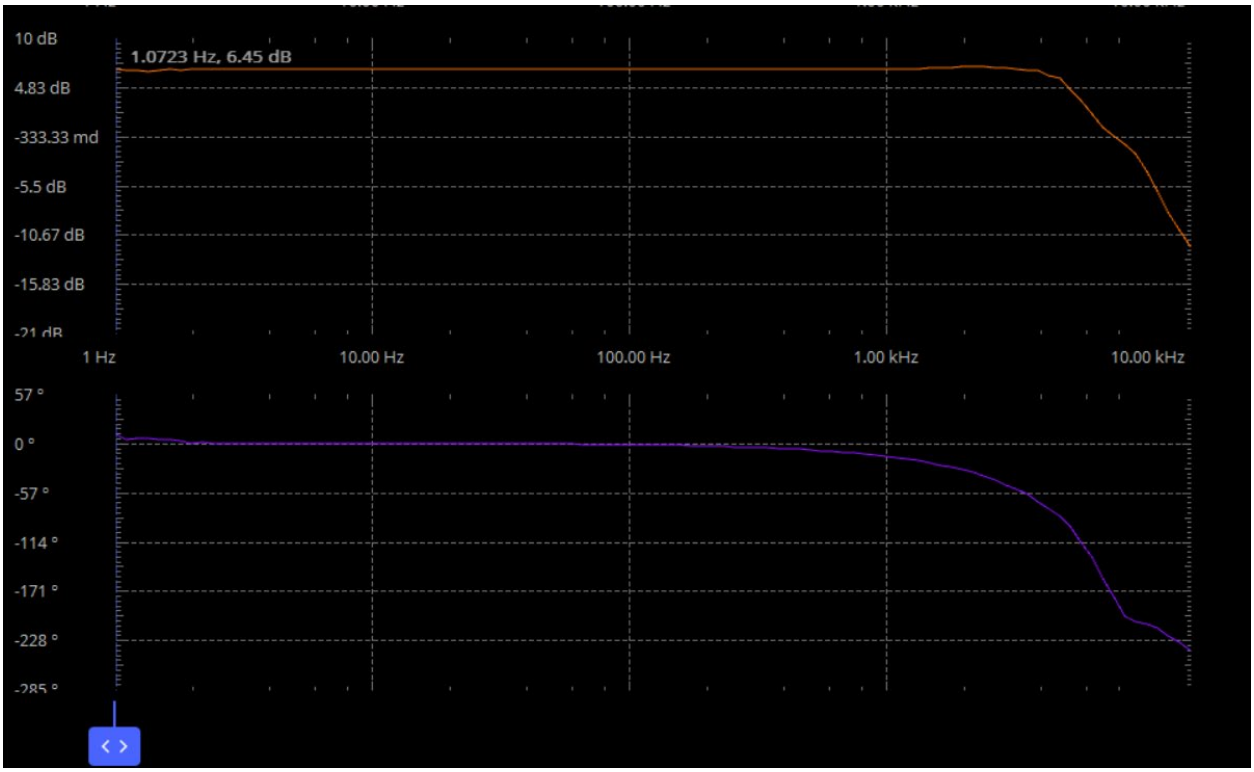


Figure 14: 6dB Bode plots

We get here 6.5dB instead of 6dB with a bandwidth of 6kHz.

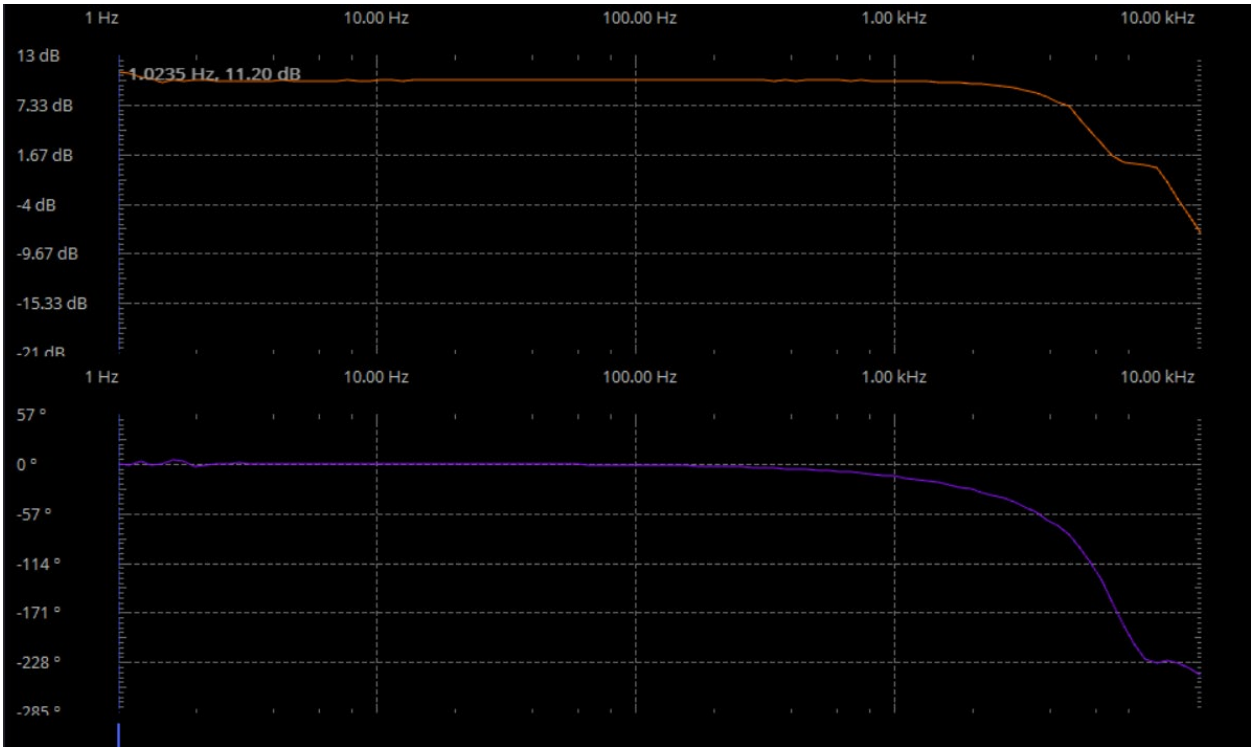


Figure 15: 12dB Bode plots

The third combination of the switches results in 11.2dB and 5.3kHz.

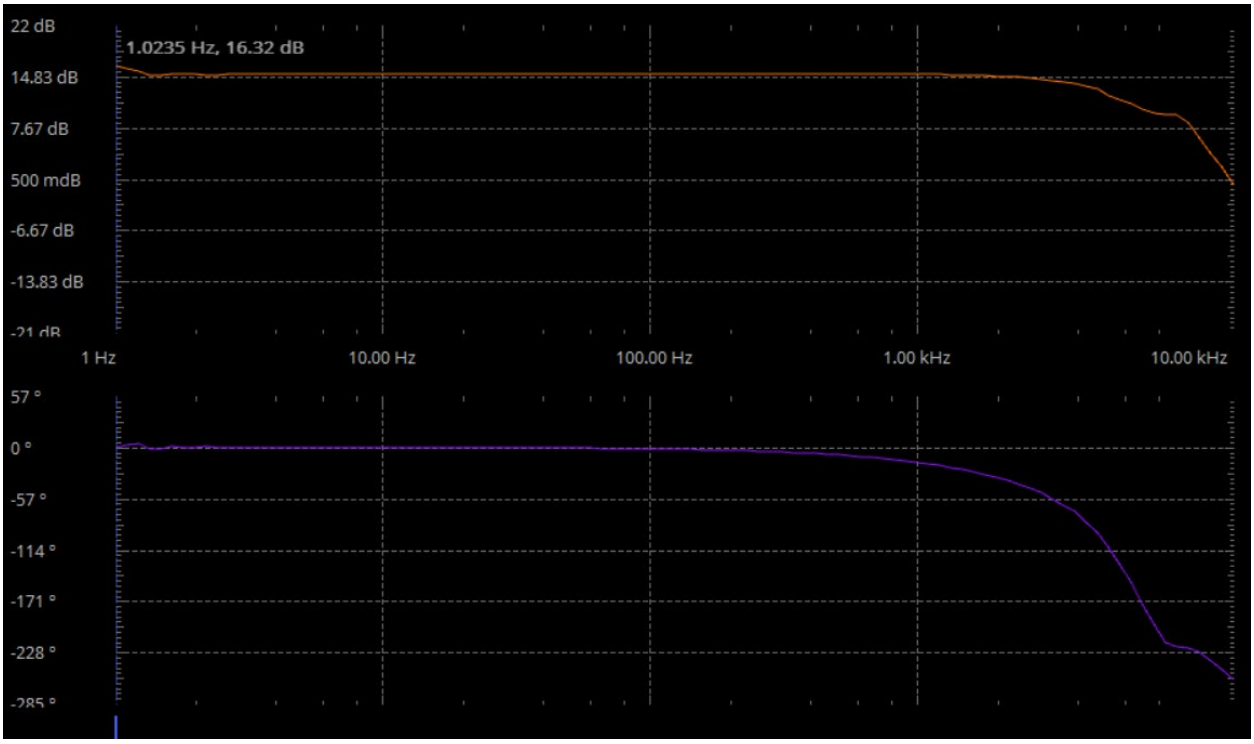


Figure 16: 18dB Bode plots

We can see that the highest low frequency gain measures around 16.3dB and 5kHz.