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Systems with Analog Integrated Circuits for Automotive Applications

LDO Design

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1. Introduction

This project's goal is to design a low-dropout linear regulator in the Cadence Virtuoso environment using specialized tools to run simulations that prove the functionality of the final integrated circuit. However, we will stop after the design stage, without going into the layout of the silicon wafer for the physical implementation. I was handed the following requirements:

1.1. Specifications

Parameter	Symbol	Requirement
Regulator	-	Linear regulator
Bangap voltage	V_{REF}	0.9V (no MC/temp variation)
Quiescent current	I_{SS}	20uA
Temp range	T	-40°C:150°C
Precision across temp & MC300	-	+/-2%
Supply Voltage	V_{IN}	1.6V:1.8V
Output voltage	V_Q	1.2V
Output current	I_Q	50uA: 100mA
Output capacitor	C_Q	1uF: 4.7uF
Over- / Undershoot	-	+/-120mV
Dropout voltage@100mA	V_{DR}	200mV
OTA	-	Free choice
Line Regulation	$\Delta V_{Q,Line}$	10mV
Load Regulation	$\Delta V_{Q,Load}$	10mV

2. Sizing strategy

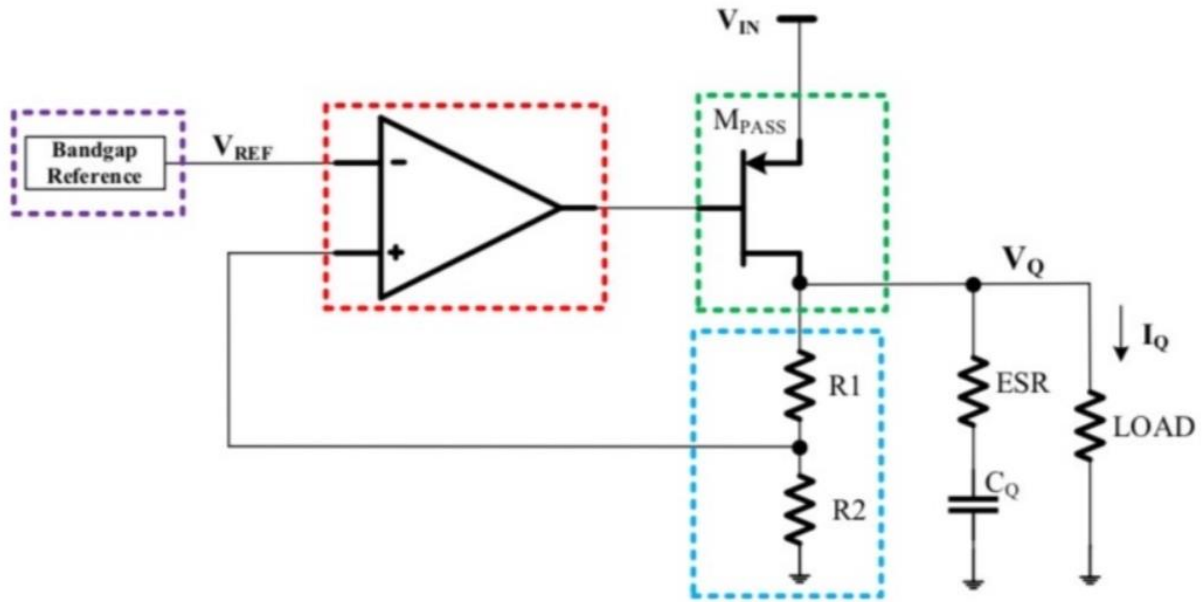*Figure 1: Schematic for a PMOS LDO*

The output voltage:

$$V_Q = V_{REF} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

The resistor values:

Since we know V_Q and V_{REF}, we can determine the relationship between the resistances:

$$\left(1 + \frac{R_1}{R_2}\right) = \frac{V_Q}{V_{REF}} = \frac{1.2V}{0.9V} => R_2 = 3 \cdot R_1$$

We want to keep the current consumption low, so we will set the current through this resistive divider at 1µA.

$$R_2 = \frac{V_{REF}}{I_{R2}} = \frac{0.9V}{1\,\mu A} = 900k\Omega$$

$$R_1 = \frac{R_2}{3} = \frac{900k\Omega}{3} = 300k\Omega$$

If we use 1µA for the resistive divider and 5µA for the bandgap reference, we are left with a current budget of 16µA for the error amplifier.

The power stage:

$$r_{on} = \frac{V_{DR}}{I_{Q\_max}} = \frac{0.2V}{0.1A} = 2\Omega$$

$$r_{on} = \frac{1}{\mu \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS-} V_{TH})} => \frac{W}{L} = \frac{1}{\mu \cdot C_{ox} \cdot r_{on} \cdot (V_{GS-} V_{TH})}$$

Although this is a value we could calculate, we will simply start with a big ratio and find the exact value through trial and error. The starting point will be $L = L_{MIN} = 180$nm and $W = 1\mu$m.

3. The ideal circuit

Before deciding on the topology of the error amplifier and doing any more computations, we will first build a circuit only using ideal components in order to simulate the behaviour we would expect from our IC in an environment that doesn't account for losses, parasitic components etc.

3.1. Ideal OpAmp

The behaviour of an Operational Amplifier without non-idealities can be simulated using a voltage-controlled voltage-source.

Figure 2: Ideal voltage-controlled voltage-source symbol

However, in order to account for the Gain-Bandwidth parameter of a real world OpAmp we need to mimic a low-pass filter behaviour. This is easily done with an RC filter and a second VCVS with unitary gain to isolate the impedances.
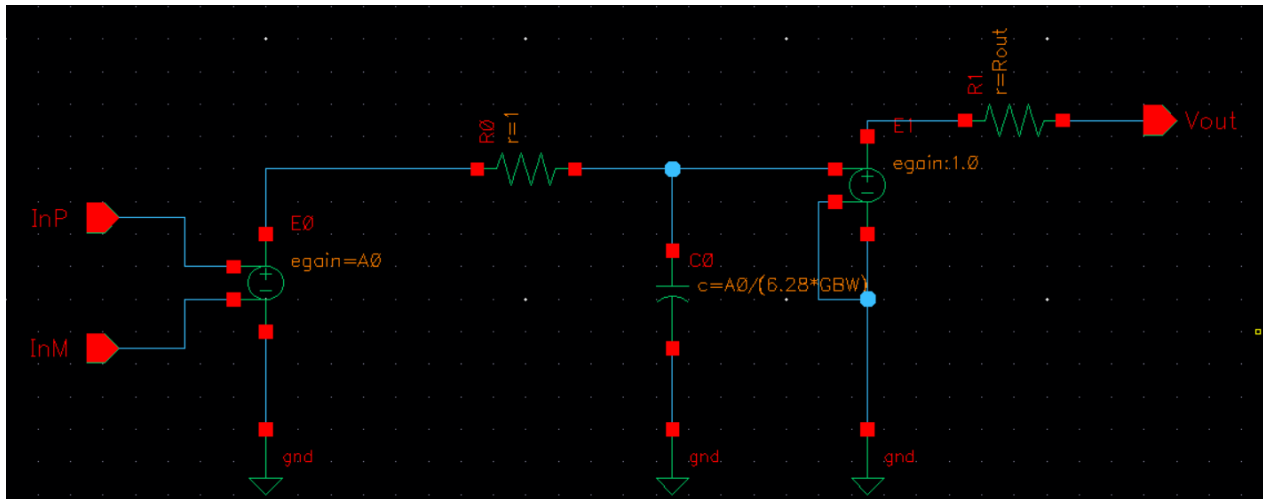
Figure 3: Ideal OpAmp schematic

3.2. Ideal LDO

After drawing up a symbol for the OpAmp, we can place it in a circuit as in Figure 1, using only components from analogLib (library for ideal components), except for the power stage transistor. The values of the components come either from the calculations above or from the requirements.
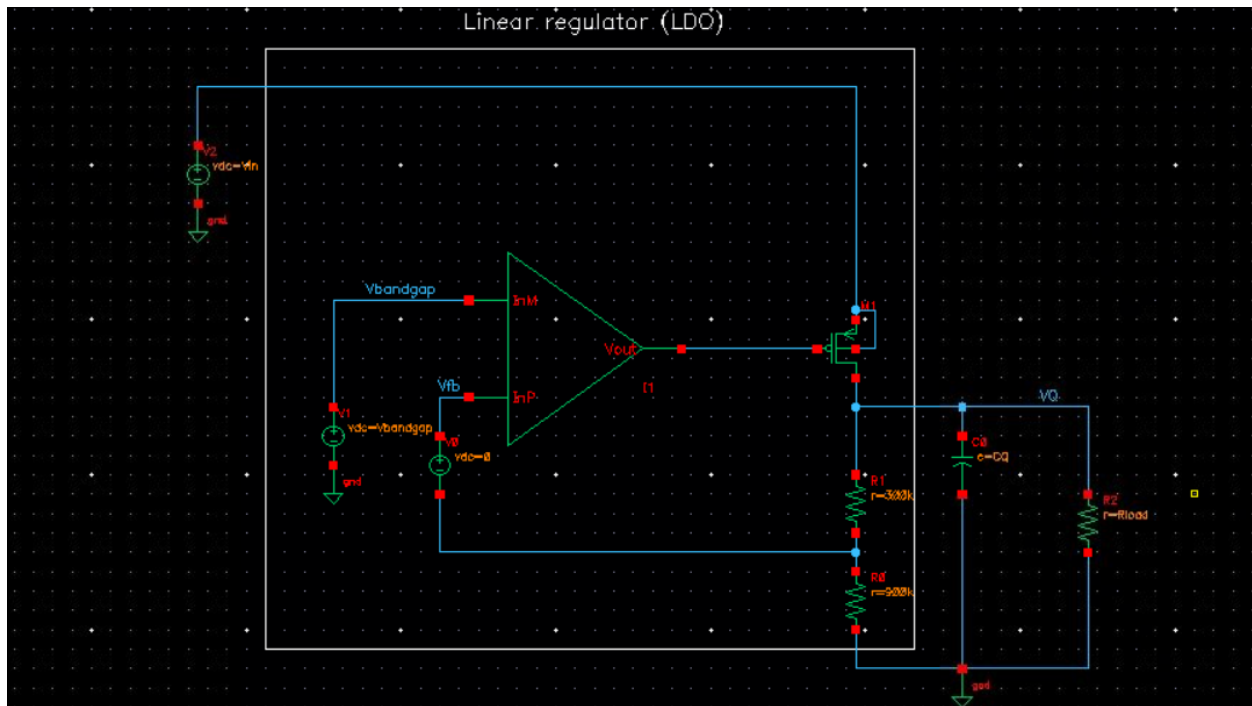

Figure 4: Ideal LDO schematic

3.3.   Simulation Results

Name	Value
1 A0	1K
2 CQ	1u
3 GBW	1M
4 mult_power	10
5 Rload	1.2/100m
6 Rout	1
7 Vbandgap	900m
8 Vin	1.8

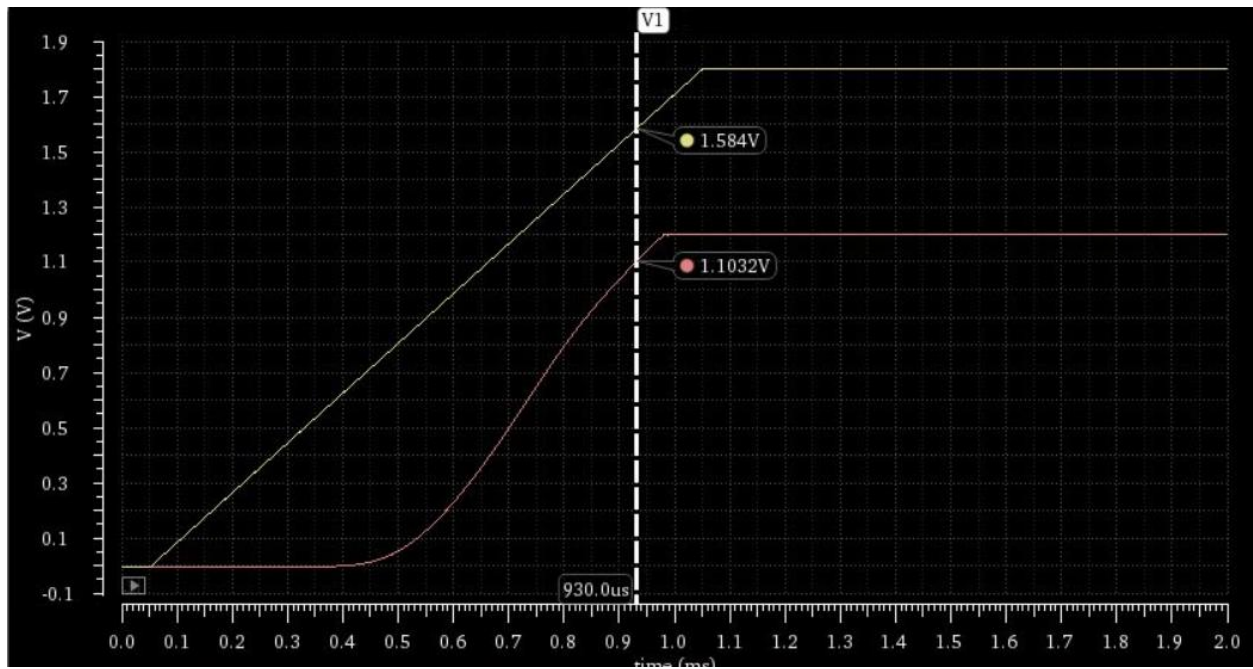*Figure 5: Simulation Setup*

Figure 6: Initial V_{DR}

We can see in this simulation that $V_{DR} = 484\text{mV}$ when $W = 1\,\mu\text{m}$, so we need to increase it further in order to obtain $r_{on} = 2\Omega$. We will do so by increasing the mult_power parameter in ADE L.

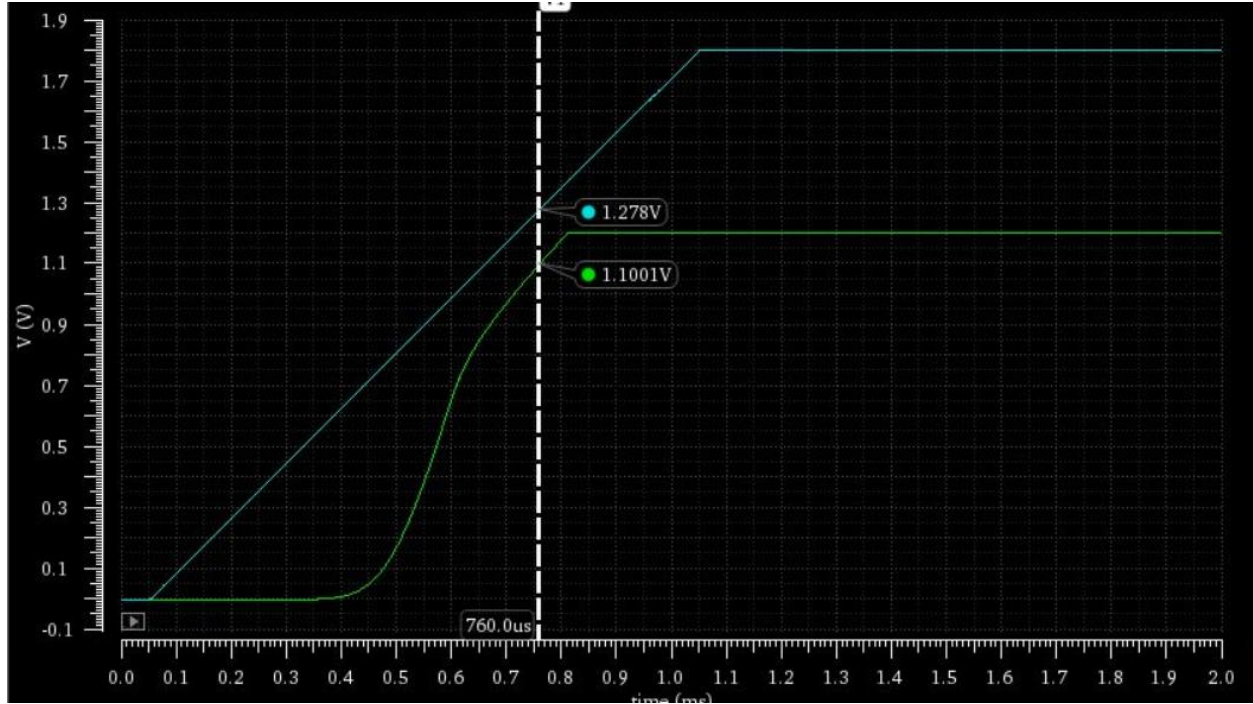| Width per Finger | 100.0000u M |
Length	180.0n M
Number of Fingers	1
Multiplier	mult_power

Figure 7: Power Stage parameters

Figure 8: V_{DR} after trial and error

By gradually increasing the multiplier, I noticed that at 25 V_{DR} becomes 200mV but we need to account for some margin of error down the road when we design a real OTA, so the final value is:

$$\text{mult\_power} = 30 \Rightarrow \frac{W}{L} = \frac{30*100\mu\text{m}}{180nm} = \frac{3mm}{180nm}$$

We can now see that at 100mA, the maximum output current, the dropout voltage is:

$$V_{DR} = 1.278\text{V} - 1.1\text{V} = 178\text{mV}$$

This was measured at 100mV less than the nominal output voltage, 1.2V.

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3.4. Corners

In order to test our chip in all conditions and determine the problematic areas of operation we will create some corners to simulate the behaviour of the circuit in the most extreme scenarios.

Figure 9: Corners setup

This setup will allow us to observe the operation at both temperature extremes, -40°C and 150°C, and also the worst combination of the parameters regarding power consumption, speed etc.
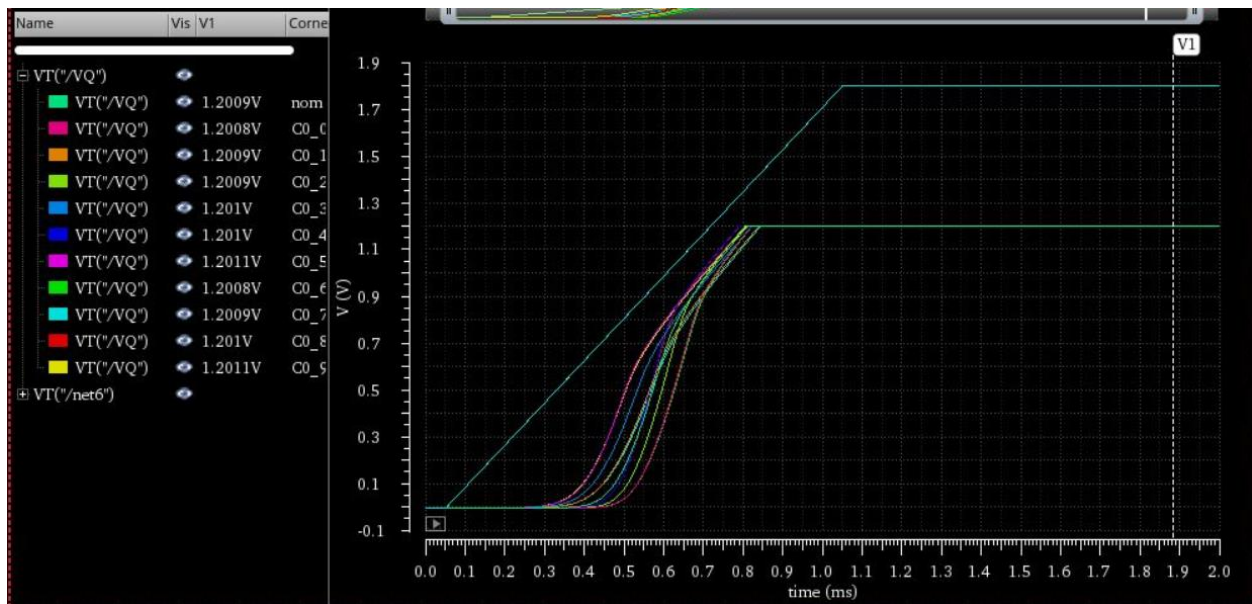

Figure 10: Dropout voltage variation in the corners

Figure 11: Calculator expression for V_{DR}

The calculator tool allows us to write an expression in order to automatically calculate the value of the voltage drop in each of the 10 corners.

4. OTA Design

4.1. Topology

In the following we will discuss the considerations when choosing a topology for our Operational Transconductance Amplifier. We would like to keep it as simple as possible while fulfilling all the requirements that the final chip has to meet.

One of the first to come to mind is the Miller topology since it has relatively few components, works well at the given power supply range and has a high gain. Additionally, we can use PMOS input transistors to obtain a high input impedance and CMMR, and a R_C-C_C network to compensate the zero.
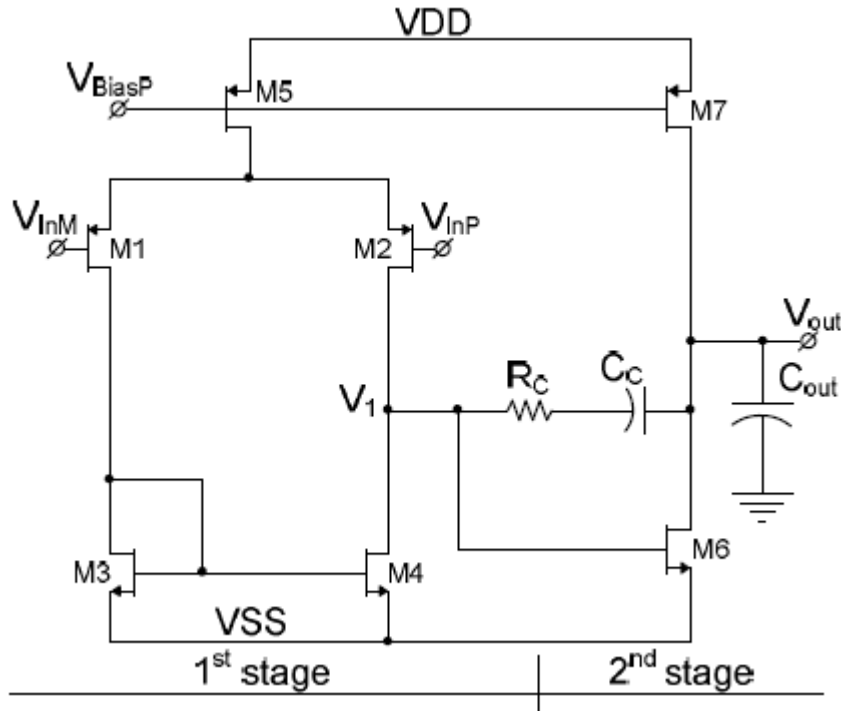

Figure 12: OTA Miller schematic

This time, the components are instanced from PRIMLIB instead of analogLib, meaning that they are no longer ideal.
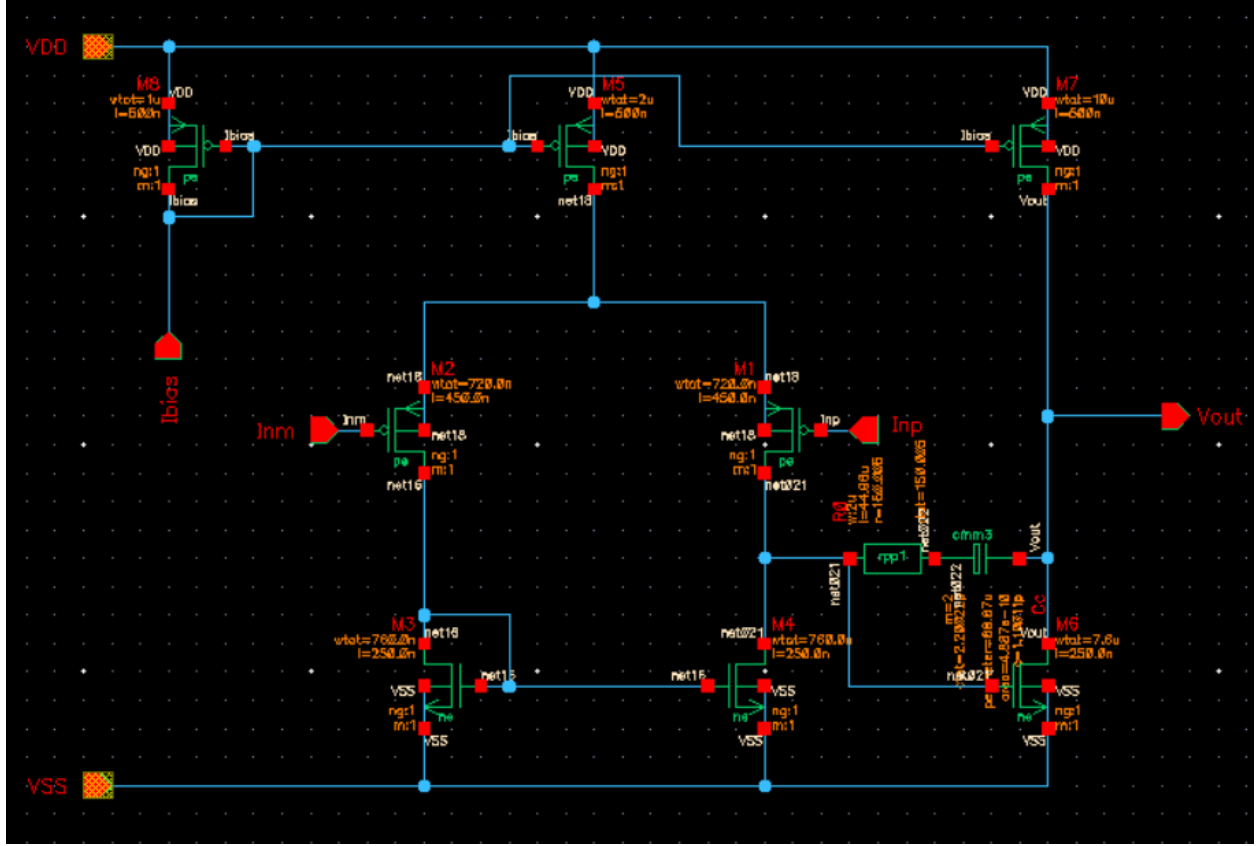
4.2. Implementation

Figure 13: OTA implementation

This is how the OTA looks like when considering I_{bias} an ideal current, without going into detail about how it is generated. This current is used to polarize the 2 stages, differential and common source amplifier.

The low frequency gain:

$$a_0 = G_{M1}G_{M2}R_{O1}R_{O2}$$

Where $R_{O1} = r_{DS1} \parallel r_{DS4}, \quad R_{O2} = r_{DS6} \parallel r_{DS7}$

Now we will draw up a symbol to give it a more familiar look and make the schematic modular and therefore easier to read.
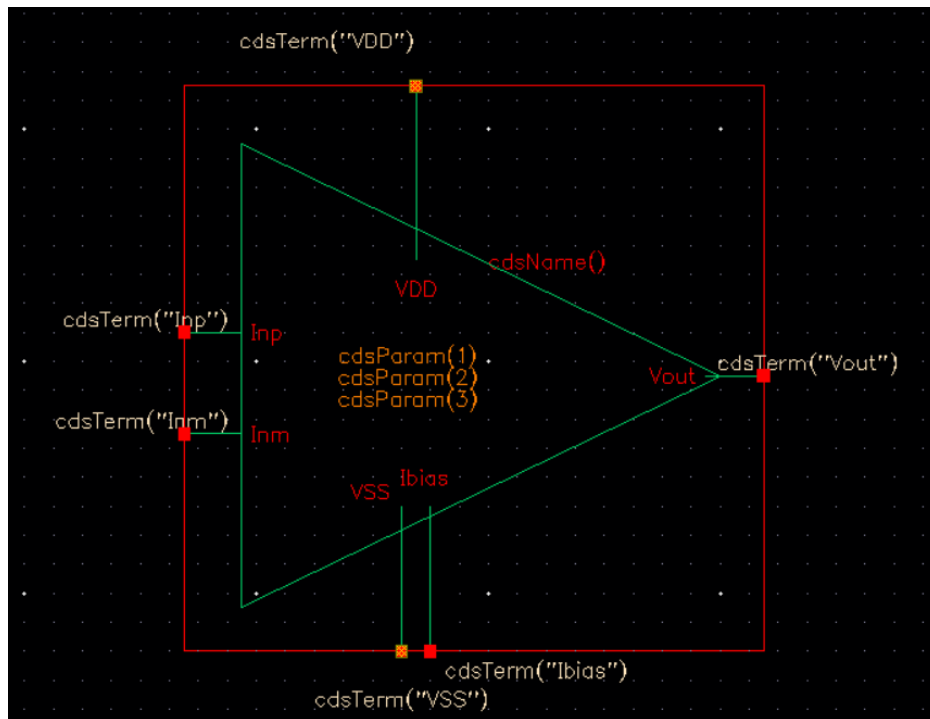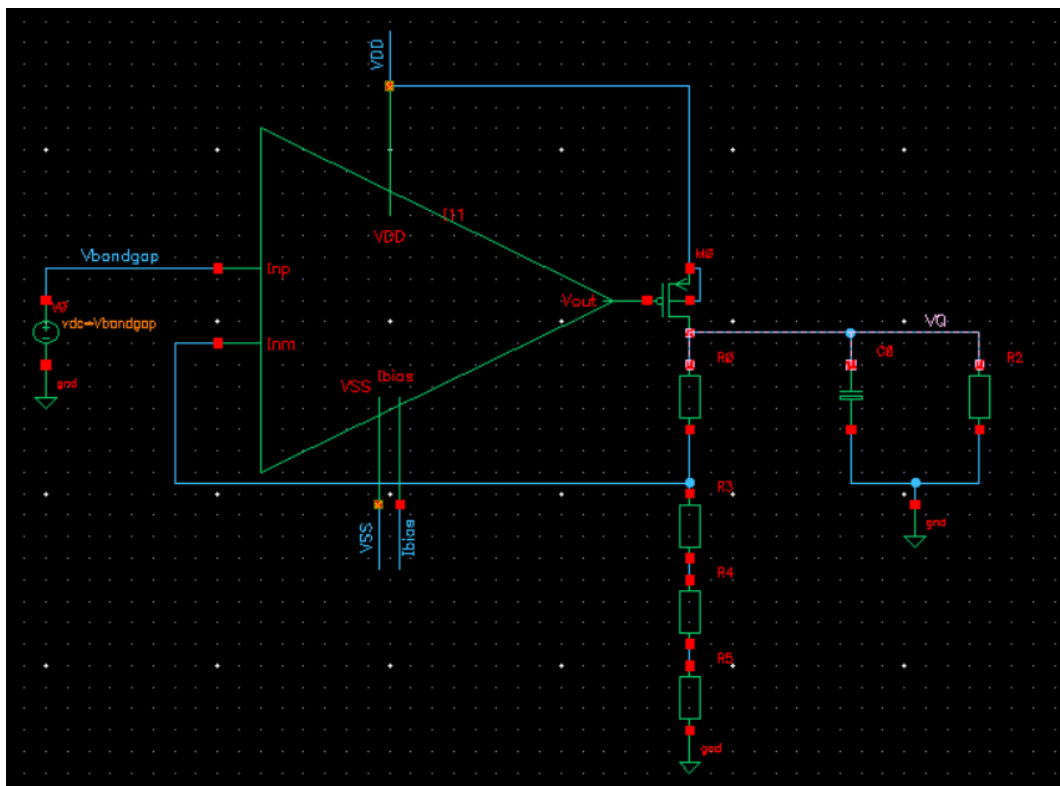
Figure 14: OTA symbol

Figure 15: LDO testbench