Simulation and Experimental Analysis of Layout-Dependent Thermal Performance of PCB-Embedded Resistive Heating Elements

Vlad Cristescu, Alexandra Fodor and Liviu Viman

Applied Electronics Department,
Faculty of Electronics, Telecommunications and Information Technology,
Technical University of Cluj-Napoca,
Cluj-Napoca, Romania,
vladcristescu1@gmail.com

Abstract— **This study examines advanced thermal management strategies for printed circuit boards (PCBs) with embedded heating elements, focusing on minimizing heat propagation toward temperature-sensitive components. The research investigates how design and material modifications influence thermal containment and temperature uniformity across the board. Several PCB configurations were analyzed, including the removal of copper pours on internal layers beneath the heating element, variation of the clearance between the heating area and adjacent circuitry, the addition of thermal vias versus non-plated through holes (NPTH) or modified copper thicknesses on the top layer. Thermal simulations reveal that a continuous row of thermal vias facilitates lateral heat transfer, reducing isolation efficiency, while NPTH structures limit spreading more effectively. Increasing copper thickness improves temperature uniformity but lowers peak temperature due to reduced electrical resistance which in turn increases power consumption. Conversely, thinner copper layers enable higher surface temperatures at lower current levels but elevate the risk of copper delamination. The findings provide practical design guidelines for minimizing unwanted thermal transfer and improving the reliability of PCBs used in high-temperature applications such as automated soldering, laboratory heating platforms, and precision thermal control systems.**

Keywords—PCB thermal management, embedded heating element, layout optimization, Joule heating

I. INTRODUCTION

Effective thermal management has become a cornerstone of modern electronic design as systems continue to evolve toward higher power densities and miniaturized form factors [1]. Maintaining appropriate temperature control is essential not only for ensuring performance and reliability but also for extending component lifetime. While the vast majority of research traditionally focuses on heat removal from power-dense or temperature-sensitive components [2], there is a parallel and growing field of work dedicated to PCBs that are deliberately engineered to generate heat. Such designs, often referred to as PCB-based heating platforms, are increasingly applied in reflow soldering, chemical processing, laboratory automation, and even aerospace environments [3], [4].

Compared to conventional metallic or ceramic heaters, PCB-based hot-plates offer a unique combination of cost efficiency, compactness, and integration flexibility. Their heating profiles can be easily customized through embedded resistive copper tracks, which enables fine control over temperature gradients and response times [5]. Previous studies have optimized several key aspects of these systems, including control algorithms, material selection, and heating element geometry, in order to enhance thermal stability and energy efficiency [6–8], while also addressing substrate degradation mechanisms that occur during prolonged exposure to high temperatures [9]. However, the influence of layout geometry, layer configuration, and via design on the resulting temperature field remains less explored despite their critical impact on thermal behavior.

The physical arrangement of copper traces, internal planes, and through-hole structures plays a decisive role in how heat propagates within a PCB. An unoptimized layout can lead to uneven temperature distribution, localized hot spots, and inefficient energy use [10], [11]. In this context, a deeper understanding of material-level heat transfer is equally important. Early benchmark studies by Graebner and Azar [12] measured the anisotropic thermal conductivity of printed wiring boards, highlighting the stark contrast between in-plane and through-thickness conduction. Their results demonstrated that copper layers primarily drive lateral heat spreading, while the glass-epoxy matrix constrains vertical heat flow—a critical factor in multilayer PCB thermal modeling. Similarly, Sarvar, Poole, and Witting [13] examined the impact of glass-fiber laminate properties on thermal simulations, revealing that ignoring anisotropy or material heterogeneity can result in large discrepancies between predicted and measured temperatures. Together, these findings emphasize the need to account for both material and geometric complexity when designing or simulating thermally active PCBs.

From a design standpoint, the integration of electrical heating elements within multilayer structures must consider both thermal and mechanical effects. Hegbom [14] underlined that uneven thermal expansion or stress gradients can compromise long-term structural reliability when resistive heating is embedded within functional circuitry. Building upon this idea, Xu et al. [15] applied finite element analysis (FEA) to optimize the structural design of solid heating elements, demonstrating that geometric refinement can significantly enhance heat uniformity and reduce localized stress concentrations. Although their work

primarily focused on metallic heating systems, the same principles can be extended to PCB-integrated heaters. Similarly, Zhang, Pennatini, and Bagnoli [16] developed an analytical model that incorporates the contribution of copper traces and vias to the overall thermal path, showing that small variations in these features can alter global temperature gradients and hotspot formation.

From a modeling perspective, multiple approaches have been used to study thermal transport in multilayer substrates. Finite element analysis (FEA) and computational fluid dynamics (CFD) remain two of the most widely employed techniques for simulating conduction and convection in complex PCB assemblies [17], [18]. Simplified numerical methods, such as the equivalent thermal resistance network proposed by Zhang and Chen [19], enable efficient steady-state analysis of multilayer PCBs, offering a practical balance between accuracy and computational cost. Additionally, Bozsóki et al. [20] provided a comprehensive comparison of reflow soldering models, reinforcing the need for combined simulation–experimental methodologies to validate thermal behavior. Dogruoz and Nagulapally [21] analyzed Joule heating effects and layer stack-up configurations on PCB temperature gradients, demonstrating how trace geometry and copper distribution strongly dictate localized thermal patterns. Similarly, Bagnoli and Zhang [22] examined electro-thermal interactions under high current flow, highlighting how local resistance variations can exacerbate hot-spot formation—an insight particularly relevant for embedded heating designs.

Motivated by these developments and building upon the PCB-based hot-plate system presented in previous work [23], this study explores how layout geometry and material variations affect thermal confinement and spreading in PCBs with embedded heating elements. The investigation introduces several new configurations, varying not only internal copper clearances and the presence of thermal vias, but also incorporating NPTH and altered copper thicknesses on the top layer. Through systematic thermal simulations, the study aims to provide a detailed understanding of how these factors interact to shape temperature uniformity, efficiency, and isolation performance.

While prior studies have examined the influence of vias and copper geometries on heat spreading, few have explored how NPTH or variations in copper thickness directly affect the confinement and dissipation of heat in PCB-integrated heaters. These parameters can substantially alter both electrical resistance and thermal conduction pathways, leading to complex trade-offs between temperature uniformity, efficiency, and mechanical reliability. By systematically analyzing these underexplored aspects, this work provides new insights into the interplay between electrical design choices and thermal behavior—an area of growing importance for applications demanding compact, thermally stable, and precisely controllable heating platforms.

The remainder of this paper is organized as follows: Section II presents the PCB design, including its electrical and structural characteristics. Section III outlines the simulation methodology and boundary conditions. Section IV discusses the simulation outcomes and their implications for thermal optimization. Finally, Section V concludes the paper with a summary of key findings and recommendations for designers aiming to optimize thermal performance.

II. PCB DESIGN

An overview of the proposed system architecture is presented in Fig. 1. The PCB-based temperature control platform employs a closed-loop regulation system specifically designed to maintain stable and uniform heating across a defined active surface. The control architecture integrates sensing, actuation, and feedback mechanisms to ensure that the surface temperature follows a precise thermal profile, even under varying load or ambient conditions.
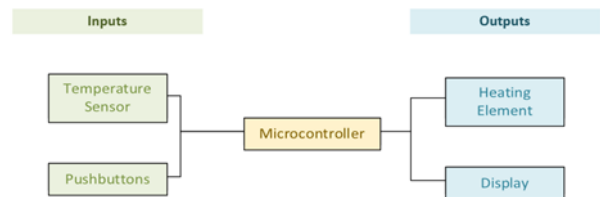

Fig. 1.   Block diagram of the system

The heating element is manufactured as a 1.4mm-wide meander-shaped copper track, extending over a total length of 2000mm and a total area of 70mm by 50mm, which is embedded in the top layer of the PCB to maximize thermal transfer to the surface.

To evaluate how geometric and material parameters influence heat propagation and confinement, a series of PCB configurations were designed and simulated. The layouts are grouped into three main configurations (C1–C3) based on the extent of copper plane removal and the clearance between the heating element and nearby components.

- C1: copper planes fully poured on all layers
- C2: copper planes voided only under the heating element but extending immediately adjacent to it
- C3: copper planes starting 7mm away from the heating element

Each of these configurations was further subdivided according to the type of thermal isolation structure implemented:

(a) no shielding (reference layout)

(b) a continuous row of plated thermal vias separating the heating area from the adjacent circuitry

(c) identical positioning but using NPTH instead of vias

Configuration C3, which represents the most thermally isolated geometry, was extended with three additional subvariants to investigate more specific effects:

(d) inclusion of two large elliptical NPTH slots, one horizontal and one vertical, positioned in the open region between the heating zone and the components

(e) C3.a) but with 70μm copper on the outer layers

(f) C3.a) but with 17.5μm copper on the outer layers

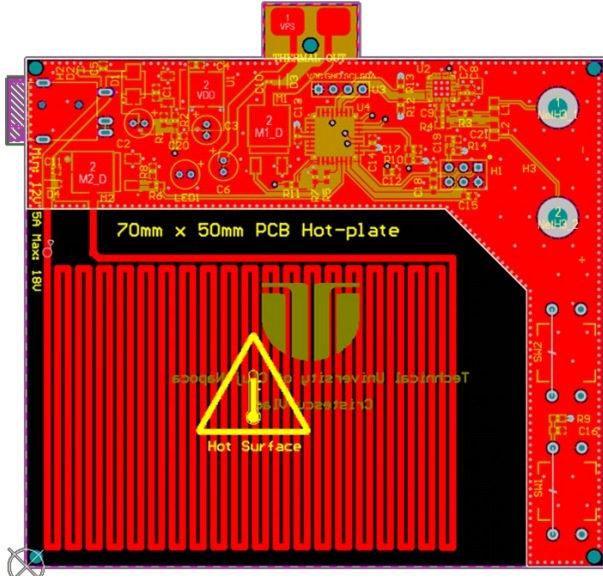Configuration C3.b) is illustrated in Fig. 2.

Fig. 2.   PCB layout configuration C3.a) – copper planes poured 7mm away from the heating element, with no shielding

Power is delivered to the heating element through a MOSFET-based driver circuit operating under the supervision of a Proportional–Integral–Derivative (PID) control loop [24]. A thermocouple sensor provides real-time temperature feedback, which is continuously compared against a reference setpoint. Based on the error, the PID controller dynamically adjusts the duty cycle of the driving signal to maintain a stable and uniform temperature over the active area. The system is powered by a 12V, 8A DC supply, which ensures sufficient current capability for both the heating element and the control electronics.

The control platform is designed to reach surface temperatures exceeding 200 °C, though in practical operation the maximum temperature is limited by the glass transition temperature (Tg) of the substrate. To preserve mechanical integrity and long-term reliability, the operating range is kept below the Tg threshold, making the system particularly suitable for processes involving low-melting-point solder alloys, such as Sn42Bi58 (138 °C) [25].

The thermal performance of the PCB is inherently constrained by the material properties of the substrate. Standard FR4 laminates exhibit a Tg around 130–140 °C, which may be insufficient for prolonged exposure to high temperatures [26]. As alternatives, high-Tg FR4 variants ($\approx$ 170–180° C) can offer improved thermal stability with only moderate cost increases, while polyimide-based materials (Tg > 250° C) are able to provide excellent heat resistance and mechanical strength, albeit at the expense of higher manufacturing complexity. For extreme-temperature applications, ceramic substrates [27] such as alumina (Al_2O_3) or aluminum nitride (AlN) achieve outstanding thermal conductivity and stability well above 500 °C, but their brittleness and cost restrict their use to specialized systems. Consequently, the selection of substrate material requires a balanced consideration of thermal endurance, mechanical robustness, manufacturability, and cost-effectiveness.

The final board employs a four-layer stack-up organized in a Signal–Ground–Power–Signal arrangement, with an overall thickness of 1.6 mm, as illustrated in Fig. 3.

Name	Material	Type	Weight	Thickness	Dk	Df
Top Overlay		Overlay				
Top Solder	Solder Resist	Solder Mask		0.01mm	3.5	
Top Layer	CF-004	Signal	1oz	0.035mm		
Dielectric 2	PP-022	Prepreg		0.2104mm	4.5	0.02
GND	CF-004	Signal	1/2oz	0.0152mm		
Dielectric 1	Core-042	Core		1.065mm	4.6	0.02
POWER	CF-004	Signal	1/2oz	0.0152mm		
Dielectric 3	PP-022	Prepreg		0.2104mm	4.5	0.02
Bottom Layer	CF-004	Signal	1oz	0.035mm		
Bottom Solder	Solder Resist	Solder Mask		0.01mm	3.5	
Bottom Overlay		Overlay				

Fig. 3.   PCB stack-up: SIG-GND-PWR-SIG

III. SIMULATION SETUP AND METHODOLOGY

All thermal simulations were carried out using Cadence Celsius EC Solver, which employs a hybrid thermal modeling approach. This method combines heat conduction in solids with empirical natural convection correlations derived from the Nusselt number. Convection is approximated using a boundary layer model, and radiation effects are included via the Stefan-Boltzmann law for higher temperatures. This strategy allows for efficient thermal analysis of electronic systems without the computational demands of full CFD simulations. In this study, the simulations were further enhanced by accounting for Joule heating, with electrical boundaries defined according to the power dissipated in the heating element.

Fig. 4 shows the setup of these electrical boundaries in the simulation. The blue bars are set to 5 A, ensuring uniform current flow through the entire heating element, while the purple bar is set at 0.1 V to serve as a reference potential for current simulation. This configuration is applied consistently across all simulations.
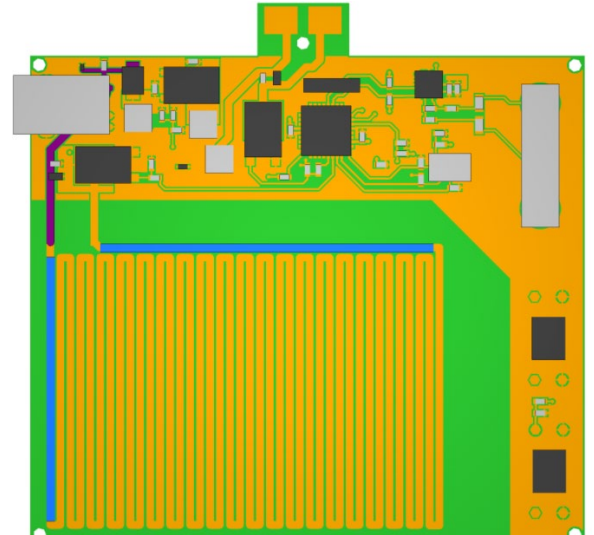

Fig. 4.   Electrical boundary setup in Cadence Celsius EC Solver

In this comparative study, each simulation adjusts a single parameter to isolate its effect on thermal performance, enabling a clear comparison of how each layout change influences heat distribution. The resulting thermal data for all configurations are presented and analyzed in the following section.

IV. RESULTS

In this section the thermal simulation results for the PCB layouts described in detail in Section II are displayed. The analysis focuses on how variations in copper plane placement, thermal isolation strategies and copper thickness affect heat distribution in and around the embedded heating element. Boundary conditions and electrical setup are kept consistent across all simulations to ensure comparability. Temperature distributions are visualized using a uniform color scale, with deep blue representing 25 °C and deep red representing 160 °C. This consistent legend allows for direct visual comparison of thermal behavior across different layouts.

Fig. 5 shows the temperature distribution for configuration C1.a), where copper planes are fully poured on all internal layers beneath the heating element with no shielding vias. The continuous copper planes promote significant lateral heat spreading, resulting in lower peak temperatures in the heating area and a wider thermal footprint across the PCB surface.
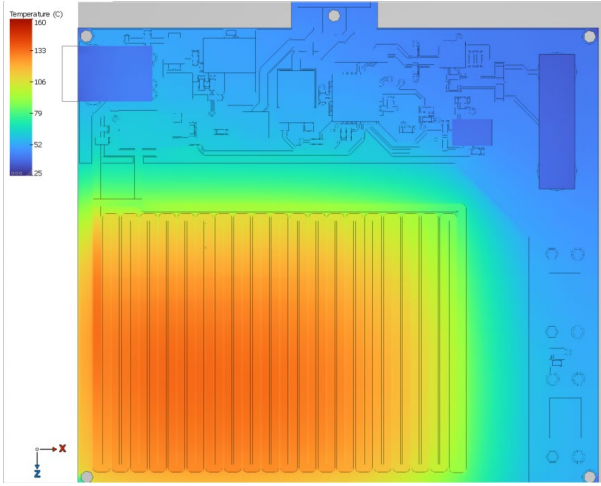

Fig. 5.   C1.a): Full copper planes without vias

Fig. 6 illustrates configuration C2.a), in which copper planes are voided directly under the heating element but extend immediately adjacent to it, again without shielding vias. Compared to C1.a), thermal spreading is more confined, producing higher peak temperatures in the heating area and reducing heat propagation toward surrounding regions.
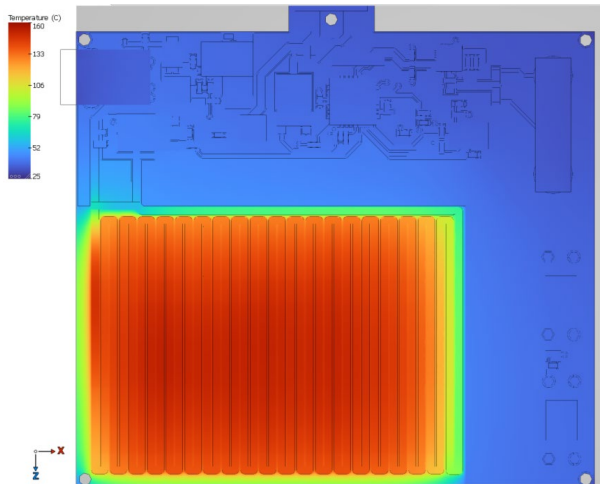

Fig. 6.   C2.a): Copper planes with no gap without vias

Figs. 7–12 present the C3 sub-configurations, where copper planes start 7 mm away from the heating element. This layout exhibits the most localized thermal behavior, maintaining high temperatures within the heating area while minimizing heat diffusion across the rest of the board.

Within this group, each variation highlights different thermal isolation strategies and material choices: C3.a) without shielding, C3.b) with a row of plated thermal vias, C3.c) with the same via layout implemented as NPTH, C3.d) with elliptical NPTH slots, and C3.e) and C3.f) with modified outer-layer copper thicknesses.

C3.a) demonstrates the baseline behavior of the 7 mm clearance geometry, with high temperatures concentrated in the heating area and minimal lateral spreading. C3.b) shows the effect of adding a row of plated thermal vias, which slightly modifies the heat path and reduces peak temperatures near the edges of the heating zone.
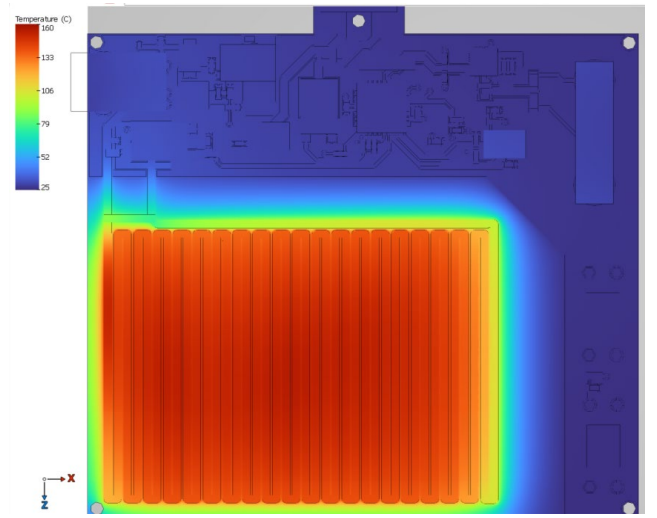

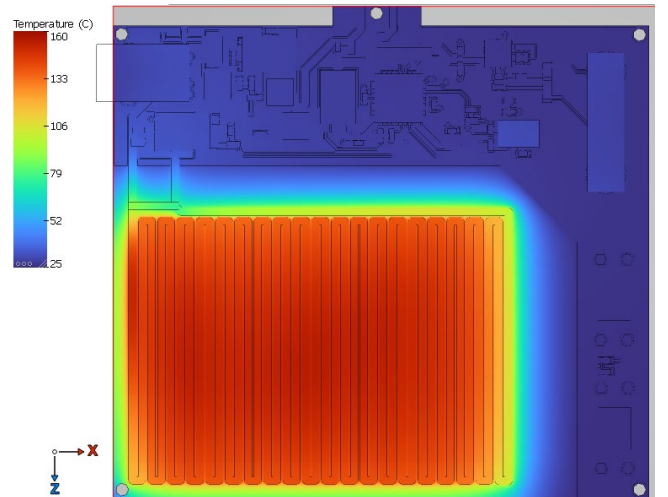Fig. 7.   C3.a): Copper planes with 7mm gap without vias

Fig. 8.   C3.b): Copper planes with 7mm gap with vias

C3.c) implements the same via pattern using NPTH, producing a similar thermal footprint but with slightly higher peak temperatures due to reduced thermal conduction. C3.d) introduces two large elliptical NPTH slots in the open region between the heating zone and adjacent components. This further restricts heat flow toward the surrounding circuitry while maintaining high temperatures in the heating area.
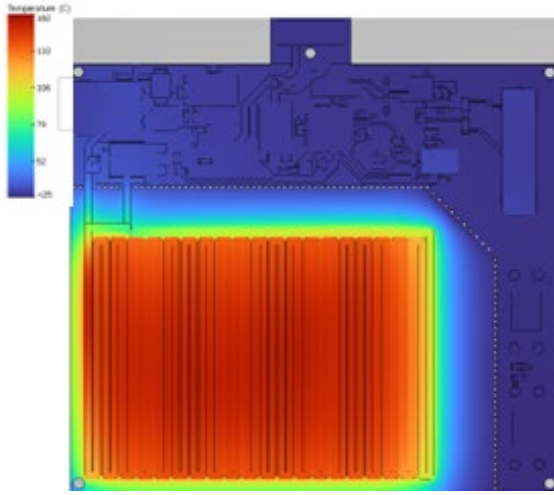
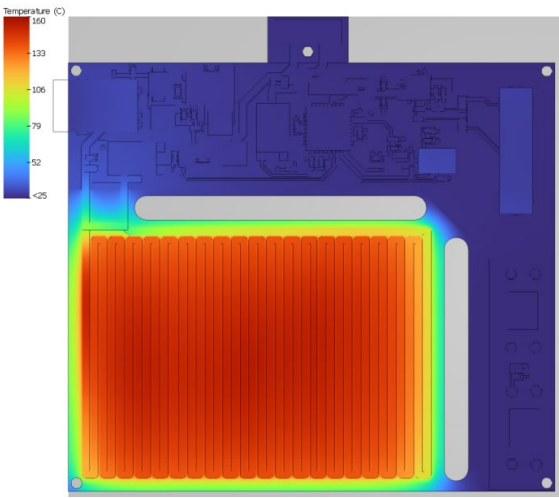Fig. 9. C3.c): Copper planes with 7mm gap with small NPTH

Fig. 10. C3.d): Copper planes with 7mm gap with big NPTH

Finally, C3.e) and C3.f) explore the impact of varying outer-layer copper thickness, showing how increased or reduced copper affects lateral heat spreading and peak temperatures. In C3.e), with 70μm instead of the standard 35μm copper, the maximum temperature is significantly lower than the reference layout. This is primarily due to the constant current: a larger cross-sectional area lowers the resistance of the heating element, reducing the power dissipated as heat. The greater thermal mass of the thicker copper may also contribute to slower temperature rise.
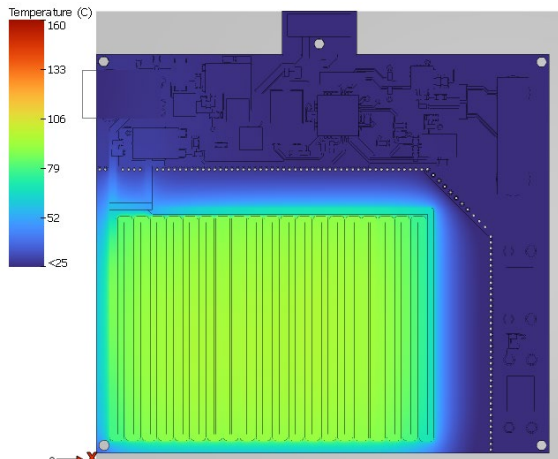

Fig. 11. C3.e): 70μm copper planes with 7mm gap

Conversely, in C3.f), with thinner copper, the maximum temperature rises well above the reference layout. The higher resistance makes the heating element more power-efficient, but the thinner copper also increases the risk of delamination due to higher localized temperatures and reduced mechanical robustness.
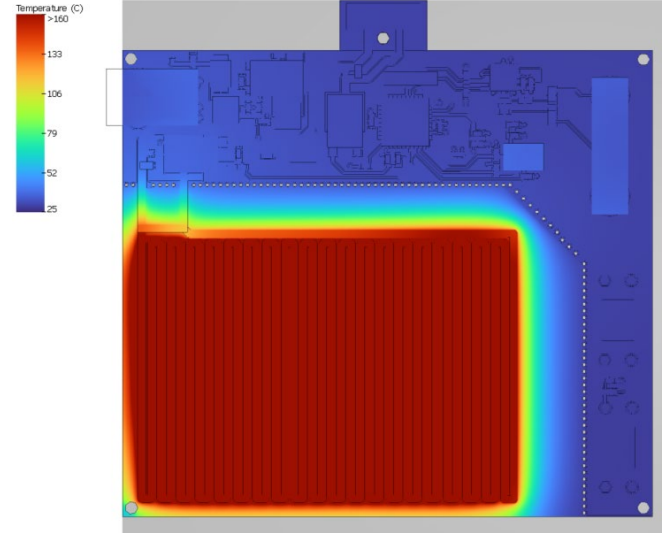

Fig. 12. C3.f): 17.5μm copper planes with 7mm gap

For the sake of visual comparability, the color scale legend is kept consistent with the other simulations. However, it should be noted that the peak temperature in this case is substantially higher, as highlighted in Table 1, which records the minimum and maximum temperature for each PCB configuration, providing a quantitative comparison of the thermal containment effectiveness.

TABLE I. MINIMUM AND MAXIMUM TEMPERATURES

PCB	Min[°C]	Max[°C]
C1.a)	40.6	134
C1.b)	41.1	134
C1.c)	39.9	134
C2.a)	32.9	153
C2.b)	33.1	153
C2.c)	32.5	153
C3.a)	26.4	155
C3.b)	26.5	155
C3.c)	26	155
C3.d)	25.4	155
C3.e)	23.5	94.7
C3.f)	29.3	262

The simulation results and the resulting table data clearly demonstrate the impact of PCB layout modifications on both heat localization and the overall thermal behavior of the system.

For configurations C1.a)–C1.c), where copper planes are fully poured beneath the heating element, the maximum temperatures remain relatively moderate, while the minimum temperatures are elevated. This reflects effective lateral heat spreading due to the continuous copper, which distributes thermal energy across the PCB and reduces localized hot spots.

Configurations C2.a)–C2.c), with copper voids directly under the heating element but extending immediately adjacent to it, exhibit higher maximum temperatures while slightly lowering minimum temperatures compared to C1. This suggests that introducing voids restricts lateral heat flow, concentrating heat within the active area, but still allows some dissipation to the surrounding copper, maintaining moderate background temperatures.

The C3 series, featuring a 7 mm clearance around the heating element, demonstrates the most localized thermal behavior. Configurations C3.a)–C3.d) consistently reach high peak temperatures in the heating area while keeping minimum temperatures across the remainder of the PCB lower than in C1 and C2, confirming superior thermal isolation.

Notably, configurations C3.e) and C3.f), where the outer-layer copper thickness is altered, show extreme thermal effects. In C3.e), the thicker copper reduces resistance in the heating element, leading to a lower peak temperature despite similar layout geometry, while the increased thermal mass further moderates temperature rise. Conversely, in C3.f), the thinner copper raises the resistance of the heating element, producing significantly higher peak temperatures in the heating zone. This demonstrates that copper thickness directly affects the power dissipated in the heating element under constant current, impacting both heating efficiency and thermal stress on the PCB. These observations highlight a trade-off: thinner copper increases power efficiency and peak temperature but may risk delamination or mechanical failure, while thicker copper provides thermal moderation at the expense of heating efficiency.

To complement the simulation results, experimental tests were carried out on the fabricated PCB (C3.b) to verify the thermal performance predicted by the models. An infrared (IR) image of the board operating under steady-state conditions is shown in Fig. 11, highlighting the concentrated heating around the embedded element and confirming the localized thermal pattern observed in simulations.
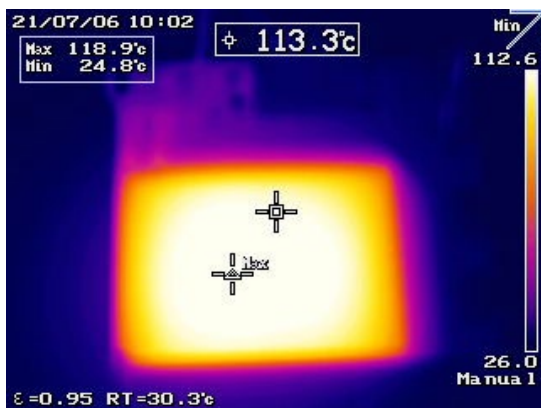

Fig. 11. IR image of the manufactured PCB (C3.b) during operation

Fig. 12 depicts the temperature profiles at two measurement points: the center of the heating element ("hot junction") and a distant point near the top-right corner of the board ("cold junction"), where the thermocouple IC is placed.
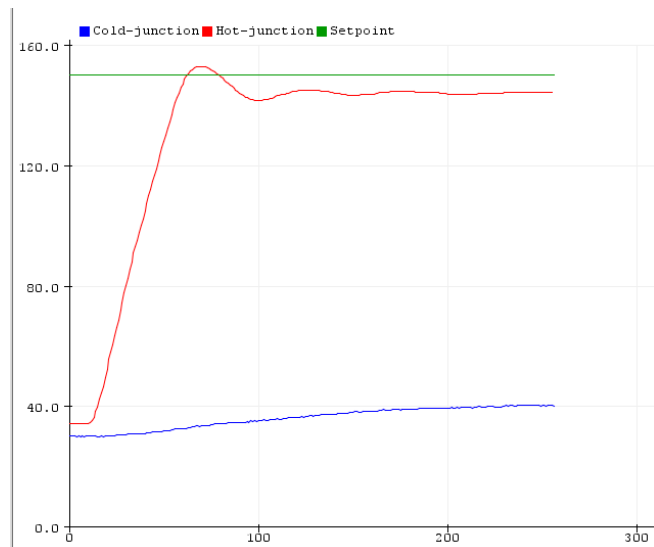

Fig. 12. Hot vs. cold junction temperature over 250 seconds of operation

Even after the heating element operated at around 150 °C for close to five minutes, the temperature at the cold junction remained below 40 °C. This indicates that heat is effectively confined to the active region, with minimal transfer to surrounding areas, supporting the efficacy of the optimized PCB layout.

V. CONCLUSIONS

This study highlights how PCB layout choices and copper distribution strategies strongly influence thermal behavior around embedded heating elements. The simulations and experimental results consistently show that continuous copper planes promote extensive lateral heat spreading, reducing peak temperatures in the heating area while raising minimum temperatures across the board. Introducing copper voids or clearance gaps around the heating element concentrates heat locally, producing higher peak temperatures in the active region while maintaining lower background temperatures elsewhere.

The choice of thermal isolation structures has a measurable, though relatively modest, effect on heat localization. NPTH structures improve thermal isolation compared to the reference layout, with larger NPTHs providing slightly better heat confinement. Conversely, plated thermal vias tend to reduce isolation performance because the additional copper provides a path for lateral heat spreading. This observation emphasizes that while thermal vias are highly effective for channeling heat vertically through the PCB—for example, to offer thermal relief for an IC from underneath—they are not effective at restricting lateral heat propagation.

Copper thickness on the outer layers plays a critical role in determining peak temperatures and overall thermal efficiency. Thicker copper results in a larger cross-sectional area which translates to lower resistance of the heating element. Under constant current, this results in lower peak temperatures due to less dissipated power, which helps

moderate temperature fluctuations but may reduce heating efficiency. Thinner copper, in contrast, increases the element's resistance, producing higher peak temperatures and greater heating efficiency while drawing the same current, but also raising the risk of thermo-mechanical stress and potential copper delamination.

For PCB designers, these findings provide several actionable guidelines. When localized heating is desired, combining copper voids or clearance gaps with NPTH slots can help confine heat, while plated vias should be used carefully, recognizing their tendency to spread heat laterally. Adjusting outer-layer copper thickness offers a powerful means of tuning thermal performance: thicker copper moderates peak temperatures and stabilizes thermal behavior, whereas thinner copper enables faster heating but at the cost of mechanical reliability. Overall, optimizing the combination of copper layout, isolation structures, and copper thickness allows designers to balance heat localization, thermal spreading, and reliability according to the system's requirements.

DECLARATION OF GENERATIVE AI AND AI-ASSISTED TECHNOLOGIES IN THE MANUSCRIPT PREPARATION PROCESS

During the preparation of this work the author used ChatGPT in order to improve readability and language. After using this tool, the author reviewed and edited the content as needed and takes full responsibility for the content of the published article.

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