Power supply

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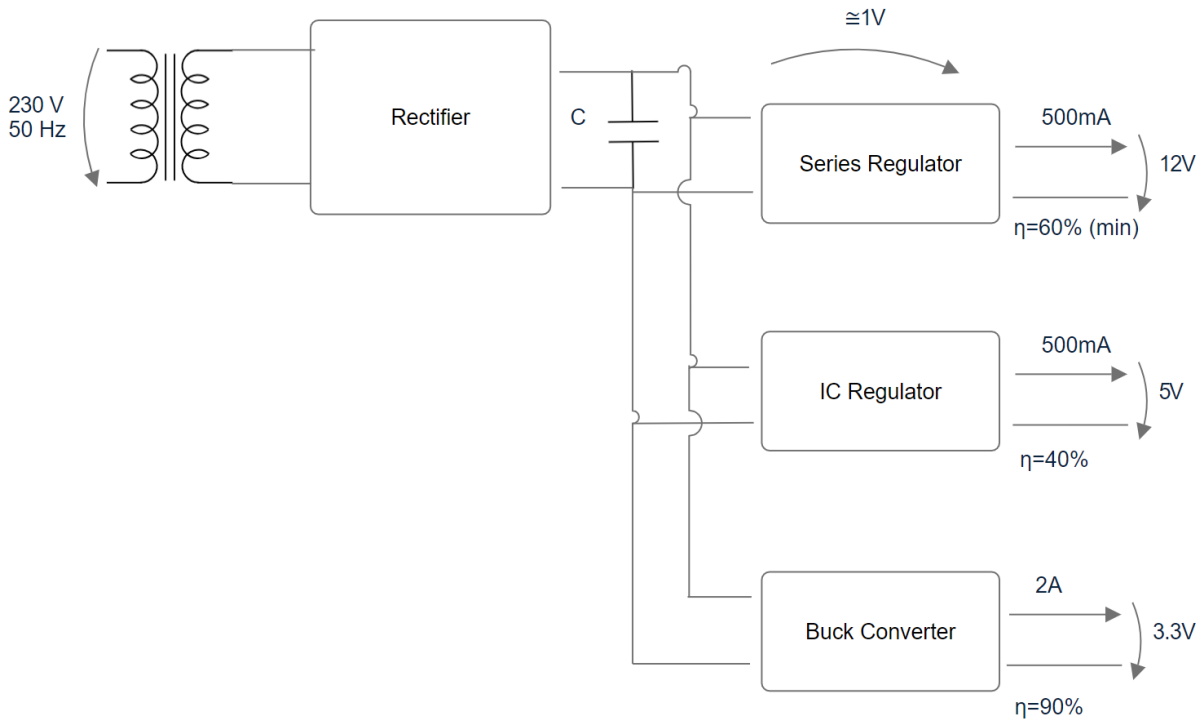
Contents

1. Introduction

The aim of the project is to design a power supply with certain specifications. For this, the knowledge accumulated in the Power Supply courses was put in practice. The software tools used (simulators) were LTspice (for designing the power circuits – rectifier, series regulator, IC regulator and the power circuit for the Buck converter) and PSIM (for designing the control circuit for the Buck converter – the PID controller).

2. Block Diagram and design specifications

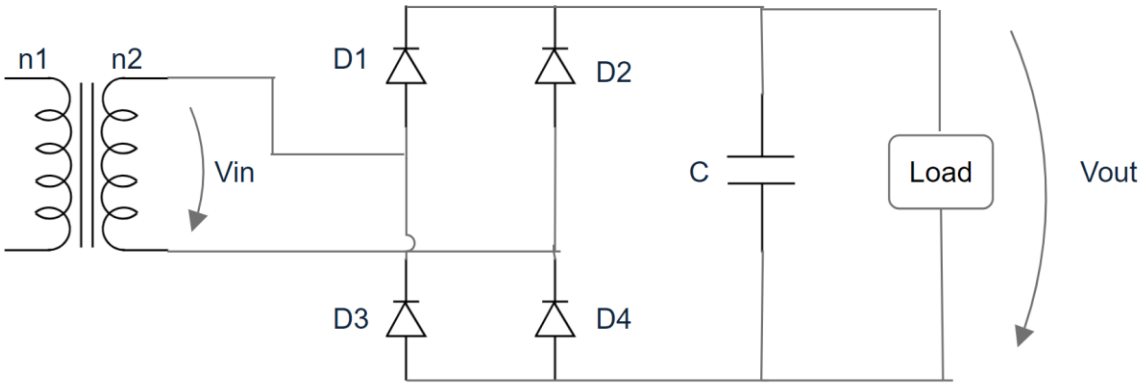


From the block diagram there can be seen that the source will be supplied from the electric grid, having a voltage RMS value of 230V and a frequency of 50Hz. Then, a transformer is needed in order to supply the rectifier with capacitive filter in order to get a voltage close enough to that required by the 3 output circuits: Series regulator, IC regulator and Buck converter.

- Approximative calculations for the rectifier:

Knowing that at the output of the series regulator 12V are needed and that a voltage of approximately 1V…1.2V drops on the series transistor (form its internal structure) which acts as a regulating element, a voltage of approximately 15V should be present at the input of the series regulator and thus at the output of the rectifier.

So, the average value of the output voltage of the rectifier should be 15V. The rectifier used is a full-wave full-bridge rectifier, having the following structure:



$Vprimar\_RMS := 230\ V$

$f := 50\ Hz$

$\omega := 2 \cdot \pi \cdot f = 314.1593\ Hz$

$T := \frac{1}{f} = 0.02\ s$

$Vout\_avg := 15\ V$

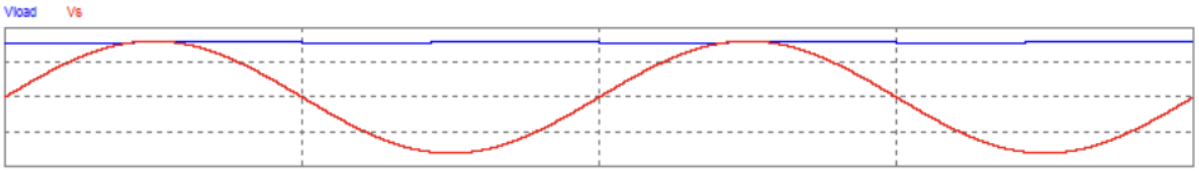
$VDiodes\_on := 3\ V$

$Vin\_max := Vout\_avg + VDiodes\_on = 18\ V$

$vin(t) := Vin\_max \cdot \sin(\omega \cdot t)$

$Vprimar\_max := Vprimar\_RMS \cdot \sqrt{2} = 325.2691\ V$

$N := \frac{Vprimar\_max}{Vin\_max} = 18.0705$



There can be seen that the amplitude of the input voltage (Vs on the graph and Vin_max in the calculus) is almost equal with the average value of the output voltage (in calculus also the voltage drop on the diodes was taken into consideration and the ripple was ignored). Taking into account the amplitude of the input voltage of the rectifier (Vin_max) and the amplitude of the voltage from the grid (Vprimar_max), the ratio of the transformer can be calculated ($N = \frac{n_1}{n_2} = 18$), so the transformer is a step-down transformer (voltage from the secondary winding is

smaller than the voltage of the primary winding). (*Remark:* For calculations, also the voltage drop of about 3V across the diodes has been taken into consideration).

In what follows, the output power of the rectifier will be calculated, expressing first the output powers of each of the 3 output circuits, then by knowing the efficiency of each circuit, the input power can be determined. The output power of the rectifier will be the sum of these input powers:

$Iout\_ser\_reg := 500\ mA$ $Iout\_IC\_reg := 500\ mA$ $Iout\_Buck := 2\ A$

$Vout\_ser\_reg := 12\ V$ $Vout\_IC\_reg := 5\ V$ $Vout\_Buck := 3.3\ V$

$\eta\_ser\_reg := 60\ \%$ $\eta\_IC\_reg := 40\ \%$ $\eta\_Buck := 90\ \%$

$$Pout\_ser\_reg := Iout\_ser\_reg \cdot Vout\_ser\_reg = 6\ W$$

$$Pout\_IC\_reg := Iout\_IC\_reg \cdot Vout\_IC\_reg = 2.5\ W$$

$$Pout\_Buck := Iout\_Buck \cdot Vout\_Buck = 6.6\ W$$

$$Pin\_ser\_reg := \frac{Pout\_ser\_reg}{\eta\_ser\_reg} = 10\ W$$

$$Pin\_IC\_reg := \frac{Pout\_IC\_reg}{\eta\_IC\_reg} = 6.25\ W$$

$$Pin\_Buck := \frac{Pout\_Buck}{\eta\_Buck} = 7.3333\ W$$

$$Pout\_rectifier := Pin\_ser\_reg + Pin\_IC\_reg + Pin\_Buck = 23.5833\ W$$

In what follows, the output current of the rectifier and the input current for the Buck converter will be calculated:

$$Iout\_rectifier := \frac{Pout\_rectifier}{Vout\_avg} = 1.5722\ A$$

$$Iin\_Buck := \frac{Pin\_Buck}{Vout\_avg} = 0.4889\ A$$

3. Designing the rectifier

The functioning of the rectifier based on the above circuit can be described as follows: the diodes D1 and D4 conduct on the positive alternance of the input voltage while D2 and D3 on the negative one. The capacitor stores energy and thus tries to keep the output voltage constant, filtering the ripple and thus acting as a filter (LPF). Without the capacitor, the output voltage would follow the input one, except the negative alternance of the input would become positive at the output.

Taking into consideration the previous calculations, the transformer that could be used for this application is **VPP20-1500**, as it has a voltage in the secondary that can reach 20V and an output current of about 1.5A. Its cost is about 18$.

Knowing the requirement of a ripple at the output of the rectifier of maximum 1V, the following calculations were done in order to choose the suitable diodes and capacitor:

$$\Delta Vout\_rectifier := 1\ V$$

$$\Delta Q := \frac{Iout\_rectifier \cdot 2 \cdot \pi}{2 \cdot \omega} = 0.0157\ C$$

$$C := \frac{\Delta Q}{\Delta Vout\_rectifier} = 0.0157\ F$$

$$\gamma := \frac{\frac{\Delta Vout\_rectifier}{2}}{Vout\_avg} = 0.0333$$

$$\theta := 2 \cdot \sqrt{\gamma} = 0.3651$$

First, the amount of charge (ΔQ) was calculated and then the value of the necessary capacitance. After that, the voltage ripple factor was calculated and then the conduction angle.

$$ID\_max := Iout\_rectifier \cdot \frac{\pi}{2 \cdot \sqrt{\gamma}} = 13.5268\ A$$

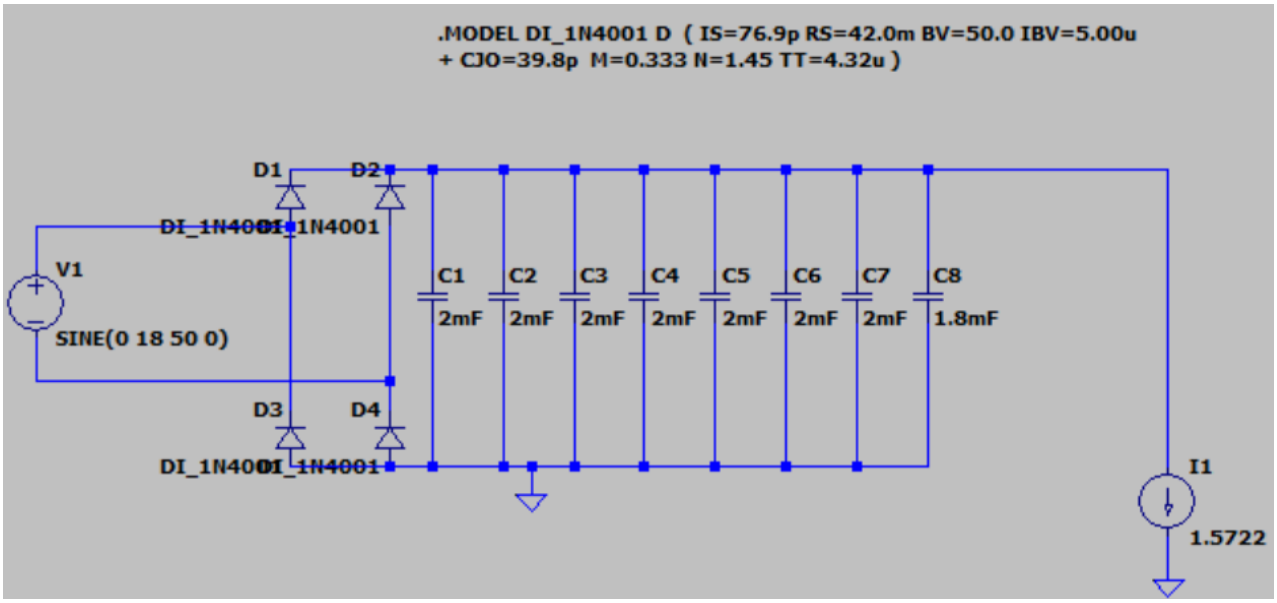
$$Urrm := Vin\_max = 18\ V$$

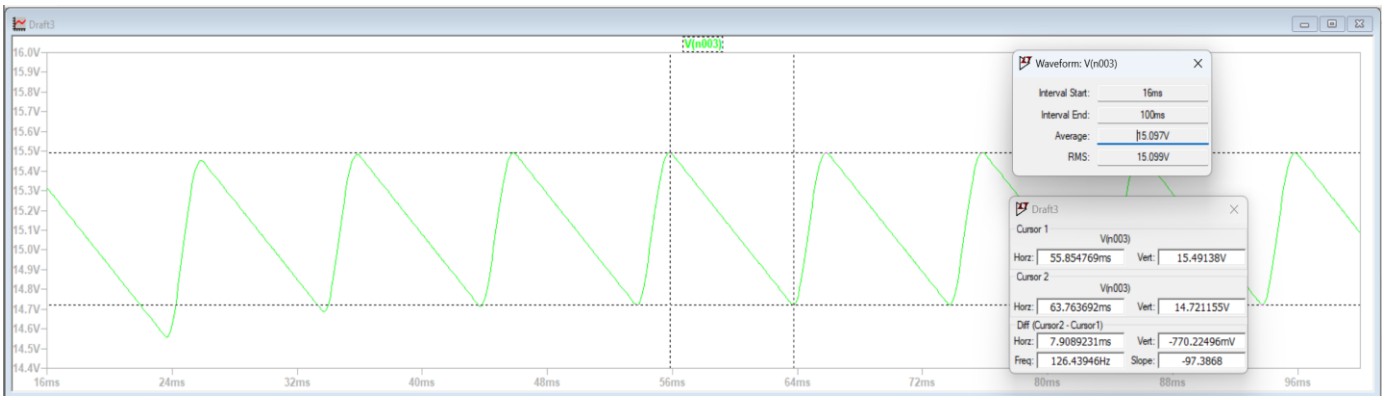
$$ID\_avg := \frac{Iout\_rectifier}{2} = 0.7861\ A$$

Afterwards, the maximum current through the diodes was calculated (depending on the output average current and the voltage ripple factor) and the maximum reverse voltage and average voltage. Knowing this information, the type of diode chosen was **1N4001**, as this diode supports a maximum reverse voltage of 50V, a maximum forward current of 30A and an average current of 1A.

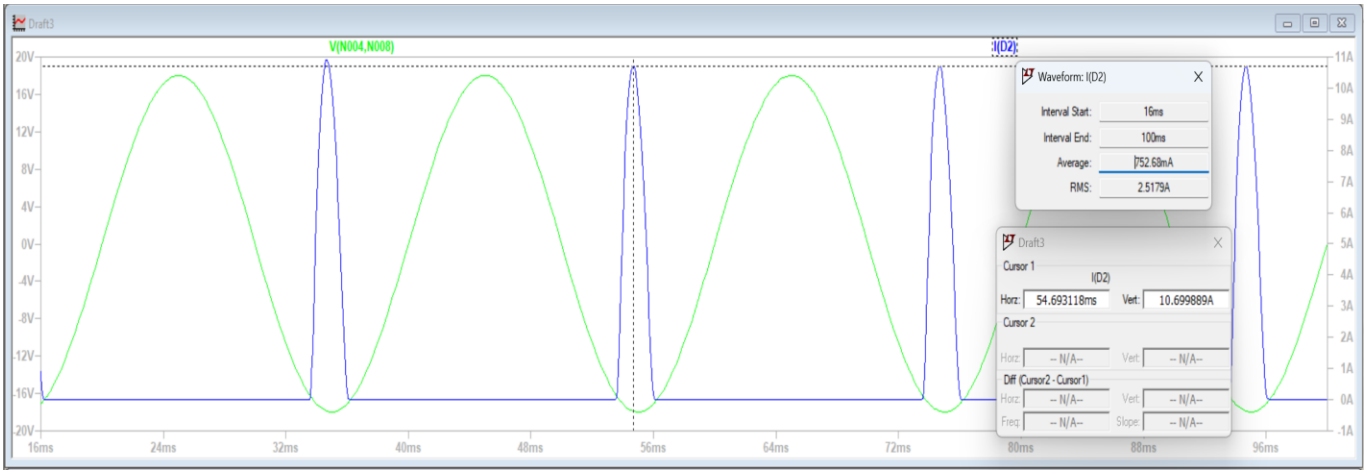
For the output voltage of 15V, a capacitor with a voltage rating of about 1.2 times greater will be chosen. So, of 18V at least. Consequently, 7 capacitors of 2mF **EKYC250ELL202MK20S** and one of 1.8mF **25ZLQ1800MEFC12.5X20**. These capacitors are electrolytic capacitors, as these are the most suitable for power supplies applications, having a high capacity for noise filtering (in this case, to filter the ripple) and for storing energy.

The circuit for the simulation would be the following:

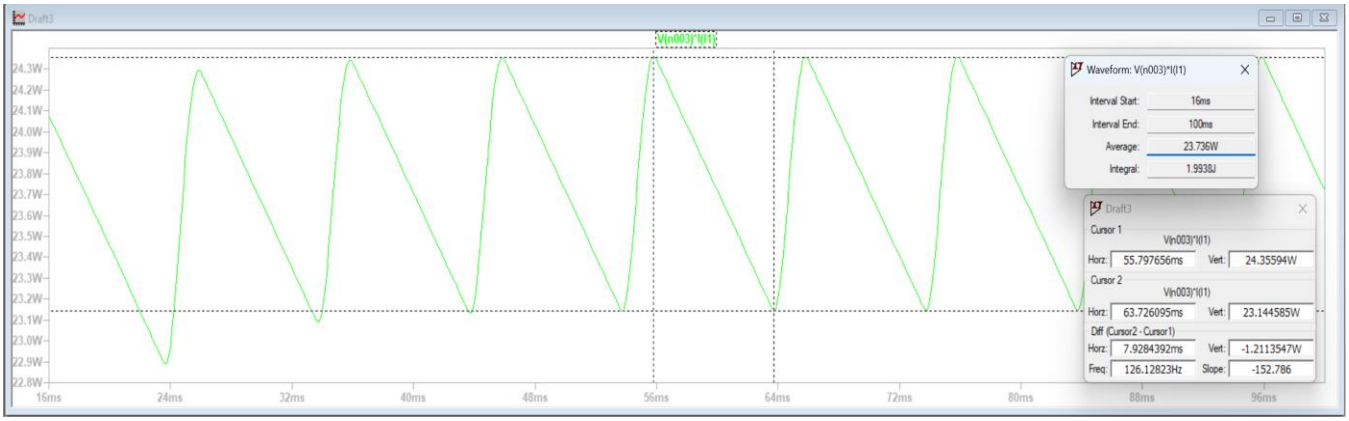




From simulation, there can be seen that the voltage ripple is of about 770 mV and the average value is approximatively 15.097V (because not all the losses from the circuit were taken into account).



The current through the diodes has a maximum value of 10.69 A and an average value of about 752mA which confirms the approximative calculations. Also, there can be seen that the diode D2 (as its current is simulated) conducts on the negative alternance of the input voltage (plotted with green).

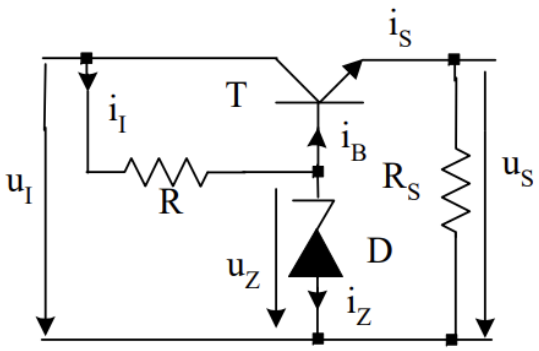


The output power also varies around an average value of 23.73W with +/- 1.2W, which also confirms the previous approximatively calculated value of 23.54W.

The components used so far:

No.	Part No.	Amount	Price per piece ($)	Total price ($)
1.	**VPP20-1500**	1	18.58	18.58
2.	**1N4001**	4	0.02	0.08
3.	**EKYC250ELL202MK20S**	7	1.14	7.98
4.	**25ZLQ1800MEFC12.5X20**	1	1.05	1.05
TOTAL				27.69

4. Designing the series voltage regulator



The series voltage regulator consists of a transistor which acts as the regulating element, a Zener diode which together with the Vbe voltage of the transistor gives the output voltage and a resistance which ensures the biasing of the Zener diode (the necessary current), called ballast resistance.

Knowing the following design requirements,

$$Sui := 100$$

$$Ro := 0.2\ \Omega$$

$$Vout\_ser\_reg = 12\ V$$

$$Iout\_ser\_reg = 0.5\ A$$

The equations for choosing the components can be written.

For the transistor: (emitter current, current gain – taken 100, base current, collector-emitter voltage)

$$IE := Iout\_ser\_reg = 0.5\ A$$

$$hfe := 100$$

$$IB := \frac{IE}{hfe + 1} = 0.005\ A$$

$$VCE := Vout\_avg - Vout\_ser\_reg = 3\ V$$

Taking these data into account, and that the output resistance must be 0.2Ω, which has the following formula:

$$gm := \frac{1}{Ro} = 5\ \mathrm{S}$$

$$hie := \frac{hfe}{gm} = 20\ \Omega$$

So, the transistor **BD135-16** is suitable for this application, as it also has a maximum collector current of 1.5A (for this application the desired collector current being the output current of 500mA). The base-emitter voltage of this transistor is approximately 1V, so to obtain at the output 12V, a Zener diode of 13V is required:

$$VBE := 1\ \mathrm{V}$$

$$VZ := VBE + Vout\_ser\_reg = 13\ \mathrm{V}$$

The diode chosen is **BZX84C13VLY** that has a nominal Zener current of 5mA, a Zener voltage that varies between 12.7V and 13.3V. In order to ensure the proper functioning of the Zener diode, one can calculate the ballast resistance:

$$VZmax := 13.3\ \mathrm{V}$$

$$VZmin := 12.7\ \mathrm{V} \qquad IZ := 5\ \mathrm{mA}$$

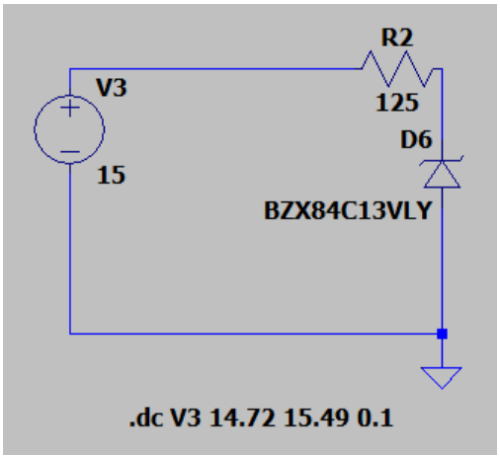
$$Iout\_ser\_reg\_min := Iout\_ser\_reg - \Delta Iout\_ser\_reg = 0.45\ \mathrm{A}$$

$$Iout\_ser\_reg\_max := Iout\_ser\_reg + \Delta Iout\_ser\_reg = 0.55\ \mathrm{A}$$

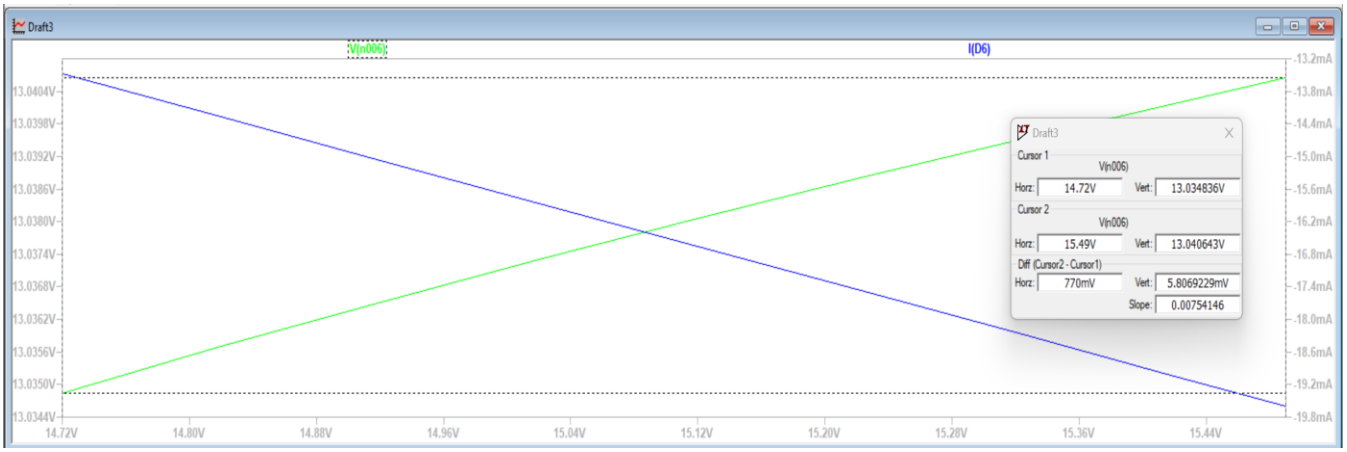
$$R1max := \frac{(Vout\_avg + \Delta Vout\_rectifier) - VZmax}{IZ + \frac{Iout\_ser\_reg\_min}{hfe + 1}} = 285.5497\ \Omega$$

$$R1min := \frac{(Vout\_avg - \Delta Vout\_rectifier) - VZmin}{IZ + \frac{Iout\_ser\_reg\_max}{hfe + 1}} = 124.455\ \Omega$$

A resistance of 125Ω has been taken into consideration to be able to calculate the internal resistance of the diode:



By varying the voltage source in the same interval as the output voltage from the rectifier, and plotting the variation of the voltage and current of the Zener diode, the internal resistance of the diode can be calculated:



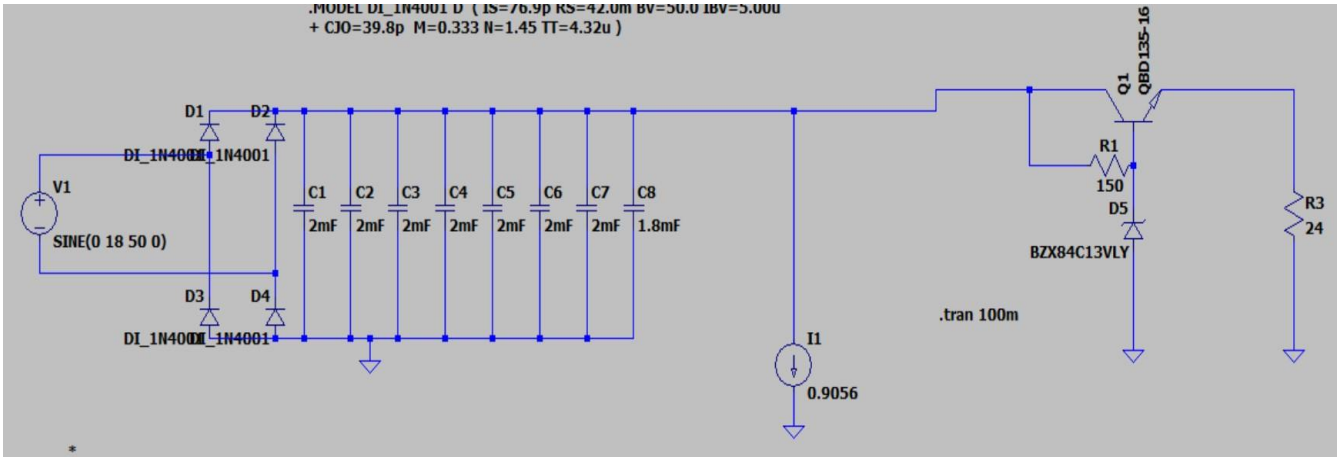
$$RZ := \frac{13.040643\ \text{V} - 13.034836\ \text{V}}{19.5948\ \text{mA} - 13.4813\ \text{mA}} = 0.9499\ \Omega$$

Knowing that the line regulation has to be 100, the ballast resistance can be adjusted in order to obtain the desired performance:

$$R1 := (Sui - 1) \cdot RZ = 94.0366\ \Omega$$

But, its minimum value was previously determined to be 124.45Ω. So, a value of 150Ω was chosen, in order to ensure a line regulation of 100 despite of all losses that were not taken into consideration and of the approximations made by the calculations. The chosen resistor is **RN55D1500FB14.**

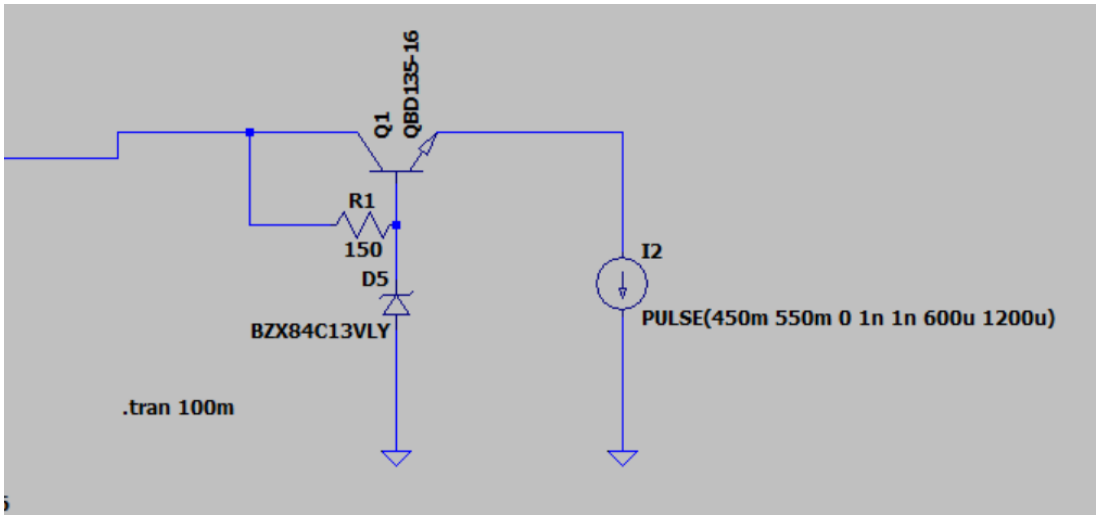
The circuit, combined with the previously designed rectifier is:

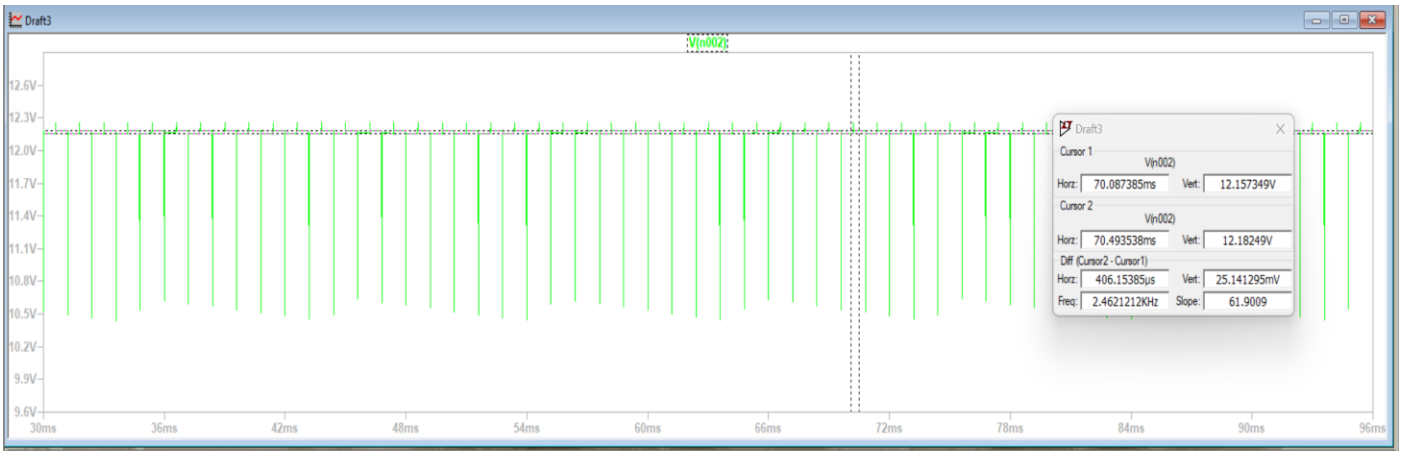


In order to verify if the circuit works properly, simulations were performed. Firstly, a current source has been put as a load and its current is varied between 450mA and 550mA (interval chosen because of the requirements – explained below):

$$\Delta Vout\_ser\_reg := \frac{\Delta Vout\_rectifier}{Sui} = 0.01\ V$$

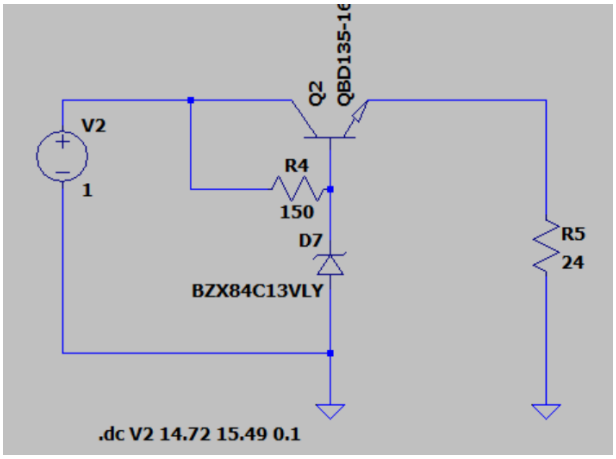
$$\Delta Iout\_ser\_reg := \frac{\Delta Vout\_ser\_reg}{Ro} = 0.05\ A$$



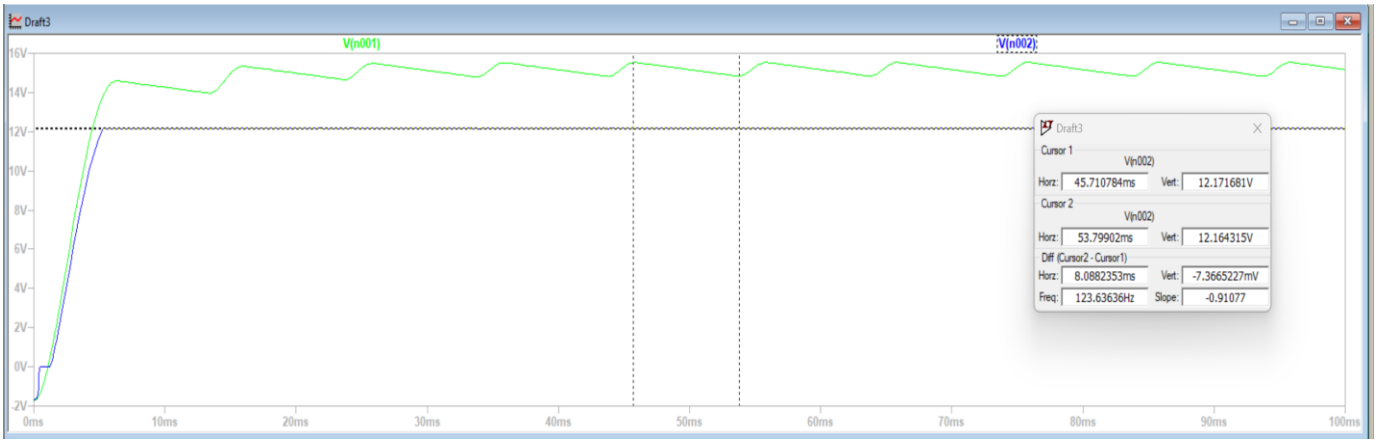


So, taking into consideration that the output voltage varies between 12.157V and 12.182V and the output current between 450mA and 550mA, it results in an output resistance of about 0.25Ω.

Next, to verify if the line regulation is properly modeled, the regulator is taken separately and its input voltage is varied:



Consequently, the line regulation, defined as the variation of the input voltage (14.72…15.49V) over the variation of the output voltage (12.162…12.171V), is about 89.87. The output voltage of the whole circuit (combined with the rectifier) is about 12.16V:



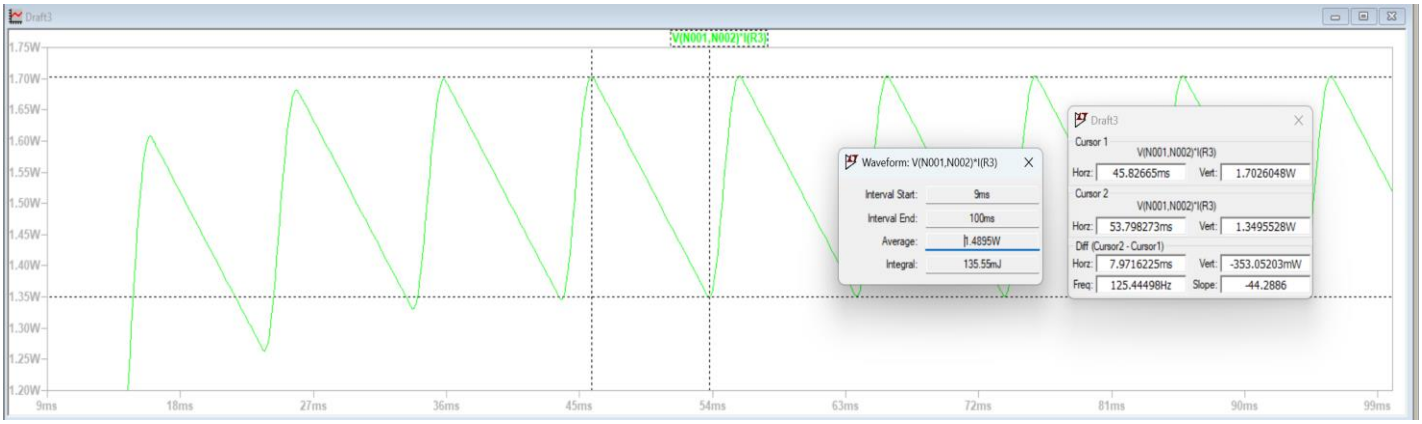
Also, the average power dissipated on the transistor can be determined (first theoretically and then simulated):

$$Pd := VCE \cdot IB \cdot hfe = 1.4851\ \mathrm{W}$$

And the maximum power:

$$VCEmax := Vout\_avg + \frac{\Delta Vout\_rectifier}{2} - Vout\_ser\_reg = 3.5\ \mathrm{V}$$

$$Pdmax := VCEmax \cdot IB \cdot hfe = 1.7327\ \mathrm{W}$$



From simulations it results that the maximum power dissipated on the transistor is 1.7W. From the datasheet of the transistor, we know that the maximum junction temperature is 150°C and the thermal resistance between the junction and the ambient has a maximum value of 100°C/W:

Table 2. Absolute maximum ratings

Symbol	Parameter	Value				Unit
		NPN		PNP		
		BD135	BD139	BD136	BD140	
V_{CBO}	Collector-base voltage (I_E = 0)	45	80	-45	-80	V
V_{CEO}	Collector-emitter voltage (I_B = 0)	45	80	-45	-80	V
V_{EBO}	Emitter-base voltage (I_C = 0)	5		-5		V
I_C	Collector current	1.5		-1.5		A
I_{CM}	Collector peak current	3		-3		A
I_B	Base current	0.5		-0.5		A
P_{TOT}	Total dissipation at $T_c \leq 25$ °C	12.5				W
P_{TOT}	Total dissipation at $T_{amb} \leq 25$ °C	1.25				W
T_{stg}	Storage temperature	-65 to 150				°C
T_j	Max. operating junction temperature	150				°C

Table 3. Thermal data

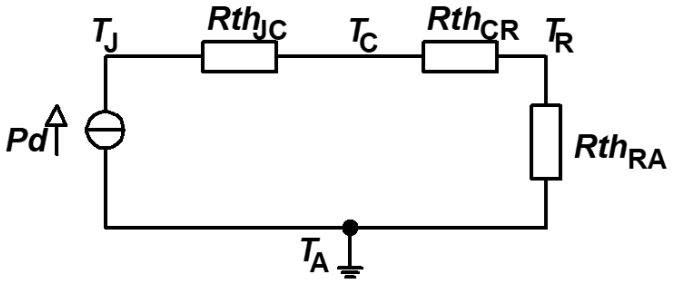
Symbol	Parameter	Max value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	10	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	100	°C/W

If the junction temperature is calculated at the maximum dissipated power of 1.7W (>1.25W specified in the datasheet) and an ambient temperature of 25°C, it results a maximum temperature of 195°C which exceeds the maximum junction temperature from the datasheet (150°C). This is the reason why a heatsink is needed.

$$TJ' := Pdmax \cdot Rth\_JA + TA$$

$$TJ' := 1.7 \cdot 100 + 25 = 195$$

In order not to reach the maximum junction temperature, for the further calculations a maximum desired junction temperature of about 20% less than the nominal maximum temperature has been chosen: 120°C. So, by designing the thermal circuit and writing the equations, the necessary thermal resistance of the heatsink can be determined:



So, by knowing that a maximum power of 1.7W can be dissipated and that the maximum junction temperature is 120°C (and the ambient temperature of 25°C), it results that the thermal resistance between the junction and the ambient is:

$$Pdmax := 1.7\ W$$

$$TJ := 120\ °C$$

$$TA := 25\ °C$$

$$Rth\_JA := \frac{TJ - TA}{Pdmax} = 55.8824\ \frac{K\ S}{A^2}$$

So, Rth_JA is around 55 °C/W (max value):

$$Rth\_JC := 10\ \frac{K}{watt}$$

$$Rth\_CA := Rth\_JA - Rth\_JC = 45.8824\ \frac{K\ S}{A^2}$$

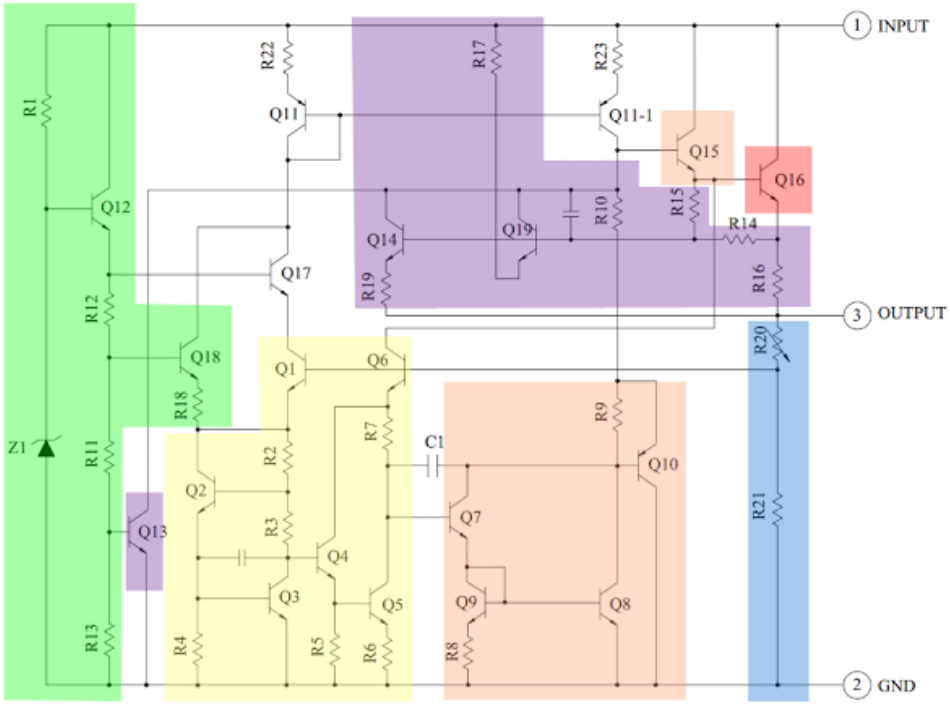
The maximum value of the resistance of the heatsink (case-heatsink and heatsink-ambient) is about 45.8 °C/W. For example, the heatsink **507302B00000G** would be suitable as it has a thermal resistance of 24 °C/W.

The used components in this section:

No.	Part No.	Amount	Price per piece ($)	Total price ($)
1.	**BD135-16**	1	0.82	0.82
2.	**BZX84C13VLY**	1	0.54	0.54
3.	**507302B00000G**	1	0.47	0.47
4.	**RN55D1500FB14**	1	0.55	0.55
TOTAL				2.38

5. Designing the IC regulator

Knowing that for the IC regulator an output voltage of 5V is required and a current of 500mA, the chosen regulator is **LM7805**. The functioning of this regulator is explained below:



Q16 controls the current between input and output and so the output voltage. In yellow there is the bandgap reference which keeps the voltage stable. The error signal from the bandgap reference is fed to Q7 and then (in the orange part) this signal is amplified. The amplified signal controls Q15 which itself controls Q16, so the output transistor, closing a negative feedback loop. The green part represents the start-up circuit, providing an initial current to the bandgap reference. Q13 provides protection from overheating, Q19 from overvoltage from the input and Q14 from overcurrent from output. The voltage divider (blue part) sets the output voltage of the regulator.[1]

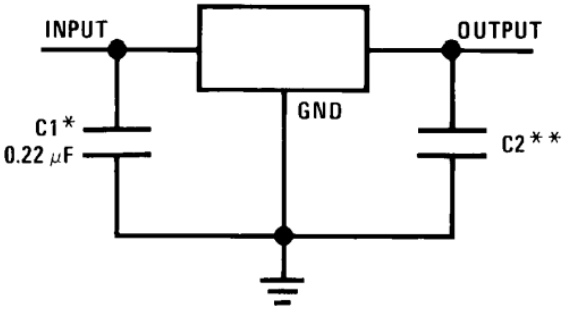
From its datasheet, there is known that the output voltage varies between 4.8V and 5.2V with an input voltage that can be between 7.5V and 20V. Also, the output current can get up to 1A, which makes the regulator suitable for this application.

6.6 LM340 / LM7805 Electrical Characteristics, V_O = 5 V, V_I = 10 V

0°C ≤ T_J ≤ 125°C unless otherwise specified(1)

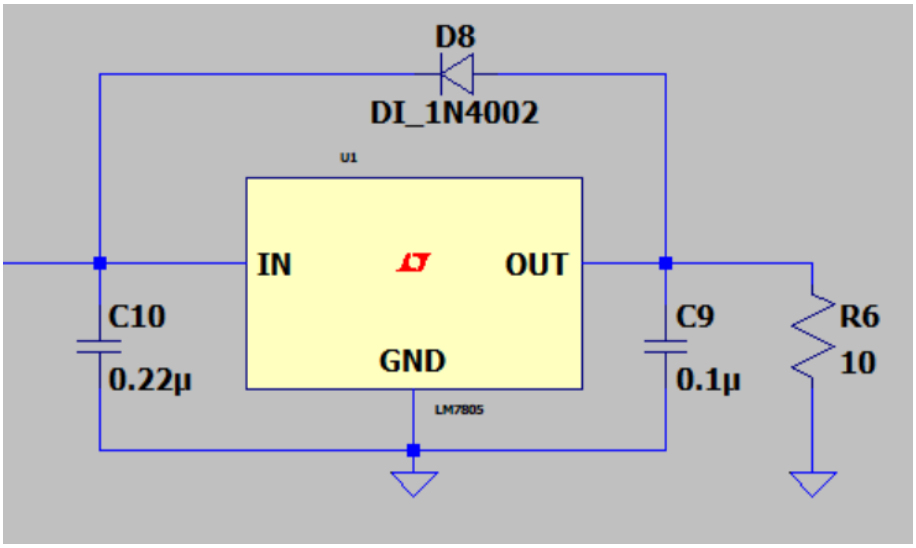
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C, 5 mA ≤ I_O ≤ 1 A		4.8	5	5.2	V
		P_D ≤ 15 W, 5 mA ≤ I_O ≤ 1 A 7.5 V ≤ V_{IN} ≤ 20 V		4.75		5.25	V
ΔV_O	Line regulation	I_O = 500 mA	T_J = 25°C 7V ≤ V_{IN} ≤ 25V		3	50	mV
			Over temperature 8V ≤ V_{IN} ≤ 20V			50	mV
		I_O ≤ 1 A	T_J = 25°C 7.5V ≤ V_{IN} ≤ 20V			50	mV
			Over temperature 8V ≤ V_{IN} ≤ 12V			25	mV
ΔV_O	Load regulation	T_J = 25°C	5 mA ≤ I_O ≤ 1.5 A		10	50	mV
			250 mA ≤ I_O ≤ 750 mA			25	mV
		Over temperature, 5 mA ≤ I_O ≤ 1 A				50	mV
I_Q	Quiescent current	I_O ≤ 1 A	T_J = 25°C			8	mA
			Over temperature			8.5	mA
ΔI_Q	Quiescent current change	0°C ≤ T_J ≤ 125°C, 5 mA ≤ I_O ≤ 1 A			0.5		mA
		7 V ≤ V_{IN} ≤ 20 V	T_J = 25°C, I_O ≤ 1 A			1	mA
			Over temperature, I_O ≤ 500 mA			1	mA
V_N	Output noise voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		µV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple rejection	f = 120 Hz 8 V ≤ V_{IN} ≤ 18 V	T_J = 25°C, I_O ≤ 1 A	62	80		dB
			Over temperature, I_O ≤ 500 mA	62			dB
R_O	Dropout voltage	T_J = 25°C, I_O = 1 A			2		V
	Output resistance	f = 1 kHz			8		mΩ
	Short-circuit current	T_J = 25°C			2.1		A
	Peak output current	T_J = 25°C			2.4		A
	Average TC of V_{OUT}	Over temperature, I_O = 5 mA			−0.6		mV/°C
V_{IN}	Input voltage required to maintain line regulation	T_J = 25°C, I_O ≤ 1 A		7.5			V

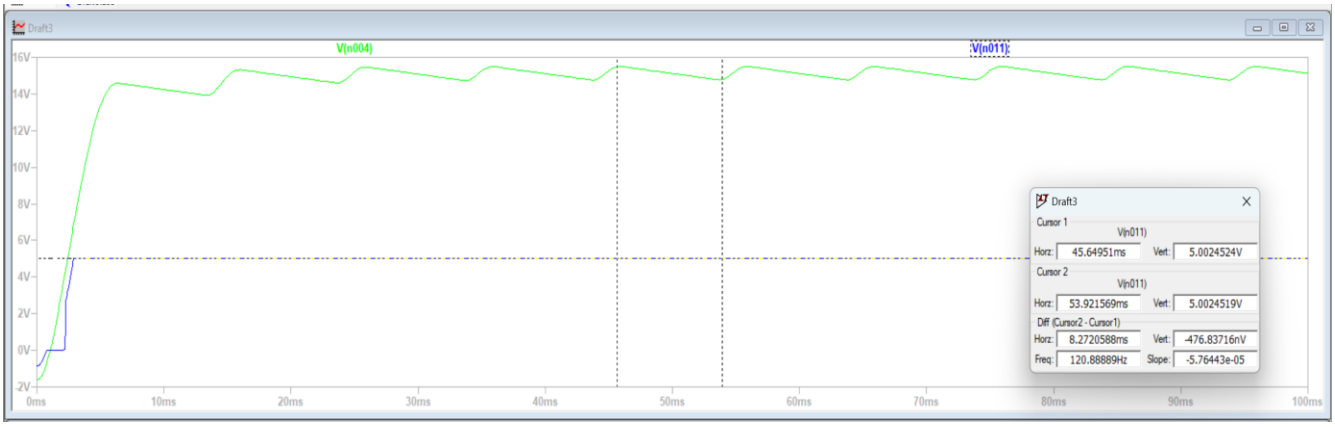
To connect the voltage regulator in the circuit, decoupling capacitors and the input and output are needed. Basically, decoupling capacitors have the role to filter out the noise (high frequency signal and transient signal) that can appear on the line, as they have at the frequency of the noise a very small impedance, thus driving the noisy component of the signal to the ground. The capacitor at the input is required if the regulator is located far away from the filter and the capacitor at the output helps the transient response (reduces rise time/fall time and overshoot).



Moreover, a diode is to be placed between the output and the input of the regulator in order to prevent the reverse biasing of the series pass transistor in case the output voltage goes higher than the input one.

The circuit in the simulator:

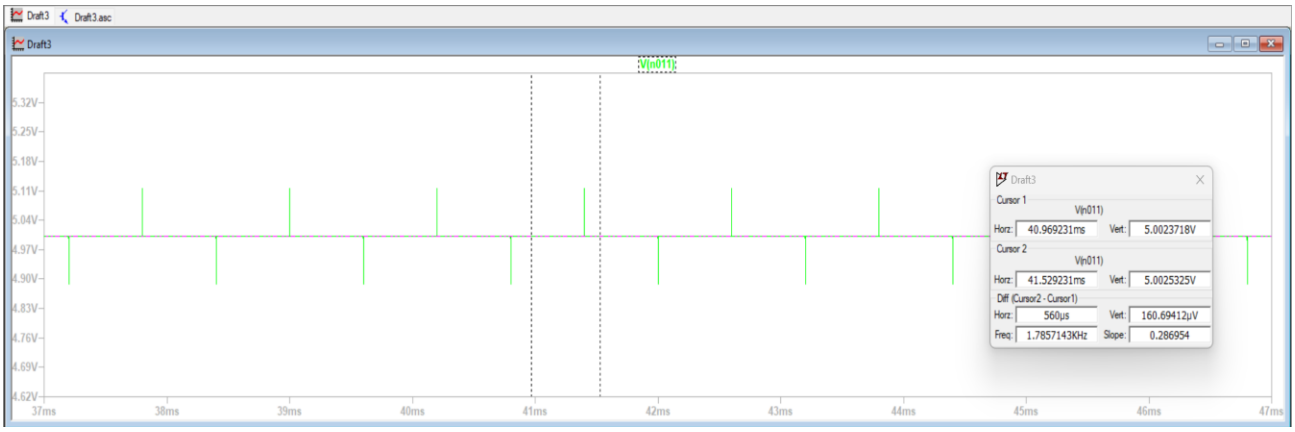




By plotting the input voltage of the regulator and its output voltage, the line regulation can be calculated:

$$Sui\_IC := \frac{\Delta Vout\_rectifier}{5.0024524\ V - 5.0024519\ V} = 2 \cdot 10^{6}$$

Also, by simulating a current source placed at the output as a pulse signal between 400mA and 600mA and measuring the variation of the output voltage, the output resistance can be determined:

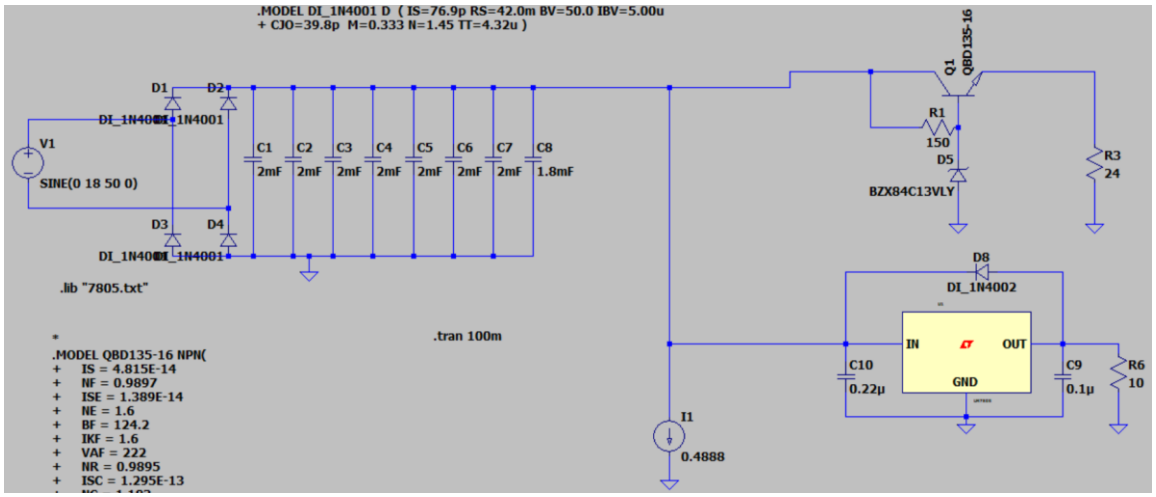


$$Ro\_IC := \frac{5.0025325\ \text{V} - 5.0023718\ \text{V}}{200\ \text{mA}} = 0.0008\ \Omega$$

The power dissipated on the IC is about 5W (less than the maximum dissipated power specified in the datasheet of 15W):

$$P\_IC := (Vout\_avg - Vout\_IC\_reg) \cdot Iout\_IC\_reg = 5\ \text{W}$$

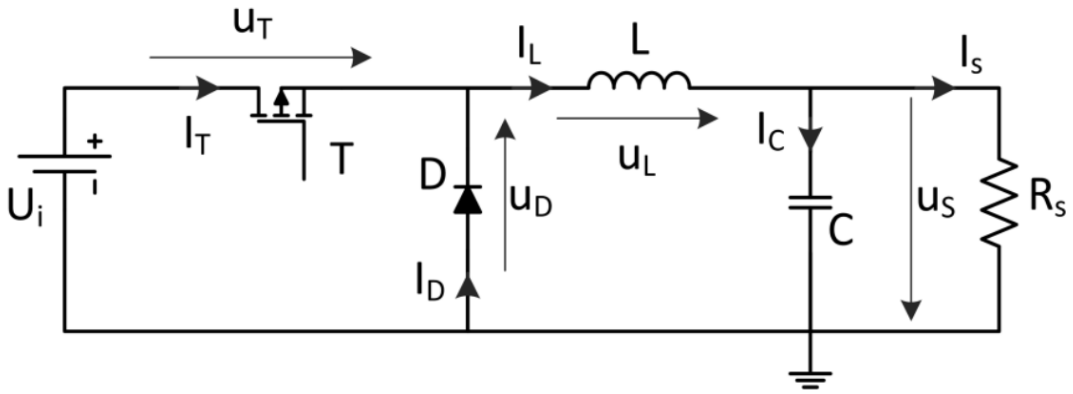
The whole circuit so far:



The components used in this section are:

No.	Part No.	Amount	Price per piece ($)	Total price ($)
1.	**LM7805MP/NOPB**	1	1.73	1.73
2.	**GRM188R71E224KA88D** (voltage rating: 25V)	1	0.1	0.1
3.	**KGM05AR51A104KH** (voltage rating: 10V)	1	0.1	0.1
4.	**1N4002**	1	0.16	0.16
TOTAL				2.38

6. Designing the Buck converter (DC-DC step-down converter)



For the Buck converter there are two modes of conduction: continuous conduction mode (for which the minimum current through the inductor doesn't reach 0) and discontinuous conduction mode (for which IL reaches 0). Moreover, the charging and discharging of the inductor is controlled by the transistor that is itself controlled by a PWM signal. When the transistor is on, the diode turns off and the current though the inductor rises (the voltage drop across L is Ui-Us) and when the transistor is off, the diode turns on, ensuring a path for the current from the inductor to close so that this current will decrease (voltage drop across L will be -Us). Also, there are some starting points to be considered before starting to design the circuit: the average voltage on the inductor is 0 and the average current through the capacitor is 0. (in steady state, the current through the inductor has the same value at the beginning and at the end of the period T. The same applies for the voltage on the capacitor):

$$uL = L * \frac{d\,iL}{d\,t} \qquad iC = C * \frac{d\,uC}{d\,t}$$

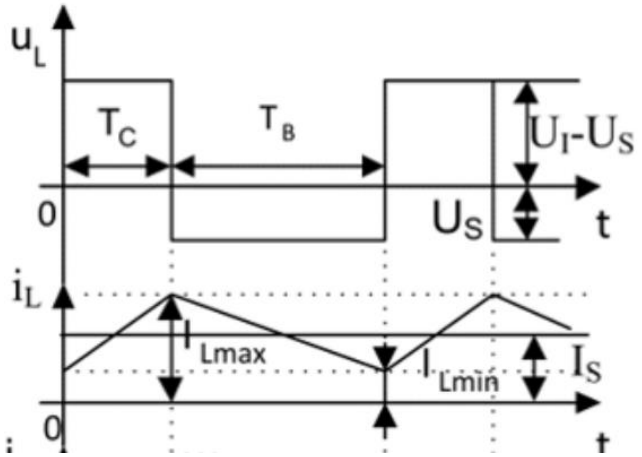
$$\Delta iL = \frac{1}{L} * \int_0^T uL(t)dt \qquad \Delta uC = \frac{1}{C} * \int_0^T iC(t)dt$$

$$IL(T) - IL(0) = \frac{1}{L} * \int_0^T uL(t)dt \qquad UC(T) - UC(0) = \frac{1}{C} * \int_0^T iC(t)dt$$

$$0 = \frac{1}{L} * \int_0^T uL(t)dt \qquad 0 = \frac{1}{C} * \int_0^T iC(t)dt$$

$$0 = \frac{1}{T} * \int_0^T uL(t)dt \qquad 0 = \frac{1}{T} * \int_0^T iC(t)dt$$

Consequently, the average current though the inductor (IL) is equal to the output average current (IS).



The waveforms from above refer to the CCM (continuous conduction mode). One can write:

$$(UI - US) * tc = US * tb$$

$$\delta = \frac{tc}{T} = \frac{US}{UI} \ (duty\ cycle)$$

And:

$$\left(\frac{ILmax + ILmin}{2} * tc + \frac{ILmax + ILmin}{2} * tb\right) * \frac{1}{T} = IL = IS$$

$$ILmax + ILmin = 2 * IS$$

According to the linearization of the equation of the voltage on the inductor:

$$ILmax - ILmin = \frac{UI - US}{L} * tc = \Delta IL$$

So:

$$ILmax = IS + \frac{\Delta IL}{2}$$

$$ILmin = IS - \frac{\Delta IL}{2}$$

There is a value for IL, called limit load current (ISL), which is calculated for ILmin=0. So:

$$ISL = \frac{\Delta IL}{2} = \frac{UI - US}{2 * L} * tc$$

Coming back to the circuit that needs to be designed. The input voltage ripple is 1V and its average value is 15V and the efficiency for the Buck converter is 90%. Thus, the maximum and minimum input and output power, as well as the minimum and maximum output current can be determined:

$$Vin\_max\_Buck := Vout\_avg + \Delta Vout\_rectifier = 16\ V$$

$$Vin\_min\_Buck := (Vout\_avg - \Delta Vout\_rectifier) = 14\ V$$

$$Pin\_max := Vin\_max\_Buck \cdot Iin\_Buck = 7.8222\ W$$

$$Pin\_min := Vin\_min\_Buck \cdot Iin\_Buck = 6.8444\ W$$

$$Pout\_max := \eta\_Buck \cdot Pin\_max = 7.04\ W$$

$$Pout\_min := \eta\_Buck \cdot Pin\_min = 6.16\ W$$

$$IS\_max := \frac{Pout\_max}{Vout\_Buck} = 2.1333\ A$$

$$IS\_min := \frac{Pout\_min}{Vout\_Buck} = 1.8667\ A$$

$$ISL := IS\_min$$

The maximum value of ISL is when the input voltage is maximum (UImax) and the duty cycle minimum. Also, for considering more losses in the circuit, the voltage on the Schottky diode and the voltage on the inductor will be taken into account when using Us in the calculations:

$$V\_Diode := 0.5\ V$$

$$V\_ind := 0.2\ V$$

$$US := Vout\_Buck + V\_Diode + V\_ind = 4\ V$$

Taking the period of the PWM signal that commands the transistor T=50µs and calculating the minimum value of the duty cycle, the minimum value of the inductor can be calculated (by expressing L from the ISL formula from above):

$$T\_Buck := 50\ \mu s$$

$$\delta min := \frac{US}{Vin\_max\_Buck} = 0.25$$

$$Lmin := \frac{Vin\_max\_Buck \cdot \left(1 - \frac{US}{Vin\_max\_Buck}\right) \cdot \delta min \cdot T\_Buck}{2 \cdot ISL} = 4.0179 \cdot 10^{-5}\ H$$

Knowing the value of the inductor, the minimum and maximum current through it can be calculated:

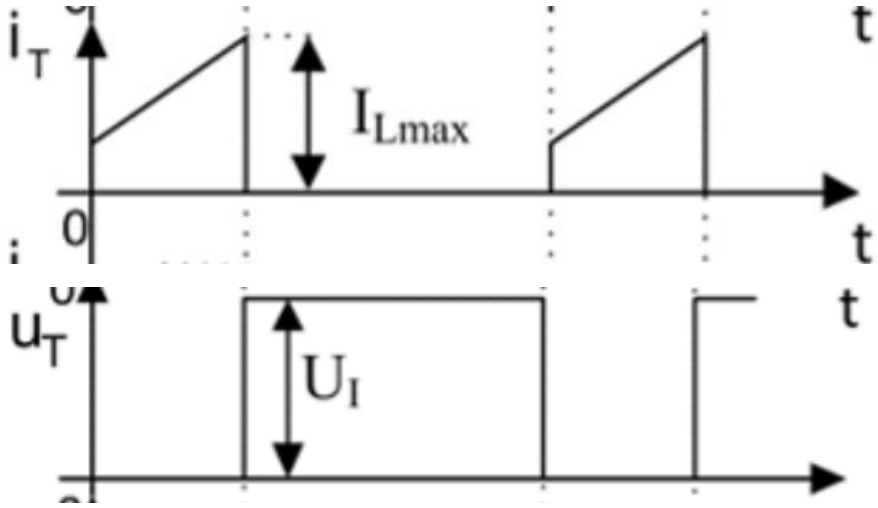
$$\Delta IL := \frac{Vin\_max\_Buck - US}{Lmin} \cdot \delta min \cdot T\_Buck = 3.7333\ A$$

$$ILmax := IS\_max + \frac{\Delta IL}{2} = 4\ A$$

$$ILmin := \left(IS\_max - \frac{\Delta IL}{2}\right) = 0.2667\ A$$

Consequently, a suitable inductor would be **PA2729.443NL**, as it has an inductance of 44µH and a maximum saturation current of 7.3A (< ILmax).

To choose the transistor, the following parameters need to be taken into consideration: maximum current through the transistor and the maximum voltage at blocking (knowing that when the transistor conducts, the current through the inductor rises):



$$ITmax := ILmax = 4\ A$$

$$UTmax := Vin\_max\_Buck = 16\ V$$

The chosen transistor is **BSC093N04LS**. It has maximum VDS voltage of 40V, a maximum drain current of 13A, a maximum VGS voltage of 20V and an RDSon of 9mΩ.

Next, the losses (conduction loss, switching loss and gate loss) will be calculated to decide if a heatsink is needed or not. From datasheet, the maximum dissipated power is known to be 2.5W, so the sum of the 3 types of powers will be calculated to see if this is below the maximum value.

First, the conduction losses:

$$Rds\_on\_max := 9.3\ mohm \qquad \delta max := \frac{US}{Vin\_max\_Buck} = 0.25$$

$$Pcond := Rds\_on\_max \cdot IS\_max \cdot IS\_max \cdot \delta max = 0.0106\ W$$

conduction losses

$Coss := 400 \cdot 10^{-12}\ F$ output capacitance

$Q\_g\_tot := 17 \cdot 10^{-9}\ C$ total Gate charge

$Q\_gd := 2 \cdot 10^{-9}\ C$ Miller Gate-Drain charge

$Q\_gs := 4.9\ nC$ Gate-Source Charge

$VGS\_th := 1.5\ V$ Gate-Source Threshold voltage

$Vdr := 33\ V$ command voltage

$Idr := 44\ mA$ command current

$$Rdron := \frac{Vdr}{Idr} = 750\ \Omega$$

$$Rdroff := Rdron = 750\ \Omega$$

$$Idriver\_LH := \frac{Vdr - VGS\_th}{Rdron} = 0.042\ A$$

$$Idriver\_HL := \frac{Vdr - VGS\_th}{Rdroff} = 0.042\ A$$

$$QGS\_sw := Q\_gd + \frac{Q\_gs}{2} = 4.45 \cdot 10^{-9}\ C$$

$$tswLH := \frac{QGS\_sw}{Idriver\_LH} = 1.0595 \cdot 10^{-7}\ s$$

$$tswHL := \frac{QGS\_sw}{Idriver\_HL} = 1.0595 \cdot 10^{-7}\ s$$

$$Psw\_max := Vin\_min\_Buck \cdot IS\_max \cdot \frac{1}{\frac{T\_Buck}{2}} \cdot (tswHL + tswLH) + \frac{Coss \cdot Vin\_min\_Buck^{2} \cdot \frac{1}{\frac{T\_Buck}{2}}}{2} = 0.2547\ W$$

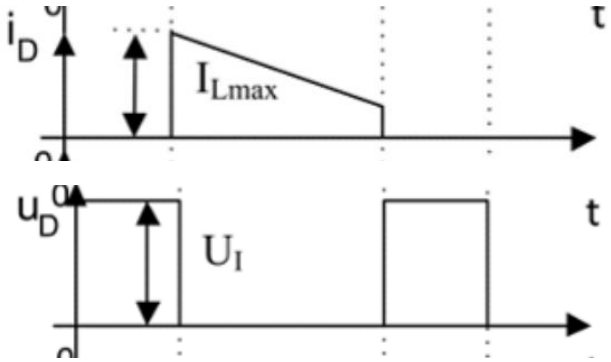
$$IGate\_avg := Q\_g\_tot \cdot \frac{1}{T\_Buck} = 0.0003\ A$$

$$Pgate := IGate\_avg \cdot Vdr = 0.0112\ W$$

$Ptot := Pcond + Psw\_max + Pgate = 0.2765\ W$ total losses

So, the total dissipated power is less than the maximum one specified in the datasheet. Consequently, a heatsink is not needed.

For the diode, the maximum current though it is the maximum current through the inductor, the maximum reverse voltage is Uimax and the average current is calculated from the area of the ID curve:



$IDmax := ILmax = 4\ A$

$UDmax := UTmax = 16\ V$

$IDavg := IS\_max \cdot (1 - \delta min) = 1.6\ A$

A suitable diode is the Schottky **B530C**, having an average maximum current of 5A and a maximum reverse voltage of 30V (and a forward voltage of 550mV). These types of diodes have very small reverse recovery times at switching and that is why they are preferred to be used in switching applications. Next, the junction temperature will be calculated in order to decide if a heatsink is necessary or not:

$VF\_max := 0.55\ V$ max forward voltage

$rd := 110\ mohm$ on resistance

$PD\_max := IS\_max \cdot VF\_max \cdot (1 - \delta min) + rd \cdot IS\_max^{2} \cdot (1 - \delta min) = 1.2555\ W$ dissipated power

$PD\_m := 1.255$

$Rth\_JA := 50$ junction-ambiant thermal resistance

$TJ\_max := 150$ max junction temperature

$TA := 25$ ambient temperature

$TJ := (PD\_m \cdot Rth\_JA + TA) = 87.75$ junction temperature

There can be seen that the junction temperature doesn't exceed the maximum junction temperature specified in the datasheet, so no heatsink is needed.

To calculate the value of the capacitor, the amount of charge accumulated in it needs to be determined as the area of the between the average value (IS) and the maximum current through the inductor (ILmax). And then, the capacitance can be calculated from the formula $C = \frac{\Delta Q}{\Delta UC}$:

$$\delta := \frac{US}{Vin\_Buck} = 0.2667$$

$$\Delta UC := 0.05\ \text{V}$$

$$\Delta Q\_C := \frac{Vin\_Buck \cdot \left(1 - \frac{US}{Vin\_Buck}\right) \cdot \delta \cdot T\_Buck \cdot T\_Buck}{8 \cdot Lmin} = 2.2815 \cdot 10^{-5}\ \text{C}$$

$$C\_Buck := \frac{\Delta Q\_C}{\Delta UC} = 0.0005\ \text{F}$$

If also the transient regime is to be analyzed, the response time can be calculated:

$$tr := -\frac{(IS\_max - IS\_min) \cdot Lmin}{US \cdot \left(\frac{\delta min}{\delta} - 1\right)} = 4.2857 \cdot 10^{-5}\ \text{s}$$

Also taking the maximum variation of the US voltage in transient regime (UStrmax) and the equivalent series resistance of the capacitor (Rc - calculated considering that the equivalent series resistance causes 75% of the voltage ripple), one can determine the range of values for the capacitance:

$$UStrmax := 0.1\ \text{V}$$

$$Rc := \frac{0.75 \cdot \Delta UC}{\Delta IL} = 0.01\ \Omega$$

$$Cmax := \frac{tr}{Rc} = 0.0043\ \text{F}$$

$$Cmin := \frac{(IS\_max - IS\_min) \cdot tr}{2 \cdot UStrmax - (IS\_max - IS\_min) \cdot Rc} = 5.7919 \cdot 10^{-5}\ \text{F}$$

Also, for choosing the capacitance, the RMS value of the current is important:

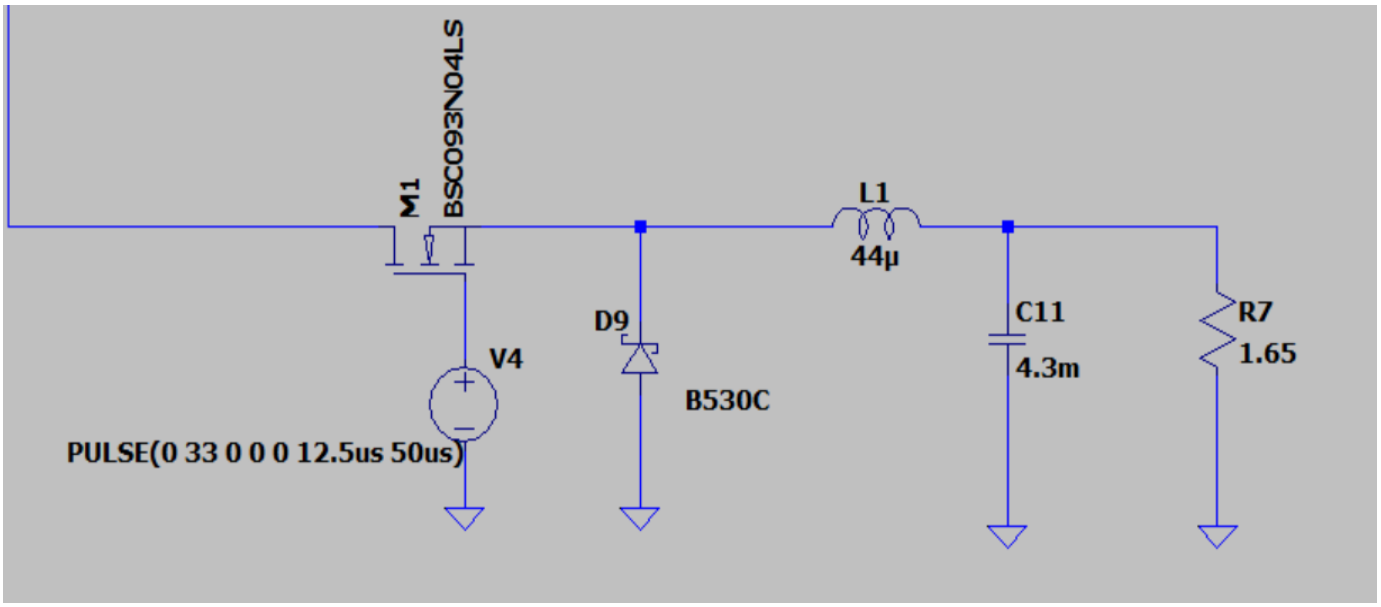
$$IC\_RMS := \frac{ISL}{\sqrt{3}} = 1.0777\ A$$

A capacitance of 4.3mF was chosen to reduce the ripple as more as possible. **EEE-FK1C432SM** is an electrolytic capacitor, having a maximum voltage rating of 16V and an RMS current of 1.35A.

$$C\_Buck\_chosen := 4.3\ mF$$

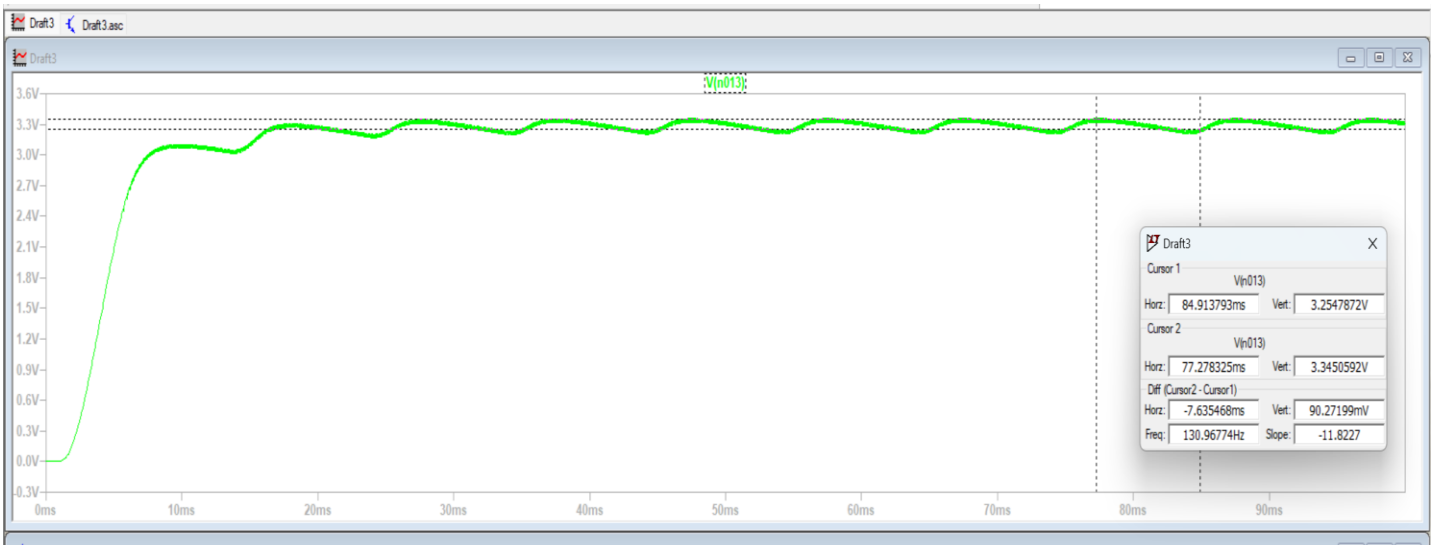
$$L\_chosen := 44 \cdot 10^{-6}\ H$$

The circuit with the components:

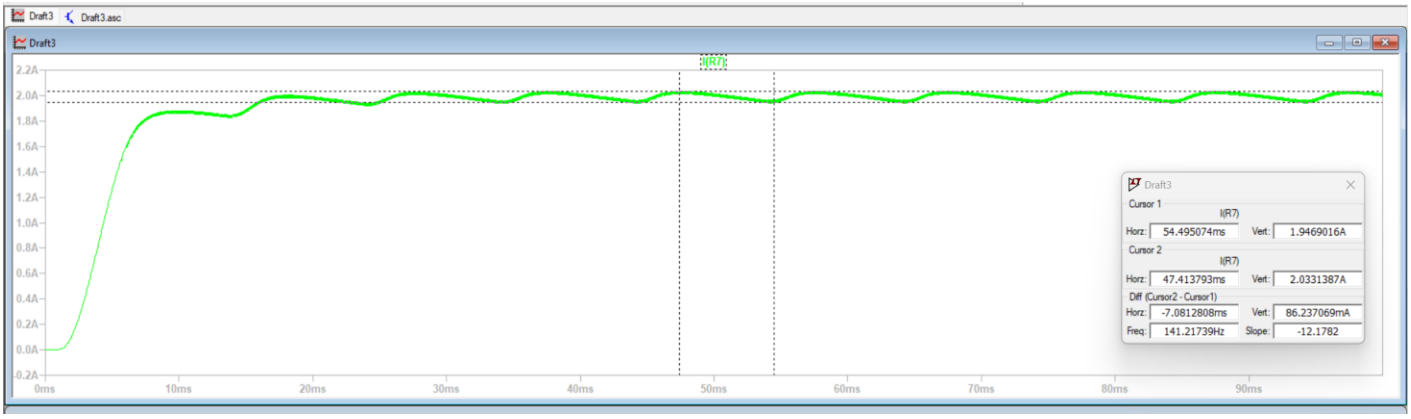


The MOS transistor will be turned off and on by a rectangular voltage source with the duty cycle of 0.25. Next, simulations are done.

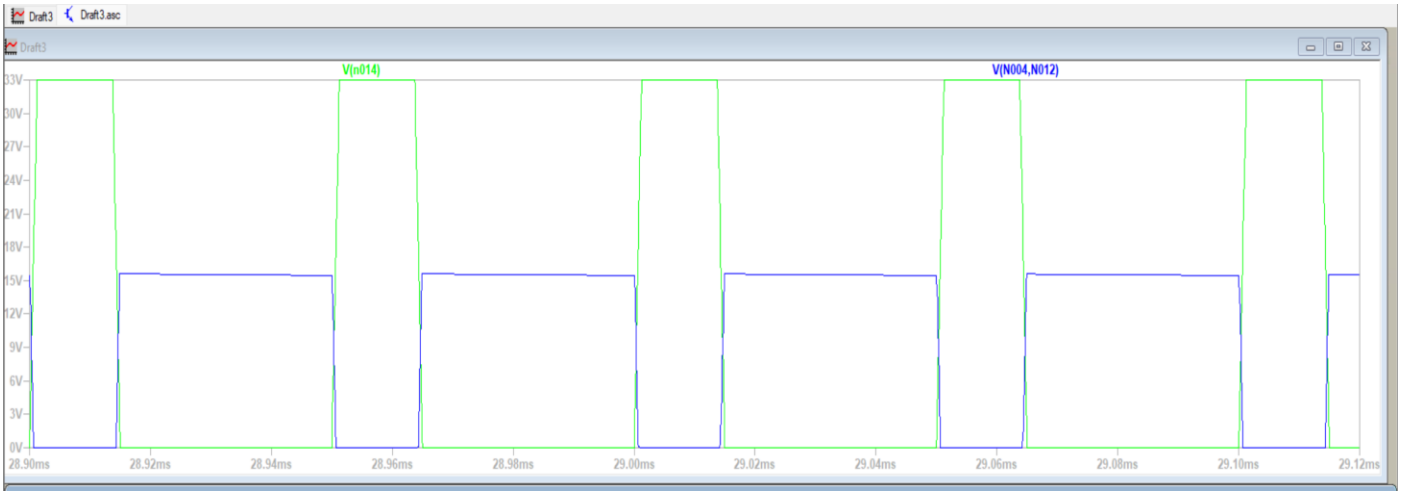
The output voltage varies between 3.25V and 3.34V:



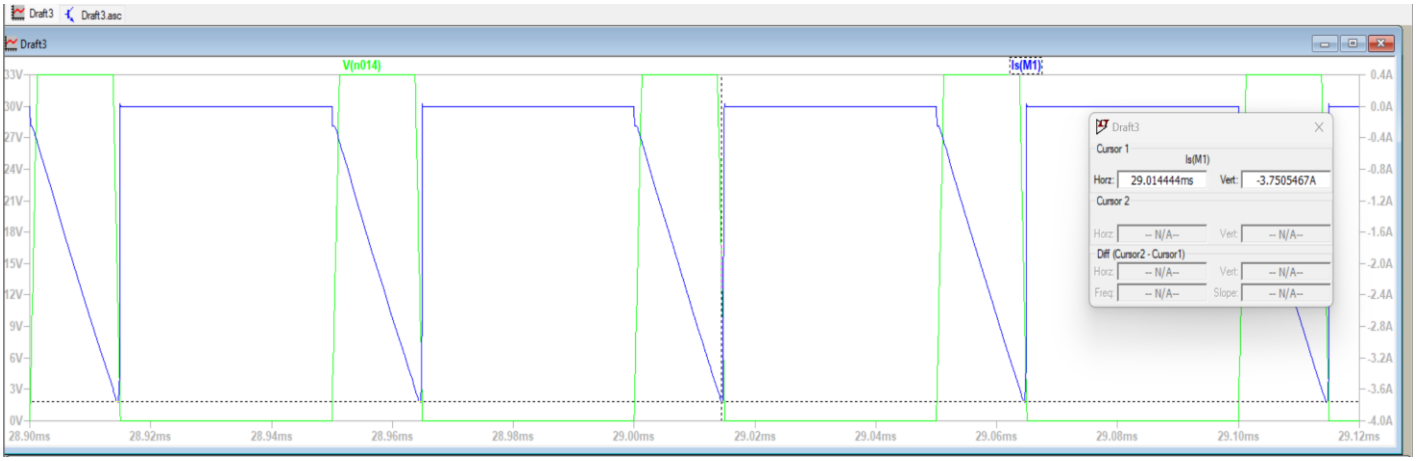
The output current varies between 1.94A and 2.03A:



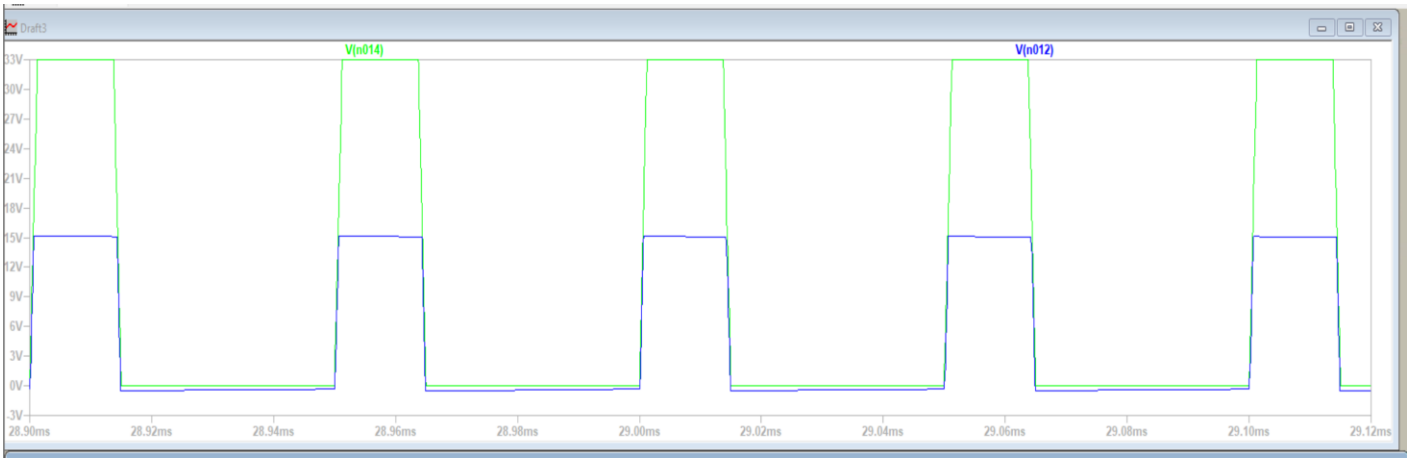
The voltage on the transistor (blue) has its maximum at 15V. In green: the PWM voltage.



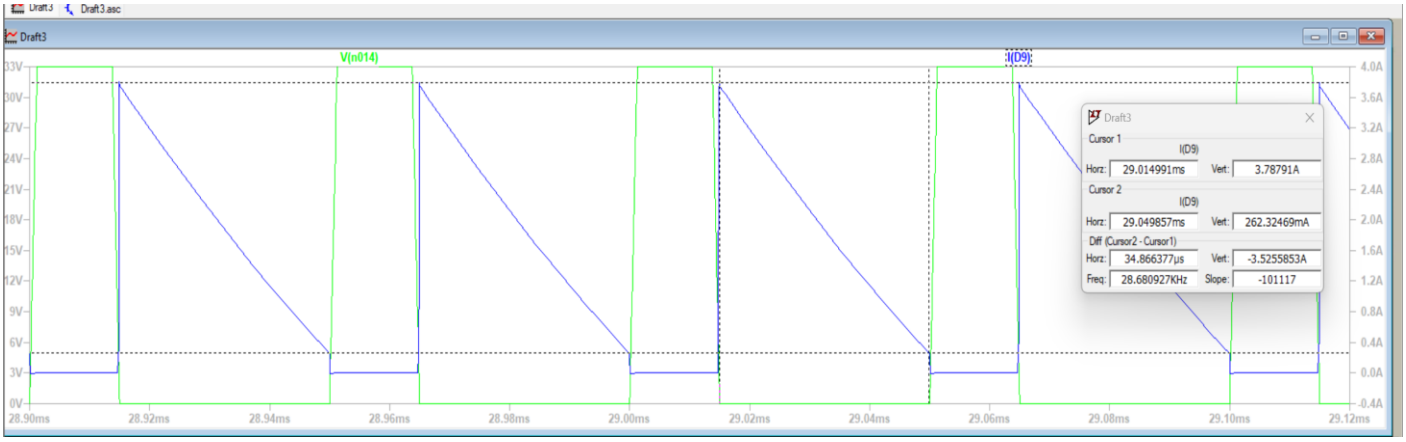
The current through the transistor (blue), max at 3.75A:



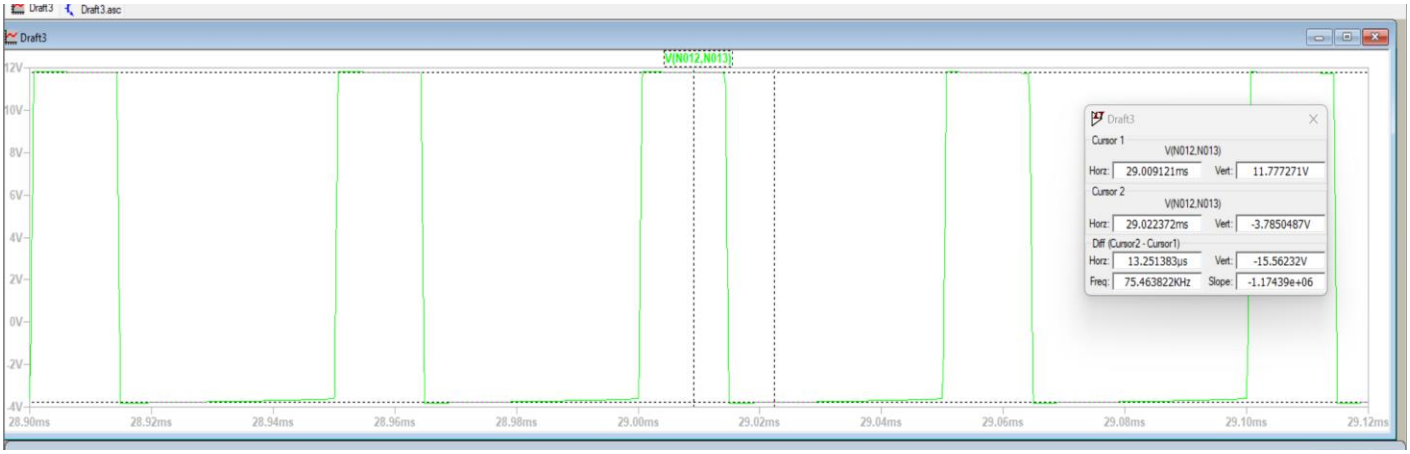
The voltage on the diode (blue), max 15V when the transistor is on:



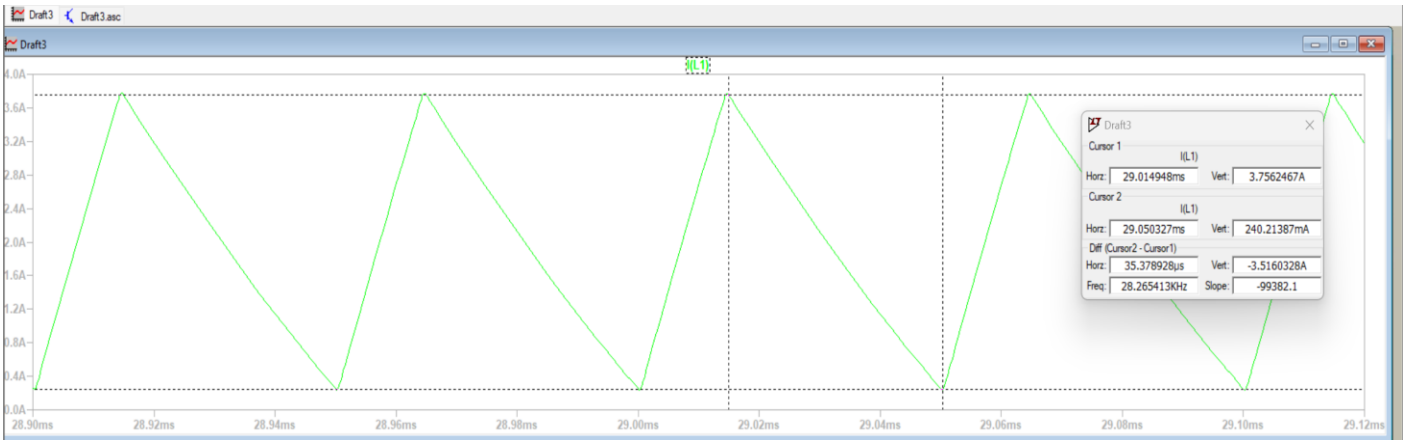
The current through the diode (blue); diode on when the transistor is off. There can be seen also the value ILmax, 3.78A (which is also IDiode max) and the value, ILmin, 262.32mA:



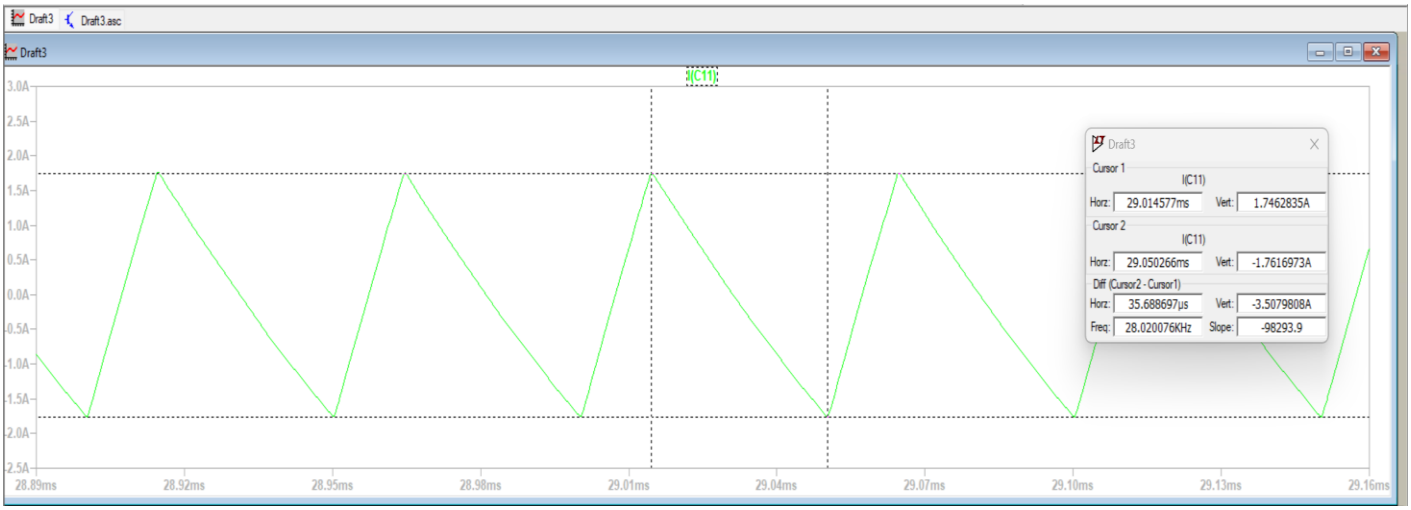
The voltage on the inductor (same shape and limits as expected in theoretical part):



The current through the inductor (with ILmax=3.76A and ILmin=240mA):



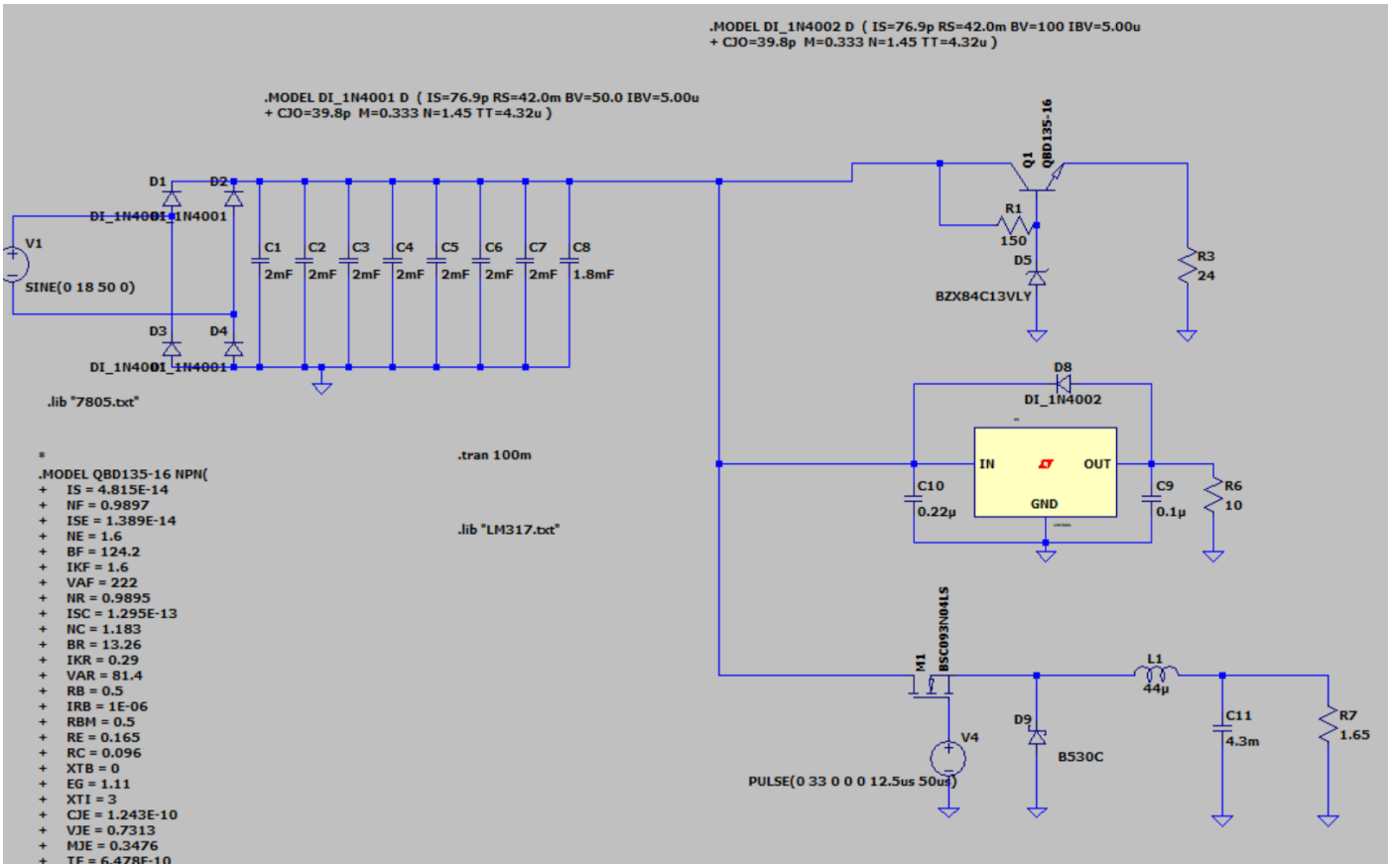
The current through the capacitor (having a peak-to-peak amplitude equal to ΔIL=3.6A)



The components used in this section:

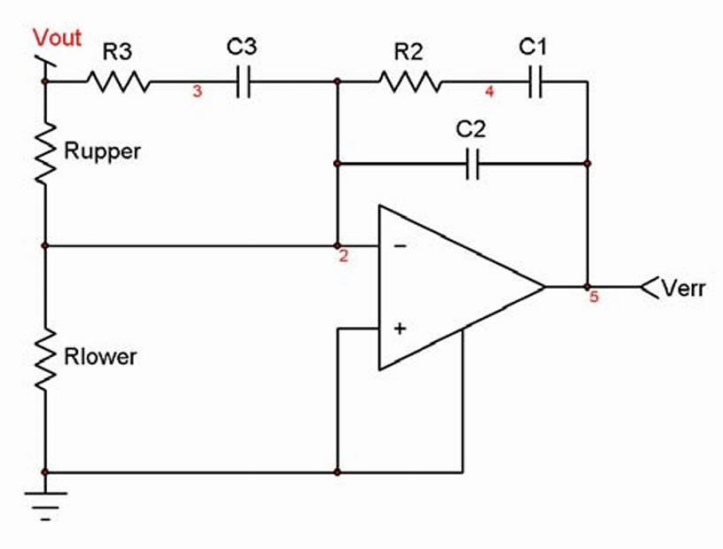
No.	Part No.	Amount	Price per piece ($)	Total price ($)
1.	**PA2729.443NL**	1	3.14	3.14
2.	**BSC093N04LS**	1	0.85	0.85
3.	**B530C**	1	0.55	0.55
4.	**EEE-FK1C432SM**	1	0.7	0.7
TOTAL				5.24

The whole circuit:



6.1. Designing the feedback loop

To maintain the voltage at the output to the desired value of 3.3V, a feedback loop is necessary. This loop has the below topology (practically, a PID controller with a LPF):



To properly size the components, the following steps need to be done.

First, the maximum and minimum load is calculated:

$$Ro1H := \frac{Vout\_Buck}{IS\_min} = 1.7679\ \Omega$$

$$Ro1L := \frac{Vout\_Buck}{IS\_max} = 1.5469\ \Omega$$

Next, calculate the frequency of the pole and of the zero of the power stage:

$$fph := \frac{1}{2 \cdot \pi \cdot \sqrt{L\_chosen \cdot C\_Buck\_chosen}} = 365.8976\ Hz$$

$$fz := \frac{1}{2 \cdot \pi \cdot Rc \cdot C\_Buck\_chosen} = 3684.8276\ Hz$$

The DC gain is determined (considering Vs=5V):

$$Kpwr := \frac{Vin\_max\_Buck}{Vs} = 3.2$$

The cut-off frequency:

$$fc := \frac{\frac{1}{T\_Buck}}{5} = 4000\ \text{Hz}$$

The quality factor at maximum load:

$$Q := \frac{Ro1H}{2 \cdot \pi \cdot fph \cdot L\_chosen} = 17.4765$$

And the angular frequency at the cut-off frequency:

$$w\_fc := 2 \cdot \pi \cdot fc = 25132.7412\ \text{Hz}$$

So, the transfer function of the power stage can be written (w is taken w_fc, because afterwards the module and phase at the cut-off frequency are calculated):

$$H\_PWRH := Kpwr \cdot \frac{1 + \frac{i \cdot w\_fc}{2 \cdot \pi \cdot fz}}{1 + \frac{i \cdot w\_fc}{2 \cdot \pi \cdot fph} \cdot \frac{1}{Q} + \left(\frac{i \cdot w\_fc}{2 \cdot \pi \cdot fph} \right)^2}$$

The module and the phase can be determined from this transfer function:

$$H\_PWRH\_module := \left| H\_PWRH \right| = 0.0399$$

$$\varphi\_PWRH\_phase := \frac{180}{\pi} \cdot \arg\left(H\_PWRH \right) = -132.3491$$

R2 resistance is taken 10kΩ and the desired phase margin 45° (for the error amplifier):

$$R2 := 10 \cdot 10^3\ \Omega$$

$$M := 45$$

So, the phase margin for the whole system (power stage + feedback) is (has to be at least 70° for stability):

$$Boost := M - \varphi\_PWRH\_phase - 90 = 87.3491$$

The gain for the error amplifier:

$$Hr\_gain := \frac{1}{H\_PWRH\_module} = 25.0923$$

The Kv factor and all the components sized:

$$Kv := \left(\tan\left(\frac{Boost \cdot \pi}{4 \cdot 180} + \frac{45 \cdot \pi}{180}\right)\right)^2 = 5.4633$$

$$C4 := \frac{1}{2 \cdot \pi \cdot fc \cdot Hr\_gain \cdot R2} = 1.5857 \cdot 10^{-10}\ \text{F}$$

$$C3 := C4 \cdot (Kv - 1) = 7.0774 \cdot 10^{-10}\ \text{F}$$

$$R5 := \frac{\sqrt{Kv}}{2 \cdot \pi \cdot fc \cdot C3} = 1.314 \cdot 10^{5}\ \Omega$$

$$R3 := \frac{R2}{Kv - 1} = 2240.4902\ \Omega$$

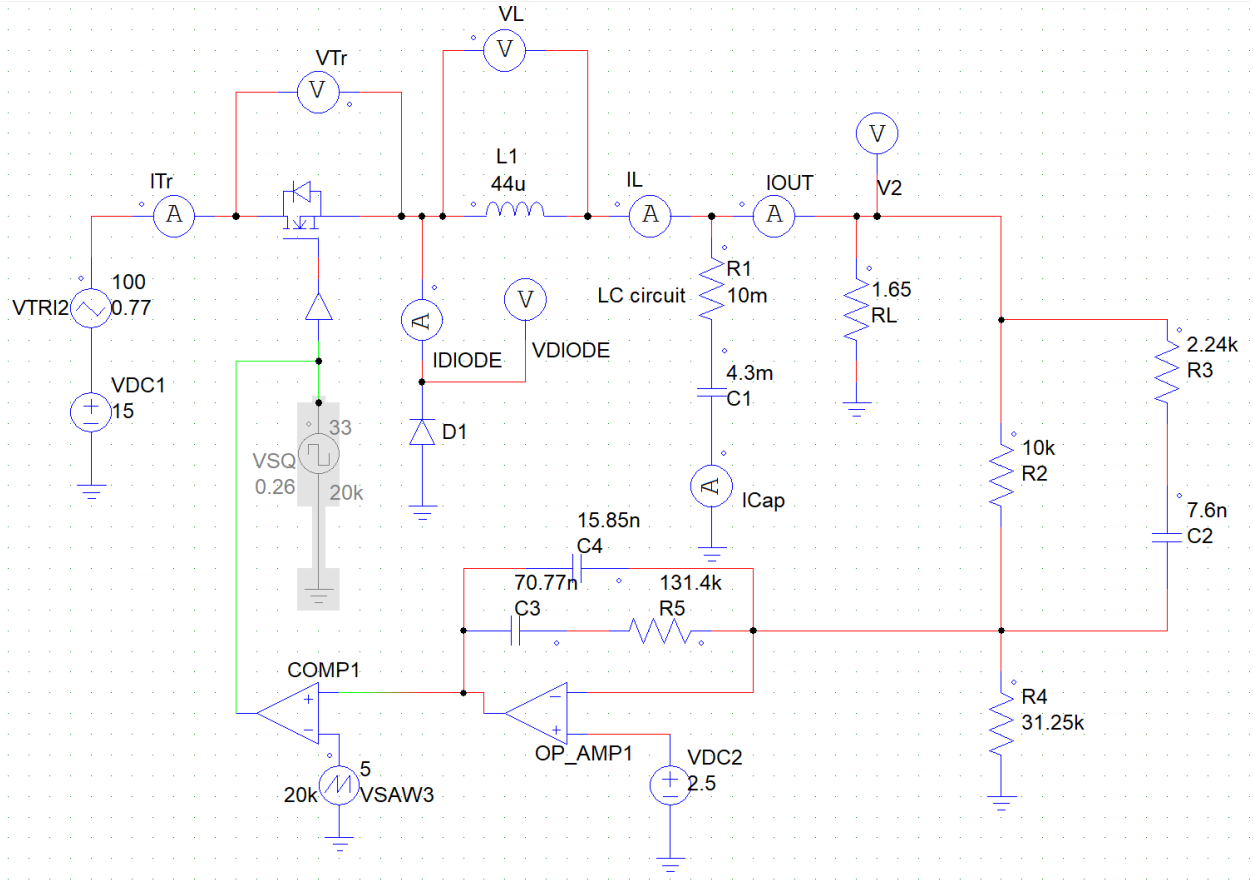
$$C2 := \frac{1}{2 \cdot \pi \cdot fc \cdot \sqrt{Kv} \cdot R3} = 7.5978 \cdot 10^{-9}\ \text{F}$$

And, the transfer function of the whole system and the module:

$$Hr\_fc := \frac{1 + i \cdot w\_fc \cdot C3 \cdot R5}{i \cdot w\_fc \cdot R2 \cdot (C3 + C4)} \cdot \frac{1 + i \cdot w\_fc \cdot C2 \cdot (R2 + R3)}{(1 + i \cdot w\_fc \cdot C2 \cdot R3) \cdot \left(1 + i \cdot w\_fc \cdot R5 \cdot C4 \cdot \frac{C3}{C4 + C3}\right)}$$

$$Hr\_fc\_module := |Hr\_fc| = 25.0923$$

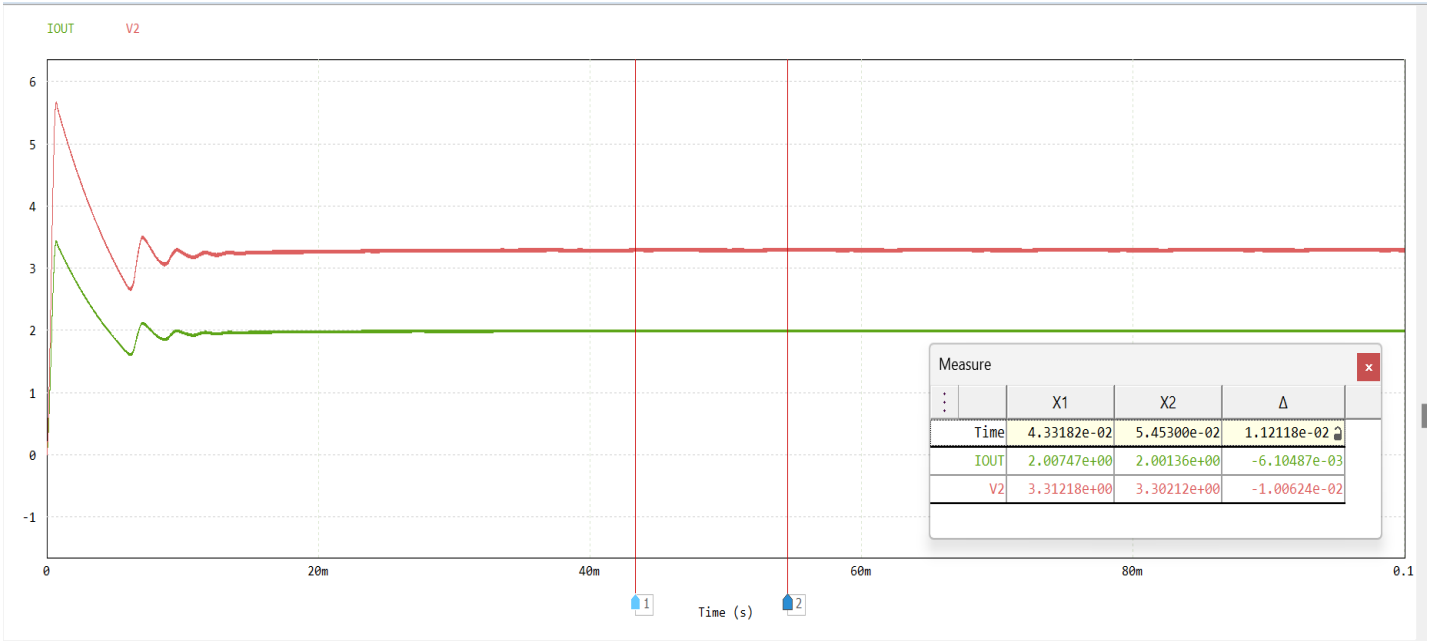
The whole circuit (in PSIM):



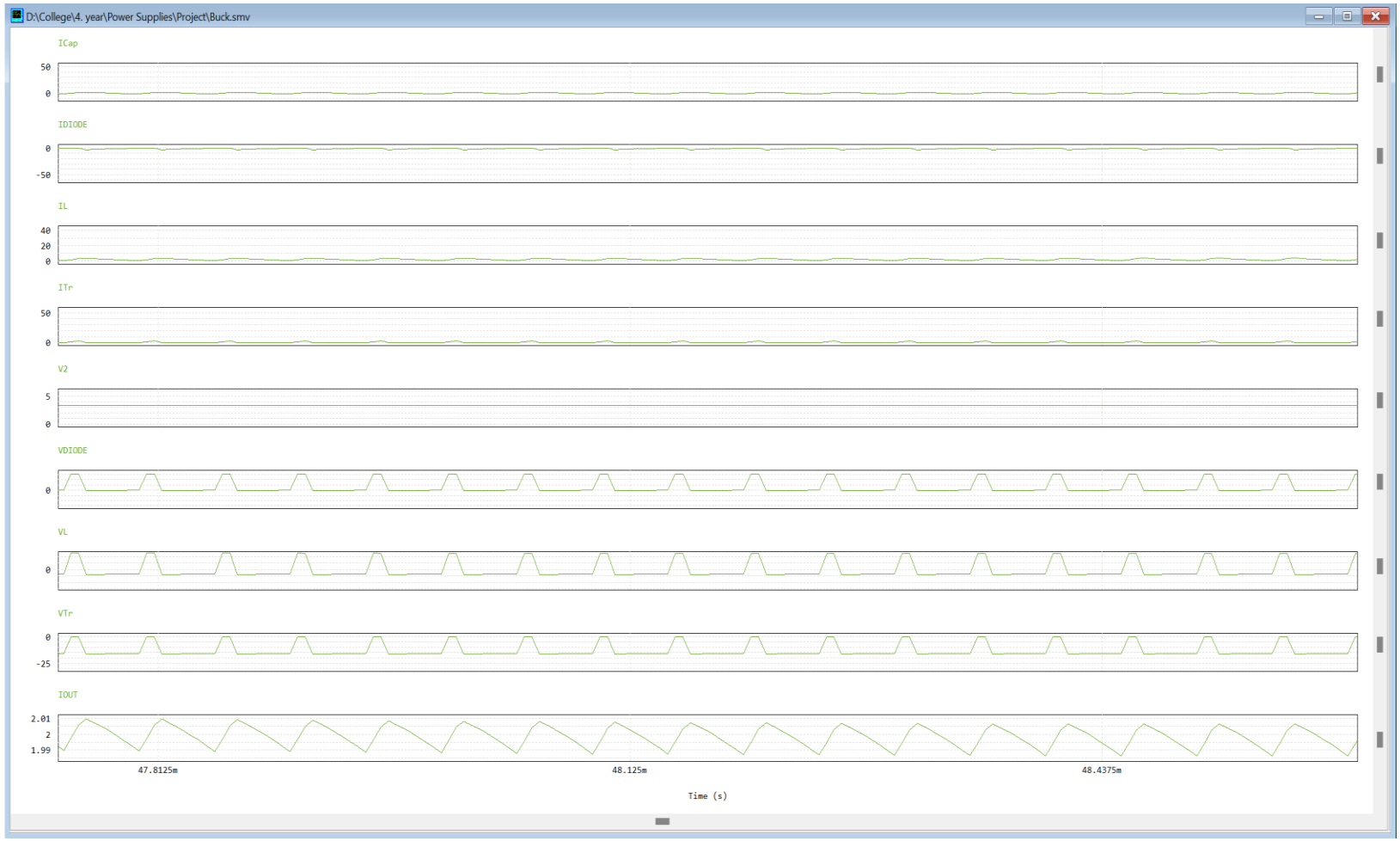
R4 is calculated in order to have at the output 3.3V (practically, on R4 there is a voltage drop of 2.5V because of the amplifier which pushes its inverting input at the same potential as the noninverting one). A voltage divider is created (in DC because the operating point of the circuit needs to be set) between R2 and R4:

$$R4\_Buck := \frac{10\ \text{kohm} \cdot \frac{2.5}{3.3}}{1 - \frac{2.5}{3.3}} = 31250\ \Omega$$

The error signal is then fed to a comparator that has at the inverting input a sawtooth signal. Practically, a PWM generator is created. Through the error signal that comes as a response from analyzing the output voltage and is then compared to a sawtooth signal, the duty-cycle of the signal that switches the transistor between the on and off state is varied in such a way that at the output a constant voltage of 3.3V is obtained:



And, all the voltages and currents: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47.8125m
48.125m
48.4375m
Time (s)

7. References

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2. Power Supplies courses