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		APPLICABLE DIVISION ■Mobile LCD DIVISION I

SPECIFICATION

DEVICE SPECIFICATION
for TFT LCD Module Model No.

LS022Q8UX07

SHARP	SPEC No. MB1-2C104-017	MODEL No. LS022Q8UX07	

RECORDS OF REVISION

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[For handling and system design]

(1) Do not scratch the surface of the polarizer film as it is easily damaged.

(2) If the cleaning of the surface of the LCD panel is necessary, wipe it swiftly with cotton or other soft cloth. Do not use organic solvent as it damages polarizer.

(3) Water droplets on polarizer must be wiped off immediately as they may cause color changes, or other defects if remained for a long time.

(4) Since this LCD panel is made of thin glass, dropping the module or banging it against hard objects may cause cracks or fragmentation

(5) Certain materials such as epoxy resin (amine's hardener) or silicone adhesive agent (de-alcohol or de-oxym) emits gas to which polarizer reacts (color change). Check carefully that gas from materials used in system housing or packaging do not hart polarizer.

(6) Liquid crystal material will freeze below specified storage temperature range and it will not get back to normal quality even after temperature comes back within specified temperature range. Liquid crystal material will become isotropic above specified temperature range and may not get back to normal quality. Keep the LCD module always within specified temperature range.

(7) Do not expose LCD module to the direct sunlight or to strong ultraviolet light for long time.

(8) If the LCD driver IC (COG) is exposed to light, normal operation may be impeded. It is necessary to design so that the light is shut off when the LCD module is mounted.

(9) Do not disassemble the LCD module as it may cause permanent damage.

(10) As this LCD module contains components sensitive to electrostatic discharge, be sure to follow the instructions in below.

① Operators

Operators must wear anti-static wears to prevent electrostatic charge up to and discharge from human body.

② Equipment and containers

Process equipment such as conveyer, soldering iron, working bench and containers may possibly generate electrostatic charge up and discharge. Equipment must be grounded through 100Mohms resistance. Use ion blower.

③ Floor

Floor is an important part to leak static electricity which is generated from human body or equipment.

There is a possibility that the static electricity is charged to them without leakage in case of insulating floor, so the countermeasure(electrostatic earth:$1 \times 10^8 \Omega$) should be made.

④Humidity

Proper humidity of working room may reduce the risk of electrostatic charge up and discharge. Humidity should be kept over 50% all the time.

⑤Transportation/storage

Storage materials must be anti-static to prevent causing electrostatic discharge.

⑥Others

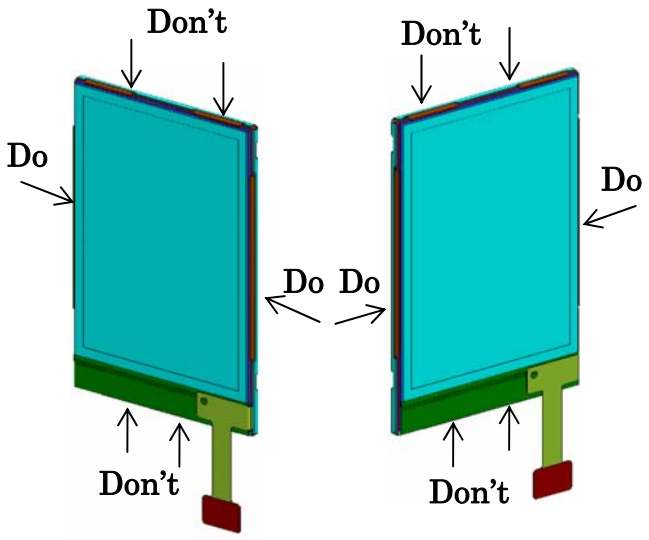
Protective film is attached on the surface of LCD panel to prevent scratches or other damages. When removing this protective film, remove it slowly under proper anti-ESD control such as ion blower.

(11) Hold LCD very carefully when placing LCD module into the system housing. Do not apply excessive stress or pressure to LCD module. Do not to use chloroprene rubber as it may affect on the reliability of the electrical interconnection.

(12) Do not hold or touch LCD panel to flex interconnection area as it may be damaged.

(13) As the binding material between LCD panel and flex connector mentioned in 12) contains an organic material, any type of organic solvents are not allowed to be used. Direct contact by fingers is also prohibited.

(14) When carrying the LCD module, place it on the tray to protect from mechanical damage. It is recommended to use the conductive trays to protect the CMOS components from electrostatic discharge. When holding the module, hold the Plastic Frame of LCD module so that the panel, COG and other electric parts are not damaged.



(15) Do not touch the COG's patterning area. Otherwise the circuit may be damaged.

(16) Do not touch LSI chips as it may cause a trouble in the inner lead connection.

(17) Place a protective cover on the LCD module to protect the glass panel from mechanical damages.

(18) LCD panel is susceptible to mechanical stress and even the slightest stress will cause a color change in background. So make sure the LCD panel is placed on flat plane without any continuous twisting, bending or pushing stress.

(19) Protective film is placed onto the surface of LCD panel when it is shipped from factory. Make sure to peel it off before assembling the LCD module into the system. Be very careful not to damage LCD module by electrostatic discharge when peeling off this protective film. Ion blower and ground strap are recommended.

(20) Make sure the mechanical design of the system in which the LCD module will be assembled matches specified viewing angle of this LCD module.

(21) This LCD module does not contain nor use any ODS (1,1,1-Trichloroethane, CCL4) in all materials used, in all production processes.

[For operating LCD module]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) At the shipment, adjust the contrast of each LCD module with electric volume. LCD contrast may vary from panel to panel depending on variation of LCD power voltage from system.

(3) As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable.

[Precautions for Storage]

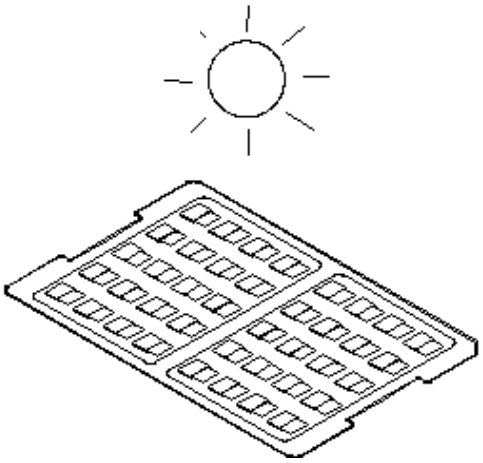
(1) Do not expose the LCD module to direct sunlight or strong ultraviolet light for long periods. Store in a dark place.

(2) The liquid crystal material will solidify if stored below the rated storage temperature and will become an isotropic liquid if stored above the rated storage temperature, and may not retain its original properties. Only store the module at normal temperature and humidity (25±5°C,60±10%RH) in order to avoid exposing the front polarizer to chronic humidity.

(3) Keeping Method

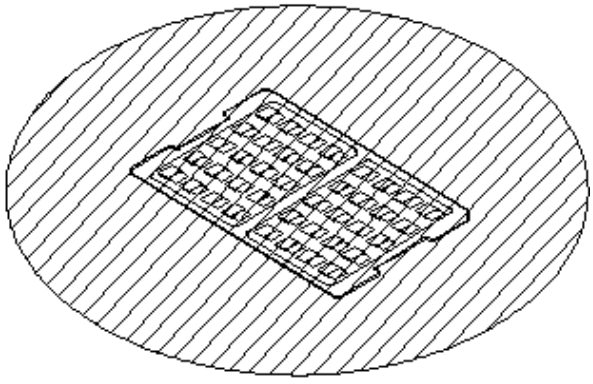
a. Don't keeping under the direct sunlight.

DON'T



b. Keeping in the tray under the dark place.

DO



(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) Be sure to prevent light striking the chip surface.

[Other Notice]

(1) Do not operate or store the LCD module under outside of specified environmental conditions.

(2) As electrical impedance of power supply lines (VCC-VSS) are low when LCD module is working, place the de-coupling capacitor near by LCD module as close as possible.

(3) Reset signal must be sent after power on to initialize LSI. LSI does not function properly until initialize it by reset signal.

(4) Generally, at power on, in order not to apply DC charge directly to LCD panel, supply logic voltage first and initialize LSI logic function including polarity alternation. Then supply voltage for LCD bias. At power off, in order not to apply DC charge directly to LCD panel, execute Power OFF sequence and Discharge command.

(5) Don't touch to PWB surface, exposed IC chip, electric parts and other parts, to any electric, metallic materials.

(6) No bromide specific fire-retardant material is used in this module.

(7) Do not display still picture on the display over 2 hours as this will damage the liquid crystal.

[Precautions for Discarding Liquid Crystal Modules]

COG: After removing the LSI from the liquid crystal panel, dispose of it in a similar way to circuit boards from electronic devices.

LCD panel: Dispose of as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal panel only contains an extremely small amount of liquid crystal (approx.100mg) and therefore it will not leak even if the panel should break.

-Its median lethal dose (LD50) is greater than 2,000 mg/kg and a mutagenetic (Aims test: negative) material is employed.

FPC: Dispose of as similar way to circuit board from electric device.

Contents Page

1. Application

This data sheet is to introduce the temporary specification of LS022Q8UX07 active matrix 16,777,216color LCD module.
Main color LCD module is controlled by Driver IC.

If any problem occurs concerning the items not stated in this temporary specification, it must be solved sincerely by both parties after deliberation.

2. Construction and Outline

Construction: LCD panel, Driver (COG), FPC with electric components,
4 White LED lump, prism sheet, diffuser, light guide and reflector, plastic frame to fix them mechanically.

Outline: See page 23

Connection: 24 pins;

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display function.

In order to realize thin module structure, double-sided adhesive tapes are used to fix LCD panels. As these tapes do not guarantee to permanently fix the panels, LCD panel may rise from the module when shipped from factory.

So please make sure to design the system to hold the edges of LCD panel by the soft material such as sponge
when LCD module is assembled into the cabinet.

3. Mechanical Specification

Table 1

Parameter		Specifications	Unit
Outline dimensions (typ)		38.68(W)×55.14(H)×2.04(D)	mm
Main LCD Panel	Active area	33.48(W)×44.64(H)	mm
	Display format	240×RGB(W)×320(H)	-
	Dot pitch	0.1395(W)×0.1395(H)	mm
	Base color (Note 1)	Normally Black	-
Mass		9.0	g

(Note1) Display module general parameters

4. Absolute maximum Ratings

(4-1) Electrical absolute maximum ratings

Table 2

Parameter (requirement)	Symbol	Rating	Unit
Power Supply Voltage (2.75V)	V_{DD}	-0.3 to +4.2	V
Power Supply Voltage (1.8V)	V_{DDI}	-0.3 to +4.2	V
Logic Signal Input Voltage	V_I	-0.3 to V_{DDI}+0.5	V

(4-2) Environment Conditions

Table 3

Item	Top		Tstg		Remark
	Min	Max	Min	Max	
Ambient temperature	-15℃	+70℃	-30℃	+80℃	Note2
Humidity	Note1		Note1		No condensation

(Note1) Ta ≤ 40 °C.....95 % RH Max

(Note2) Ta > 40 °C.....Absolute humidity shall be less than Ta=40 °C /95 % RH.

As opt-electrical characteristics of LCD will be changed, dependent on the temperature, the confirmation of display quality and characteristics has to be done after temperature is set at 25 °C and it becomes stable. Be sure not to exceed the rated voltage, otherwise a malfunction may occur.

5. Electrical Specifications

(5-1) Electrical characteristics

Table 4

Parameter(requirement)		Condition	Symbol	Specification			Unit
				min	typ	max	
Power Supply Voltage		Operating Voltage	V_{DD}	2.60	2.75	2.90	V
Power Supply Voltage (logic)		I/O Supply Voltage	V_{DDI}	1.65	1.80	1.95	V
Logic High Level Input Voltage		-	V_{IH}	0.7V_{DDI}	-	VDDI	V
Logic Low Level Input Voltage		-	V_{IL}	0.0	-	0.3 V_{DDI}	V
Logic High Level Output Voltage		I_{OUT} = -1mA	V_{OH}	0.8 V_{DDI}	-	VDDI	V
Logic Low Level Output Voltage		I_{OUT} = +1mA	V_{OL}	0.0	-	0.2 V_{DDI}	V
Logic High Level Input Current		Except D[7:0]	I_{IH}	-	-	10	uA
		D[7:0]	I_{IHD}	-	-	10	uA
Logic Low Level Input Current		Except D[7:0]	I_{IL}	-10	-	-	uA
		D[7:0]	I_{ILD}	-10	-	-	uA
Current Consumption	Partial Mode off Idle Mode off Sleep Out Mode	All pixels white(1)	IDDI	-	0.43	-	mA
			IDD	-	4.50	-	mA
		All pixels black(1)	IDDI	-	0.40	-	mA
			IDD	-	3.90	-	mA
	Sleep In Mode	N/A(1)	IDDI	-	0.020	-	mA
			IDD	-	0.001	-	mA

Notes:

1. Conditions : Ta = 25°C, VDD = 2.75V, VDDI = 1.8V, CPU access is inactive.
2. Ambient temperature,Ta = -15°C to +70°C operational
3. Measurement Point

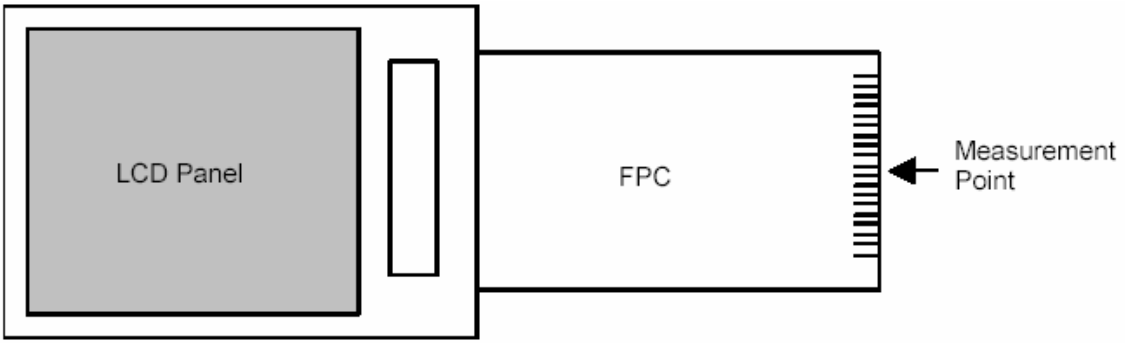


Fig.1 Measurement point for all characteristics

(5-2) LED back light

At main panel the back light uses 4pcs edge light type white LED.

Table 5

Item	Value			Unit
	Min	Nominal	Max	
Forward voltage (Vf) @ If	-	3.2	3.5	V
Forward current for LED (If)	-	15	18	mA
Number of LED components	4 pcs			
Connection type (Serial / Parallel / Other)	Two branches of two LEDs in series.			

LED lamp: NSSW20B

*4pcs of LED

*Please consider Allowable Forward Current on used temperature
(refer to Ambient Temperature vs. Allowable Forward Current curve)

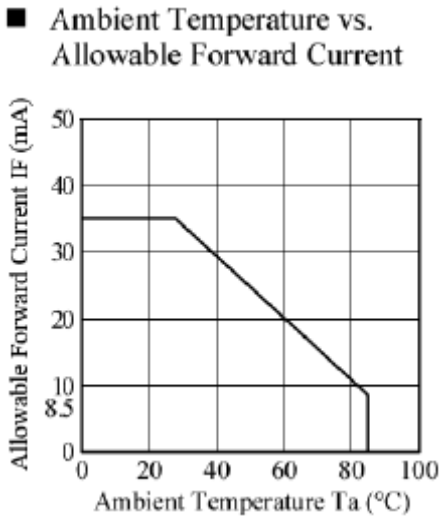


Fig.2

*Schematics drawing of lighting

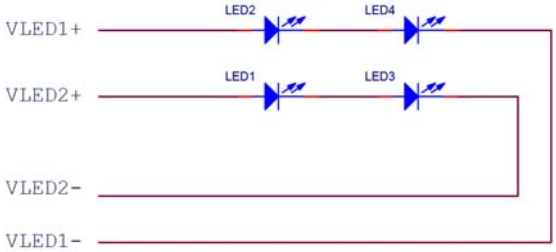


Fig.3

(5-3) Interface signals

Table 6

Pin No	Symbol	Description	I/O(1)	Remarks
1	VLED1-	Power supply for LED	-	
2	VLED2-	Power supply for LED	-	
3	VDDI	Power supply for LCD	-	typ=1.8V
4	GND	Ground	-	0V
5	WRX	Write signal	I	
6	D0	Data bus	I/O	
7	GND	Ground	-	0V
8	D2	Data bus	I/O	
9	D4	Data bus	I/O	
10	D6	Data bus	I/O	
11	CSX(2)	Chip select	I	
12	RESX	Reset signal	I	
13	TE	Tearing effect output	O	
14	D7	Data bus	I/O	
15	D5	Data bus	I/O	
16	GND	Ground	-	0V
17	D3	Data bus	I/O	
18	D1	Data bus	I/O	
19	D/CX	Command/data select	I	
20	RDX	Read signal	I	
21	GND	Ground	-	0V
22	VDD	Power supply for LCD	-	typ=2.75V
23	VLED2+	Power supply for LED	-	
24	VLED1+	Power supply for LED	-	

Notes:

1.The direction is named with respect to the display module, I = from host to module, O = from module to host.

2.When CSX is '1' RDX, WRX, D[7:0] and D/CX are ignored.

Table 7

Assembled on	Item	Description
Phone PWB	Connector type	Two piece board to board
	Pin amount	24
	Manufacturer	JST
	Part number	24P-JANK-GSAN-2-TF(LF)(SN)

Connector pin layout of the display module is presented in Fig.4

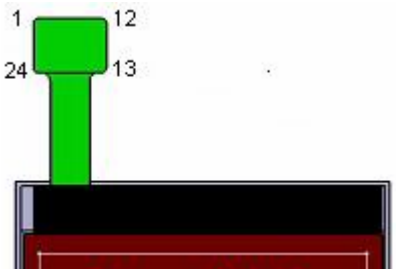


Fig.4

(5-4) Host Interface Timing Diagrams (Parallel 8-bit bus)

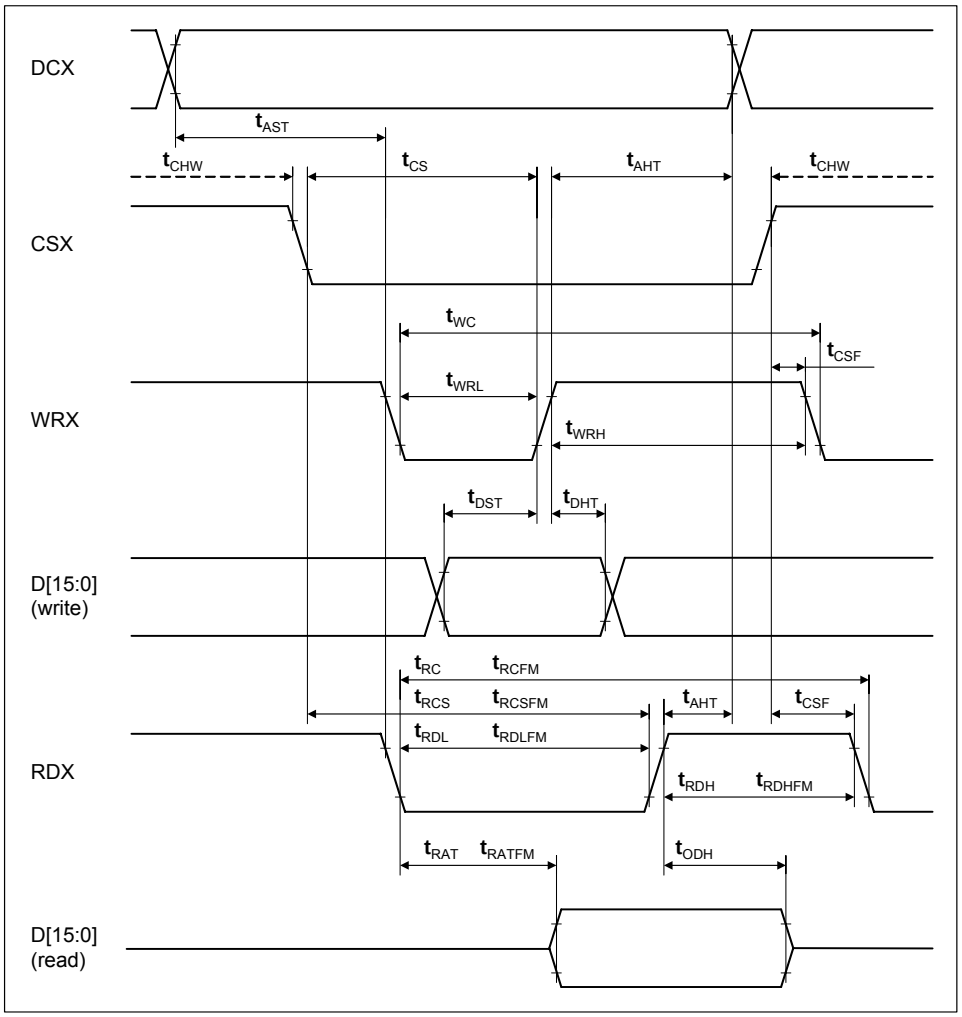


Fig.5 Parallel interface characteristics

Table 8

Parameter	Symbol	Description	Min	Max	Unit
DCX	t_{AST}	Address setup time	0	-	ns
	t_{AHT}	Address hold time (Write/Read)	10	-	ns
CSX	t_{CHW}	CSX 'H' Pulse Width	0	-	ns
	t_{CS}	Chip Select setup time (Write)	15	-	ns
	t_{RCS}	Chip Select setup time (Read ID)	45	-	ns
	t_{RCSFM}	Chip Select setup time (Read FM)	355	-	ns
	t_{CSF}	Chip Select Wait time (Write/Read)	10	-	ns
WRX	t_{WC}	Write cycle	66	-	ns
	t_{WRH}	Control pulse H duration	15	-	ns
	t_{WRL}	Control pulse L duration	15	-	ns
RDX (ID)	t_{RC}	Read cycle (ID)	160	-	ns
	t_{RDH}	Control pulse H duration (ID)	90	-	ns
	t_{RDL}	Control pulse L duration (ID)	45	-	ns
RDX (FM)	t_{RCFM}	Read cycle (FM)	450	-	ns
	t_{RDHFM}	Control pulse H duration (FM)	90	-	ns
	t_{RDLFM}	Control pulse L duration (FM)	355	-	ns
D[7:0]	t_{DST}	Data setup time	10	-	ns
	t_{DHT}	Data hold time	10	-	ns
	t_{RAT}	Read access time (ID)	-	40	ns
	t_{RATFM}	Read access time (FM)	-	340	ns
	t_{ODH}	Output disable time	20	80	ns

(5-5) Tearing Effect Modes

Mode 1 , the Tearing Effect Output signal consists of V-Blanking information only.

Mode 2 , the Tearing Effect Output signal consists of V-Blanking and H-Blanking information, there is one V-sync and 320 H-sync pulses per field.

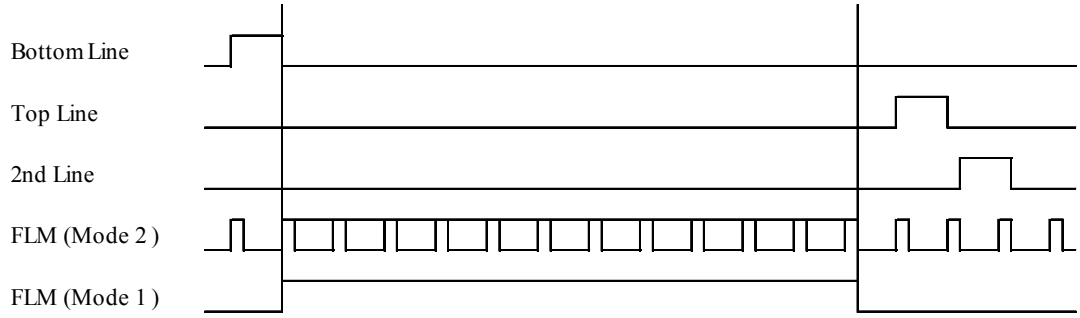


Fig.6 FLM output waveform

(5-6) /Reset Input Timing

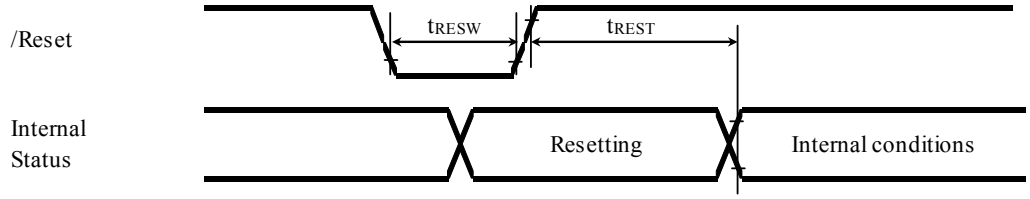


Fig.7 Reset input timing

Table 9

Symbol	Parameter	Min	Typ	Max	Unit	Remark
t_{RESW}	Reset low pulse width	10	-	-	us	-
t_{REST}	Reset complete time	-	-	120	ms	-

(5-7) Schematic of LCD module system

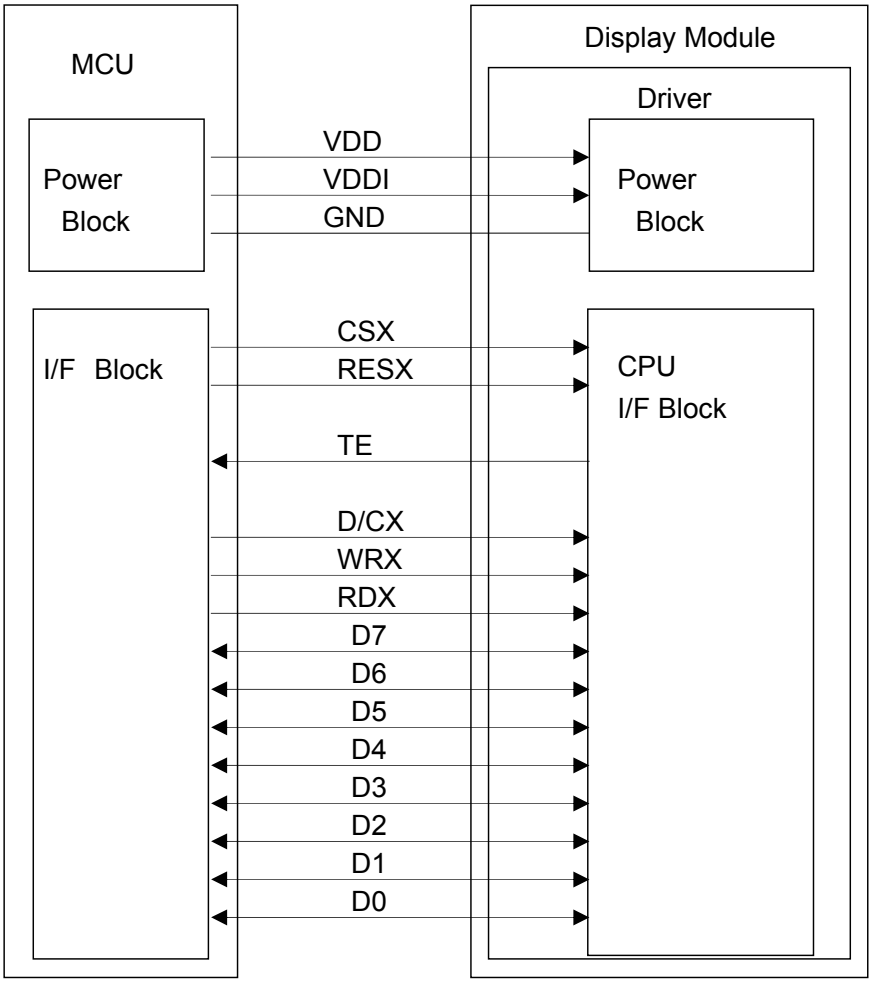


Fig.8 Schematic of LCD module system

6. Optical Characteristics

Table 10 transmissive mode VDD=2.75,Ta = 25℃

Parameter	Symbol	Condition	Typ	Unit	Remark
Brightness	Br	θ_1=0°	225	cd/m²	Note 1, 2
Contrast	Co	θ_1=0°	370	-	Note 1, 2, 3
Viewing Angle (Contrast)	φ=0°	θ_1=15°	215	-	Note 1, 2, 3
	φ=90°		210		
	φ=180°		220		
	φ=270°		220		
	φ=0°	θ_1=30°	65	-	Note 1, 2, 3
	φ=90°		70		
	φ=180°		70		
	φ=270°		70		
	φ=0°	θ_1=45°	25	-	Note 1, 2, 3
	φ=90°		25		
	φ=180°		25		
	φ=270°		25		
Response Time	τr1	θ_1=0°	10	ms	Note 4
	τr2		20		
White Chromaticity	u'	θ_1=0°	0.195	-	-
	v'		0.456		
Uniformity	-	θ_1=0°	77	%	Note 1, 2, 5
NTSC ratio	-	θ_1=0°	80	%	

Table 11 reflective mode VDD=2.75,Ta = 25℃

Parameter	Symbol	Condition	Typ	Unit	Remark
Reflectance	Ref	θ_1=0°	3.3	%	
Contrast	Co	θ_1=0°	27	-	Note 2
White Chromaticity	u'	θ_1=0°	0.195	-	
	v'		0.480		
NTSC ratio	-	θ_1=0°	0	%	

(Note 1) Definition of range of visual angle

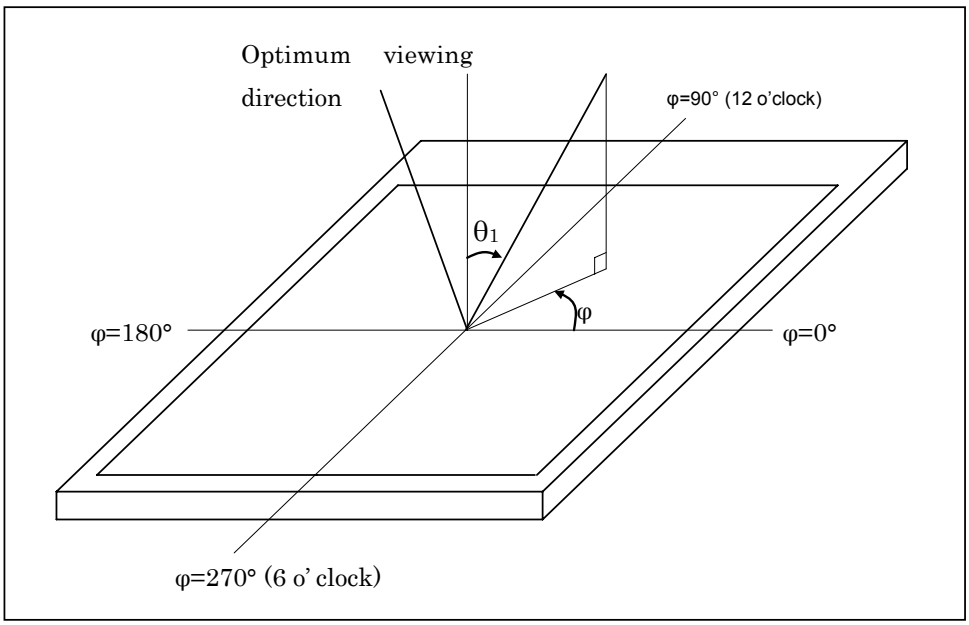


Fig.9 Definition of viewing angle

(Note 2) Brightness is measured as shown in Fig.9, and is defined as the brightness of all pixels "White" at the center of display area on optimum contrast.

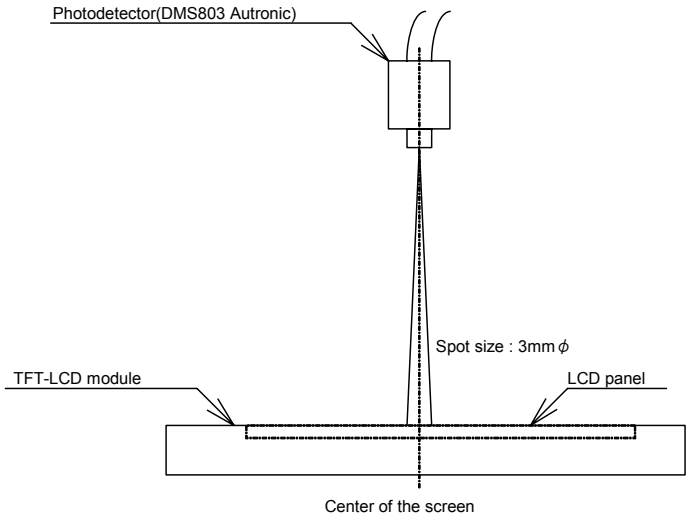


Fig.9 Optical characteristics Test Method (Brightness)

(Note 3) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance(brightness) all pixcels "White"}}{\text{Luminance(brightness) all pixcels "Black"}}$$

(Note 4) Response time is defined as follows:

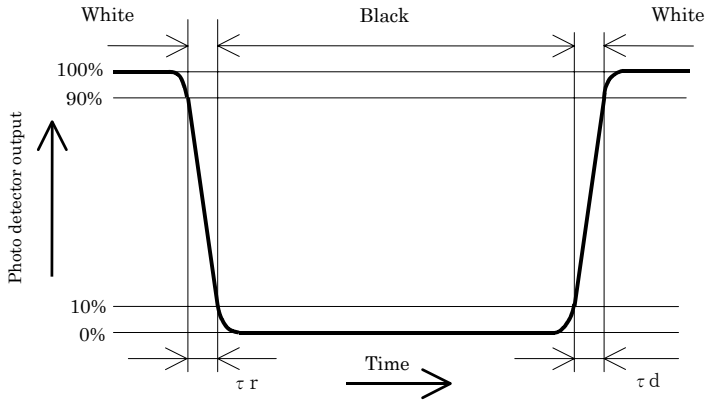


Fig.10 Response time

(Note 5) Uniformity is defined as follows:

$$\text{Uniformity} = \frac{\text{Minimum Brightness}}{\text{Maximum Brightness}} \times 100\ [\%]$$

The brightness should be measured on the 9-point as shown in the below figure.

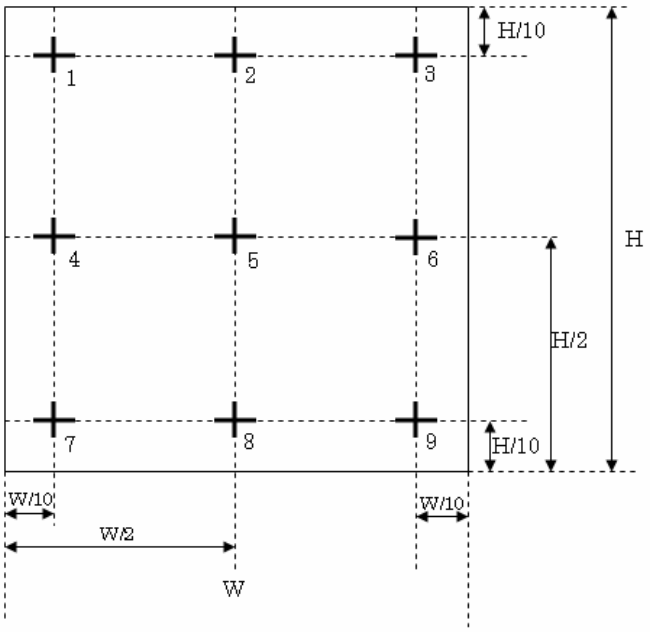


Fig.11 Definition of measurement points

(Note 6) Reflection ratio is defined as follows:

$$\text{Reflection ratio} = \frac{\text{Light detected level of the reflection by the LCD}}{\text{Light detected level of the reflection by the standard}} \times 100\ [\%]$$

7. Command List

Table 12

Op-code (Hex)(1)	Mnemonic	Function	Type(4)
00	NOP	No operation	C+0
01	SWRESET	Software Reset	C+0
04	RDDIDIF	Read display ID information	R+d3
09	RDDST	Read display status	R+d4
0A	RDDPM	Read Display Power Mode	R+d1
0B	RDDMADCTL	Read Display MADCTL	R+d1
0C	RDDCOLMOD	Read Display Pixel Format	R+d1
0D	RDDIM	Read Display Image Mode	R+d1
0E	RDDSM	Read Display Signal Mode	R+d1
0F	RDDSDR	Read Display Self Diagnostic Result	R+d1
10	SLPIN	Sleep In(3)	C+0
11	SLPOUT	Sleep Out	C+0
12	PTLON	Partial mode on(3)	C+0
13	NORON	Normal mode on(3)	C+0
20	INVOFF	Display Inversion Off(3)	C+0
21	INVON	Display Inversion On(3)	C+0
26	GAMSET	Gamma set(3)	W+1
28	DSPOFF	Display off(3)	C+0
29	DSPON	Display on(3)	C+0
2A	CASET	Column address set	W+4
2B	PASET	Page address set	W+4
2C	RAMWR	Memory write	W+n
2D	RGBSET	Color Set(3)	W+192
2E	RAMRD	Memory read	R+dn
30	PLTAR	Partial area(3)	W+4
33	VSCRDEF	Vertical Scrolling Definitor(3)	W+6
34	TEOFF	Tearing effect line off	C+0
35	TEON	Tearing effect line on	W+1
36	MADCTL	Memory data access control(3)	W+1
37	VSCRSADD	Vertical Scrolling start Address(3)	W+2
38	IDMOFF	Idle mode off	C+0
39	IDMON	Idle mode on	C+0
3A	COLMOD	Inertface Pixel format(3)	W+1
B0 to D9	-	Reserved(2)	
DA	RDID1	Read ID1	R+1
DB	RDID2	Read ID2	R+1
DC	RDID3	Read ID3	R+1
DE to FF	-	Reserved(2)	

Notes:

1. Undefined commands are treated as NOP (00h) command.

2. B0h to D9h and DEh to FFh are defined by Sharp. Before shipping, and by agreement with Sharp, these commands can be made available to the customer. By default these commands operate as NOP.

3: Commands which affect the displayed image, (10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 2Dh,30h,33h.36h,37h, and 3Ah), take effect during the Vertical sync pulse when the display module is in 'Sleep Out' mode to avoid abnormal visual effects. During 'Sleep In' mode, these commands take effect immediately. Read commands, (04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, DAh, DBh, DCh), are updated immediately both in 'Sleep In' mode and 'Sleep Out' Mode.

4. C=command, W=write, R=read, +=number of following parameters, (in Bytes), d=dummy clock cycle.

8. Initial Sequence

During power on, 'RESX' must be applied for a minimum of 10us after both VDD and VDDI have been applied. 'RESX' can be undefined during power-on but must be applied subsequently to ensure correct LCD controller operation. VDDI and VDD can be applied in any order.

During power-off, if the LCD controller is in 'Sleep Out' mode, VDD and VDDI must be powered down a minimum of 120ms after RESX has been released. If the LCD controller is in 'Sleep In' mode, VDDI and VDD can be powered down a minimum of 0ms after 'RESX' has been released. VDDI and VDD can be powered down in any order.

'CSX' can be applied at any time. 'RESX' has priority over 'CSX'.

(8.1) Case 1 - RESX line is held high or unstable by host at power-on

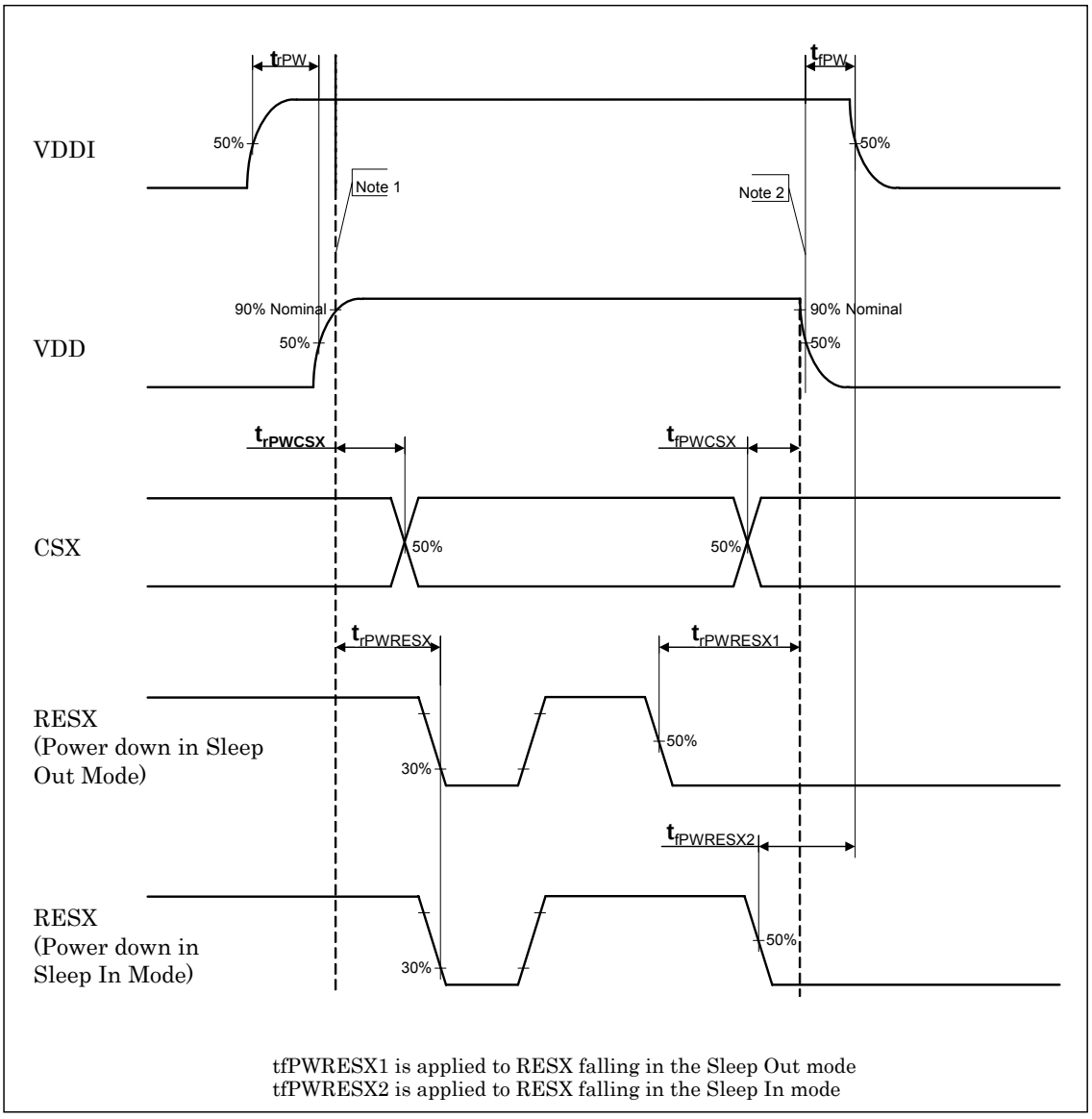


Fig.10 RESX line is held high or unstable by host at power-on.

Note 1. Time when the latter signal rises up to 90% of its typical value, e.g. when VDD comes later. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Note 2. Time when the former signal falls down to 90% of its typical value, e.g. when VDD falls earlier. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Table 13 RESX parameters (case 1)

Parameter	Value
trPW	+/- no limit
tfPW	+/- no limit
trPWCSX	+/- no limit
tfPWCSX	+/- no limit
trPWRESX	+ no limit
tfPWRESX1	min 120mS
tfPWRESX2	+ no limit

(8.2) Case 2 - RESX line is held low by host at power-on

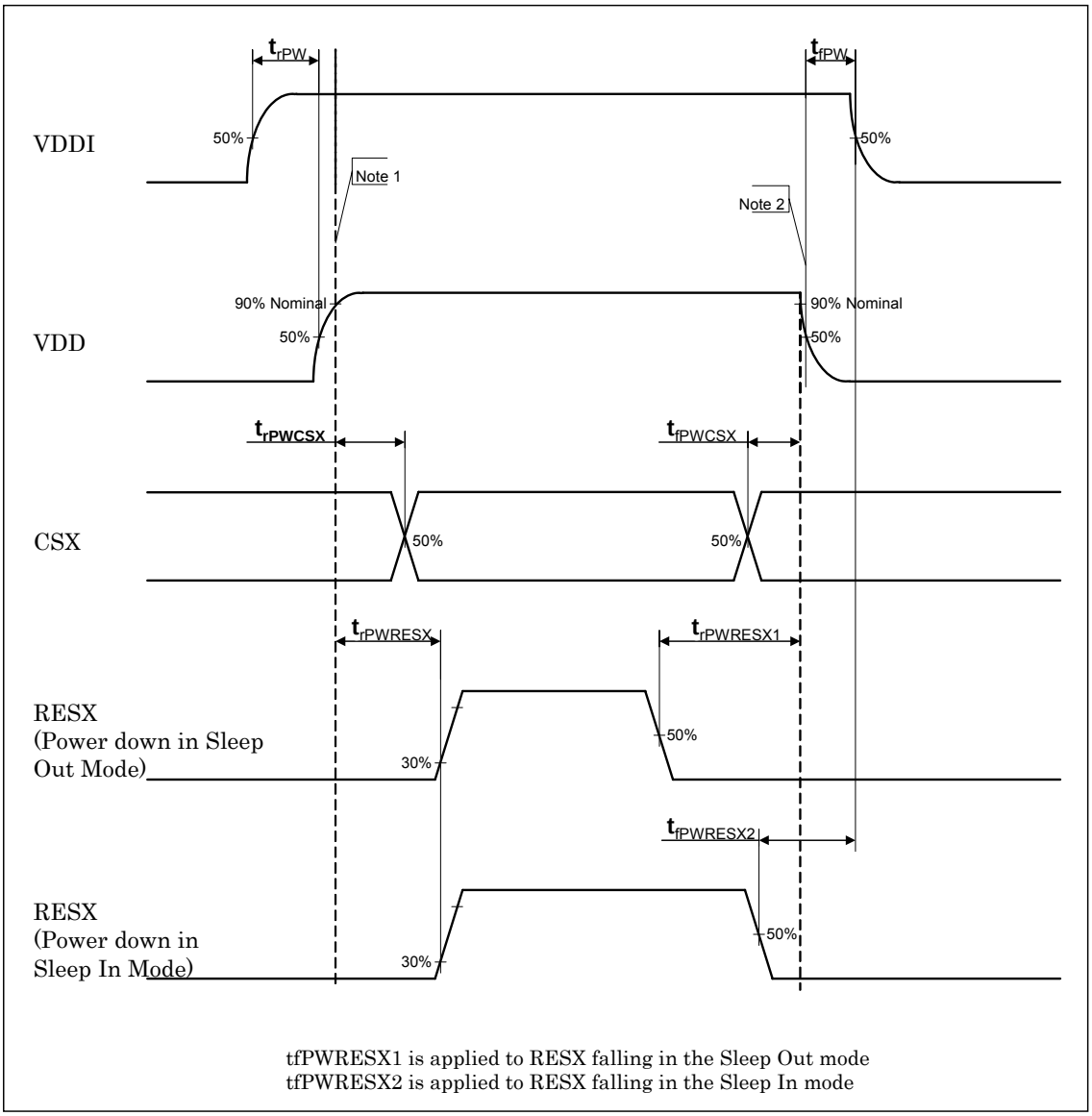


Fig.11 RESX line is held low by host at power-on.

Note 1. Time when the latter signal rises up to 90% of its typical value, e.g. when VDD comes later. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Note 2. Time when the former signal falls down to 90% of its typical value, e.g. when VDD falls earlier. This time is defined at the cross point of 90% of VDD Typ, not VDD Min, (see Table4).

Table14 RESX parameters (Case 2)

Parameter	Value
trPW	+/- no limit
tfPW	+/- no limit
trPWCSX	+/- no limit
tfPWCSX	+/- no limit
trPWRESX	min 10 us
tfPWRESX1	min 120mS
tfPWRESX2	min 0mS

Notes.

There will be no damage to the display module if the above power sequences are not met.

There will be no abnormal visible effects on the display panel during the sequence.

There will be no abnormal visible effects on the display between the end of power on sequence and before entering Sleep Out mode. Also between entering Sleep In mode and power off sequence.

There are no limits for RESX timings during power on sequence. (e.g. from the undefined level to high or low, when the first RESX low pulse after VDD and VDDI are powered-on, etc.)

(8.3) Uncontrolled power-off

Uncontrolled power-off (e.g. the battery is removed without following the proper power-off sequence), will not damage the LCD module or cause the LCD module to inflict any damage on the host.

There will not be any abnormal visible effects left on the display after a period of 5 seconds following an uncontrolled power-off. The display will remain blank until the power on sequence is initiated.

9. LCD module FPC Circuit diagram

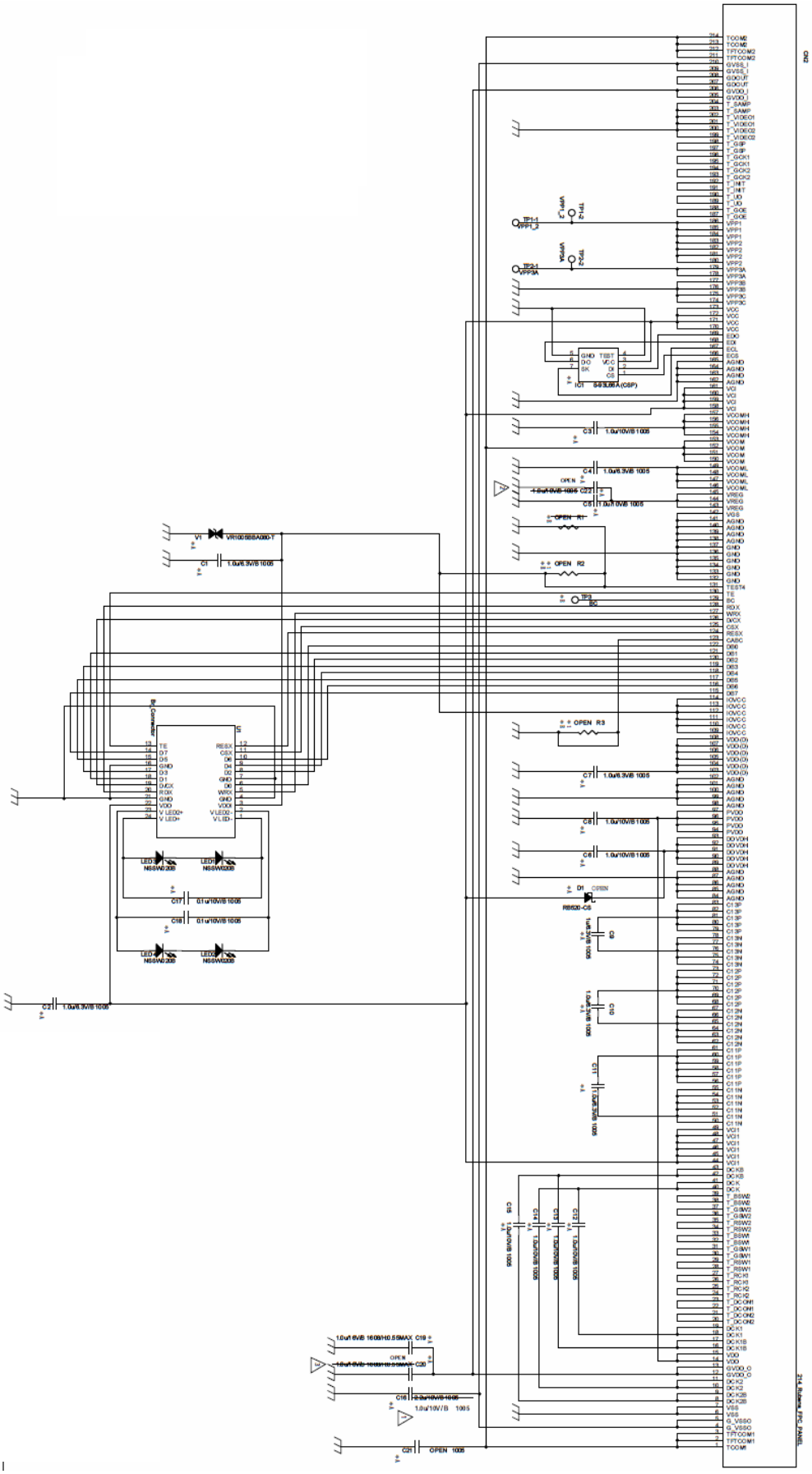


Fig.12 FPC circuit

10. LCD module outline dimensions

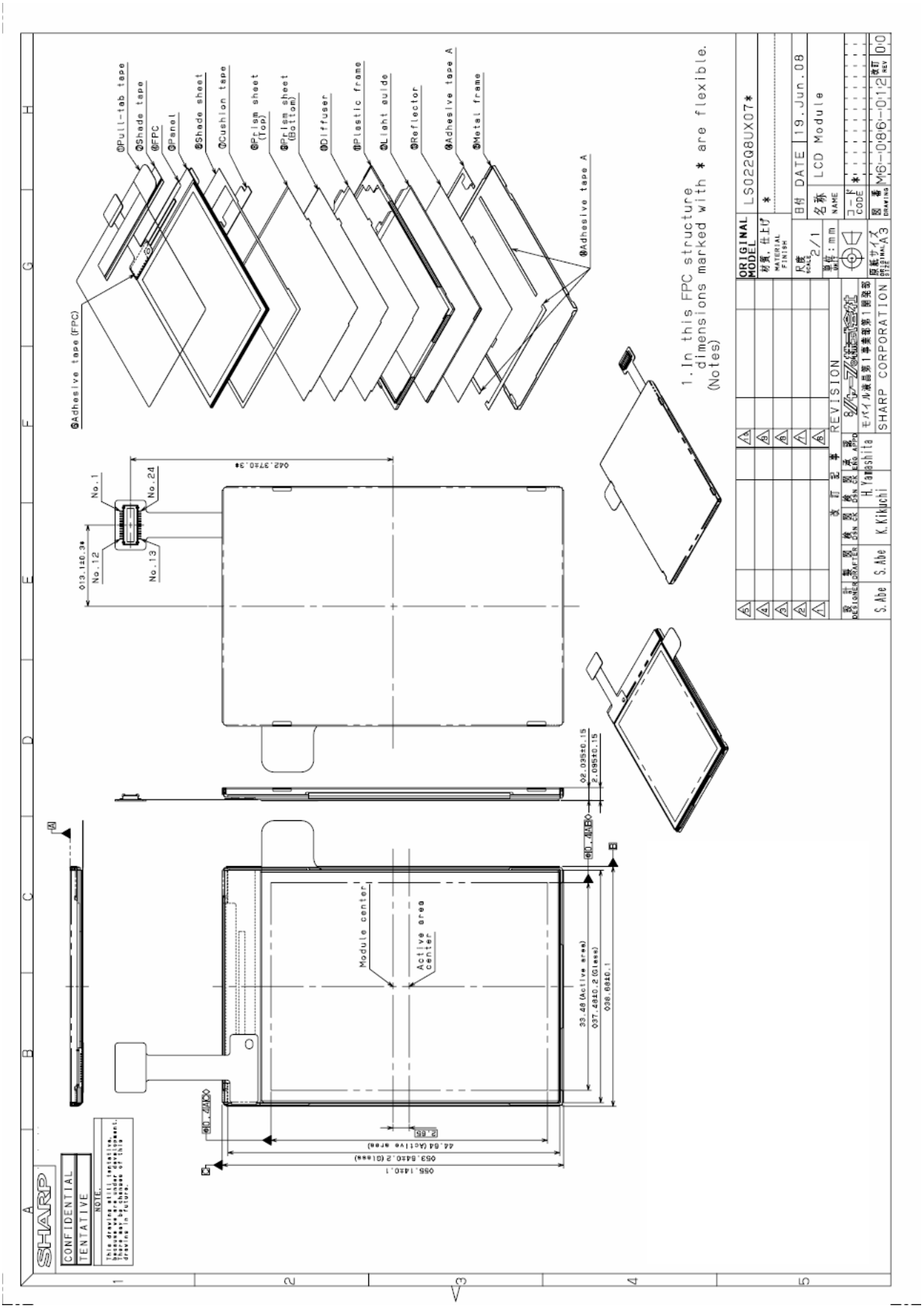


Fig.13 Outline

11. Packaging specification

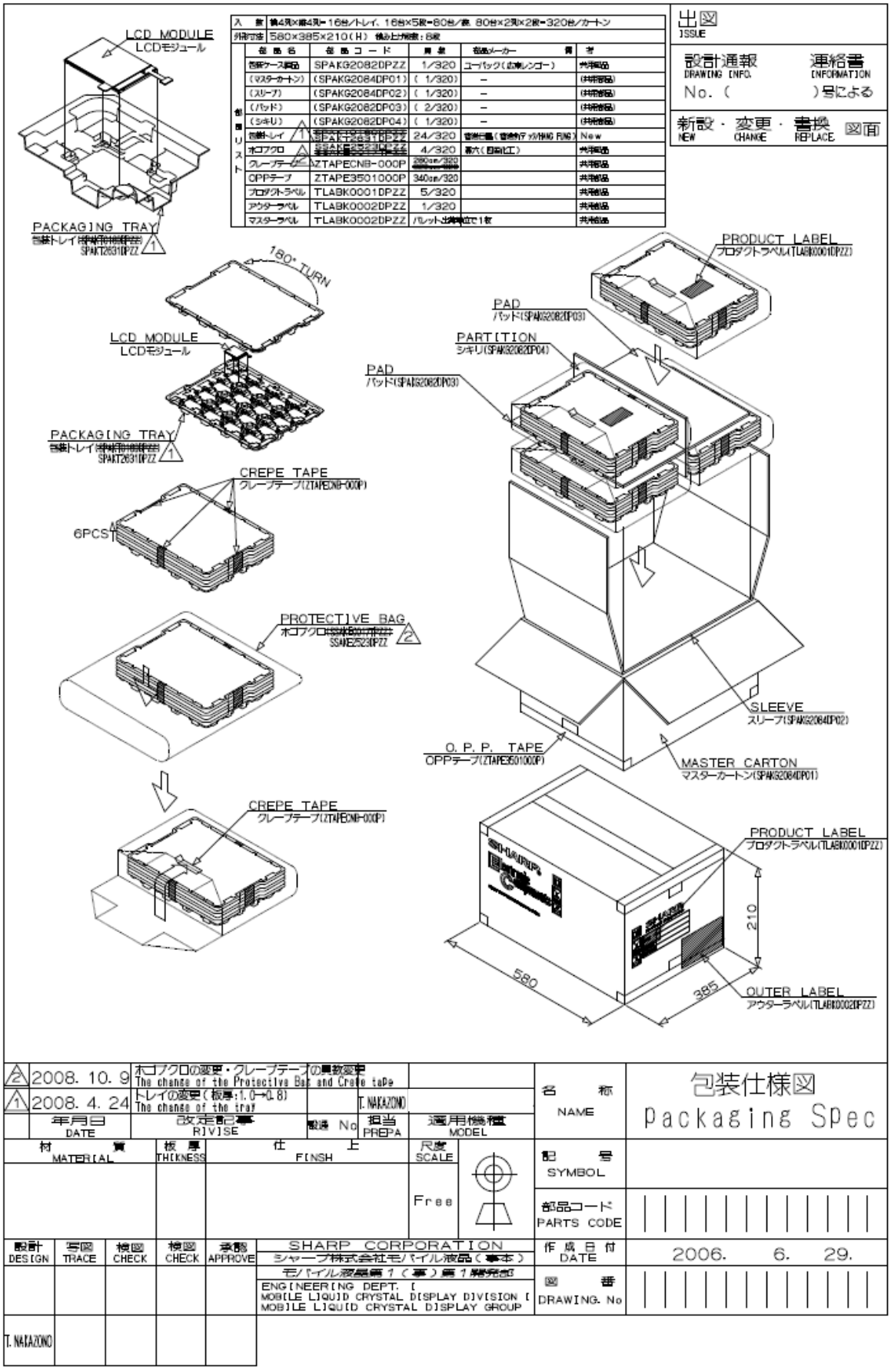
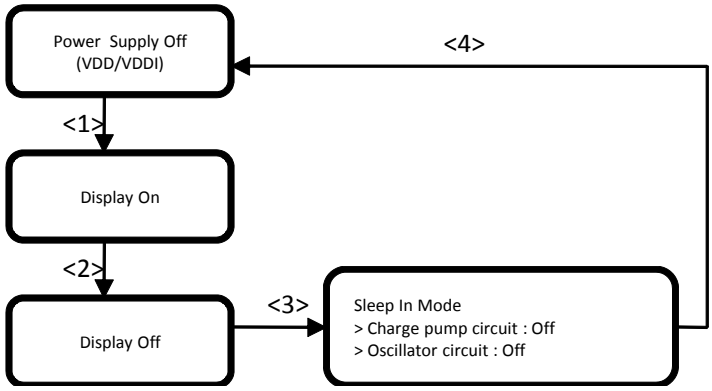


Fig.14 Outline

Appendix

1. Initial Sequence

Sequence transition chart:



<1> Power supply OFF -> Display On

Item	CSX [H / L]	D/CX [H / L]	"Command" or "Data"	D[7:0] Value	Remark
Initial Condition (D[7:0],D/CX,WRX,RDX,CSX,RESX="Low")					
VDDI On					
VDD On					
WAIT Min. 10us					
Reset release (RESX = "High")					
WAIT Min. 120ms					
[SWRESET] S.W. Reset	H	L	Command	01	
WAIT Min. 120ms					
[SLPOUT] Sleep Out	H	L	Command	11	
WAIT Min. 120ms					
[RAMWR] Memory Write	H	L	Command	2C	
	H	H	Data	**	24bit colors (8*R, 8*G, 8*B)
[DISPON] Display On	H	L	Command	29	

<2> Display On -> Display Off

Item	CSX [H / L]	D/CX [H / L]	"Command" or "Data"	D[7:0] Value	Remark
[DISPOFF] Display Off	H	L	Command	28	

<3> Display Off -> Sleep In Mode

Item	CSX [H / L]	D/CX [H / L]	"Command" or "Data"	D[7:0] Value	Remark
[SLPIN] Sleep In	H	L	Command	10	

<4> Sleep In Mode -> Power supply Off

Item	CSX [H / L]	D/CX [H / L]	"Command" or "Data"	D[7:0] Value	Remark
Reset (RESX = "Low")					
VDD Off					
VDDI Off					