MODEL No.	LS024Q8DD92
FILE No.	
ISSUE	Feb. 3, 2004
PAGE	39 pages

SPECIFICATION

DEVICE SPECIFICATION for

TFT LCD Module

Model No.

LS024Q8DD92

«Precautions on handling this specification and use of this product»

- Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.
- Application examples in this specification are only for reference to explain about typical application using our products. This specification is not to assure the enforcement of industrial property rights or other rights, or to permit enforcement right. If any dispute related to any industrial property or the like arises from the use of our product between you and any third party, we take no responsibility for such dispute unless it is directly related to the structure or manufacturing process of our product.
- This product is developed and produced to use for communication devices (terminals).

«Handling precautions»

- Those contemplating using this product for equipment which demands high reliability and safety on functions and accuracy etc. such as transportation equipment (airplanes, trains, automobiles, etc.), rescue and security equipment, other safety devices and safety equipment, and so on, should use this product after incorporating fail-safe design, redundancy design, etc. to ensure reliability and safety of the whole system and equipment.
- This product is not intended to be used for equipment which demands extremely high performance in terms of reliability and safety such as aerospace equipment, nuclear control device, medical equipment related to life support, etc. Do not use this product for such purposes.
- When using the products covered herein, in no event shall the company be liable for any damages resulting from failure to strictly adhere to the conditions and the precautions written herein.

«Cautions in mounting»

(1) Glass is used for LCD panel. Handle carefully as dropping or hitting to hard object will cause fractures and chips.
(2) Polarizer is sensitive to damage. Please pay enough attention during handling.
(3) A droplet of water for 10 minutes or more cause discoloration and stain, so wipe it off quickly.
(4) Clean the surface (front surface) of LCD module with cotton or soft cloth etc. when it is tainted. If the taint is left, use IPA (isopropyl alcohol) and wipe only the surface of polarizer lightly. Organic material is used for connection part of LCD panel and driver IC, and connection part of LCD panel and FPC. Organic solvent on this part causes failure. Handle with extra caution. Do not touch directly with fingers.
(5) Do not touch COG wiring area to avoid circuit failure.
(6) If gate driver which is set on driver IC (COG) or panel is exposed to strong light, it may interfere with normal operation; driver IC and gate driver need lightproof design when mounting LCD module. Pay enough attention to it.
(7) Pay enough attention for supporting and touching LCD module at the curve of connection part because they frequently cause failure.
(8) Confirm that the LCD module is designed with consideration for viewing angle when incorporated into a carrier.
(9) LCD panel should be set on flat place to avoid stresses of twist, bent pressure, etc. because its background color tone is easily changed by mechanical stress.

(10) Wavelength of the applied light which is 400nm or less should be cut regarding backlight for LCD module.

(11) Wiring inside the panel is exposed at the opposite edge of the edge where driver IC is mounted; therefore, pay enough attention not to touch the part by metals or other conductive material.
Adding to that, for handling LCD module, it is recommended to use jigs.

(12) To avoid being added mechanical stress during transferring LCD modules, put them in trays. To protect LCD modules from static electricity, carry on conductive trays. In addition, when setting LCD modules, set in plastic chassis to avoid hurting LCD panel, driver IC, and electronic parts.

(13) Gas of epoxy resin (amine hardening agent), silicone adhesive (dealcoholized and oxime) etc. may cause alteration of polarizer.
Confirm the adaptability with the materials you use.

(14) Do not use chloroprene rubber as it generates chlorine gas and affect the reliability of LCD panel connecting part.

(15) This LCD module is mounted with CMOS-LSI, therefore, be careful with static electricity (200V or more) when handling and in addition, pay attention to the items described below.

Workers

If clothes, footwear, gloves that workers wear are insulators (insulator like nylon, polyethylene, rubber etc.), static electricity may be charged to human body, hence wear antistatic products (static electricity prevention processed products).

Hardware, Facilities

Hardware and facilities which have features and functions of friction and peeling (for example, automatic machines, conveyors, inspection machines, soldering irons, mats, workbenches, containers, etc.) possibly generate static electricity; therefore, make provisions against static electricity (static electricity ground: 100MΩ).

Floor

Floors have an important role in leaking static electricity generated from human bodies, hardware, and facilities. If the floor is insulator (polymeric materials, rubber, etc.), human bodies, machines on it may possibly charge static electricity without leaking; therefore, make provisions against static electricity (static electricity ground: 100MΩ)

Humidity

Humidity in each workplace relates to surface resistance of objects which generates static electricity, and have important connection with antistatic measures. Keep humidity to 40% or more because humidity less than 40% increases static ground resistance of the whole physical object and accelerate static charge. Especially for laminate peeling process and processes which involves hand operation, keep humidity to 50% or more, and at the same time, use antistatic blower.

Distribution

Transportation and storage may possibly cause static charge on containers, storage material like Styrofoam etc. by their operation (friction and peeling, etc.), or static charge etc. on human body may cause induction charging etc.; therefore, antistatic measures should also be taken on storage material and so forth.

«Precautions during Operation»

(1) Operation over the specified voltage causes failure of this LCD module. Make sure to operate within the rating.

(2) Operation other than rating of AC timing etc. specified in this specification causes display failure. Make sure to operate within the rating.

(3) Freeze-frame display should be within two hours (normal temperature, normal humidity), and if it is longer, add refresh function to avoid afterimage.

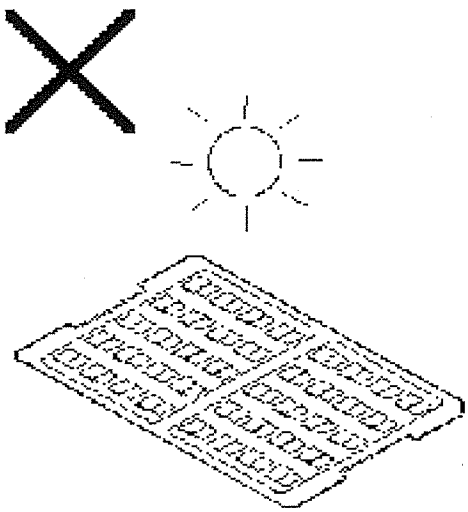
«Precautions on Storage»

(1) Do not leave the LCD module under direct sunlight or strong ultraviolet rays after it has been unpackaged. Store it in a dark place.

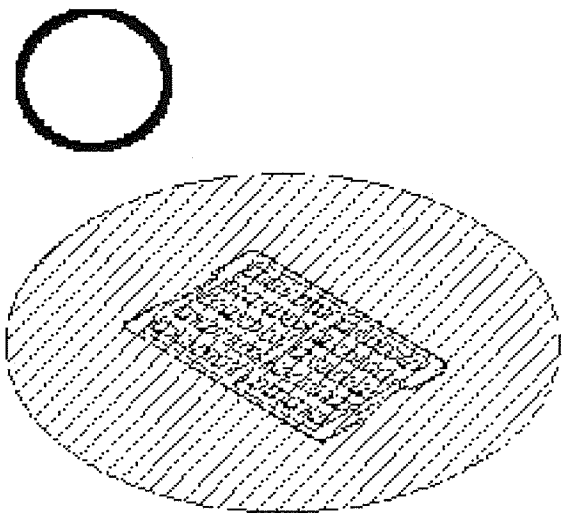
(2) The liquid crystal materials may be solidified at temperature below the rated storage temperature or become isotropic liquid at temperature above the rated storage temperature and may no longer return to the original state. Preserve at around ambient temperature as far as possible.
If it is stored in a place of high humidity, the polarizer will be damaged. Preserve at around ambient humidity as far as possible.

(3) Storage method

a. Avoid direct sunlight.



b. Place the LCD module on a tray and store it in a dark place.



«Other Precautions»

(1) Do not use under any conditions other than specified in the specification.

(2) In order to use the LCD module with reduced impedance of the power supply (VDC-GND, VCC-GND), insert a bypass capacitor as close as possible to the LCD module.

(3) The reset signal is sent to initialize after the power has been turned ON. The LCD module will not properly act until it has been initialized with the reset signal. Make sure to input reset, as the state of each part is not in prescribed operation after the power is supplied.

(4) Liquid crystal contained in LCD panel degrades by ultraviolet rays. Do not leave under direct sunlight or strong ultraviolet rays for long time.

(5) Do not dismantle this LCD module because it causes critical damage.

(6) If LCD panel is broken, do not put liquid crystal contained in it to your mouth. Wash away with soap as soon as possible if any liquid crystal spots your body part or clothes.

(7) This product does not use or contain any ODS (specific CFCs, specific halon, 1-1-1 trichloroethane, carbon tetrachloride) in the whole production process from raw material to the completion of the product. Nor it does not contain them.

(8) Other than that, abide by the precautions which is normally applied to electronic parts.

«Precautions on Disposing of LCD Modules»

FPC : After removing from the LCD panel, dispose like circuit boards of electronic devices.

Driver IC : After removing from the LCD panel, dispose like circuit boards of electronic devices.

LCD panel : Dispose as glass waste.

There are no hazardous materials in this LCD module.

LCD panel does not contain dangerous or hazardous substance.

The liquid crystal materials contained in the LCD panel is of a very small amount (approx. 100 mg). Even if the panel is broken, no liquid crystal will leak out. The material chosen for the LCD panel is of LD(lethal dose)50 >/= 2,000 mg/kg and its mutagenicity (Aims test result) is negative

1. Scope

This specification applies to the system LCD, 262,144-color module LS024Q8DD92, LS024Q8DD92G 1

LCD module is operated by driver IC (iPD161831).

Refer to IC data sheet for basic specification of driver IC.

2. Structure and Exterior

This module consists of TFT-LCD panel, driver IC, and FPC.

External dimensions are shown in Diagram15-1.

3. Mechanical Specifications

Table 3-1

Item	Specifications	Unit
Dot Configuration	240 x RGB (Horizontal) x 320 (Vertical)	Dot
Guaranteed appearance area (Panel display surface)	36.72 (Horizontal) x 48.96 (Vertical)	mm
Display size (Diagonal)	6.12 [2.4 inch]	cm
Dot Pitch	0.051 (Horizontal) x 0.153 (Vertical)	mm
Pixel Array	Red, Green, Blue stripe array	-
Module External Dimensions (not including projections)	41.2(W)x58.0(H)x1.67(D) *1	mm
Weight	8(Typ .)	g
Polarizer Surface Hardness	3H or more (Initial)	Pencil hardness

*1) Refer to Dimension 15-1 for detailed dimensions and tolerance

4. Absolute Maximum Rating

(4-1) Electrical Maximum Rating

Table 4-1

Ta=25°C

Items	Symbol	Min.	Max.	Unit	Notes
Logic Supply Voltage	VCC-GND	-0.3	+4.5	V	
Driver Power Supply Voltage	VDC-GND	-0.3	+6.0	V	
Input Voltage	V_{IN}	-0.3	VCC+0.3	V	*1

*1) Logic input terminal: Reference value of voltage is GND (=0V).

(4-2) Environmental Conditions

Table 4-2

Items	Top		Tstg		Notes
	Min.	Max.	Min.	Max.	
Ambient temperature	-10°C	+60°C	-20°C	+70°C	There should be no condensation.

5. Input Terminal

Table 5-1

Terminal No.	Symbol	I/O	Function	Terminal No.	Symbol	I/O	Function
1	T-COM	I	COM electric potential input for CS	2	T-COM	I	COM electric potential input for CS
3	TFT-COM	I	COM voltage input terminal	4	COMC	O	COM signal output
5	COMC	O	COM signal output	6	COMDC	O	COM center voltage output
7	VCOMH	O	COM amplitude voltage output	8	BO	I	Blue data signal (LSB)
9	B1	I	Blue data signal	10	B2	I	Blue data signal
11	B3	I	Blue data signal	12	B4	I	Blue data signal
13	B5	I	Blue data signal (MSB)	14	G0	I	Green data signal (LSB)
15	G1	I	Green data signal	16	G2	I	Green data signal
17	G3	I	Green data signal	18	G4	I	Green data signal
19	G5	I	Green data signal (MSB)	20	R0	I	Red data signal (LSB)
21	R1	I	Red data signal	22	R2	I	Red data signal
23	R3	I	Red data signal	24	R4	I	Red data signal
25	R5	I	Red data signal (MSB)	26	DCLK	I	Data sampling clock
27	HSY	I	Horizontal Synchronizing Signal	28	VSY	I	Vertical Synchronizing Signal
29	SO	O	Serial data output	30	SI	I	Serial data input
31	SCLK	I	Serial clock input	32	CS	I	Serial interface chip select
33	RESET	I	Hard Reset	34	VCC	—	Logic Power Supply
35	GND	—	Ground Electric Potential	36	GND	—	Ground Electric Potential
37	VDC	—	Analog power supply	38	VDC	—	Analog power supply
39	COM2	—	COM control for CS	40	VCLAMP	O	Voltage output for CS
41	VSS2	O	DC/DC converter output	42	NC	—	NC terminal
43	VSS1	O	DC/DC converter output	44	NC	—	NC terminal
45	VDD2	O	DC/DC converter output	46	C5-	—	Step-up condenser connecting terminal
47	C5+	—	Step-up condenser connecting terminal	48	C4-	—	Step-up condenser connecting terminal
49	C4+	—	Step-up condenser connecting terminal	50	C3-	—	Step-up condenser connecting terminal
51	C3+	—	Step-up condenser connecting terminal	52	C2-	—	Step-up condenser connecting terminal
53	C2+	—	Step-up condenser connecting terminal	54	C1-	—	Step-up condenser connecting terminal
55	C1+	—	Step-up condenser connecting terminal	56	VDC2	O	DC/DC converter output
57	VDC2	O	DC/DC converter output	58	VR	O	Reference power supply
59	VS		Source power supply output	60	VS	O	Source power supply output

6. Electrical Specification

(6-1) Appropriate use conditions

Table 6-1

GND=0V, Ta=25°C

Items		Symbol	Conditions	Min.	Typ.	Max.	Unit	Applied Pin
Logic Power Supply Voltage		VCC-GND		+2.9	+3.0	+3.1	V	VCC
Liquid Crystal Operating Power Supply Voltage		VDC-GND		+2.9	+3.0	+3.1	V	VDC
"H" Level Input Voltage		V_{IH}		0.8VCC	-	VCC	V	
"L" Level Input Voltage		V_{IL}		0	-	0.2VCC	V	
Current Consumption (during Operation)	Logic current	I_{CCOP}		-	0.6	1.0	mA	(Note 1)
	Analog current	I_{DDOP}			6.0	8.0	mA	
Current Consumption (Standby)	Logic current	I_{CCSTB}			—	0.04	mA	(Note 2)
	Analog current	I_{DDSTB}			—	0.08	mA	

Note 1: Gray-scale full-screen display pattern

No access (CS=SCLK=SI=L),fclk=5.4MHz,

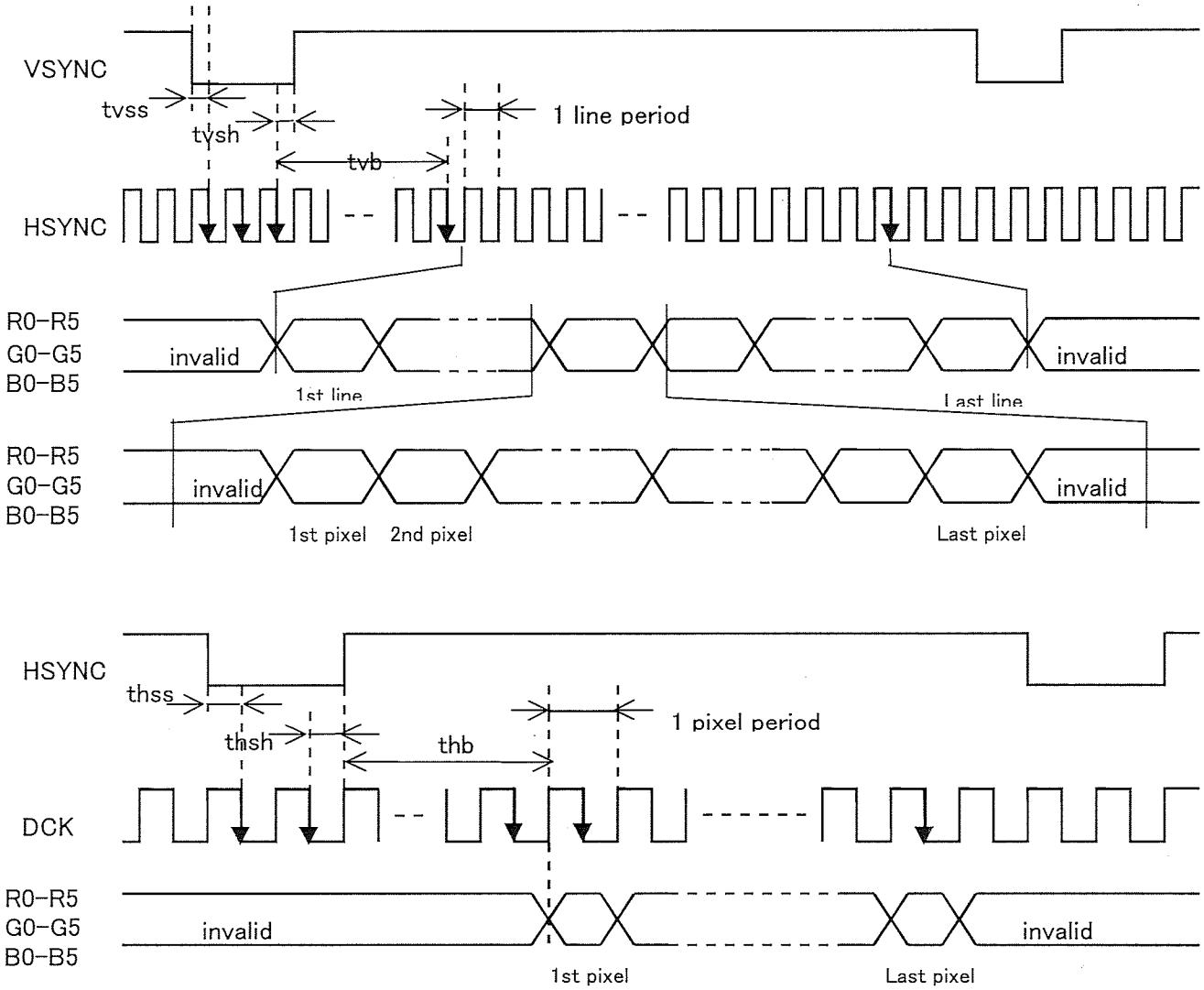
Register setting is as per separate description.

Note 2: Input signal is considered not to be varied. It is considered to be the measurement after operating transition sequence for standby which is described in separate description.

7. RGB Interface

Input display data by each terminal of DCK, HSYNC, VSYNC, R0-5, G0-G5, B0-B5. Valid data number in horizontal period of this mode is the value set in R3 register. Timing chart is shown in Diagram7-1.

During front porch period, at least one dot clock should be inputted.



tvb = vertical back porch period
thb = horizontal back porch period

Diagram7-1 HSYNC, VSYNC mode timing chart

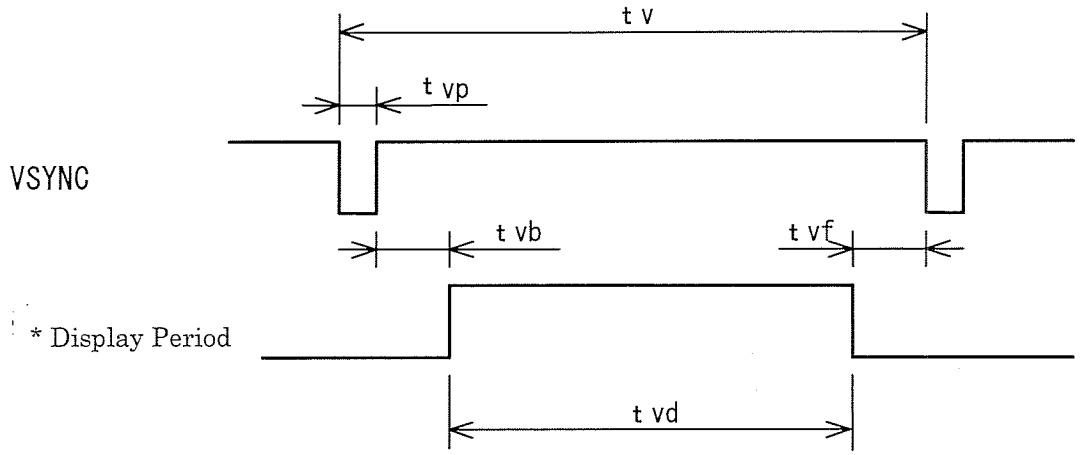


Diagram7－2

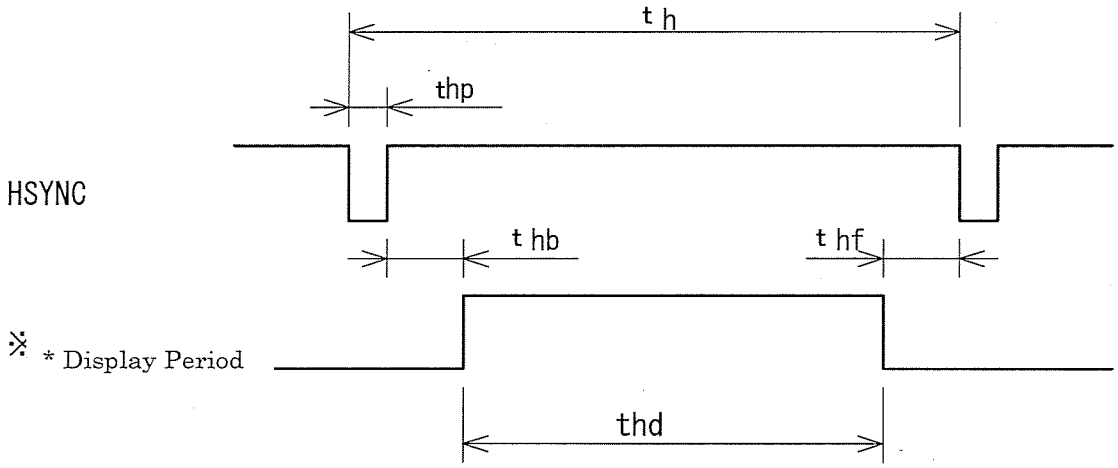


Diagram7－3

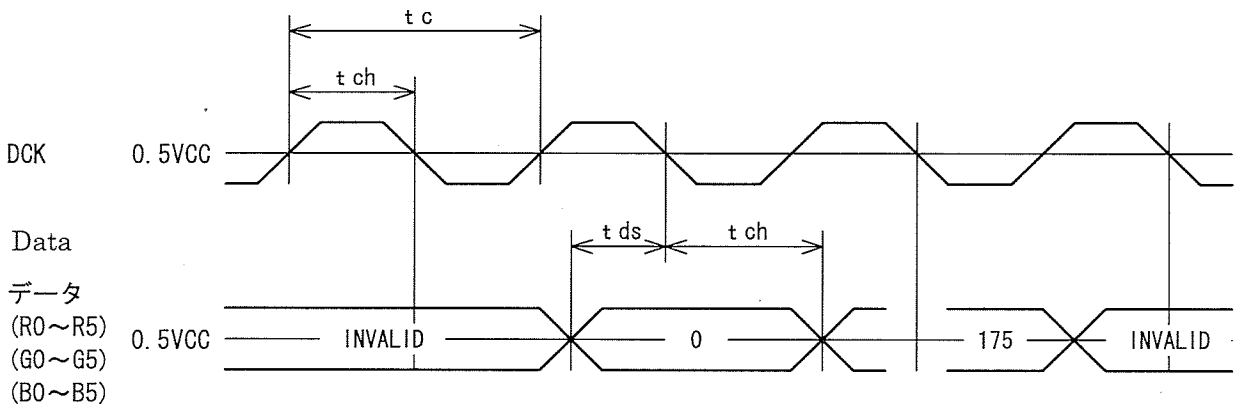


Diagram7－4

Table7-1 RGB Interface Timing

Ta=－10 to＋60℃, VCC=2.9 to 3.1V

Name		Symbol	Conditions	Min.	Typ.	Max.	Unit	Compatible Terminal
Vertical Synchronizing Signal	Cycle	tv		5	330		H	VSYNC
	(Frequency)	Fv			16.67		Ms	
	Front Porch	tvf		1	2	-	H	
	Back Porch	tvb		1	3	-	H	
	Pulse Width	tvp		1	5	-		
	Display Period	tHD			320		H	
	tvf+tvp+tvb			4	10	-	H	
Horizontal Synchronizing Signal	Cycle	Th		-	-	-	CLK	HSYNC
	(Frequency)	Fh			50.51		μs	
	Front Porch	thf		1	3		CLK	
	Back Porch	thb		2	4		CLK	
	Pulse Width	thp		2	5		CLK	
	Display Period	tVD			240		CLK	
	thp+thb		(Quarter data not used)	4	10	255	CLK	
			(Quarter data used)	10	10	255	CLK	
Dot Clock		f_{CLK}			5	10	MHz	DCLK

* This table is described based on driver characteristics. Use the value described in "(10) recommended sequences" for operating conditions of this module. Notice to us in case of using other values.

Table7-2 RGB Interface AC Characteristics

GND=0V

Name		Symbol	Conditions	Min.	Typ.	Max.	Unit	Compatible Terminal
Vertical Synchronizing Signal	Setup Time	tvss	Ta=-10 to 60 °C VCC=2.9 to 3.1V	20	-	-	ns	VSY
	Hold Time	tvsh		20	-	-		
Horizontal Synchronizing Signal	Setup Time	thss		40	-	-	ns	HSY
	Hold Time	thsh		40	-	-		
Dot Clock	Setup Time	tdh		20	-	-	ns	DCLK
	Hold Time	tds		20	-	-		
	Duty	tch/tc		40	50	60	%	

8. Serial Interface

It is possible to control strobe signal output timing to gate driver etc. by setting registers of horizontal period, vertical period etc. from CPU by 8 bit serial interface.

Setting of Read/Write operation is done by command. When read operation was specified by command (A5 bit =1), the next 8 bit transmission becomes read operation. Specifically, it works like Diagram7-2. In addition, note that SO terminal becomes Hi-z while it is not outputting data.

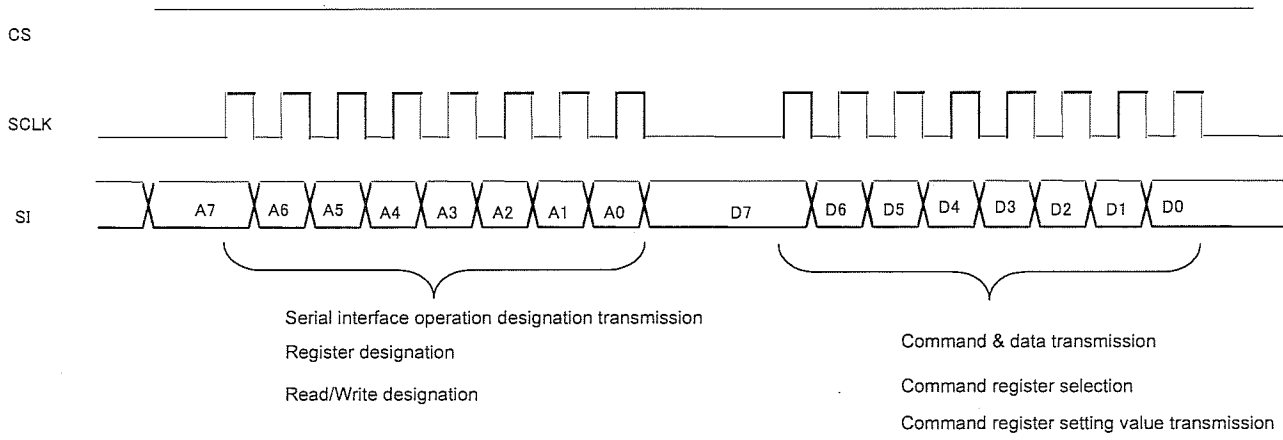


Diagram 8-1: Serial interface signal chart (Write sequence)

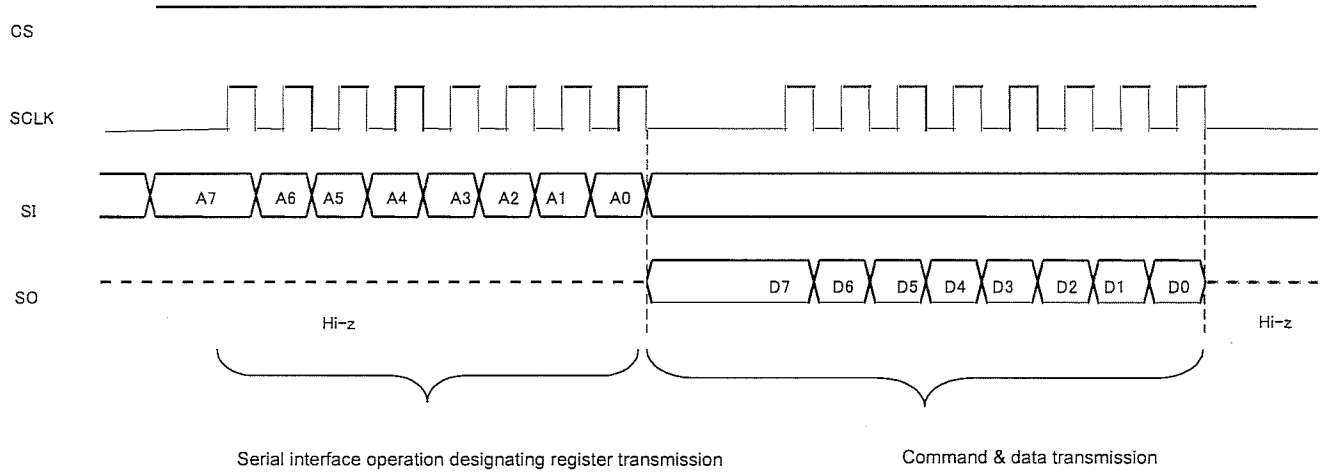


Diagram 8-2 Serial interface signal chart (Read sequence)

Driver Register Setting

It is possible to set horizontal period and vertical period by register. Specification of register and setting of register value is done by serial interface. Simple timing chart is shown in Diagram8-1.

This serial interface is composed by 8-bit data. However, access two times by 8 bit for setting register. First, transmit data to **"Serial interface operation specifying register"** (A7 - A0 of Diagram 8-1) by the first 8-bit transmission. Serial interface operation specifying register specifies the operation of the following 8-bit transmission (D7-D0 of the Diagram8-1). In addition, second 8-bit transmission selects each command register or transmits command register setting value etc.

Keep chip select (LCDCS) active during transmission of total 32 bits of 8 bits + 8 bits transmission which selects command register (A7-A0 + D7-D0) and 8 bits + 8 bits transmission which writes/reads setting to command register (A7-A0 + D7-D0). **(Set LCDCS to "L level" each time one setting is completed.)**

Serial interface operation specifying register is shown in Table 9-2, and register number and register name of each command register is shown in Table 9-1.

There are three kinds of executing pattern **for each command** while using timing generator. Those are **executing just after setting**, **executing at the next line of setting**, and **executing at the next frame of setting**. Specific timing of executing command at the next line or the next frame is described in the diagram below.

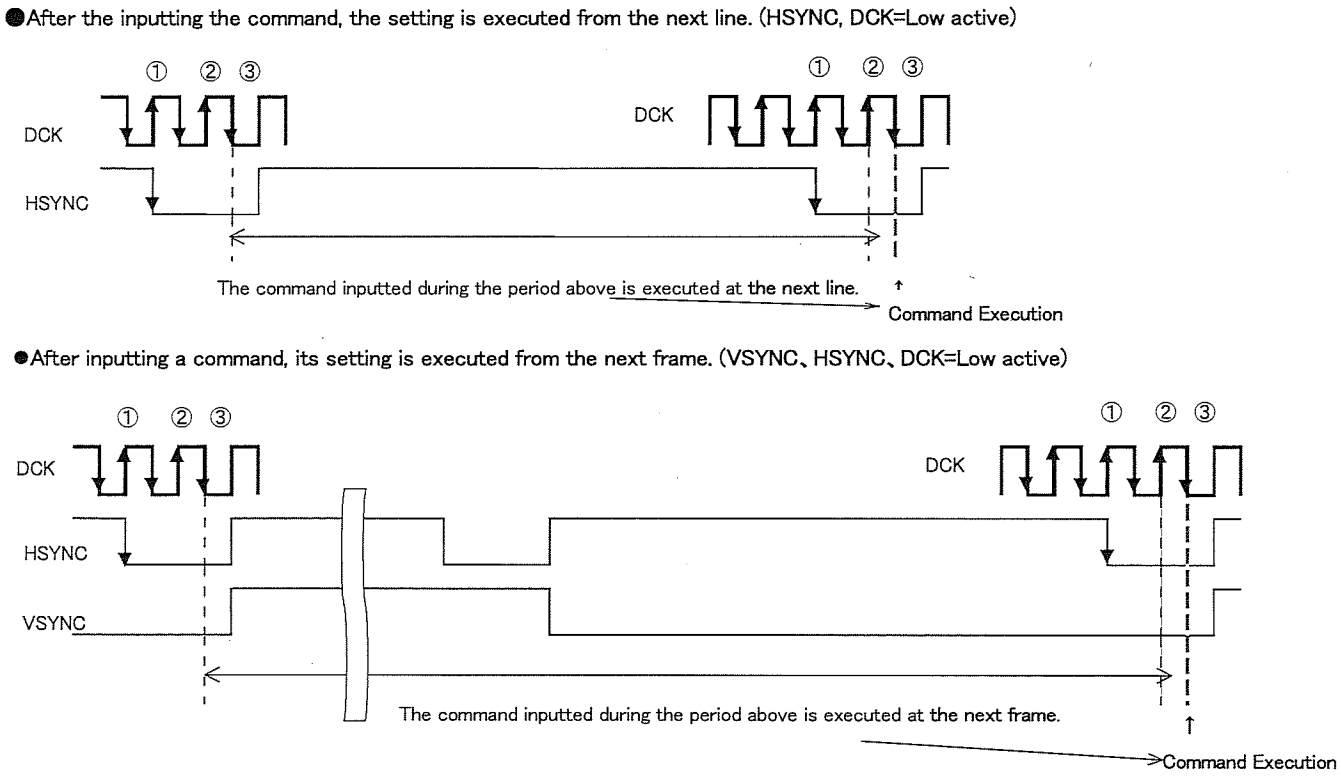


Diagram 8-3: Register Setting Timing Chart

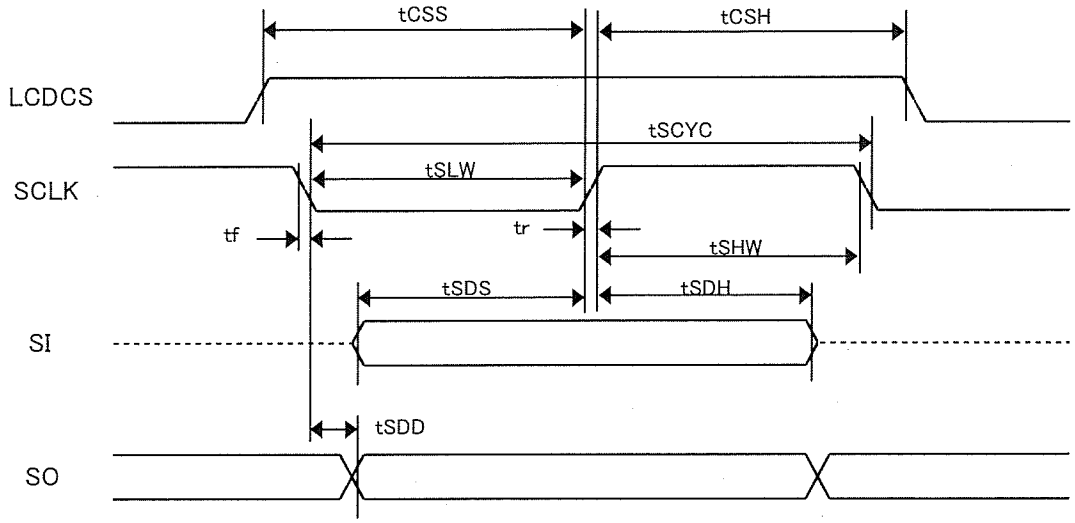


Diagram 8-4: Serial Interface between CPU and Driver

Table 8-1: Serial interface AC characteristics GND = 0 V

Item	Symbol	Conditions	Min.	TYP.	MAX.	Unit
Serial Clock Cycle	tSCYC	Ta=-10 to 60 °C VCC=2.9 to 3.1V	150			ns
SCLK_SUB High level pulse width	tSHW		60			ns
SCLK_SUB Low Level Pulse Width	tSLW		60			ns
Data Setup Time	tSDS		60			ns
Data Hold Time	tSDH		60			ns
CS-SCL Time	Tcss		90			ns
	Tcsh		90			ns
SCLK↓→SO Output Delay Time	Tsdd		70			ns

Remark1. Rising time and falling time (t_r, t_f) of input signal is defined to 15 ns or less.

Remark2. All the timing is defined with reference to 20-80% of Vcc.

9. Command Register

(9-1) Command List

Table 9-1-1: Command Register List (1/2)

Register No.	D7 to D0						Register Name	Initial Value	Timing Generator Function		Reset		Internal Set Timing
	D5	D4	D3	D2	D1	D0			Assigned	Unassigned	Command	Hard	
R0	0	0	0	0	0	0	Switching between 65K/260K Colors	00h	O	—	O	—	F
R1	0	0	0	0	0	1	Horizontal Period/ Valid Data Input Start Timing	0Ah	O	—	O	—	F
R2	0	0	0	0	1	0	Vertical Period/ Valid Data Input Start Timing	02h	O	—	O	—	F
R3	0	0	0	0	1	1	Horizontal Valid Pixel Data Number Setting	00h	O	O	O	—	C
R4	0	0	0	1	0	0	Standby	00h	O	O	O	—	F
R5	0	0	0	1	0	1	8 Colors Mode	00h	O	O	O	—	L
R6	0	0	0	1	1	0	Various Setting	02h	O	Δ1	O	Note2	Note 1
R7	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—
R8	0	0	1	0	0	0	Amplifier Driving Period Setting	0Eh	O	—	O	—	C
R9	0	0	1	0	0	1	Quarter Data Function	00h	O	O	O	—	F
R10	0	0	1	0	1	0	Level Shifter Voltage Setting	00h	O	O	O	—	C
R11	0	0	1	0	1	1	Amplitude Voltage Adjustment D/A Converter	0FH	O	O	O	—	C
R12	0	0	1	1	0	0	Common Center Voltage Adjustment D/A Converter	35H	O	O	O	—	C
R13-R14	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—
R15	0	0	1	1	1	1	Command Reset	00h	O	O	—	—	C
R16-R23	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—
R24	0	1	1	0	0	0	DC/DC Operation Setting	00h	O	O	O	O	C
R25	0	1	1	0	0	1	DC/DC Step Setting	16h	O	O	O	O	C
R26	0	1	1	0	1	0	DC/DC Oscillation Setting	15h	O	O	O	O	C
R27	0	1	1	0	1	1	Regulator Output Setting	2Ah	O	O	O	O	C
R28	0	1	1	1	0	0	Power Supply Function LPM Setting	00h	O	O	O	O	C

Remark 1. o:valid, —:invalid, Δ1:only bit3 is invalid, Δ2:only bit7 is valid

Remark2. Internal setting timing is the timing a command becomes valid.

C: Valid when command is set.

F: Valid at the top of the frame.

L: Valid at the top of the line.

Note1. Bit0 becomes valid when the line is set, bit3 becomes valid when the frame is set, other bits become valid when the commands are set.

Note2. Hard-reset is valid at bit4 and bit5. Other bits are invalid.

Table 9-1-2: Command Register List (2/2)

Register No.	D7 to D0						Register Name	Initial Value	Timing Generator Function		Reset		Internal Set Timing D0
	D5	D4	D3	D2	D1	D0			Assigned	Unassigned	Command	Hard	
R29-R32	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—
R33	1	0	0	0	0	1	DC/DC start-up setting	00h	O	O	O	O	C
R34-35	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—
R36	1	0	0	1	0	0	RSW_O Start Timing Setting	0Fh.	O	—	O	—	C
R37	1	0	0	1	0	1	RSW_O End Timing Setting	1Dh.	O	—	O	—	C
R38	1	0	0	1	1	0	GSW_O Start Timing Setting	1Eh	O	—	O	—	C
R39	1	0	0	1	1	1	GSW_O End Timing Setting	2Ch	O	—	O	—	C
R40	1	0	1	0	0	0	BSW_O Start Timing Setting	2Dh	O	—	O	—	C
R41	1	0	1	0	0	1	BSW_O End Timing Setting	3Bh	O	—	O	—	C
R42	1	0	1	0	1	0	EXT1_OStart Timing Setting	0Ah	O	—	O	—	C
R43	1	0	1	0	1	1	EXT1_O End Timing Setting	0Ah	O	—	O	—	C
R44	1	0	1	1	0	0	EXT2_O Start Timing Setting	0Ah	O	—	O	—	C
R45	1	0	1	1	0	1	EXT2_O End Timing Setting	0Ah	O	—	O	—	C
R46	1	0	1	1	1	0	EXT3_O Start Timing Setting	0Ah	O	—	O	—	C
R47	1	0	1	1	1	1	EXT3_O Start Timing Setting	0Ah	O	—	O	—	C
R48	1	1	0	0	0	0	EXT1, EXT2, EXT3 Function Setting	80h	O	Δ2	O	—	C
R49	1	1	0	0	0	1	GOE1 Start Timing Setting	04h	O	—	O	—	C
R50	1	1	0	0	1	0	GOE1 End Timing Setting	38h	O	—	O	—	C
R51	1	1	0	0	1	1	Dummy Line Setting	00h	O	—	O	—	F
R52-R53	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—
R54	1	1	0	1	1	0	COM2, VCLAMP Control	00h	O	O	O	O	C
R55	1	1	0	1	1	1	Test Mode Setting	00h	O	O	O	—	C
R56-R255	—	—	—	—	—	—	Disabled (Unassigned)	—	—	—	—	—	—

Remark 1. O:valid, —:invalid, Δ1:only bit3 is invalid, Δ2:only bit7 is valid

Remark 2. Internal setting timing is the timing a command becomes valid.

C: Valid when command is set.

F: Valid at the top of the frame.

L: Valid at the top of the line.

Note1. Bit0 becomes valid when the line is set, bit3 becomes valid when the frame is set, other bits become valid when the commands are set.

Note2. Hard-reset is valid at bit4 and bit5. Other bits are invalid.

(9-2) Serial interface operation specifying register

Function of serial interface operation specifying register is shown in Table9-2.

Table 9-2: Serial Interface Operation Specifying Register (A7~A0) / Function Explanation

No.	Bit Name	Functions
A7	-	Set to 0.
A6	-	Set to 0.
A5	Read/ Write Selection Bit	It selects whether the data transmission of D7~D0 becomes read operation or write operation. Read operation is only possible to the driver register. 0: D7~D0 is write operation. 1: D7~D0 is read operation.
A4	-	Set to 0.
A3	-	Set to 0.
A2	-	Set to 0.
A1	-	Set to 0.
A0	Command/ Data Selection	It selects whether the data of D7~D0 is the specified data of register number of command register or setting data for command register. 0: D7~D0 is register number. 1: D7~D0 is register setting value.

(9-3) Switching Register Between 65K/260K Colors

Select the color number of one pixel (65,536 colors or 262,144 colors) and data transmission process during 262,144 colors.

If 262,144 colors two times transmission is selected, period of one pixel data transmission takes two times of one transmission (if the dot clock frequency is same.). Therefore, if the frame frequencies of one transmission and two-times transmission are the same, dot clock frequency of two-times transmission should be twice of one transmission.

This register reflects the value from the next frame operation after setting register value.

Table 9-3: Switching Register between 65K/260K Colors (R0)

Register Setting Value	Functions
00h	65,536 colors: Data transmission mode is 16-bit one-time transmission
01h[NOTE]	262,144 colors: Data transmission mode is 12 bits + 6 bits two-times transmission
02h[NOTE]	262,144 colors: Data transmission mode is 9 bits +9 bits two-times transmission
03h	262,144 colors: Data transmission mode is 18-bit one-time transmission
04h to FFh	Disabled

The relation of data transmission process and display data input terminal (R0-R5, G0-G5, B0-B5) is shown below. Underlined **Red5**, **Green5**, and **Blue5** are data lines which need to be inputted during 8 colors mode.

Table 9-3-2 Data transmission process and display data input terminal ("-" means input data invalid.))

Display Data Input Terminal	65,536 Colors	262,144 Colors				
		Once Transmission on 18bit	Twice Transmission of 12 bits + 6 bits		Twice Transmission of 9 bits + 9 bits	
			First Transmission on	Second Transmission on	First Transmission on	Second Transmission on
R5	**Red5**	**Red5**	**Red5**	**Blue5**	**Red5**	Green2
R4	Red4	Red4	Red4	Blue4	Red4	Green1
R3	Red3	Red3	Red3	Blue3	Red3	Green0
R2	Red2	Red2	Red2	Blue2	Red2	**Blue5**
R1	Red1	Red1	Red1	Blue1	Red1	Blue4
R0	- Note	Red0	-	-	-	-
G5	**Green5**	**Green5**	Red0	Blue0	Red0	Blue3
G4	Green4	Green4	-	-	**Green5**	Blue2
G3	Green3	Green3	-	-	Green4	Blue1
G2	Green2	Green2	**Green5**	-	Green3	Blue0
G1	Green1	Green1	Green4	-	-	-
G0	Green0	Green0	Green3	-	-	-
B5	**Blue5**	**Blue5**	Green2	-	-	-
B4	Blue4	Blue4	Green1	-	-	-
B3	Blue3	Blue3	Green0	-	-	-
B2	Blue2	Blue2	-	-	-	-
B1	Blue1	Blue1	-	-	-	-
B0	- Note	Blue0	-	-	-	-

Note: There is no need to input data to R0 and B0 terminals during 65,536 colors, but each of them does amplifier output as if it is inputted the same data as inputted data in R5 and B5.

(9-4) Horizontal Period Valid Data Input Starting Timing Setting Register

It sets the timing to start inputting valid data during horizontal period of Hsync and Vsync mode.

Specifically, it sets the dot clock number from the falling edge of Hsync signal until the input data becomes valid. If twice transmission of display data was selected, set 1/2 of the value actually needed for the dot clock number. This register reflects the value from the next frame operation after setting register value.

Table 9-4: Horizontal Period Valid Data Input Starting Timing Setting Register (R1)

Register Setting Value	Dot Clock Number
00h	4 Clock
01h	4 Clock
:	:
04h	4 Clock
05h	5 Clock
06h	6 Clock
07h	7 Clock
:	:
FDh	253 Clock
FEh	254 Clock
FFh	255 Clock

(9-5) Vertical Period Valid Data Input Starting Timing Setting Register

It sets the timing to start inputting valid data during vertical period of Hsync and Vsync mode.

Specifically, it sets the Hsync number from the falling edge of Vsync signal until the input data becomes valid.

This register reflects the value from the next frame operation after setting register value.

Table 9-5: Vertical Period Valid Data Input Starting Timing Setting Register (R2)

Register Setting Value	Hsync Number
00h	2
01h	2
02h	2
03h	3
04h	4
05h	5
06h	6
:	:
FDh	253
FEh	254
FFh	255

(9-6) Horizontal Valid Pixel Data Number Register

It sets the data number of valid pixel data during horizontal period of Hsync and Vsync mode. This register reflects the value from the next frame operation after setting register value.

Table 9-6: Horizontal Valid Pixel Data Number Register (R3)

Register Setting Value	Valid Data Number
00h	240
01h	244
02h	480
03h	488

(9-7) Standby Register

It sets input/return to standby mode. The data which is set to bit 7-1 will be ignored.

When standby command is inputted, after issuing command, driver starts white display from the next frame (outputs VSS level by source output and COMC). After executing this command, execute commands of regulator off and DC/DC converter off to the power supply function. To cancel the standby, on the contrary to the standby input operation, execute commands of DC/DC converter ON and regulator ON first, then issue the normal operation command (R4="0").

Table 9-7: Standby Register (R4)

Bit 0 Setting Value	Mode
0	Normal Operation Mode
1	Standby Mode

(9-8) 8 Colors Mode Register

It sets switching to 8 colors mode. The data which is set to bit 7-1 will be ignored. Data line to be inputted during 8 colors mode depends on the selection of 65K and the variety of transmission mode of 260K colors. Refer to Table 9-4 for the specific data line to use.

This register reflects the value from the next line operation after setting register value.

Table 9-8: 8 Colors Mode Register (R5)

Bit 0 Setting Value	Mode
0	65K/260K Colors (R0 register is valid)
1	8 Colors Mode

(9-9) Various Setting Register

It sets driver output low power mode, scan direction etc. The data which is set to bit 6 and bit 7 will be ignored.

Table 9-9: Various Setting Register (R6)

Bit Name	Mode
Bit0	It can adjust driver bias current (of driver) and shift to low power mode. Sufficient panel evaluation should be done because the operational amplifier slew rate of internal IC will change. This bit reflects the value from the next line operation after setting register value. Bit0=0: Driver output low power mode Bit0=1: Normal mode
Bit1	Switching of up and down scan direction of the gate can be done by using GRL_0 terminal and GSTB_0 terminal. This bit is executed as soon as being set. Therefore, setting of this bit should be done after one frame gate scan has finished and before the next frame scan starts. This bit is reflected to the operation just after setting register value. Bit1=0: Reverse scan (scan from the bottom to the top, GRL_0=low output) Bit1=1: Forward scan (scan from the top to the bottom, GRL_0=high output)
Bit2	Select whether the display data inputted to driver should be inputted to S3→S242 or S242→S3. <Selected 240 output> <Selected 244 output> Bit2=0:S242→S3 Bit2=0:S244→S1 Bit2=1:S3→S242 Bit2=1:S1→S244 This bit is reflected to the operation just after setting register value.
Bit3	Bit3=0
Bit4	Bit4=1
Bit5	Bit4=1
Bit6, Bit7	Disabled

(9-10) Quarter Data Functional Register

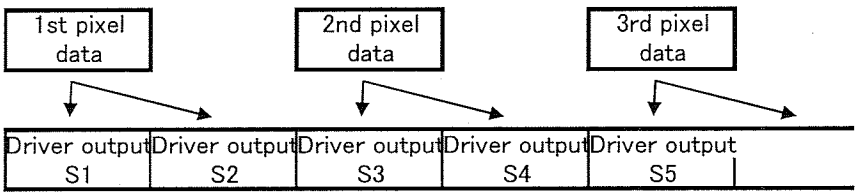
It selects quarter data function by setting bit 0.

Table 9-10: Quarter Data Function Register (R9)

Bit0	Mode
0	Normal Operation
1	Quarter Data Function Operation

When quarter data function is selected, inputted one pixel data is also used as the next one pixel data. The next data inputted from outside becomes pixel data spacing one pixel amount of the data inputted just before.

<When quarter data is chosen>



<Normal Operation>

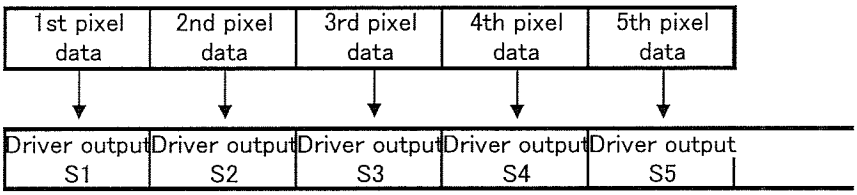


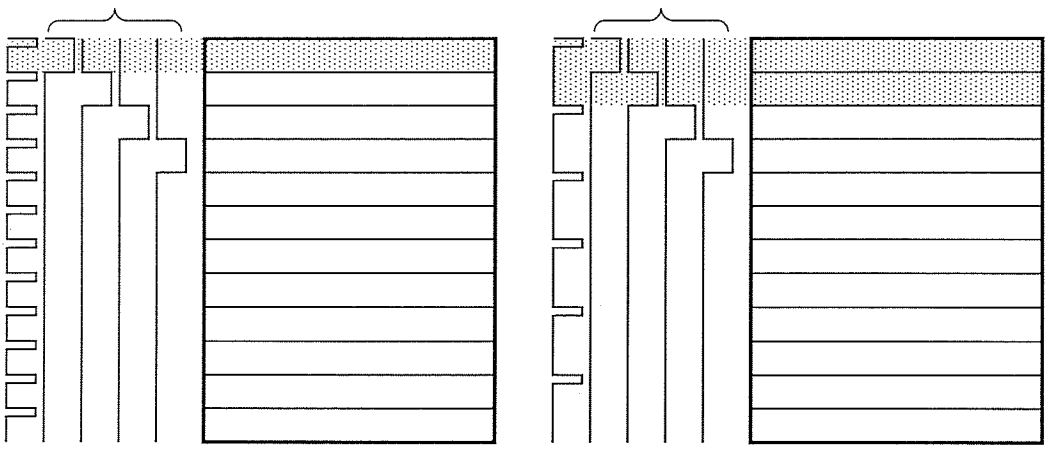
Diagram 9-1: Quarter Data Function

Normal Operation Mode

One execution of gate scan during one horizontal period.

Quarter Data Function Mode

Two execution of gate scan during one horizontal period.



When quarter data is functioning, during one line of horizontal period, it does two lines amount of data output and gate scanning.

Diagram 9-2: Gate Scan Operation during Quarter Data Function

(9-11) Command Reset Register

Command register is initialized by setting bit 0. The data which is set to bit 7-1 will be ignored.

Command reset is canceled automatically after setting. This register reflects the value to the operation after setting register value.

Table 9-11: Command Reset Register (R15)

Bit0	Mode
0	Normal Operation
1	Command Reset

10. Recommended Sequences

(10-1) Power Supply Sequence

1. Turn the VCC/ VDC Power ON
2. Fix Reset terminal to L
3. Fix the Logic signal at initial level

DCLK=L, HSY=H, VSY=H, R0 to R5, G0 to G5, B0 to B5=LorH

CS=L, SCLK=L, SI=LorH

(10-2) Command Setting Sequence for Display On

Command to change non-display status to display status is shown in the table below.

Table 10-1: Display On Sequence

Step	Timing	Register and Write Value	
RESET signal =L→H			
WAIT=1μs以上			
1		R15=01h	Command Reset
2		R4=01h	
3		R0=03h	
4		R1=1Ch	
5		R2=02h	
6		R9=00h	
7		R10=03h	QVGA display mode
8		R25=18h	
9		R26=15h	
10		R27=48h	
11		R28=00h	
12		R33=10h	
Start output of DCLK, HSY, VSY. (It is desirable not to change the data signal.)			
14		R24=09h	

15		R3=00h	
16		R5=00h	26K colors mode
17		R6=25h	
18		R8=0Eh	
19		R11=05h	
20		R12=00h	
21		R36=01h	
22		R37=0Dh	
23		R38=11h	
24		R39=1Dh	
25		R40=21h	
26		R41=2Dh	
27		R48=80h	
28		R49=01h	
29		R50=36h	
30		R51=00h	
31	Wait=5V		
32		R24=79h	
33	Wait=4V		
35		R27=49h	
36	Wait=4V		
37		R24=7Dh	
38	Wait=5V		
39		R54=03h	
41		R4=00h	
42		R12=58h	
43		R33=00h	
44	Wait=1V		
45	VSYNC	R6=35h	Display start

Note: Contact our company previously if you want to change this sequence.

This setting is applied when HSY, VSY, and DCLK is the value below.

1DCLK=5.376MHz(TYP) or 5.525MHz(TYP)

1H=270DCLK, thp=2DCLK, thb=26DCLK, thf=2DCLK

1V=328H, tvp=1H, tvb=1H, tvf=2H

(10-3) Command setting sequence for display off

Command to change display status to non-display status is shown in the table below.

Table 10-2 Display off sequence

Step	Timing	Register and Write Value	
	White data display (3V)		
0		R12=00h	
1		R4=01h	
2		R54=00h	
3	Wait=2V		
4		R24=79h	
5	Wait=1V		
6		R24=39h	
7		R24=48h	
8	Wait=2V		
9		R24=00h	
10	Fix the logic signal output level (Same as sequence 3 during power supply)		
11	Reset signal=H→L		

Note: Contact our company previously if you want to change this sequence.

(10-4) Command Setting Sequence for 8 Colors Driving On (Start)

Command to make 8-color display status is shown in the table below.

Table 10-3: 8-Color Display Sequence

Step	Timing	Register and Write Value	
0	VSYNC	R6=25h	
1		R5=01h	
2		R11=00h	
3		R6=35h	

Note: Contact our company previously if you want to change this sequence.

(10-5) Command Setting Sequence for 8 Colors Driving Off (End)

Command to cancel 8 color-display status and make it 18bpp colors is shown in the table below.

Table 10-4: 8 Colors Display→260K Colors Display Sequence

Step	Timing	Register and Write Value	
0	VSYNC	R6=25h	
1		R5=00h	
2		R11=05h	
3		R6=35h	

Note: Contact our company previously if you want to change this sequence.

(10-6) Command setting sequence for starting quarter mode

Command to make quarter mode status is shown in the table below.

Table 10-5 Quarter mode display sequence

Step	Timing	Register and Write Value	
0	Stopping DCLK, HSY, VSY.		
1	VSYNC	R6=25h	
2		R1=3Ah	
3		R41=31h	
		R40=23h	
		R39=20h	
		R38=12h	
		R37=0Fh	
		R36=01h	
		R8=10h	
		R49=01h	
		R50=39h	
		R9=01h	
	Shifting display data cycle to 120x160 timing and start DCLK, HSY, VSY		
	VSYNC	R6=35h	

Note: Contact our company previously if you want to change this sequence.

This setting is applied when HSY, VSY, and DCLK is the value below.

1DCLK=1.792MHz(TYP)

1H=180DCLK, thp=2DCLK, thb=56DCLK, thf=2DCLK

1V=164H, tvp=1H, tvb=1H, tvf=2H

(10-7) Command setting sequence for canceling quarter mode

Command to cancel quarter mode status is shown in the table below.

Table 10-6 Quarter mode cancellation sequence

Step	Timing	Register and Write Value	
0	Stopping DCLK, HSY, VSY.		
1	VSYNC	R6=25h	
2		R1=1Ch	
3		R8=0Eh	
		R36=01h	
		R37=0Dh	
		R38=11h	
		R39=1Dh	
		R40=21h	
		R41=2Dh	
		R49=01h	
		R50=36h	
		R9=00h	
	Shifting display data cycle to 240x320 timing and start DCLK, HSY, VSY		
	VSYNC	R6=35h	

Note: Contact our company previously if you want to change this sequence.

11. LCD Wiring Diagram

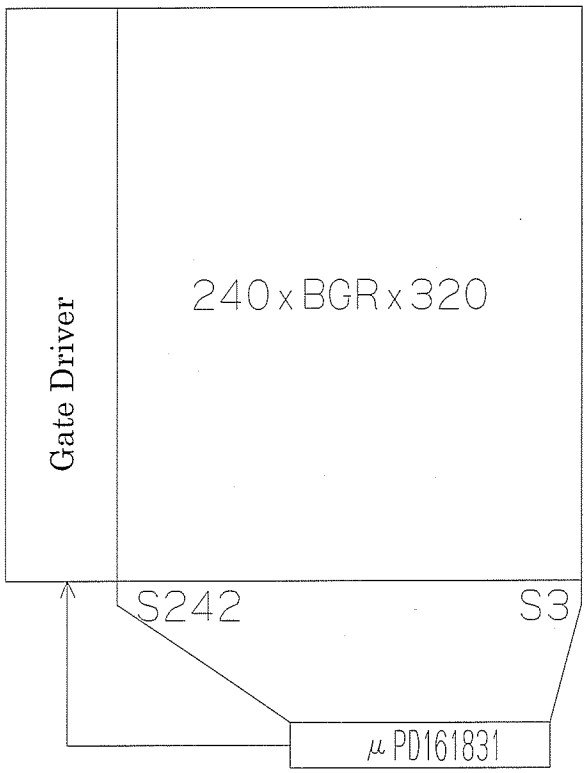
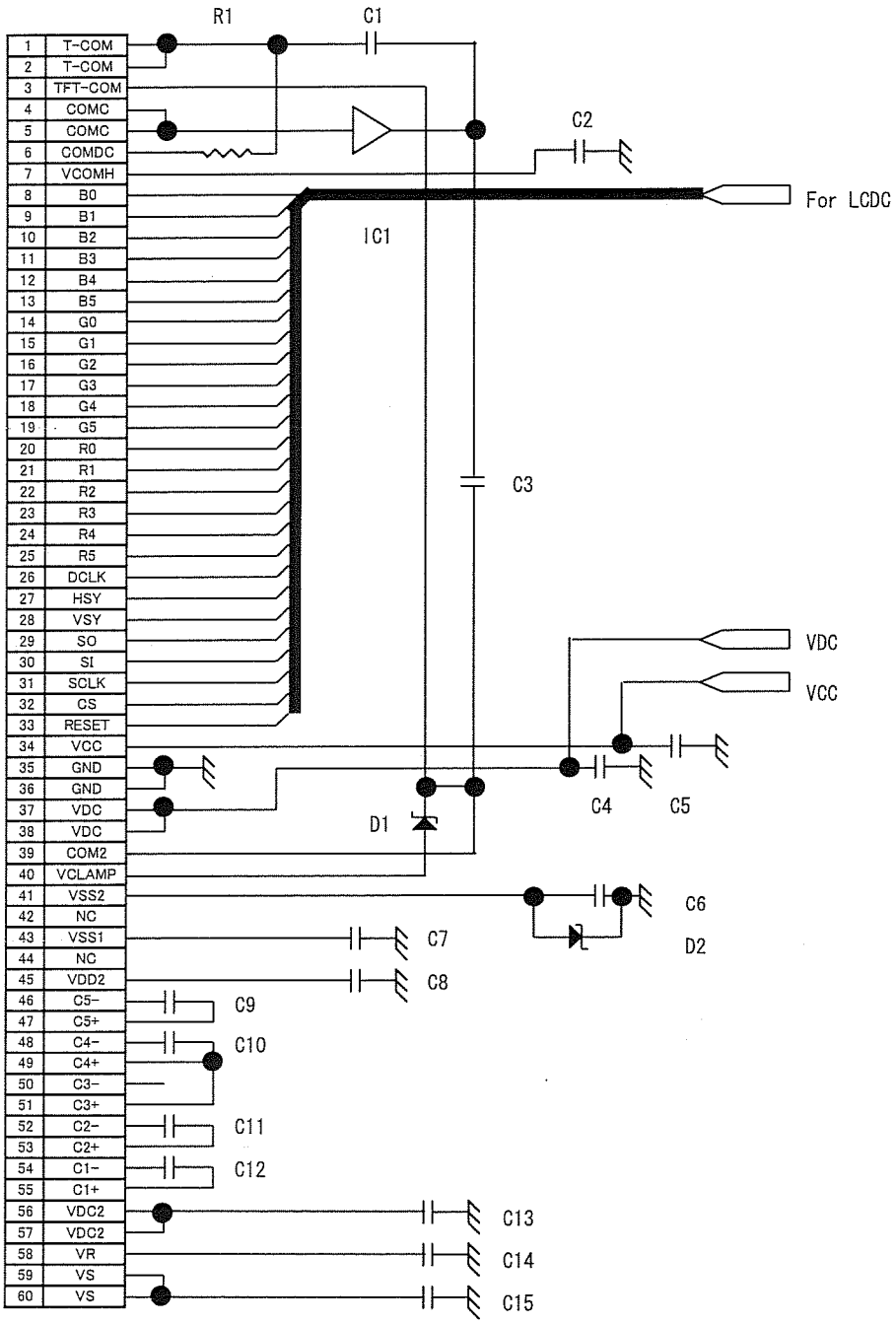


Diagram11-1: LCD Panel Wiring Diagram

12. Example for external circuit



External Circuit Parts List

Ref.No	
R1	56kΩ
C1	4.7uF/6.3V
C2	4.7uF/6.3V
C3	1uF/16V
C4	4.7uF/6.3V
C5	2.2uF/6.3V
C6	1uF/16V
C7	1uF/6.3V
C8	1uF/16V
C9	1uF/10V
C10	1uF/10V
C11	4.7uF/6.3V
C12	4.7uF/6.3V
C13	4.7uF/6.3V
C14	2.2uF/6.3V
C15	4.7uF/6.3V
D1	1SS405
D2	RB520S-30
IC1	Buffer (VHC)

*The circuits and parts above are recommended examples.

Evaluate compatibility with your system when using before designing.

Diagram12-1: External Circuit Diagram (Recommended)

13. FPC circuit diagram

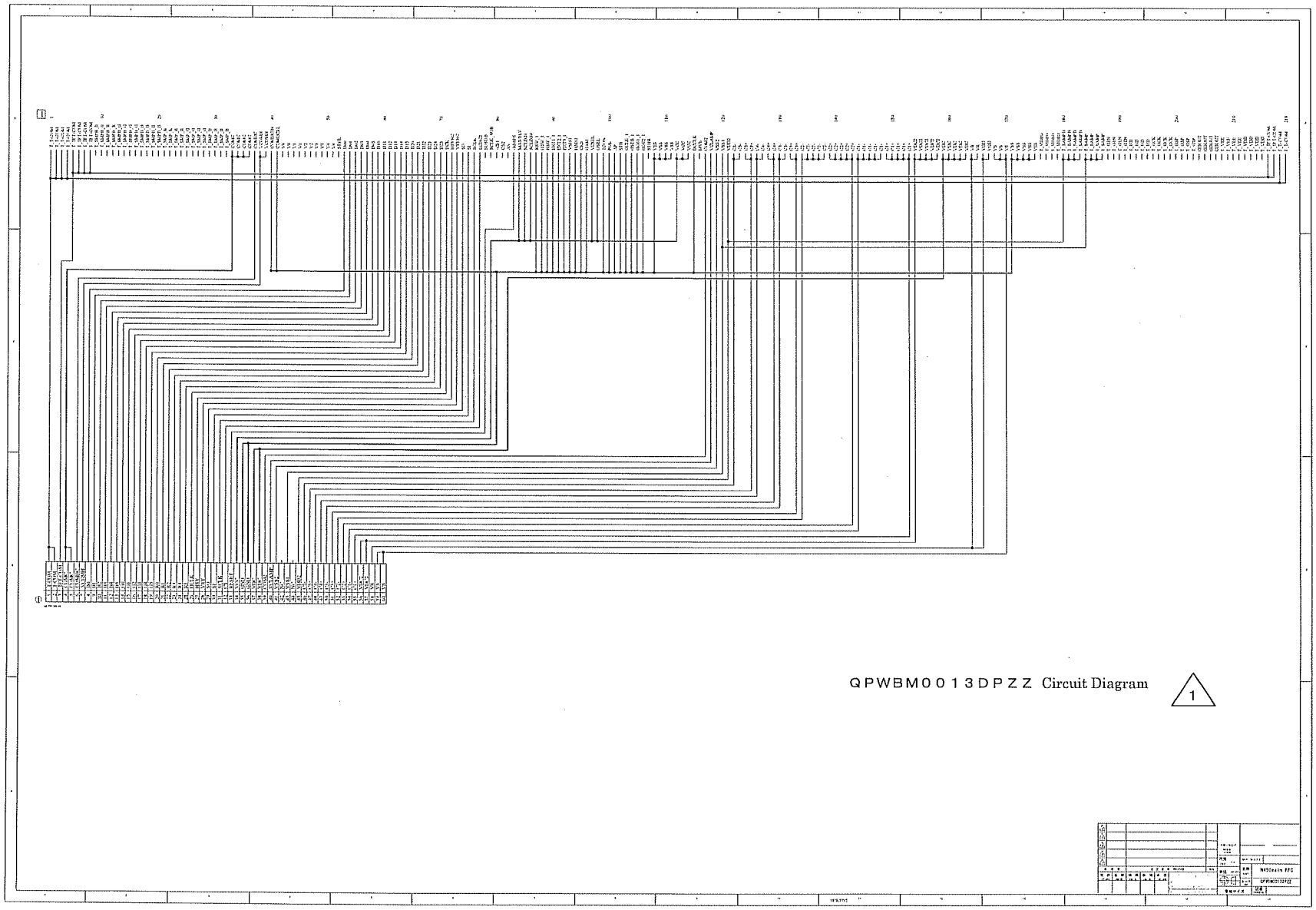


Diagram13-1: FPC Circuit

14. Optical Characteristics

Table 14-1: Optical characteristics

Ta=25°C

	Items		Symbol	Conditions	Min.	Typ.	Max.	Unit	Notes
Transmissive Mode	Transmittance		%	θ=0°	7.0	8.5	-	%	Note2
	Contrast Ratio		Co	θ=0°	70	100	-	-	Note 2, 3
	Viewing Angle Range		θ11	Co≥3	40	45	-	degree (°)	Note 1, 4
			θ12		30	35	-		
			θ21		40	45	-		
			θ22		40	45	-		
	Response Speed	Rising Time	τr		-	13	30	ms	Note 2, 5
		FallingTime	τd		-	35	70		
	Whiteness Shifting Degree		Δx	θ=0° Backlight: (0.290,0.277)	-	-	-	—	Note2
			Δy		-	-	-		
Reflective Mode	Reflectance		%	θ=0°	1.4	2.0	-	%	Note 8, 9
	Contrast Ratio		Co	θ=0°	4.0	8.0	-	-	Note 7, 9
	Viewing Angle Range			Co≥2	40	50	-	degree (°)	Note 1, 6
					40	50	-		
					40	50	-		
					40	50	-		
	Response Speed		τr	θ=0°	-	13	30	ms	Note 5, 6
			τd		-	18	40		
	Whiteness Degree		X	θ=0°	0.270	0.310	0.360	-	Note 9
			Y		0.310	0.350	0.400		

Note 1: Definition of Viewing Angle

θ of maximum contrast is at θ11 direction.

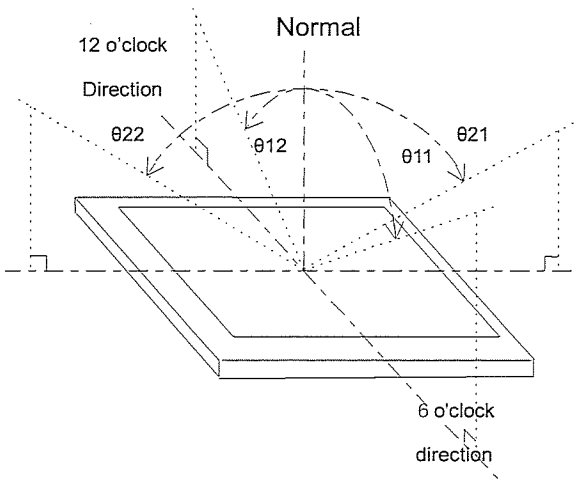
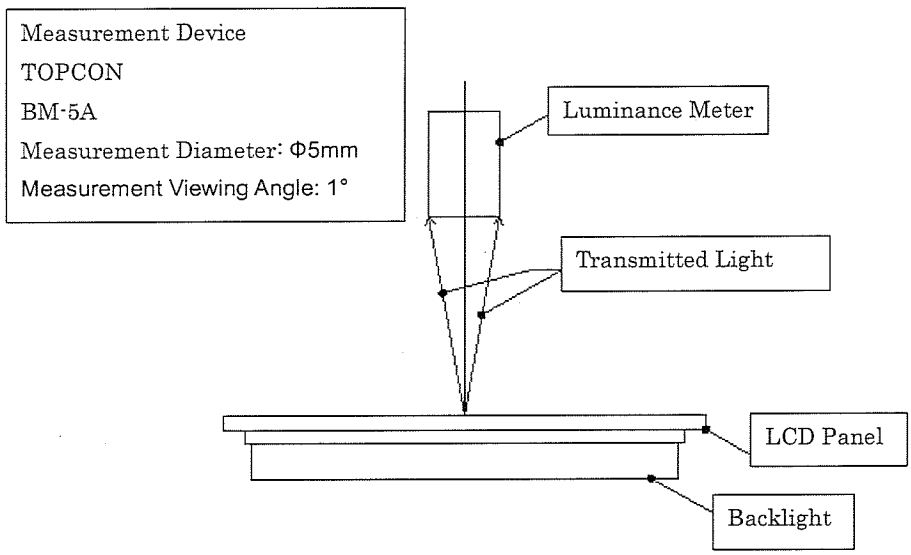


Diagram 14-1: Definition of Viewing Angle

Note 2: Measure luminance at the center of the panel by transmissive optical characteristic method with white display.



Note 3) Transmissive contrast rate is defined as below.

$$\text{Contrast Ratio} = \frac{\text{Output of receiving part while White}}{\text{Output of receiving part while Black}}$$

Note 4) Measurement by Ez-Contrast, simplified measuring device for viewing angle made by Nagase & Co.,Ltd.

Note 5) Response speed is defined as below.

Adding input signal of White or Black, and measure the time change of the photodetector output value then.

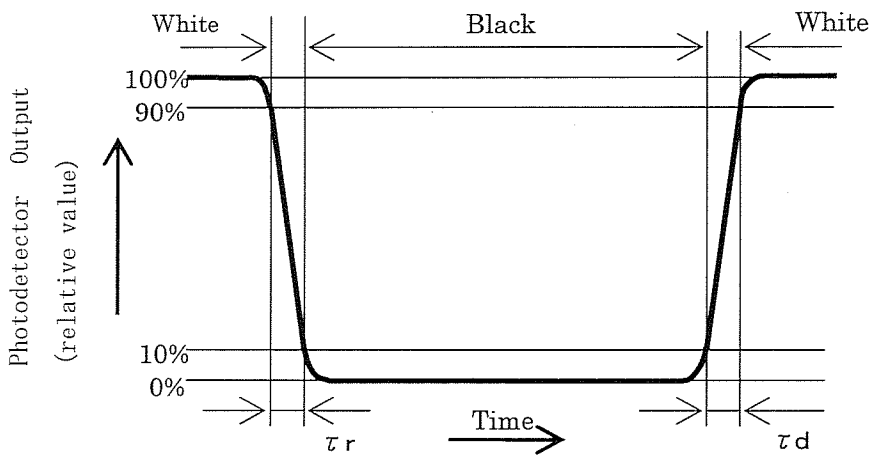
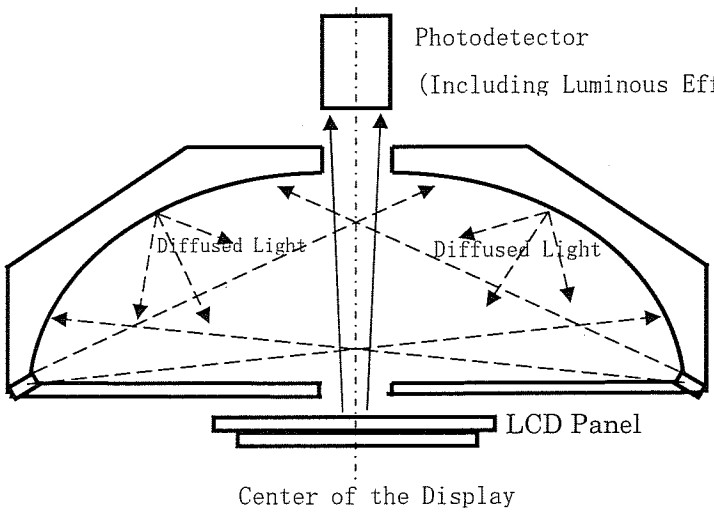


Diagram14-3: Definition of Response Speed

Note 6 Measure reflective mode viewing angle range by optical characteristics measurement method below.



Measurement Device : LCD5200(Ohtsuka)

Device14-4: Measurement Method of Catoptoric Characteristics

Note 7: Reflective contrast ratio is defined as below.

$$\text{Contrast Ratio} = \frac{\text{Reflectance of center of the display while White}}{\text{Reflectance of center of the display while Black}}$$

Note 8: Reflectance is defined as below.

$$\text{Reflectance} = \frac{\text{Reflected light intensity of LCD panel when applying no voltage}}{\text{Reflected light intensity of standard white board}}$$

Note 9) Measurement by MINOLTA spectral chromatometer CM-2002

White display chromaticity of LCD panel with reference to light source (D65)

Light Source Chromaticity: (X, Y) = (0.313, 0.329)

15. Mechanical Performance

(15-1) Appearance: External dimensions are shown in Diagram 15-1.

(15-2) FPC Performance

(1) Compatible Connecter

JAE FF02 series 0.3mm pitch 60 pins connector

(2) FPC Elasticity

Bending test should be done with bending radius 0.6mmR and bending angle 180°, and should not break with less than 30 times bending.

16. Handling of TFT-LCD modules

(16-1) Connecting and disconnecting FPC to connector

Make sure to cut off the power supply of the set side (cabinet side) when connecting and disconnecting FPC to connector.

(16-2) Handling of FPC

(1) Bending R of FPC should be 0.6mm or more and homogeneous.

Do not bend FPC to the front polarizer side at the connecting part of LCD panel.

(2) Do not hang LCD module holding FPC or apply any forcing power.

(16-3) Mounting modules

(1) When attaching module to the device, if it contacts directly with drivers and substrates, electrical leak may occur.

(2) Fix at the same plane to mount and avoid adding stress to the module like warp and twist.

If you have to hold LCD module surface for mounting, pay attention not to apply mechanical stress excessively to the LCD module.

(3) For the design of a set without protection board at the front panel to reduce plate reflection, you should design to absorb static electricity by enclosing to the rim of the polarizer by cabinet of the set and stick grounded conductive sheet etc. at the backside because applied static electricity at the outer region of the panel may cause electrostatic discharge damage. (Refer to Diagram 16-1)

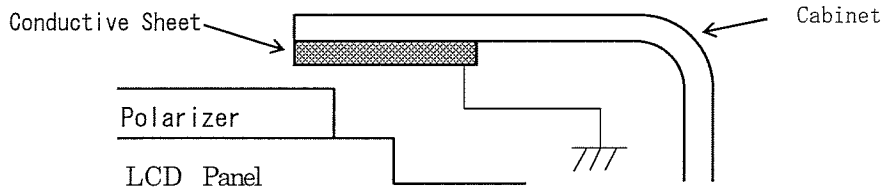


Diagram16-1

17. Reliability Test Requirements

Reliability Test Requirements are shown in Table 17-1.

There should not be any changes in standard condition which interfere with actual using under display quality test conditions.

Table17-1: Reliability

	Test Item	Contents
1	High Temperature Storage	Ta=70℃ 240h
2	Low temperature Storage	Ta=－20℃ 240h
3	High Temperature & High Humidity Operation	Tp=40℃, 95%RH 240h
4	High Temperature Operation	Tp=60℃ 240h
5	Low Temperature Operation	Tp=－10℃ 240h
6	Electrostatic Pressure Resistance	±200V, 200pF(0Ω) Once per each terminal
7	Thermal Shock	Ta=－20℃ to ＋70℃ x 5 cycle (1h) (1h)

【Note】Ta=Ambient Temperature、Tp=Panel Temperature

(Evaluation Method)

There should not be any changes in standard condition which interfere with actual using under display quality test conditions.

18. Shipping Form

(18-1) Carton Preservation Requirement

(1) Number of Cartons to pile up: Max.8 Cartons

Maximum Storage Number: 300

(2) Environment

- Temperature: 0-40□
- Humidity: 60%RH or less (at 40□)

No condensation should occur even under low temperature and high humidity.

- No toxic gas should be detected which harms electronic parts and wiring material like acid and alkali.
- Period: About three month
- Opening packages: Open the package with effective countermeasure like electrostatic grounding after conditioning humidity to 50%RH or more to avoid damage by static electricity to the LCD modules when opening the package.

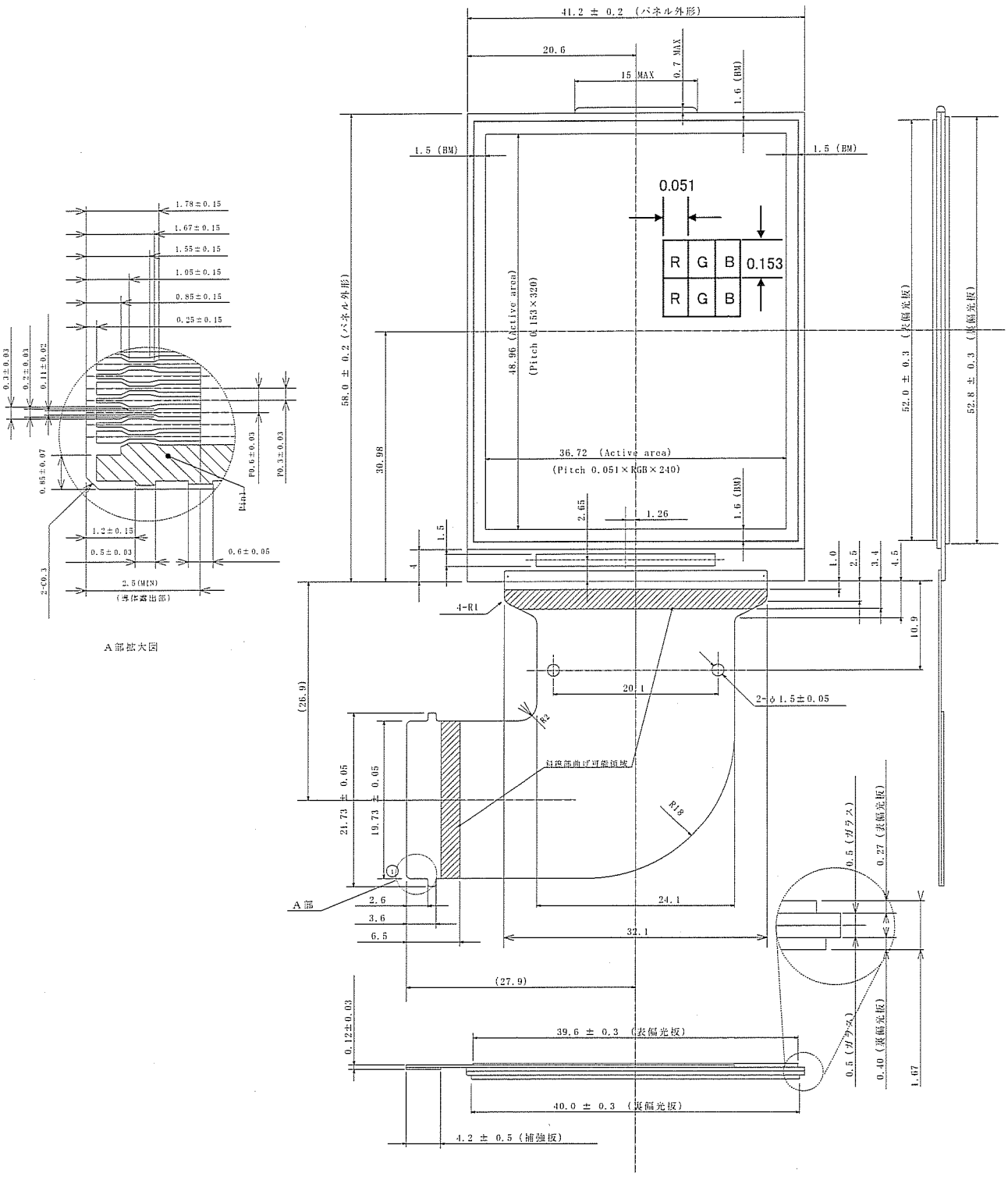
19. Packaging Form

Packaging form is shown in Diagram19-1.

Regarding the packing, it is designed to protect modules from breakage during transportation.

20. Display Quality

The display quality standard of the color LCD module is compliant with shipping inspection guideline.



1) The appearance guaranteed area is the display area (the screen size).

2) The outside shape of LCD panel might have partial projection or chipping.
They will be included in the tolerance of the panel outer dimensions.

3) The dimensions (numbers) are reference values.

4) Tolerances other than specified are +/- 0.4mm.

Diagram 15-1: Outline Drawing

1