1. Description

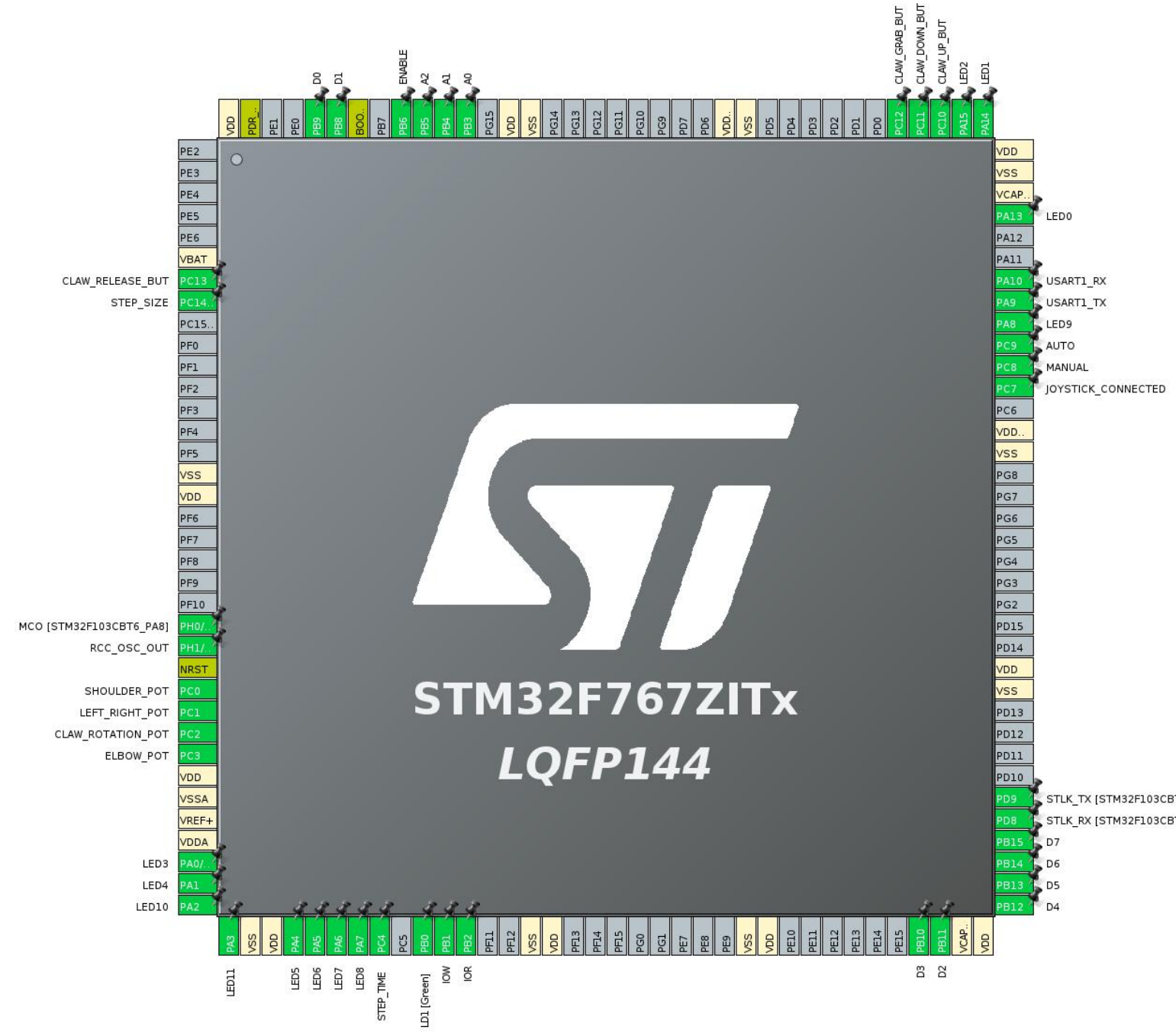
1.1. Project

Project Name	ROBKO_01_F767
Board Name	NUCLEO-F767ZI
Generated with:	STM32CubeMX 5.4.0
Date	09/22/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x7
MCU name	STM32F767ZITx
MCU Package	LQFP144
MCU Pin number	144

2. Pinout Configuration



3. Pins Configuration

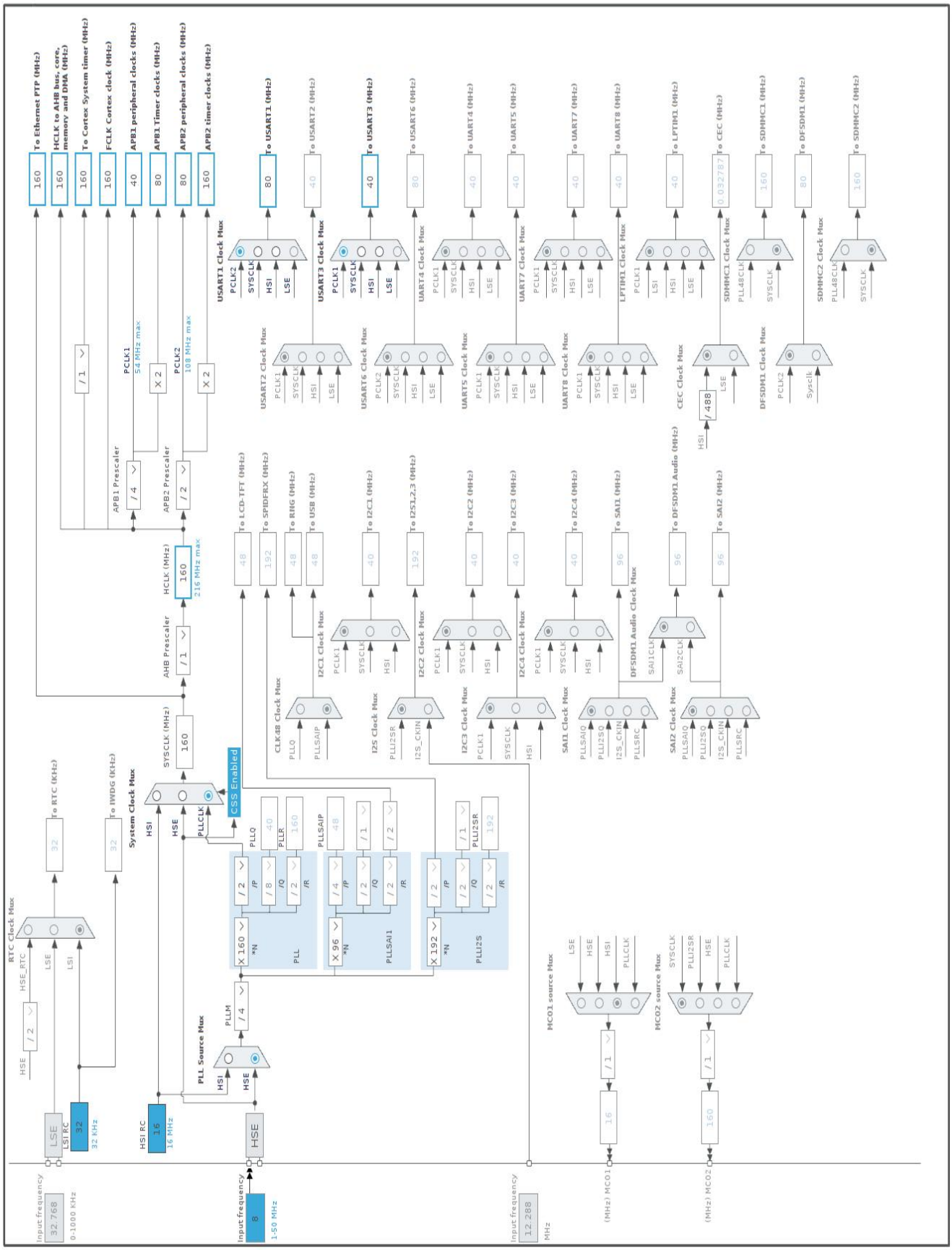
Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Input	CLAW_RELEASE_BUT
8	PC14/OSC32_IN *	I/O	GPIO_Input	STEP_SIZE
16	VSS	Power		
17	VDD	Power		
23	PH0/OSC_IN	I/O	RCC_OSC_IN	MCO [STM32F103CBT6_PA8]
24	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
25	NRST	Reset		
26	PC0	I/O	ADC1_IN10	SHOULDER_POT
27	PC1	I/O	ADC1_IN11	LEFT_RIGHT_POT
28	PC2	I/O	ADC1_IN12	CLAW_ROTATION_POT
29	PC3	I/O	ADC1_IN13	ELBOW_POT
30	VDD	Power		
31	VSSA	Power		
32	VREF+	Power		
33	VDDA	Power		
34	PA0/WKUP *	I/O	GPIO_Output	LED3
35	PA1 *	I/O	GPIO_Output	LED4
36	PA2 *	I/O	GPIO_Output	LED10
37	PA3 *	I/O	GPIO_Output	LED11
38	VSS	Power		
39	VDD	Power		
40	PA4 *	I/O	GPIO_Output	LED5
41	PA5 *	I/O	GPIO_Output	LED6
42	PA6 *	I/O	GPIO_Output	LED7
43	PA7 *	I/O	GPIO_Output	LED8
44	PC4 *	I/O	GPIO_Input	STEP_TIME
46	PB0 *	I/O	GPIO_Output	LD1 [Green]
47	PB1 *	I/O	GPIO_Output	IOW
48	PB2 *	I/O	GPIO_Output	IOR
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
69	PB10 *	I/O	GPIO_Output	D3

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
70	PB11 *	I/O	GPIO_Output	D2
71	VCAP_1	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Input	D4
74	PB13 *	I/O	GPIO_Input	D5
75	PB14 *	I/O	GPIO_Input	D6
76	PB15 *	I/O	GPIO_Input	D7
77	PD8	I/O	USART3_TX	STLK_RX [STM32F103CBT6_PA3]
78	PD9	I/O	USART3_RX	STLK_TX [STM32F103CBT6_PA2]
83	VSS	Power		
84	VDD	Power		
94	VSS	Power		
95	VDDUSB	Power		
97	PC7 *	I/O	GPIO_Input	JOYSTICK_CONNECTED
98	PC8 *	I/O	GPIO_Input	MANUAL
99	PC9 *	I/O	GPIO_Input	AUTO
100	PA8 *	I/O	GPIO_Output	LED9
101	PA9	I/O	USART1_TX	
102	PA10	I/O	USART1_RX	
105	PA13 *	I/O	GPIO_Output	LED0
106	VCAP_2	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 *	I/O	GPIO_Output	LED1
110	PA15 *	I/O	GPIO_Output	LED2
111	PC10 *	I/O	GPIO_Input	CLAW_UP_BUT
112	PC11 *	I/O	GPIO_Input	CLAW_DOWN_BUT
113	PC12 *	I/O	GPIO_Input	CLAW_GRAB_BUT
120	VSS	Power		
121	VDDSDMMC	Power		
130	VSS	Power		
131	VDD	Power		
133	PB3 *	I/O	GPIO_Output	A0
134	PB4 *	I/O	GPIO_Output	A1
135	PB5 *	I/O	GPIO_Output	A2
136	PB6 *	I/O	GPIO_Output	ENABLE
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	D1

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
140	PB9 *	I/O	GPIO_Output	D0
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	ROBKO_01_F767
Project Folder	/home/cartogan/Ac6/workspace/ROBKO_01/STM CubeMX/F767
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F7 V1.15.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x7
MCU	STM32F767ZITx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN10

mode: IN11

mode: IN12

mode: IN13

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 10
Sampling Time	**112 Cycles ***
Rank	**2 ***
Channel	**Channel 11 ***
Sampling Time	**112 Cycles ***
Rank	**3 ***
Channel	**Channel 12 ***
Sampling Time	**112 Cycles ***
Rank	**4 ***
Channel	**Channel 13 ***
Sampling Time	**112 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. GFXSIMULATOR

7.2.1. Simulator Graphic:

7.3. GPIO

7.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Over Drive	Disabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 2

7.5. SYS

Timebase Source: SysTick

7.6. USART1

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**9 Bits (including Parity) ***
Parity	**Odd ***
Stop Bits	**2 ***

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.7. USART3

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	SHOULDER_POT
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	LEFT_RIGHT_POT
	PC2	ADC1_IN12	Analog mode	No pull-up and no pull-down	n/a	CLAW_ROTATION_POT
	PC3	ADC1_IN13	Analog mode	No pull-up and no pull-down	n/a	ELBOW_POT
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO [STM32F103CBT6_PA8]
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_RX [STM32F103CBT6_PA3]
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	STLK_TX [STM32F103CBT6_PA2]
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CLAW_RELEASE_BUT
	PC14/OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STEP_SIZE
	PA0/WKUP	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED10
	PA3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED11
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED5
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED6
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED7
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED8
	PC4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STEP_TIME
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD1 [Green]
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IOW
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IOR
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D3
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D2
	PB12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D4
	PB13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D5
	PB14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D6

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	D7
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	JOYSTICK_CONNECTED
	PC8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	MANUAL
	PC9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	AUTO
	PA8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED9
	PA13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PA14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PC10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CLAW_UP_BUT
	PC11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CLAW_DOWN_BUT
	PC12	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	CLAW_GRAB_BUT
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	A0
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	A1
	PB5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	A2
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ENABLE
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D1
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D0

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**Medium ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
USART3 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report