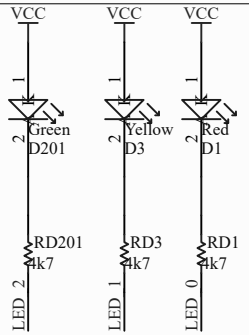

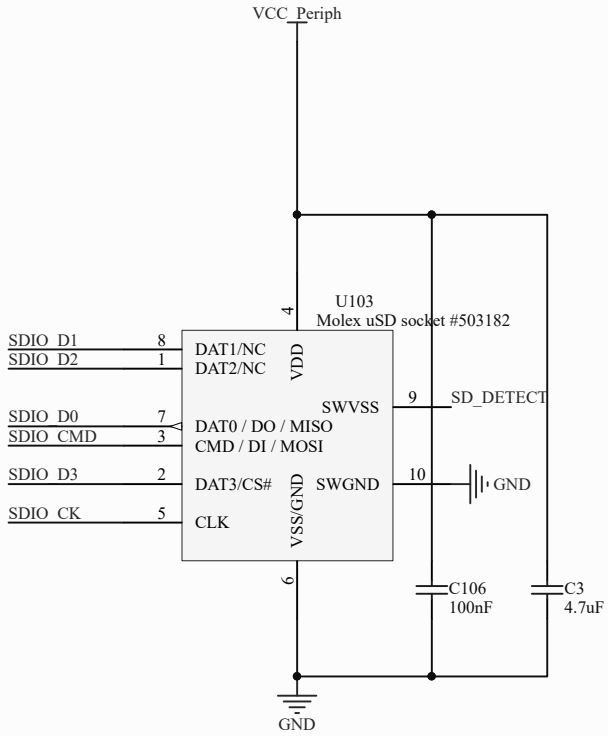

App note AVR042
C = 2xCl - Cs
Cs is 5-10pF in AVR
Cl is crystal load capacitance (crystal datasheet)
C=2x18-5 = 31pF
C=2x18-10=26pF
12pF with 18pF crystal worked (v1)
C=2x10-5=15
C=2x10-10=10
12pF with 10pF crystal for v3
other sources:
Cl = C1C2/(C1+C2)+Cs (Cs=5)
->

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BOOT1	BOOT0	Mode
x	0	Main flash
0	1	System memory
1	1	Embedded SRAM

Pattern1 Boot0(pin) = 1 and Boot1(pin) = 0

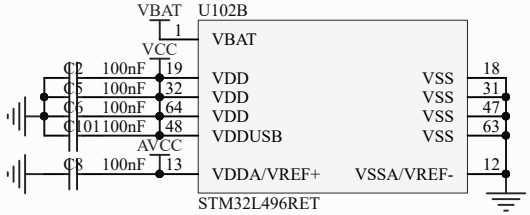
Programming / debug connector:
P_SW_CLK
P_SW_DIO
P_SWO
NRST

PA6 with internal pullup. RTC_INT pulled up to Vbat. Diode protects PA6 from sinking current.

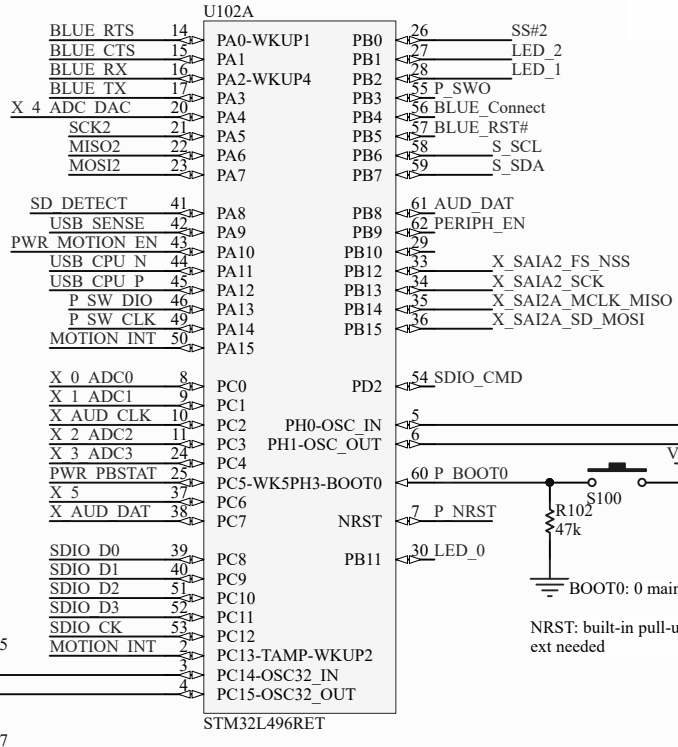
Motion int: must be on a counter and edge detect

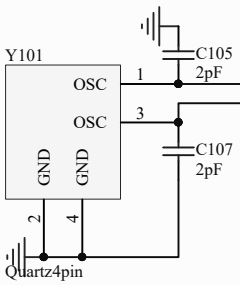
ADC:
PA0: ADC1_IN0
PA1: ADC1_IN1
PA2: ADC1_IN2
PA3: ADC1_IN3
PA4: ADC1_IN4
PA5: ADC1_IN5
PA6: ADC1_IN6
PA7: ADC1_IN7
PB0: ADC1_IN8
PB1: ADC1_IN9

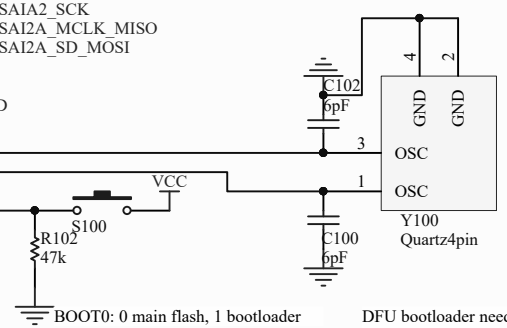
todo:
- pull down on power switch
- bluetooth connect on wake up interrupt
X power low/high control



BT:
- BLUE_TX is output
- BLUE_RTS is output
STM:
- RX is input
- CTS is input







BOOT0: 0 main flash, 1 bootloader

NRST: built-in pull-up, no ext needed

DFU bootloader needs MHz multiple

SPI2: motion sensor:
SPI pins: PB 12, 13, 14, 15
Motion Interrupt: ??
Motion int: must be on a counter and edge detect

I2C main bus: I2C1
SCL: PB8, SDA: PB9

STM32F401 has embedded pull up so DB pull-up not

USB_SENSE: must use 5V-tolerant pin (PA9 is 5V-tol)
USB powered but LTC off -> max 3.6V tolerance
-> use voltage divider

SPI1: SD card
SPI pins: PA4, PA5, PA7, PB4
SPI_SCK with SWO debug wire

USART2: Bluetooth
Pin direction checked.

App note AN2867
CL: specified by manufacturer
ABS04W-32.768KHZ-6-D2-T5:
CL=6pF
Cs = 5pF (AN2867 gives as example)
CL = CL1xCL2/(CL1+CL2)+Cs
CL = CL1^2/2CL1+Cs
2(CL-Cs)=CL1=CL2

CL = 6pF
Cs = 5pF
CL1=CL2 = 2pF

App note AN2867
CL: specified by manufacturer
ABM10-166-12.000MHZ-T3: CL=8pF
Cs = 5pF (AN2867 gives as example)
CL = CL1xCL2/(CL1+CL2)+Cs
CL = CL1^2/2CL1+Cs
2(CL-Cs)=CL1=CL2

CL = 8pF
Cs = 5pF
CL1=CL2 = 6pF

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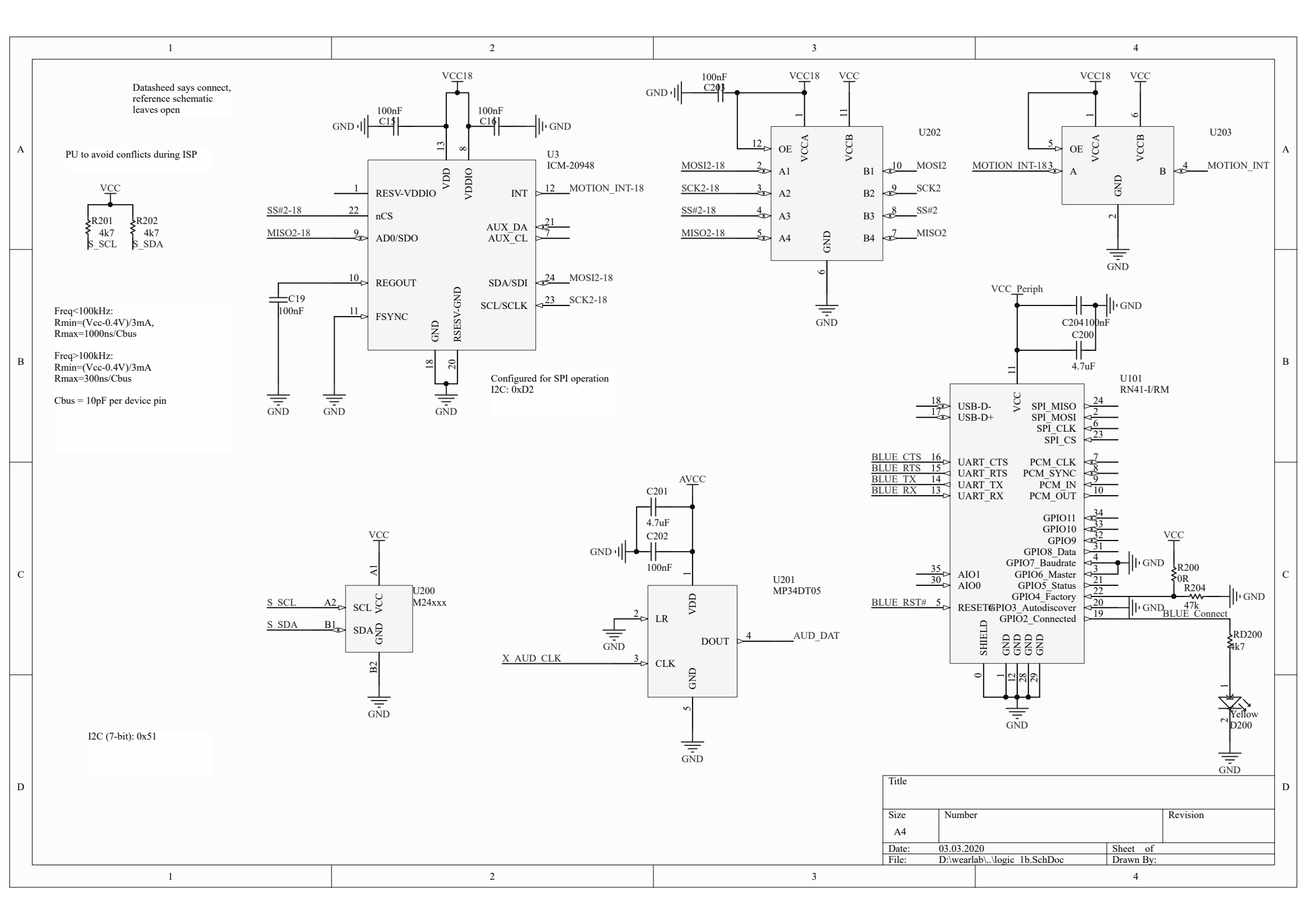
Datasheed says connect, reference schematic leaves open
PU to avoid conflicts during ISP
VCC
R201 4k7 S_SCL
R202 4k7 S_SDA
Freq<100kHz:
Rmin=(Vcc-0.4V)/3mA,
Rmax=1000ns/Cbus
Freq>100kHz:
Rmin=(Vcc-0.4V)/3mA
Rmax=300ns/Cbus
Cbus = 10pF per device pin
I2C (7-bit): 0x51
VCC18
100nF C15
100nF C16
GND
U3
ICM-20948
RESV-VDDIO
VDD
VDDIO
INT
MOTION_INT-18
SS#2-18
nCS
AUX_DA
AUX_CL
MISO2-18
AD0/SDO
REGOUT
SDA/SDI
MOSI2-18
SCL/SCLK
SCK2-18
FSYNC
GND
RSESV-GND
C19 100nF
Configured for SPI operation
I2C: 0xD2
100nF C203
U202
OE
VCCA
VCCB
MOSI2-18
SCK2-18
SS#2-18
MISO2-18
A1
A2
A3
A4
B1
B2
B3
B4
MOSI2
SCK2
SS#2
MISO2
U203
MOTION_INT-18
MOTION_INT
VCC_Periph
C204 100nF
C200 4.7uF
U101
RN41-I/RM
USB-D-
USB-D+
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_CS
BLUE_CTS
BLUE_RTS
BLUE_TX
BLUE_RX
UART_CTS
UART_RTS
UART_TX
UART_RX
PCM_CLK
PCM_SYNC
PCM_IN
PCM_OUT
GPIO11
GPIO10
GPIO9
GPIO8_Data
GPIO7_Baudrate
GPIO6_Master
GPIO5_Status
GPIO4_Factory
GPIO3_Autodiscover
GPIO2_Connected
AIO1
AIO0
BLUE_RST#
RESET
SHIELD
R200 0R
R204 47k
BLUE_Connect
RD200 4k7
Yellow D200
C201 4.7uF
C202 100nF
AVCC
U201
MP34DT05
LR
DOUT
CLK
AUD_DAT
X_AUD_CLK
U200
M24xxx
S_SCL
S_SDA
SCL
SDA
A1
A2
B1
B2
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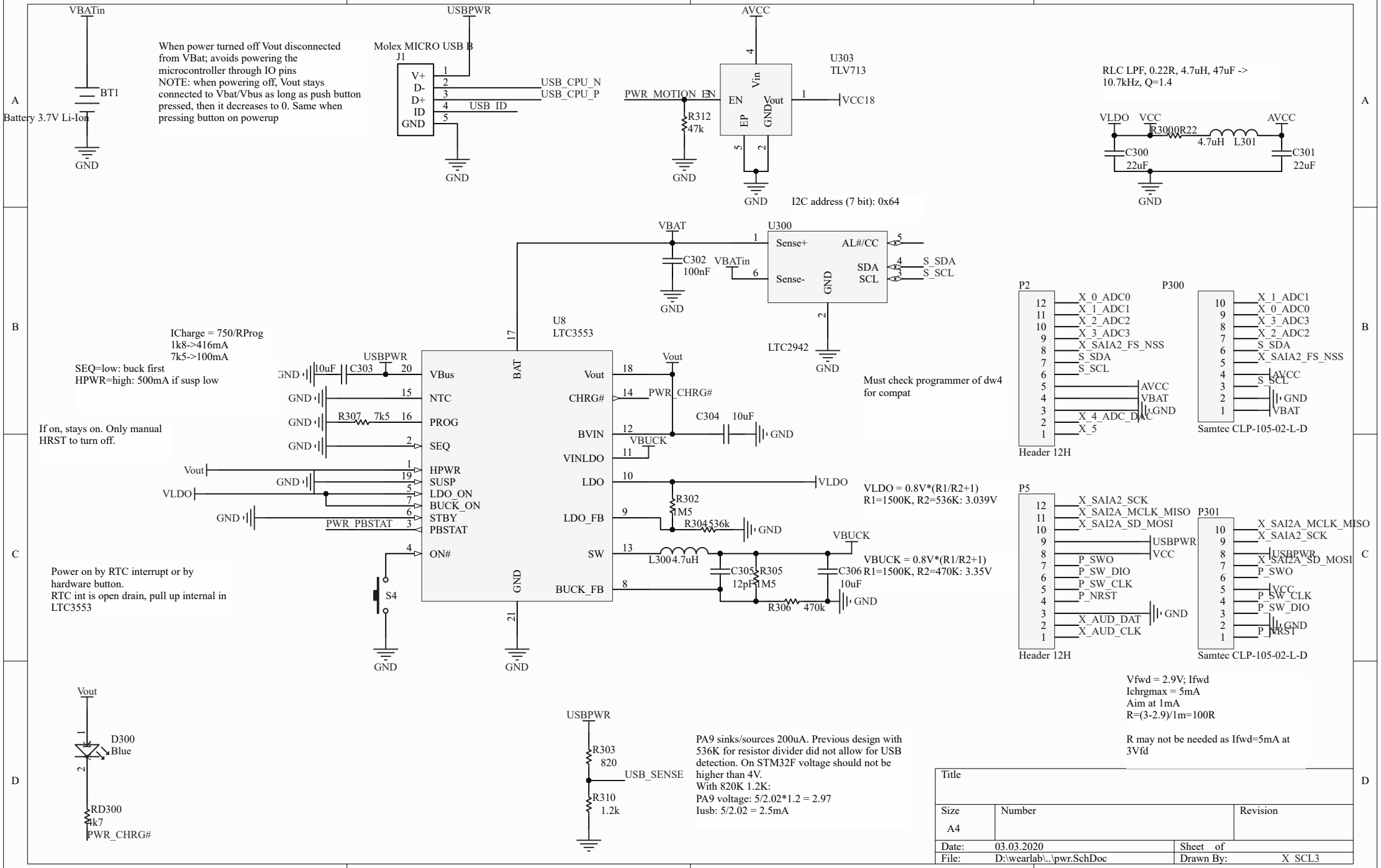
VBATin
BT1
Battery 3.7V Li-Ion
GND
When power turned off Vout disconnected from VBat; avoids powering the microcontroller through IO pins
NOTE: when powering off, Vout stays connected to Vbat/Vbus as long as push button pressed, then it decreases to 0. Same when pressing button on powerup
USBPWR
Molex MICRO USB B
J1
V+
D-
D+
ID
GND
USB_CPU_N
USB_CPU_P
USB_ID
AVCC
U303
TLV713
PWR_MOTION_EN
R312
47k
EN
Vin
Vout
EP
GND
VCC18
I2C address (7 bit): 0x64
RLC LPF, 0.22R, 4.7uH, 47uF -> 10.7kHz, Q=1.4
VLDO
VCC
AVCC
R3000R22
4.7uH
L301
C300
22uF
C301
22uF
VBAT
U300
Sense+
Sense-
AL#/CC
SDA
SCL
S_SDA
S_SCL
C302
100nF
VBATin
LTC2942
U8
LTC3553
ICharge = 750/RProg
1k8->416mA
7k5->100mA
SEQ=low: buck first
HPWR=high: 500mA if susp low
If on, stays on. Only manual HRST to turn off.
Power on by RTC interrupt or by hardware button.
RTC int is open drain, pull up internal in LTC3553
S4
VBus
NTC
PROG
SEQ
HPWR
SUSP
LDO_ON
BUCK_ON
STBY
PBSTAT
ON#
BAT
GND
Vout
CHRG#
PWR_CHRG#
BVIN
VINLDO
LDO
LDO_FB
SW
BUCK_FB
C303
10uF
R307
7k5
C304
10uF
VBUCK
R302
1M5
R304
536k
L300
4.7uH
C305
12pF
R305
1M5
C306
10uF
R306
470k
VLDO
PWR_PBSTAT
Must check programmer of dw4 for compat
VLDO = 0.8V*(R1/R2+1)
R1=1500K, R2=536K: 3.039V
VBUCK = 0.8V*(R1/R2+1)
R1=1500K, R2=470K: 3.35V
P2
Header 12H
X_0_ADC0
X_1_ADC1
X_2_ADC2
X_3_ADC3
X_SAIA2_FS_NSS
S_SDA
S_SCL
AVCC
VBAT
GND
X_4_ADC_DAC
X_5
P300
Samtec CLP-105-02-L-D
X_1_ADC1
X_0_ADC0
X_3_ADC3
X_2_ADC2
S_SDA
X_SAIA2_FS_NSS
AVCC
S_SCL
GND
VBAT
P5
Header 12H
X_SAIA2_SCK
X_SAI2A_MCLK_MISO
X_SAI2A_SD_MOSI
USBPWR
VCC
P_SWO
P_SW_DIO
P_SW_CLK
P_NRST
GND
X_AUD_DAT
X_AUD_CLK
P301
Samtec CLP-105-02-L-D
X_SAI2A_MCLK_MISO
X_SAIA2_SCK
USBPWR
X_SAI2A_SD_MOSI
P_SWO
VCC
P_SW_CLK
P_SW_DIO
GND
P_NRST
Vout
D300
Blue
RD300
4k7
PWR_CHRG#
USBPWR
R303
820
USB_SENSE
R310
1.2k
PA9 sinks/sources 200uA. Previous design with 536K for resistor divider did not allow for USB detection. On STM32F voltage should not be higher than 4V.
With 820K 1.2K:
PA9 voltage: 5/2.02*1.2 = 2.97
Iusb: 5/2.02 = 2.5mA
Vfwd = 2.9V; Ifwd
Ichrgmax = 5mA
Aim at 1mA
R=(3-2.9)/1m=100R
R may not be needed as Ifwd=5mA at 3Vfd
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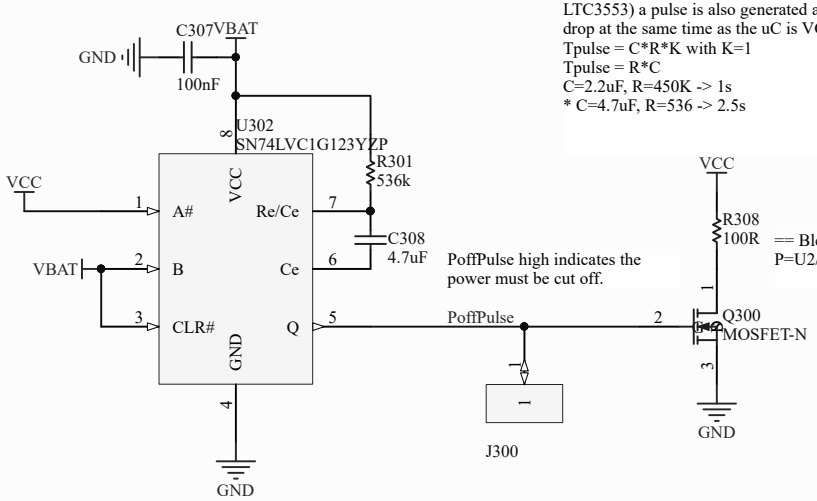
X_SCL3

Has to operate with Vbat: 3.4V-4.3V

== Falling edge detector on PWR_ON==
This generates a positive puse on the falling edge of PWR_ON (CPU controlled) or when VCC drops (e.g. through HRST). PWR_ON is a uC digital out and is pulled up to keep the supply active when the CPU is unprogrammed, in reset, or undergoing programming. Consequently, if VCC falls due to other reasons (e.g. due to a long-press/HRST on the LTC3553) a pulse is also generated as either VCC drops or PWR_ON drops (generally both drop at the same time as the uC is VCC powered).
Tpulse = C*R*K with K=1
Tpulse = R*C
C=2.2uF, R=450K -> 1s
* C=4.7uF, R=536 -> 2.5s

ON semi NSR05F40NXT5G has
Vf=0.1V 75C
Vf=0.2V 25C
Vf=0.3V -25C

Input voltage range: 3.4-4.3
Output voltage range: 2.5-4.0V

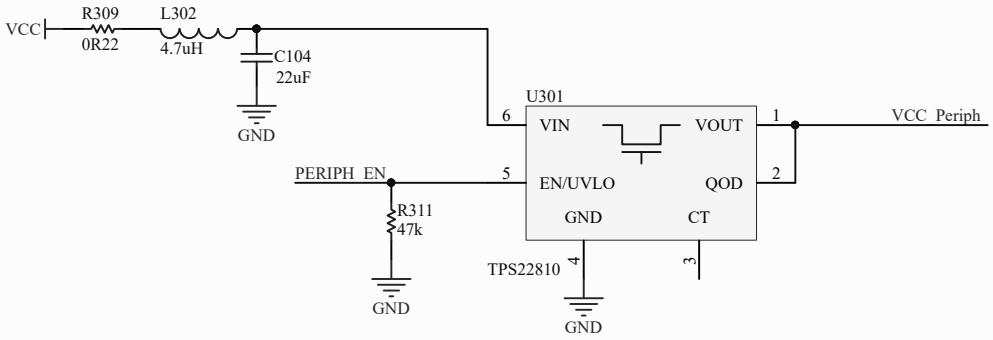


== Bleeder circuit ==
P=U2/R=90mW

Put NMOS transistor to discharge
NXP PMZ200UNE

== Power circuit ==
There are 4 cases:
A. Power is off, pwron through extpwr or PB
B. Power is off, pwron through RTC interrupt
C. Power is on, pwroff through CPU (pull up/down pwron)
D. Power is on, pwroff through hrst (long-press pb)

Power switch TPS22810



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