Version change history

version number	date	description
V0.2	2013 year 1 month 25 day EG8030	Internal test version of data sheet. This version is for internal testing only!

table of Contents

EG8030 Chip data sheet

1. Features

- 5V single power supply
- External 16MHz crystal oscillator
- Four working modes of pin configuration
  - Three-phase synchronous open-loop voltage regulation
  - Three-phase synchronous closed-loop voltage regulator
  - Three-phase independent open-loop voltage regulation
  - Three-phase independent closed-loop voltage regulator
- Real-time processing of voltage, current and temperature feedback
- Overvoltage, undervoltage, overcurrent, short circuit, overheat protection function
- Pin 3S soft start
- Phase sequence reversal function
- Phase clear function
- All the way LED status indication and buzzer alarm
- One basic frequency output and one sinusoidal analog signal output
- One fan control output
- Pin set 2 kinds of three-phase pure sine wave output frequency:
  - 50Hz pure sine wave fixed frequency
  - 60Hz pure sine wave fixed frequency
- PWM carrier frequency can be set
  - 20KHz carrier frequency
  - 10KHz carrier frequency
  - 5 KHz carrier frequency
  - 2.5KHz carrier frequency
- Built-in dead zone control, the pin sets 4 kinds of dead zone time:
  - 300nS dead time
  - 500nS dead time
  - 1.0uS dead time
  - 2.0uS dead time
- According to the customer's application, Yijing Microelectronics provides modifications to the corresponding functions or parameters

2. description

EG8030 is a digital, complete function three-phase pure sine wave inverter generator chip with dead zone control, configurable four

The operating mode can be applied to the DC-DC-AC two-stage power conversion architecture or the DC-AC single-stage power frequency transformer boost conversion architecture. External 16MHz cryst

It can generate three-phase SPWM signals with high accuracy, low distortion and harmonics. And has a perfect sampling mechanism, can collect current signals, temperature

Degree signals and three-phase voltage signals are processed to realize output voltage regulation and various protection functions. The chip adopts CMOS technology and integrates SPWM inside

Sine generator, dead time control circuit, amplitude factor multiplier, soft start circuit.

3. Application field

- Three-phase pure sine wave inverter

4. Pin

4.1. Pin definition

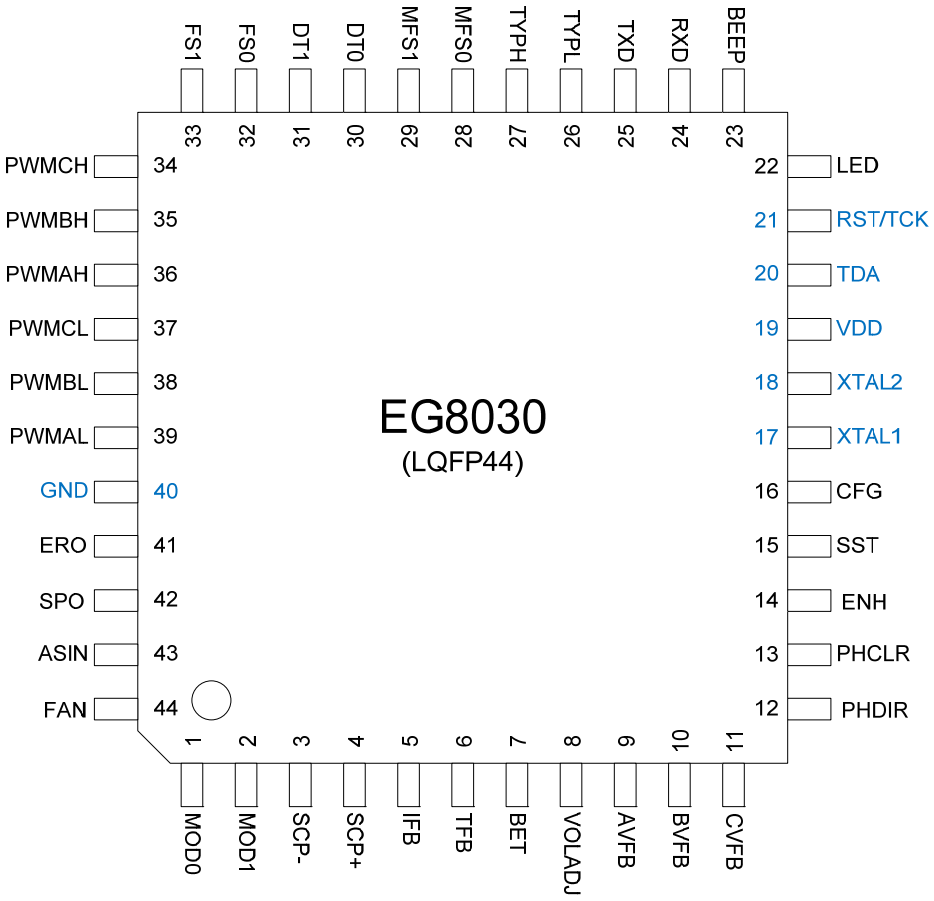


Figure 4-1. EG8030 Pin definition

Description:

1 , All configuration pins of the chip (DI) Are weak pull-up input ports, the internal pull-up resistor value is 30K Ω, when the pin is left floating,

The pin is high, that is, the configuration word read by the chip is " 1 "; if necessary, configure to " 0 ", the pin can be directly grounded.

2 , Chip feedback signal input pin (AI) Is the analog signal input port, high-impedance mode, when the pin is floating outside, it is an uncertain value, the chip internal

ADC Read AD The value is uncertain.

3 , All digital output pins of the chip (DO) Are push-pull output ports, the current sourcing capability is 5mA , The current sink capability is 20mA .

4 , Sine wave signal output of the chip (AO) The pin is an analog signal output port, which is only used for small signals and has no current capability.

4.2. Pin description

Pin number	Pin name	Port mode	description
1	MOD0	DI	MOD1, MOD0 is to set the working mode of three-phase inverter, "11" is a three-phase synchronous open-loop voltage regulation mode, that is, an external VOLADJ pin provides an analog signal to control the modulation depth of the three-phase SPWM. 0-5V can set the modulation depth of 0%-100%; "10" is three In phase-synchronous closed-loop voltage regulation mode, the chip collects the three-phase output phase voltage, performs PI adjustment, and automatically calculates the modulation depth. At this time, the three-phase output is synchronous output, that is, the three-phase SPWM modulation depth is the same; "01" is the three-phase independent open loop Voltage regulation mode, that is, sampling three sets of external analog signals through AVFB\BVFB\CVFB to independently control the modulation depth of ABC three "00" is a three-phase independent closed-loop voltage regulation mode. After processing, the output three-phase voltage is directly fed back to the AVFB\BVFB\CVFB pin. The chip performs PI adjustment and independently calculates the modulation depth for the three ph **Note: Modulation depth It is the ratio of the difference between the maximum amplitude and minimum amplitude of the current** modulated wave to the sum of the maximum amplitude and minimum amplitude of the carrier wave, expressed as a percentage. For the inverter, under the same DC bus input and load conditions, the modulation depth of SPWM is basically proportional to the ampl
2	MOD1	DI	
3	NC	AI	Keep
4	NC	AI	Keep
5	**I FB**	AI	Load current feedback input
6	**T FB**	AI	Temperature feedback input
7	BET	AI	Battery voltage monitoring port for overvoltage and undervoltage protection
8	FRQADJ	AI	Three-phase sine wave feedback voltage threshold, can be used as three-phase synchronous voltage regulator
9	**V FB A**	AI	Phase A sine wave output voltage feedback input
10	**V FB B**	AI	Phase B sine wave output voltage feedback input
11	**V FB C**	AI	Phase C sine wave output voltage feedback input
12	PHDIR	DI	Phase sequence reversal control pin "0" sets the current three-phase output phase sequence to ACB "1" sets the current three-phase output phase sequence to ABC
13	PHCLR	DI	Phase sequence clear port, triggered by falling edge signal, adjust the phase of phase A sine wave to 0°
14	ENH	DI	Three-phase SPWM output enable pin "0" turns off three-phase SPWM signal output "1" turns on three-phase SPWM signal output
15	SST	DI	Soft start setting pin "0" to turn off soft start Each time “1” restarts the SPWM output, a soft start is performed for 3 seconds, during which the amplitude of the sine wave increases linearly.
16	CFG	DI	SPWM configuration selection pin EG8030's SPWM output frequency, modulation frequency, dead zone size, output level, working mode, soft start, three-phase phase sequence have two configuration methods, usually the chip adopts external pin configuration when working in a single machine, by setting FS\MFS\ DT\TYP\MOD\SST\PHDIR pin implementation; when using serial communication, you can select the internal register configuration by setting this pin. For serial communication and internal register settings, see **** "0" to select the internal register configuration, Use "1" to select the external pin configuration during serial communication, used when the chip works independently

Pin number	Pin name	Port mode	description
17	XTAL1		16M crystal oscillator pin 1, need to connect a 22pF capacitor to ground
18	XTAL2		16M crystal oscillator pin 2, need to connect a 22pF capacitor to ground
19	VCC	VCC	+5V working power terminal of the chip
20 , twenty one	NC		**The system reserves pins and must be left floating!**
twenty two	led	DO	External LED alarm output, when the fault occurs, output low level "0" to light the LED normal: long light Shutdown: 1 blink, 2 seconds off, keep looping Overcurrent: flashing 2 times, off for 2 seconds, keep cycling; Undervoltage: flashing 4 times, off for 2 seconds, keep cycling Overvoltage: flashing 3 times, off for 2 seconds, keep cycling; Over temperature: flashing 5 times, off 2 Seconds, keep looping
twenty three	BEEP	DO	Buzzer alarm function: normal: do not call Shutdown: call once, stop for 2 seconds, keep looping; Overcurrent: call 2 times, stop for 2 seconds, keep looping; Overtemperature: call 5 times, stop for 2 seconds, keep looping; Overpressure: call 3 times, stop for 2 seconds, keep looping; Undervoltage: call 4 times, stop 2 seconds, keep looping;
twenty four	RXD	DI	Serial communication function pin, baud rate 2400, data bit 8 bits, stop bit 1 bit, no verification Normally when using serial communication, CFG pin needs to be configured as "0"
25	TXD	DO	
26	TYPH	DI	TYPH, TYPL are PWM upper and lower tube output type selection "00" is output low level to open the power tube upper tube, output low level to open the power tube down tube; "01" is output low level to open the power tube upper tube, output high level to open the power tube down tube; "10 "" is to output high level to open the power tube upper tube, output low level to open the power tube down tube; "11" is to output high level to open the power tube upper tube, output high level to open the power tube down tube; **When designing the application, please refer to the typical application circuit diagram, and configure the pin state according to the driving device. Otherwise, the inconsistency will cause the upper and lower power MOS transistors to turn on at the**
27	TYPL	DI	
28	MFS0	DI	MFS1, MFS0 is to set the output SPWM wave modulation frequency "00" is to output 2.5KHz modulation frequency; "01" is to output 5KHz modulation frequency; "10" is to output 10KHz modulation frequency; "11" is to output 20KHz modulation frequency;
29	MFS1	DI	
30	DT0	DI	DT1, DT0 is to set the dead time of PWM output upper and lower MOS tube: "00" is 1.5uS dead time; "01" is 1.0uS dead time; "10" is 0.5uS dead time; "11" is 0.3uS dead time
31	DT1	DI	
32	FS1	DI	Output sine wave frequency setting pin "00" reserved "01" reserved
33	FS0	DI	"10" sets the output sine wave frequency to 60Hz "11" sets the output sine wave frequency to 50Hz
34	SPWMCH	DO	SPWM output of phase C bridge arm upper tube
35	SPWMBH	DO	SPWM output of B-phase upper arm
36	SPWMAH	DO	SPWM output of phase A bridge arm upper tube

Pin number	Pin name	Port mode	description
37	SPWMCL	DO	SPWM output of phase C bridge arm
37	SPWMCL	DO	SPWM output of phase C bridge arm
38	SPWMBL	DO	SPWM output of B-phase lower arm
39	SPWMAL	DO	SPWM output of phase A bridge arm
40	GND	GND	Chip ground
41	ERO	DO	Fault signal output pin When the chip is in the protection output off state, it outputs "0". Normal operation outputs "1"
42	SPO	DO	Voltage sampling output pin Output a high level during voltage sampling, low level when not sampling
43	ASIN	AO	Sine wave analog signal output pin Output a sine wave signal with the same frequency and phase as the A phase SPWM wave, see 9.1 Voltage feedback
44	FANCTR	DO	External fan control, when T_{FB} When the pin detects that the temperature is higher than 45°C, it outputs a high level "1" to run the fan. When the temperature drops below 40°C, it outputs a low level "0" to stop the fan

5. Structure diagram

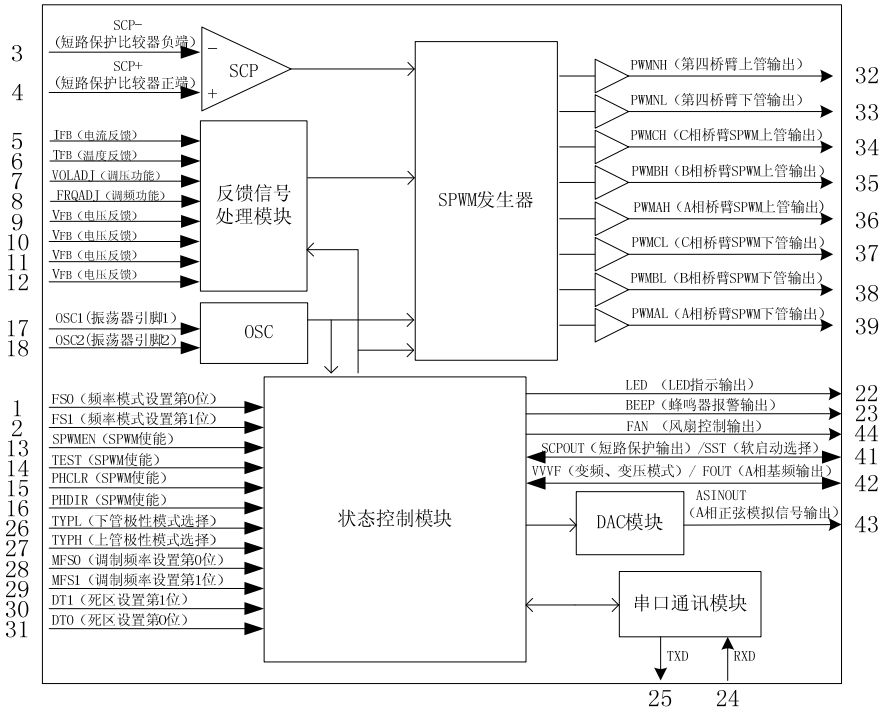
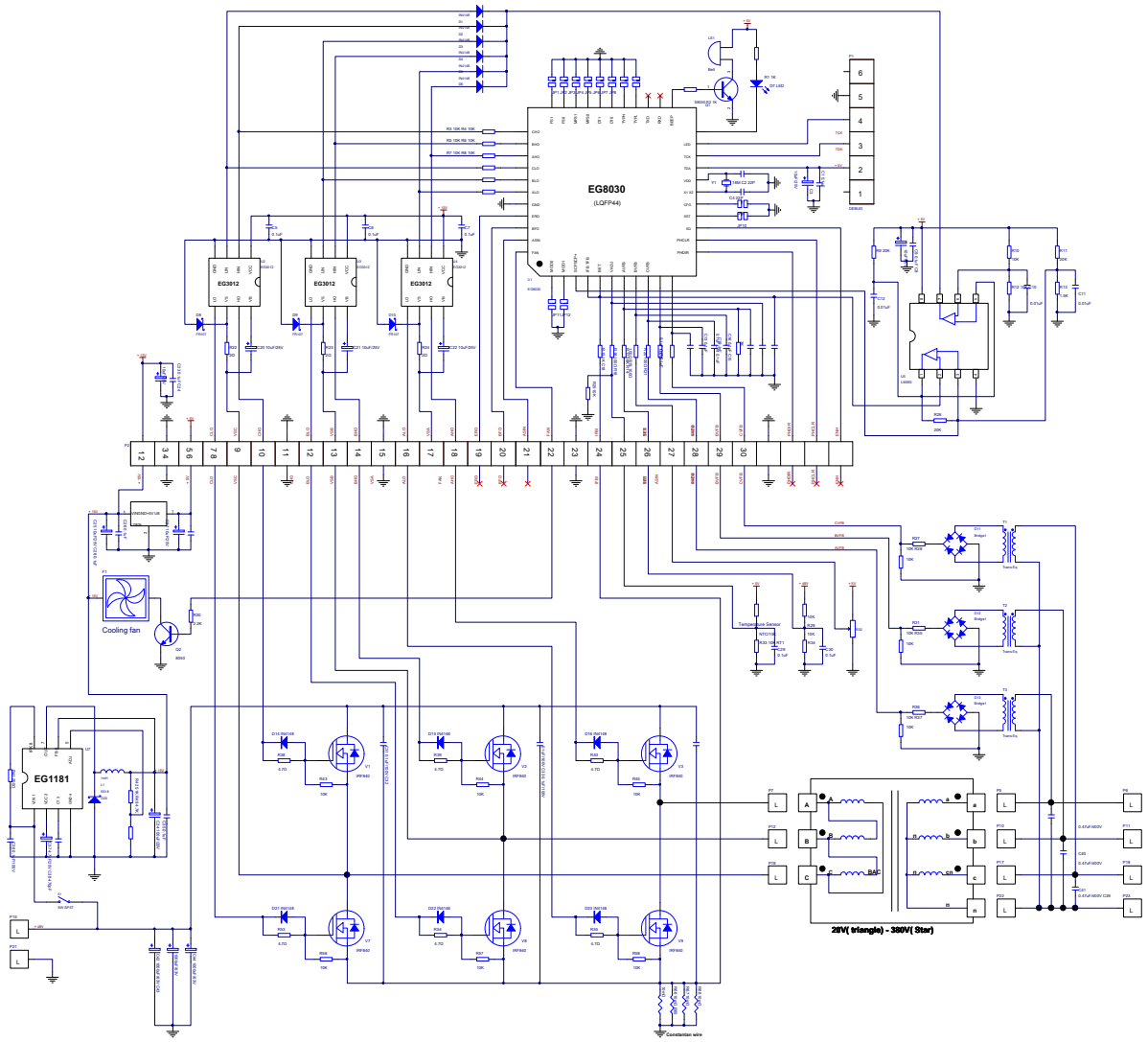


Figure 5-1. EG8030 Structure diagram

6. Typical application circuit

6.1 Three-phase synchronous closed-loop voltage regulation mode—— DC-AC-AC Power frequency transformer Δ- Y Boost structure (recommend



EG8030+EG3012+EG1181 Typical application circuit diagram of three-phase pure sine wave inverter

This application uses 48V The battery supplies the DC bus with EG8030 It is the main control unit of the inverter, driving the chip through the half bridge EG3012 Driving power MOSFET , Three-phase full-bridge inverter output three-phase SPWM After three-phase power frequency transformer boost filtering. Three-phase power frequency step-up transformer adopts Δ- Y Connection mode, the four-wire output phase voltage is 220V , The line voltage is 380V Pure sine wave three-phase power supply. Required on board+ 15V Drive power DC-DC Buck power supply chip EG1181 get on 48V Buck conversion. In this application EG8030 Working in three-phase synchronous closed-loop voltage stabilization mode, voltage feedback uses three small transformers for isolation sampling. Due to the use of synchronous voltage regulation, three-phase SPWM The modulation depth is the same, so when the load is unbalanced, there will be a certain offset in the three-phase voltage. EG8030 With voltage imbalance protection function, this function will limit the maximum voltage of each phase will not exceed the preset 10% , And when the three-phase voltage is seriously unbalanced, shutdown protection will be taken. The synchronous closed-loop voltage regulation mode is EG8030 The recommended working mode has the advantages of easy implementation and high reliability.

6.2 Three-phase independent closed-loop voltage regulation mode-high-voltage DC inverter three-bridge four-wire output structure (test)

(Unavailable)

Figure 6-2. EG8030+TLP250 Typical application circuit diagram of three-phase pure sine wave inverter

7. Electrical characteristics

7.1 Limit parameter

Without additional explanation, at T A=25℃

symbol	parameter name	Test Conditions	Min	Max	Unit	
VCC	power supply	Vcc pin relative to GND Voltage	-0.3	6.5		V
I/O	All input/output ports and all	I/O pins to GND Voltage	-0.3	5.5		V
Isink	Maximum output sink of output pin Electric current	-	-	25		mA
Isource	Maximum output pull of output pin Electric current	-	-	-5		mA
T A	Ambient temperature	-	- 45	85		℃
Tstr	Storage temperature	-	- 65	125		℃

Note: Exceeding the listed limit parameters may cause permanent damage to the chip. Long-term operation under the limit conditions will affect the reliability of the chip.

7.2 Typical parameters

Without additional explanation, at T A=25℃, Vcc=5V, OSC=12MHz

symbol	parameter name	Test Conditions	Minimum	typical	maximum	unit
Vcc	power supply	-	3.5	5	5.5	V
VREF	Reference power input	-	-	5	-V	
I/O	All inputs and outputs	The voltage of all I/O pins to GND	0	-	5	V
Icc	Quiescent Current	Vcc=5V, OSC=12MHz	-	10	15	mA
V FB	Peak feedback reference voltage	Vcc=5V	-	3.0	-V	
I FB	Current protection reference voltage	Vcc=5V	-	0.5	-V	
T FB	Temperature protection reference voltage	Vcc=5V	-	4.3	-V	
Vin(H)	Input logic signal high potential	Vcc=5V	2.0	5.0	5.5	V
Vin(L)	Input logic signal low potential	Vcc=5V	-0.3 0		1.0	V
Vout(H)	Output logic signal high level	Vcc=5V, IOH=-3mA	3.0	5.0	-	V
Vout(L)	Output logic signal low level	Vcc=5V, IOL=10mA	-	-	0.45	V
Isink	Maximum output sink of output pin Electric current	-	-	-	20	mA
Isource	Maximum output pull of output pin Electric current	-	-	-	-3	mA

8. working principle

EG8030 There are four working modes: three-phase synchronous open-loop voltage regulation, three-phase synchronous closed-loop voltage regulation, three-phase independent open-loop voltag

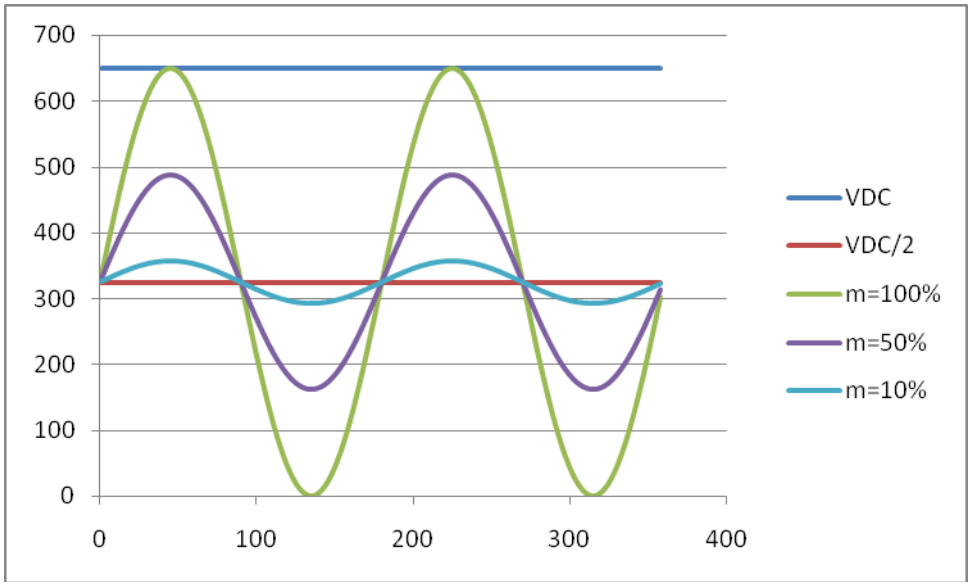
Independent closed-loop voltage regulator. The four working modes have their own characteristics and can be selected by users according to their needs. Before introducing the four working modes, first in

a bit EG8030 An important parameter of the voltage control system- **Modulation depth** .

Modulation depth Is defined as: the ratio of the difference between the maximum amplitude and minimum amplitude of the current modulated wave to the sum of the maximum amplitude and minir

Expressed as a percentage. For the inverter, under the same DC bus input and load conditions, SPWM The modulation depth and output sine wave

The amplitude is basically proportional.



DC bus voltage and modulation depth, output sine wave relationship diagram

The image below shows the comparison of the image **DC bus voltage** with **Modulation depth, output sine wave** The relationship between. In the picture VDC DC bus

Voltage, m Denotes the modulation depth. In an ideal state, the output impedance of the inverter is 0 , When the modulation depth m=100% , The peak of the sine wave

The peak value is just equal to the DC bus voltage. From this we can get the relationship between the single-phase sine wave voltage and the DC bus voltage as:

$$VAC_{TOP} = 2 \quad \frac{1}{} * m * VDC$$

$$VAC_{RMS} = 4 \quad \frac{\sqrt{2}}{} * m * VDC$$

E.g:

1) DC bus voltage VDC = 650V , Depth of modulation m = 100% , The effective value of the current AC output voltage can be calculated as:

$$VAC_{RMS} = \frac{\sqrt{2}}{4} * 650 * 100\% = 230V$$

2) DC bus voltage VDC = 650V , Depth of modulation m = 50% , The effective value of the current AC output voltage can be calculated as:

$$VAC_{RMS} = \frac{\sqrt{2}}{4} * 650 * 50\% = 115V$$

in EG8030 In, we define three-phase SPWM The modulation depth is M_A , M_B , M_C .

8.1 Three-phase synchronous open-loop voltage regulation

The three-phase synchronous open-loop voltage regulation mode is EG8030 The simplest working mode. The chip works in open loop mode, the user adjusts VOLADJ The voltage of the foot directly controls the three-phase SPWM Modulation depth M_A , M_B , M_C , And the three-phase modulation depth M_A= M_B= M_C . VOLADJ On feet 0-5V Of the voltage corresponds to the modulation depth M_A of 0-100% . In order to ensure that the waveform is a complete sine wave in one cycle, the modulation of each phase The control depth is only refreshed once per cycle, that is A Phase phase is 0 ° hour VOLADJ Sample and convert M_A , M_B , M_C Value.

Three-phase synchronous open-loop voltage regulation can be used in applications where the accuracy of the three-phase AC output voltage is not high. Just provide a relatively stable high DC power supply and a three-phase output filter can be adjusted VOLADJ The voltage on the pin makes the output voltage reach the target value. Simple structure Easy to implement. The disadvantage is that, because the actual inverter power supply is not an ideal voltage source, there will always be a certain output impedance. When the load increases, The internal resistance of the inverter will consume part of the voltage, resulting in a decrease in the actual output voltage. The magnitude of the voltage drop is related to the internal resistance of the inver The fluctuation of the DC power supply will also affect the three-phase output voltage.

The three-phase synchronous open-loop voltage regulation can also be applied to the occasions where users build feedback loops by themselves. Users can participate in the implementation throu Various control algorithms for closed-loop voltage regulation, at this time EG8030 As an implementing agency, according to VOLADJ The voltage input on the foot adjusts the sine wave Output. This way of working opens up the application of the chip more, and provides developers with an open space for independent play. But it should be noted that EG8030 The output adjustment mechanism is **Weekly adjustment** , That is, the output is changed every cycle, and in one cycle, VOLADJ The voltage change on the foot will Will not be responded to.

8.2 Three-phase synchronous closed-loop voltage regulator

The three-phase synchronous closed-loop voltage regulation mode is EG8030 The recommended application mode is suitable for occasions where accuracy is required for the output voltage. In this Mode, chip sampling AVFB , BVFB , CVFB The feedback signal on the foot and take the average to get the average feedback voltage of the current three phases, and then Inside PI The regulator calculates three phases SPWM Modulation depth M_A , M_B , M_C , And M_A= M_B= M_C , Synchronously adjust the three-phase output. VOLADJ Determine the threshold for feedback control, such as the current VOLADJ The voltage on the foot is 2.5V , Then when the average feedback voltage is greater than 2.5V Time, EG8030 Through internal PI Regulator operation gradually decreases M_A , M_B , M_C , Which lowers the output voltage and the feedback voltage

Decrease; otherwise, when A Phase feedback voltage is less than 2.5V Time, EG8030 Through internal PI Regulator operation decreases synchronously M_A , M_B , M_C , Which reduces the output voltage and the feedback voltage will also decrease; in this way, the voltage feedback can be stabilized at 2.5V ,The output voltage Naturally it will remain constant.

In this mode, when the DC bus voltage fluctuates or the load changes, the three-phase output voltage can be kept basically constant. Suitable for losing The occasions where the accuracy of the output voltage is high and the load balance or load difference is not large. When any one phase voltage is greater than the set voltage 110% Or less than the set p Pressed 90% Time, EG8030 The three-phase unbalance protection shutdown operation will be performed.

Three-phase synchronous closed-loop voltage regulation requires sampling high-voltage output for feedback, so it is generally recommended that users use three-phase power frequency transform The phase voltage needs to use three small feedback transformers for isolated buck feedback. Ensure that the DC output is isolated from the AC output, and the control circuit is AC output isolation. Three-phase power frequency step-up transformer is recommended to use Δ- Y Connection mode, you can get a four-wire output, and can increase the DC voltage Utilization. The high-voltage end of the three-phase power frequency transformer needs to be a small CBB Filtering capacitor can get smooth three-phase sine wave.

8.3 Three-phase independent open-loop voltage regulation

The three-phase independent open-loop voltage regulation mode is EG8030 Another open-loop working mode. User adjusts AVFB , BVFB , CVFB foot The voltage on the independent control three-phase SPWM Modulation depth M_A , M_B , M_C . The corresponding relationship is 0-5V correspond 0-100% ,among them AVFB control system M_A , BVFB control M_B , CVFB control M_C . In this mode, VOLADJ The foot function is blocked. In order to ensure that in a cycle The waveform is a complete sine wave, and the modulation depth of each phase is only refreshed once per cycle, that is, the phase of each phase is 0 °When the feedback is collected Sample and convert M_A , M_B , M_C Value.

The three-phase independent open-loop voltage regulation can be applied to the occasions where the accuracy of the three-phase AC output voltage is not high but the three-phase different voltage Only need to provide a relatively stable high-voltage DC power supply and a three-phase output filter, can be adjusted independently AVFB , BVFB , CVFB The voltage on the pin makes the output voltage of each phase reach different target values. The structure is simple and easy to realize. The disadvantage is that because the actual inverter power supply i It is an ideal voltage source, there will always be a certain output impedance. When the load is heavier, the internal resistance of the inverter will lose part of the voltage, resulting in The output voltage has decreased. The magnitude of the voltage drop is related to the internal resistance of the inverter. In addition, the fluctuation of the DC power supply will also affect the three-phase ou

The three-phase independent open-loop voltage regulation can also be applied in the occasion where the user builds the feedback loop, and the user can participate in the realization through the ha Various control algorithms for closed-loop voltage regulation, at this time EG8030 As an implementing agency, according to VOLADJ The voltage input on the foot adjusts the sine wave Output. This working mode opens the application of the chip more on the basis of the synchronous open-loop voltage regulation mode, providing developers with a wide range of The main play space. But it should be noted that EG8030 The output adjustment mechanism is **Weekly adjustment** , That is, the output is changed every cycle, in one cycle in, AVFB , BVFB , CVFB The voltage change on the pin will not be responded

8.4 Three-phase independent closed-loop voltage regulator

The three-phase independent closed-loop voltage regulation mode is EG8030 Is a test mode suitable for fields with high output voltage accuracy and three-phase unbalanced load Together. This mode has high DC voltage, complicated structure, and lower reliability than other modes, so it is defined as a test mode.

Choose this mode of operation carefully.

In this working mode, the chip sampling AVFB , BVFB , CVFB The feedback signal on the foot, after each phase is independent PI Regulator operation, Get the modulation depth of each box M_A , M_B , M_C . . VOLADJ Still determine the threshold for feedback control, such as the current VOLADJ Voltage on the foot for 2.5V , Then when A Phase feedback voltage is greater than 2.5V Time, EG8030 Through internal PI Reduced regulator operation M_A The value of Output voltage, and the feedback voltage will decrease accordingly; conversely, when A Phase feedback voltage is less than 2.5V Time, EG8030 Through internal PI Regulator Less operation M_A , Which reduces the output voltage and the feedback voltage will also decrease; in this way, the voltage feedback can be stabilized at 2.5V , The output voltage will naturally remain constant. The other two phases also achieve the same independent voltage regulation.

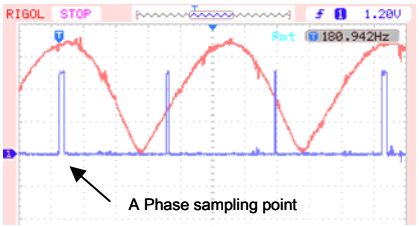
In this mode, when the DC bus voltage fluctuates or the load changes, the three-phase output voltage can be kept basically constant. Suitable for losing The occasion with high output voltage accuracy and three-phase unbalanced load. This mode requires the use of two large capacitors in series to form the fourth bridge arm to achieve three-phase Four-wire output, and can independently regulate the voltage of each phase. Further technical support for this model will gradually improve.

9. Application Design

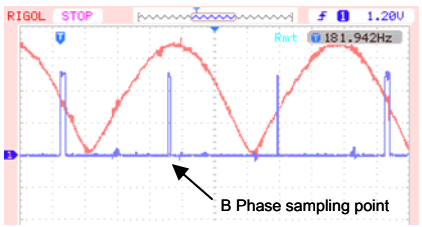
9.1 Voltage feedback

EG8030 The chip's voltage feedback sampling is used **Weekly sampling** , The phase of the sampling point is determined by the current working mode, three-phase independent feedback working In the formula, the sampling point of each phase is the peak position of the sine wave of each phase, that is, each phase 90 The voltage feedback is sampled during the phase. Sampling in three-phase syn The point phase is 60 °. chip SPO The signal output by the pin is the sampling signal, namely SPO During the high level, the chip performs voltage feedback sampling.

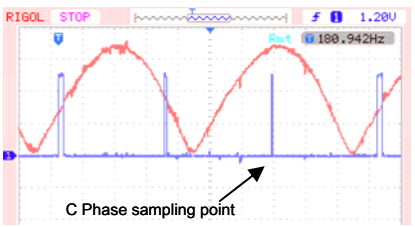
To distinguish A , B , C The sampling point of three-phase feedback, the wide level in the figure is A Phase voltage feedback sampling point, followed by B Phase sampling point and C Phase sampling point. If phase reversal is set (PHDIR= ' 0 '), the wide level is followed by C Phase sampling points and B Phase sampling point.



SPO versus VFBA Waveform



SPO versus VFBB Waveform



SPO versus VFBC wave

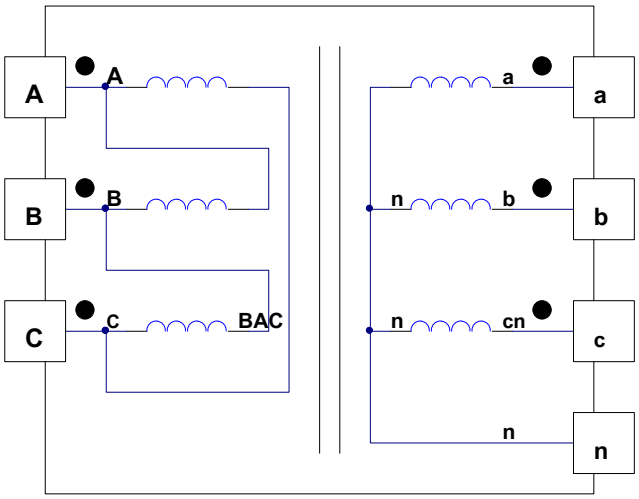
The waveform above is taken from the use of power frequency transformer Δ- in three-phase synchronous closed-loop voltage regulation mode Y Feedback waveform during type connection. Circu

Section, Typical application schematic diagram of three-phase synchronous closed-loop voltage stabilization. AVFB The phase of the sampling point is 30 °, due to the use of power

frequency transformer Δ- Y Type connection, input stage AC Corresponding output end with the same name an , BA Corresponding to the same name end bn , CB Corresponding to the end of

the same name cn . A Phase is 0 °, C Phase is- 120 °, then the line voltage AC The phase is- 60 °, output stage an The phase is also- 60 °. So the phase is 30 The position of ° happens to be sampled an

BVFB , CVFB 'S waveforms move backwards in turn 120 °. If phase reversal is set (PHDIR= ' 0 '), then BVFB , CVFB The sampling points will be swapped.



Three-phase power frequency transformer Δ- Y Type connection

9.2 Current feedback

EG8030 Chip pins I_{FB} It measures the output load current of the inverter and is mainly used for overcurrent protection detection. The circuit structure is shown in Figure 8.1a.

In the sampling feedback part, the reference peak voltage inside this pin is set to 0.5V Overcurrent detection delay time 600mS , When some reason causes the load

The current is too high to exceed the load current of the inverter, EG8030 According to the pin TYPH , TYPL The setting status of will be output xHO , xLO To " 0 "or

" 1 "Level, turn off all power MOSFET Bring the output voltage to low level, this function is the main protection power MOSFET And load once

After entering the overcurrent protection, EG8030 will be 16S After re-opening the power MOSFET The tube then judges the load overcurrent situation and releases the open power

MOS The duration of the tube is 100mS, Released 100mS Determine the overcurrent event in time, if there is still an overcurrent event, EG8030 Again

Turn off all power MOSFET Make the output voltage low, wait again 16S Release, if the starting current is relatively large for some occasions

If it is relatively long and it is not suitable for applying this function, you can change I_{FB} The pin is grounded.

9.3 Temperature feedback

EG8030 Chip pins T_{FB} It is to measure the working temperature of the inverter, mainly used for over-temperature protection detection and control fan output, circuit structure

As shown in Figure 8.3a temperature detection circuit, as shown NTC thermistor RT1 and measurement resistor RF1 form a simple voltage divider circuit, the voltage divider value

As the temperature value changes and the value changes, the magnitude of this voltage will reflect the magnitude of the NTC resistance to obtain the corresponding temperature value. NTC selects 25℃

Corresponding to the thermistor with a resistance of 10K, T_{FB} The overtemperature voltage of the pin is set at 4.3V , When over-temperature protection occurs, EG8030 According to the pin TYPH , TYPL The setting status of will be output PWMXH , PWMXL To " 0 "or" 1 "Level, turn off all power MOSFET Bring the output voltage to Low level, once over temperature protection is entered, EG8030 Will re-judge the operating temperature if T_{FB} The voltage of the pin is lower than 4.0V , EG8030 will The over-temperature protection is exited and the inverter works normally. If the over-temperature protection function is not used, this pin needs to be grounded.

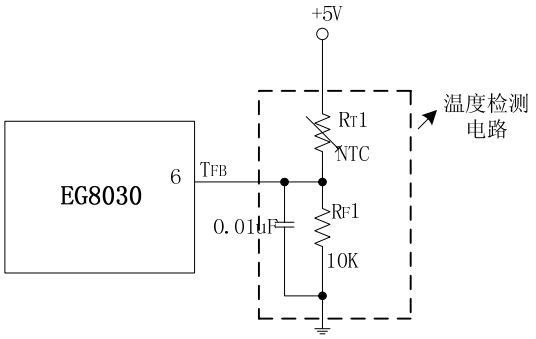


Figure 8.4a EG8030 Temperature detection circuit

9.4 PWM output type

EG8030 Chip pins TYPH , TYPL Can be set independently PWM The upper and lower tube output types are suitable for various drives. TYPH , TYPL for" 00 ", the output PWM Type output is used when the dead zone level is at the same time low level (such as driving IR2110 or IR2106 Driver core Piece), picture 8.4a Yes EG8010 Pin SPWMOUT Output waveform, high level effective drive power MOS Tube, illustration 8.4b Yes TYPH , TYPL for" 11 "Drive IR2110 Application circuit.

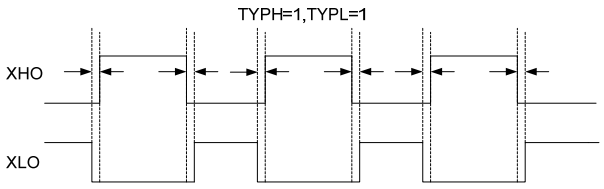


Figure 8.4a THPH=1,TYPL=1 Time PWM Waveform output

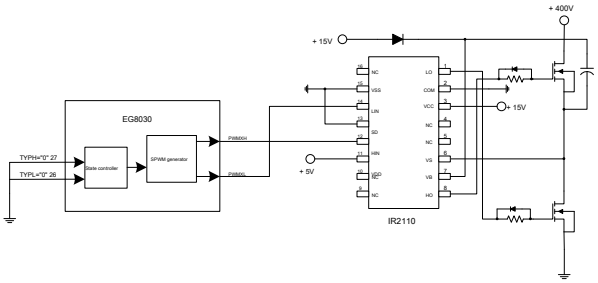


Figure 8.4b EG8030 drive IR2110

TYPH , TYPL for" 10 ", the output PWM Type output is applied to the drive where the upper tube is open at high level and the lower tube is open at low level Dynamic circuit (such as drive IR2103 Driver chip), picture 8.4c Yes EG8030 Pin xHO , xLO Output waveform.

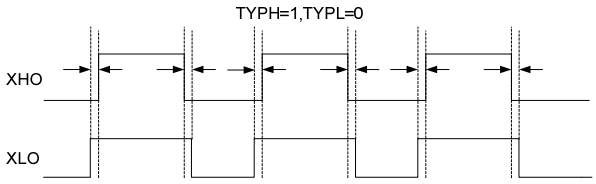


Figure 8.4c THPH=0, TYPL=1 Time PWM Waveform output

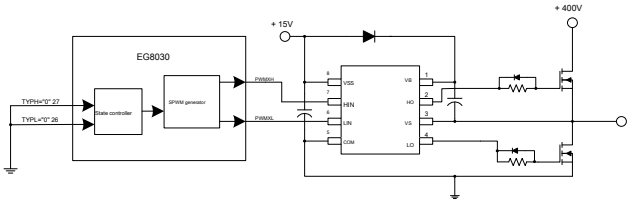


Figure 8.4d EG8030 drive IR2103

TYPH , TYPL for" 01 ", the output PWM Type output is applied to the drive where the upper tube is open at low level and the lower tube is open at high level

Moving circuit (this type of driving method is not commonly used), figure 8.4e Yes EG8030 Pin xHO , xLO Output waveform.

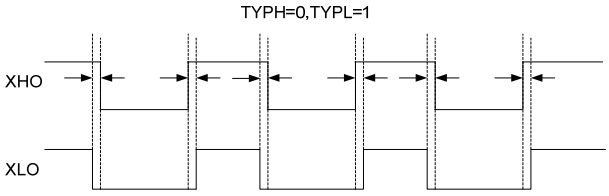


Figure 8.4e THPH=1, TYPL=0 Time PWM Waveform output

TYPH , TYPL for" 11 ", the output PWM The type output is applied to the driving circuit where the upper tube and the lower tube are open at a low level (such as

drive TLP250 Such as the cathode of the optocoupler device), picture 8.4f Yes EG8030 Pin xHO , xLO Output waveform. , The low level effectively drives the optocoupler,

Optocoupler output high level drive power MOS Tube, figure 8.4g Yes TYPH , TYPL for" 11 "Time, EG8030 drive TL250 Optocoupler

Application circuit.

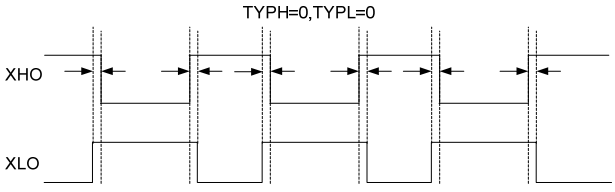


Figure 8.4f THPH=0, TYPL=0 Time PWM Waveform output

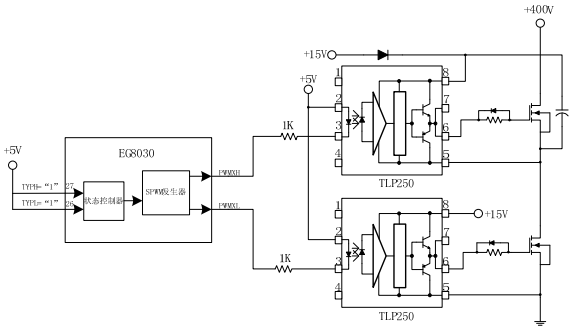


Figure 8.4g EG8030 drive TLP250

9.5 Dead time

EG8010 The pins DT1 and DT0 of the chip are used to control the dead time. The dead time control is one of the important parameters of the power MOS tube. If there is no dead time

If the zone time is too small, it will cause the upper and lower power MOS tubes to turn on at the same time and burn the MOS tube.If the dead zone is too large, it will cause waveform distortion and power

There is a serious thermal phenomenon. Figure 8.5a is the internal dead zone control timing of EG8010. As shown in the figure, pins DT1 and DT0 are used to set 4 kinds of dead zone time, "00" is 300nS dead time, "01" is 500nS dead time, "10" is 1uS dead time, "11" is 1.5us dead time.

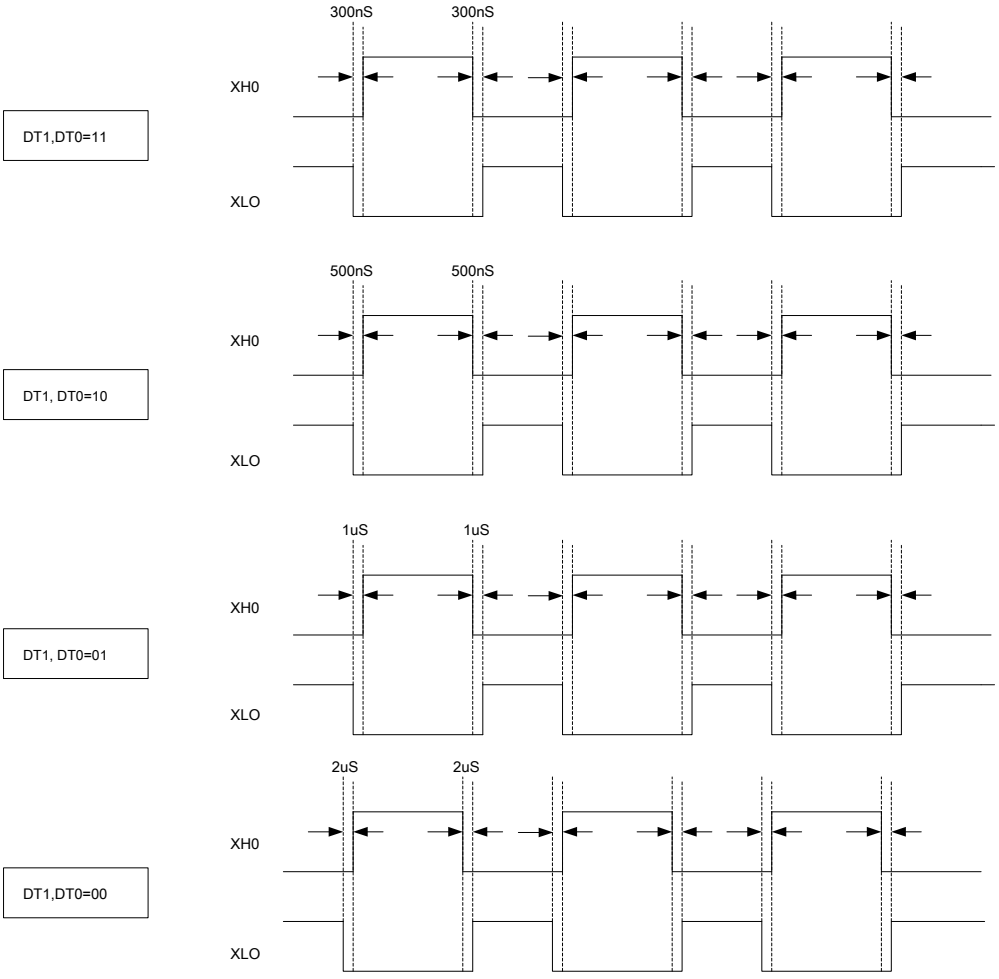


Figure 8.5a EG8010 Dead zone control settings

9.6 Frequency setting

EG8030 Two output sine wave frequencies can be configured by FS0 Pin settings. when FS0 When the pin is floating or connected to a high level, EG8030 Will produce 50HZ Sine wave, FS0 When the pin is connected to low level, EG8030 Will produce 60HZ Sine wave.

In addition EG8030 You can also configure four SPWM Modulation frequency, by pin MS1 , MS0 set up.

MS1 , MS0 = 11 : Modulation frequency 20KHz MS1 , MS0 =10 : Modulation frequency 10KHz MS1 , MS0 = 01 : Modulation frequency 5KHz MS1 , MS0 =00 : Modulation frequency 2.5KHz

9.7 Soft start

EG8030 Provides soft-start mode, suitable for loads with large current at start-up. SST The pin is configured as "with a pull-up resistor" 1 "Time, Enable this function. Soft start continues 3S , 3S After that, it will automatically enter the voltage stabilization state. Set as" 0 ", the soft start function is disabled. EG8030 recommend Enable the soft start function. If the soft start function is enabled, when the chip is EN When the foot or protection function is turned off and restarted, the chip will still be soft start up.

9.8 Phase sequence reversal

EG8030 With phase sequence reversal function, the phase sequence direction can be adjusted. PHDIR Pin realization. when PHDIR for" 1 "时 B The phase leads the phase A by 120°, the phase C lags the phase A by 120°, when “0”, the phase B lags the phase A by 120°, and the phase C leads the phase A by 120°. Phase sequence reversal It can be used for motor control, but in order to prevent the motor from suddenly switching to reverse rotation caused by high current impact, the output should be turned off first, and wait for the motor to sto After downloading, the phase sequence is reversed, and then the output is enabled.

9.9 Phase clear

EG8030 With phase clear function, can synchronize phase sequence online. PHCLR This function will be triggered when the level on the pin is increased. After clearing A The phase sequence is forced to be cleared, B Compatible C Phase will be based on PHDIR The upward direction adjusts the phase to lead and lag 120°. The user wants to When the EG8030 is used synchronously, the FOUT pin of one piece can be connected to the PHDIR pin of another piece, so as to realize the phase synchronization of the two chips.

9.10 Sinusoidal analog signal output

EG8030 Internal integration DA Module, able to output with A Sine wave analog signal of the same phase.

10. RS232 Serial communication interface

EG8030 Apply to RS232 The serial port communication interface sets the parameters such as the voltage, frequency, and dead zone of the inverter. Optocoupler isolation communication is required

As shown 8.9a .

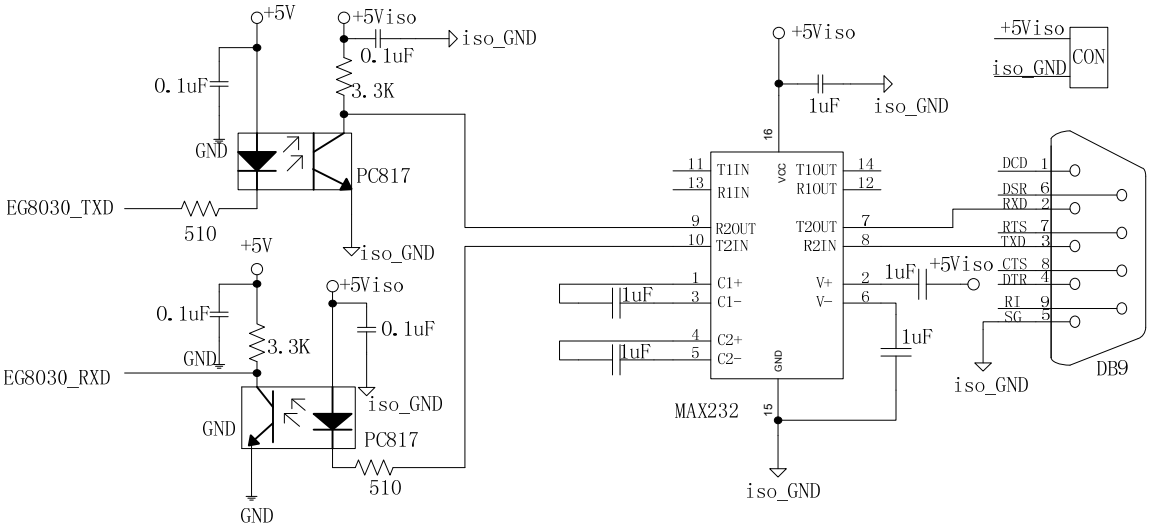


Figure 8.9a RS232 Optocoupler isolated communication circuit

Serial port parameters:

Baud rate: 2400

Data bits: 8

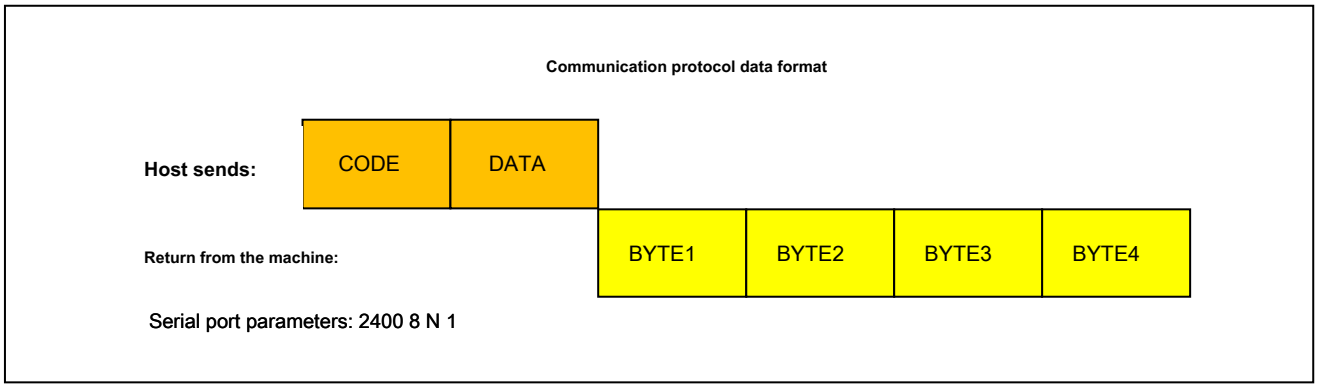
Check digit: none

Stop bit: 1

Protocol description:

In communication, EG8010 acts as a slave, and users can use MCU or PC as a master. Once the slave receives the command sent by the master, immediately

Generate a response and reply data to the host.

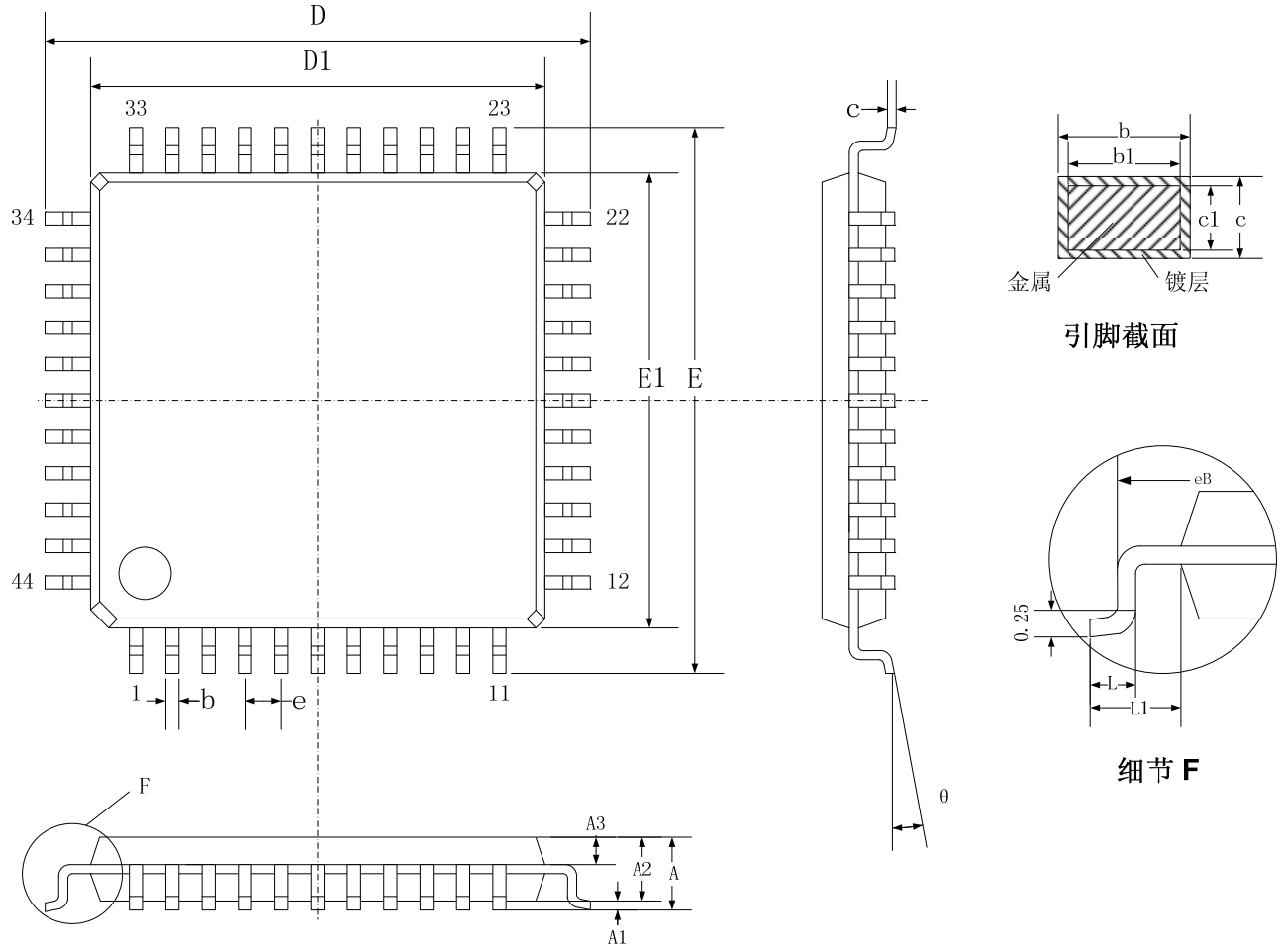


The data format is shown in the figure. In one operation, the host sends two bytes of data, the first byte is the command byte, and the second byte is the data byte. After receiving two bytes from the master, the slave immediately returns four bytes of data.

Command format: **(Reserved)**

11. Package size

LQFP44 Package size:



symbol	A	A1	A2	A3			b	b1	c	c1	D	D1		E	E1		e	eB	L	L1		θ
MIN-		0.05	1.35	0.59	0.29	0.28	0.13	0.12	11.80	9.90	11.80	9.90	0.80					11.25	0.45	1.00		0
NOM-		-	1.40	0.64		-	0.30	-	0.13	12.00	10.00	12.00	10.00				BSC	-	-		BSC	-
MAX	1.60	0.20	1.45	0.69	0.37	0.33	0.18	0.14	12.20	10.10	12.20	10.10						11.45	0.75			7
unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm						o