THE IMAGINATION UNIVERSITY PROGRAMME

RVfpga-SoC
Lab 1 Solution Instructions

1. Overview

This Lab solution requires the installation of Vivado 2019.2 Webpack and Digilent Board files. You can download and install them by following the detailed instructions given in the RVfpgaSoC's Installation Guide.

- Vivado 2019.2 Webpack   (Refer to Installation Guide (Page No.04))
- Digilent Board Files   (Refer to Installation Guide (Page No.05))

This Lab project was created on Vivado 2019.2 Webpack and will only work on the same version of Vivado.

This Lab project must be placed at the following location to avoid any path conflicts.

[RVfpgaSoCPath]/RVfpgaSoC/Labs/LabSolution/Lab1

2. Critical Warnings

A couple of warnings might pop up when you open the Block Design and click "Refresh IP Catalog" (see Figures 1 and 2). Ignore these warning messages by clicking OK.
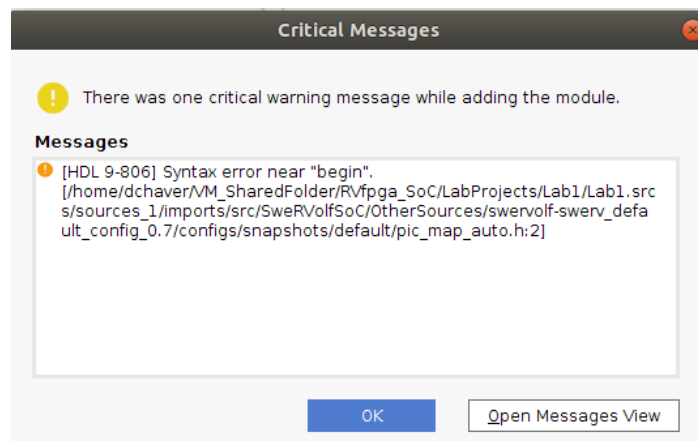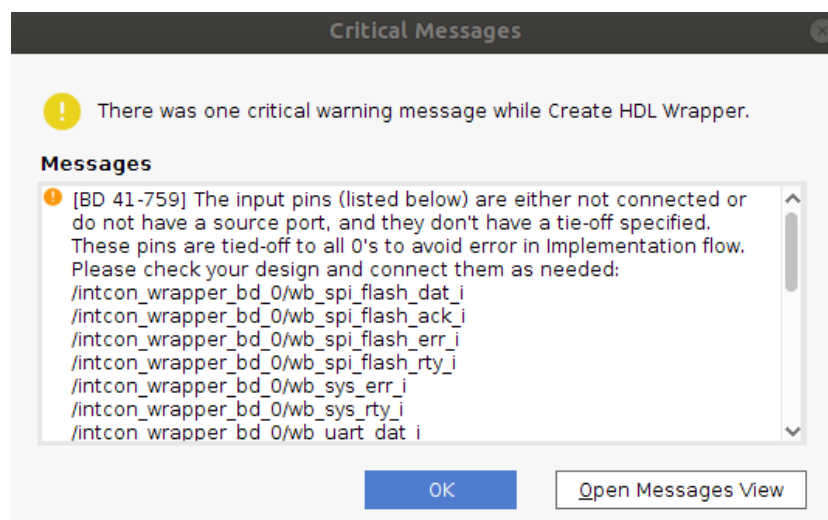

Figure 1. Warning Pop-Up

Figure 2. Warning Pop-Up

If this Lab project is not placed at the following path :

[RVfpgaSoCPath]/RVfpgaSoC/Labs/LabSolution/Lab1

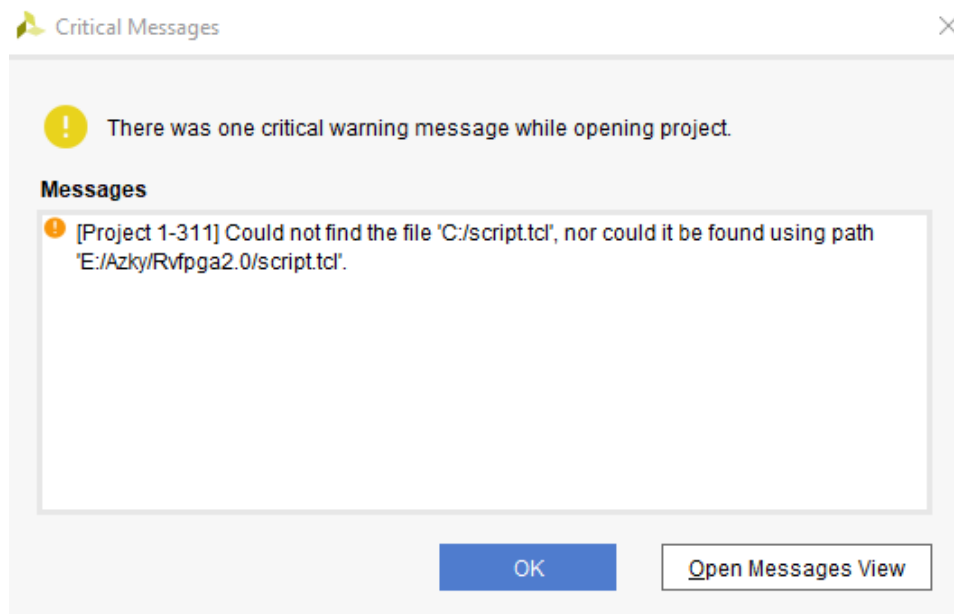It may give you the following critical message warning (see Figure 3).

Figure 3. Warning Pop-Up

In case of this warning message, you will have to provide the correct path to the "script.tcl" file.

You can navigate to Tools > Settings > Bitstream. Click on "tcl.pre".

Add the "script.tcl" file from the following path :

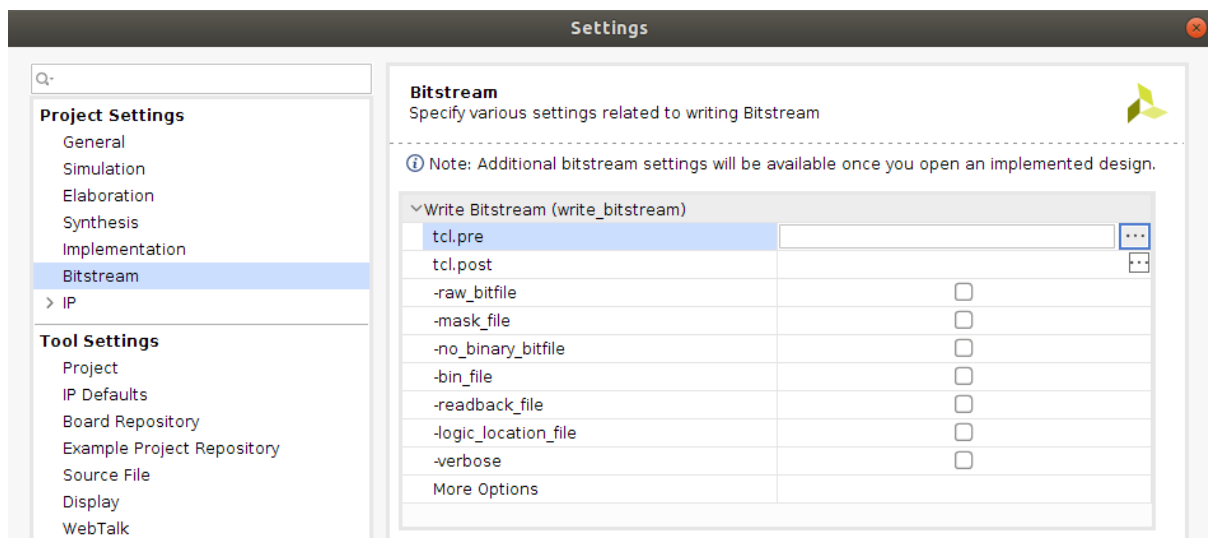*[RVfpgaSoCPath]/RVfpgaSoC/Labs/LabResources/Lab1/script.tcl*

Figure 4. Settings