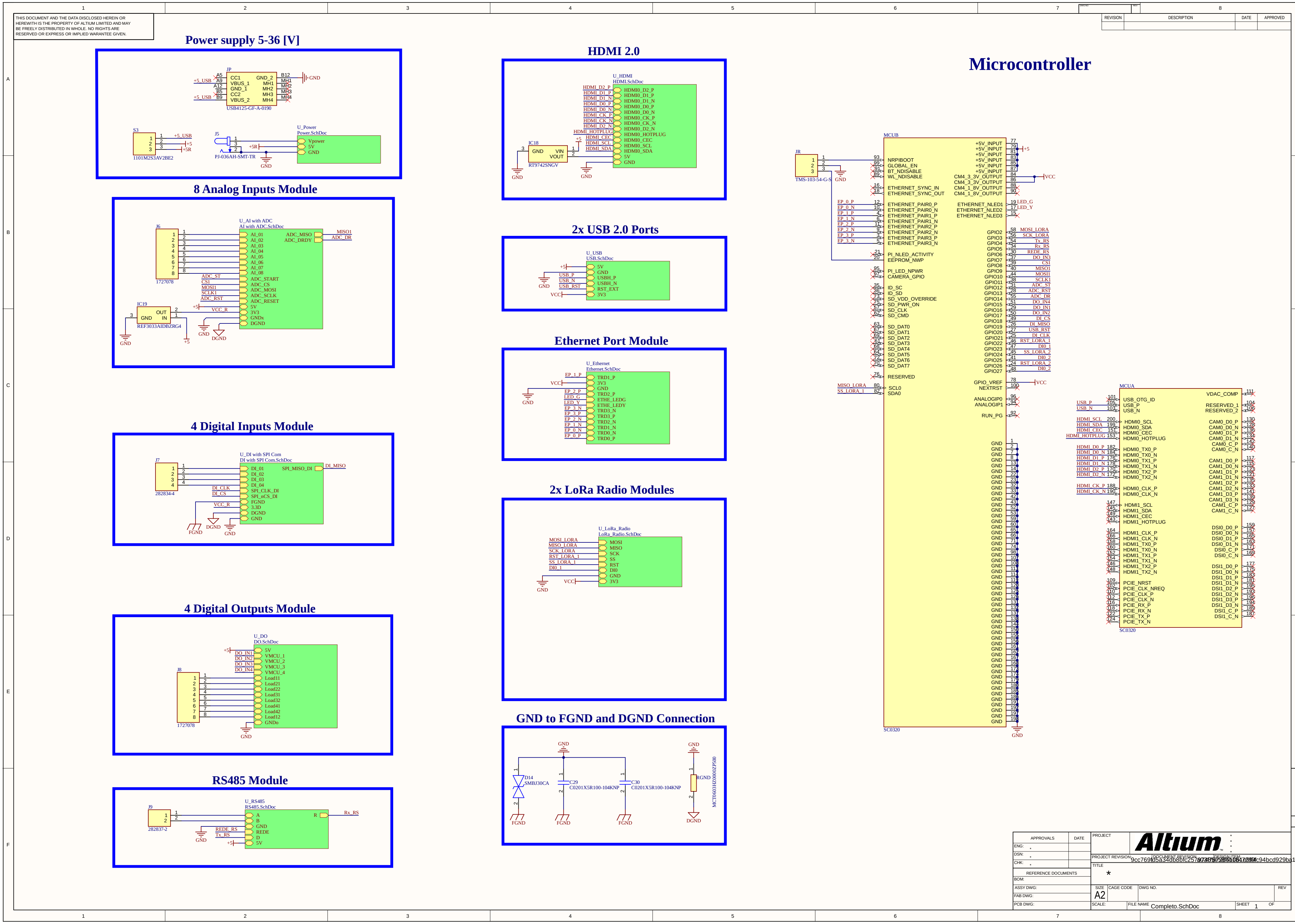
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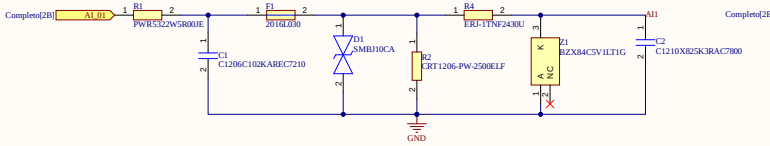
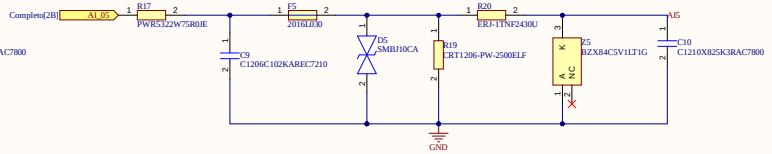
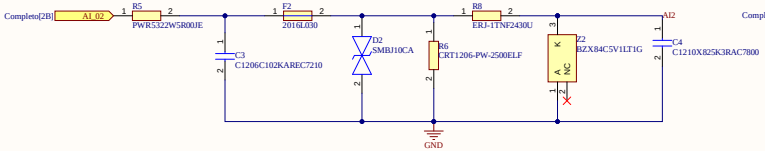
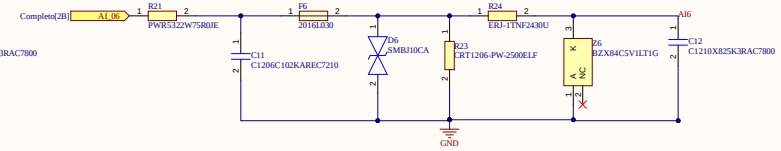
Power supply 5-36 [V]
8 Analog Inputs Module
4 Digital Inputs Module
4 Digital Outputs Module
RS485 Module
HDMI 2.0
2x USB 2.0 Ports
Ethernet Port Module
2x LoRa Radio Modules
GND to FGND and DGND Connection
Microcontroller
REVISION
DESCRIPTION
DATE
APPROVED
APPROVALS
ENG:
DSN:
CHK:
REFERENCE DOCUMENTS
BOM:
ASSY DWG:
FAB DWG:
PCB DWG:
PROJECT
PROJECT REVISION
TITLE
SIZE
A2
CAGE CODE
DWG NO.
REV
SCALE:
FILE NAME
Completo.SchDoc
SHEET
1
OF

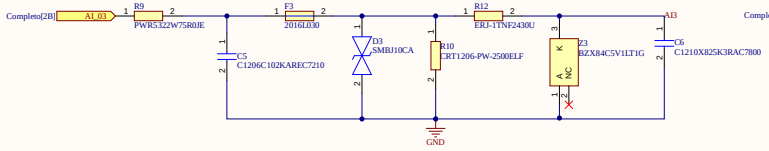
REVISION	DESCRIPTION	DATE	APPROVED

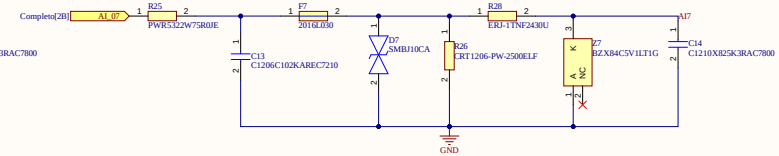


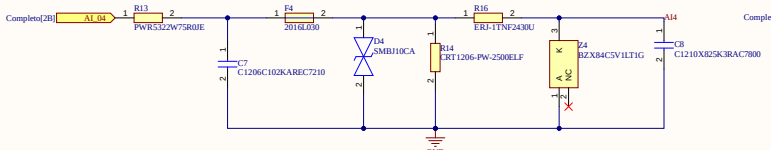


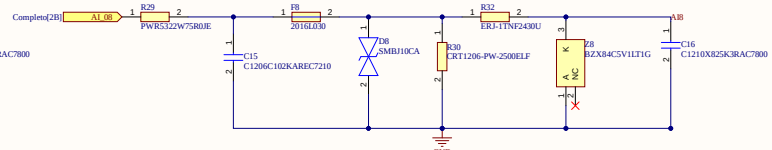


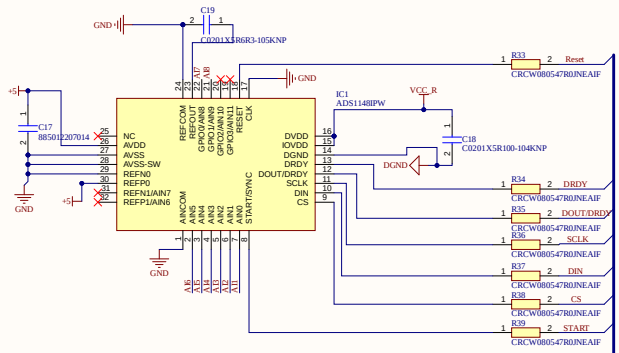


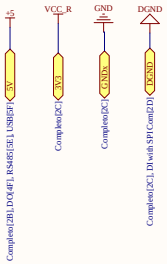












-Reset is a input from the mcu

- DRDY is a output that indicate that the DATA is READY at the output (0 is DATA READY).

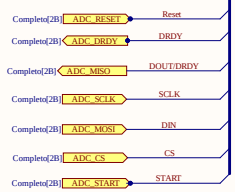
-DOUT/DRDY is a output that indicate serial data at the output is ready (0 is Dout and DRDY is ready).

-SCLK is a clock signal to the slaves of SPI communication.

-DIN or DATA IN is a MOSI port of the SPI communication.

-CS is the chip selector from de MCU. It is the same Chip Select of the SPI communication.

-START is a additional port for the communication and indicate from the MCU to the ADC that the conversation will starts. It should be connected to a GPIO port in the MCU.



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ENG: *	
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REFERENCE DOCUMENTS	
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ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: Altium

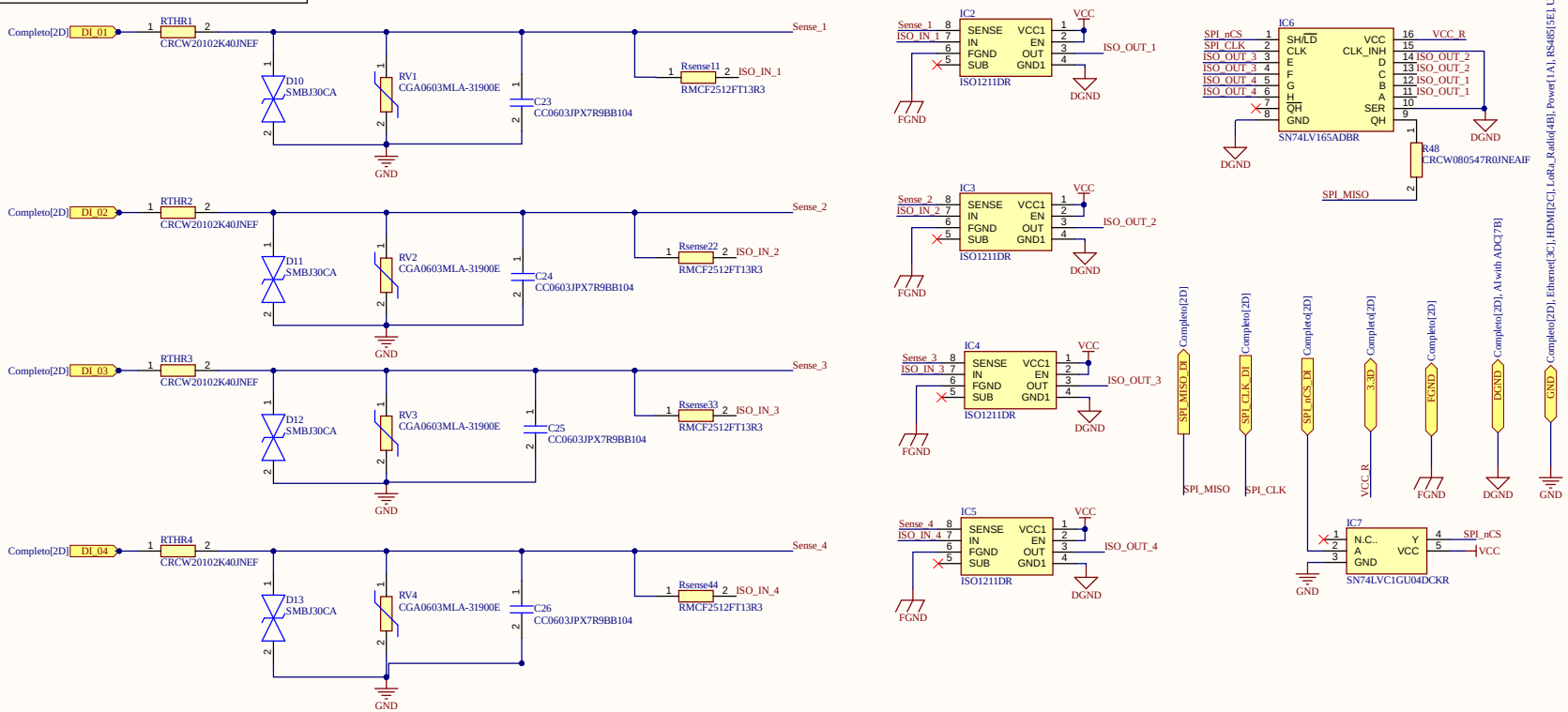
PROJECT REVISION: [illegible]

TITLE: *

SIZE	CAGE CODE	DWG NO.	REV
C			

SCALE: | FILE NAME: AI with ADC.SchDoc | SHEET 2 OF 10

9cc76915a34d8e0fce27[illegible]e2d1d8e4ba230eb712



REVISION	DESCRIPTION	DATE	APPROVED

APPROVALS	DATE
ENG: *	
DSN: *	
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REFERENCE DOCUMENTS
BOM:
ASSY DWG:
FAB DWG:
PCB DWG:

PROJECT *

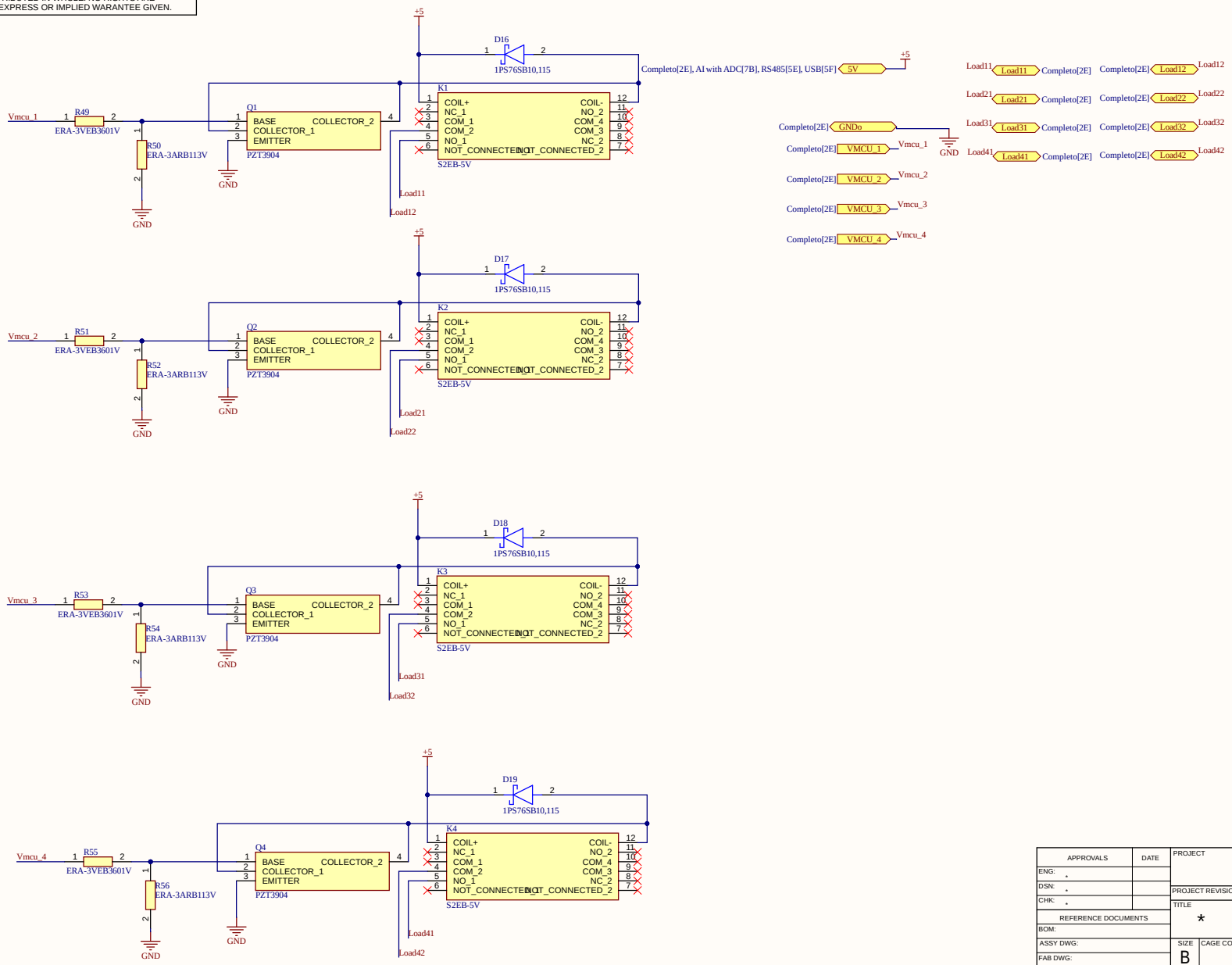
PROJECT REVISION: DOCUMENT REVISION: DESIGN ITEM ID: 9cc769fd5a34db8bfc257[illegible]e2d1d8e4ba230eb8

TITLE *

SIZE	CAGE CODE	DWG NO.	REV
B			

SCALE: FILE NAME DI with SPI Com.SchDoc SHEET 3 OF 10

REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
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REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: *

PROJECT REVISION: DOCUMENT REVISION: 9cc769fd5a34db8bfc257[illegible]e2d1d8e4ba230eb8

TITLE: *

SIZE	CAGE CODE	DWG NO.	REV
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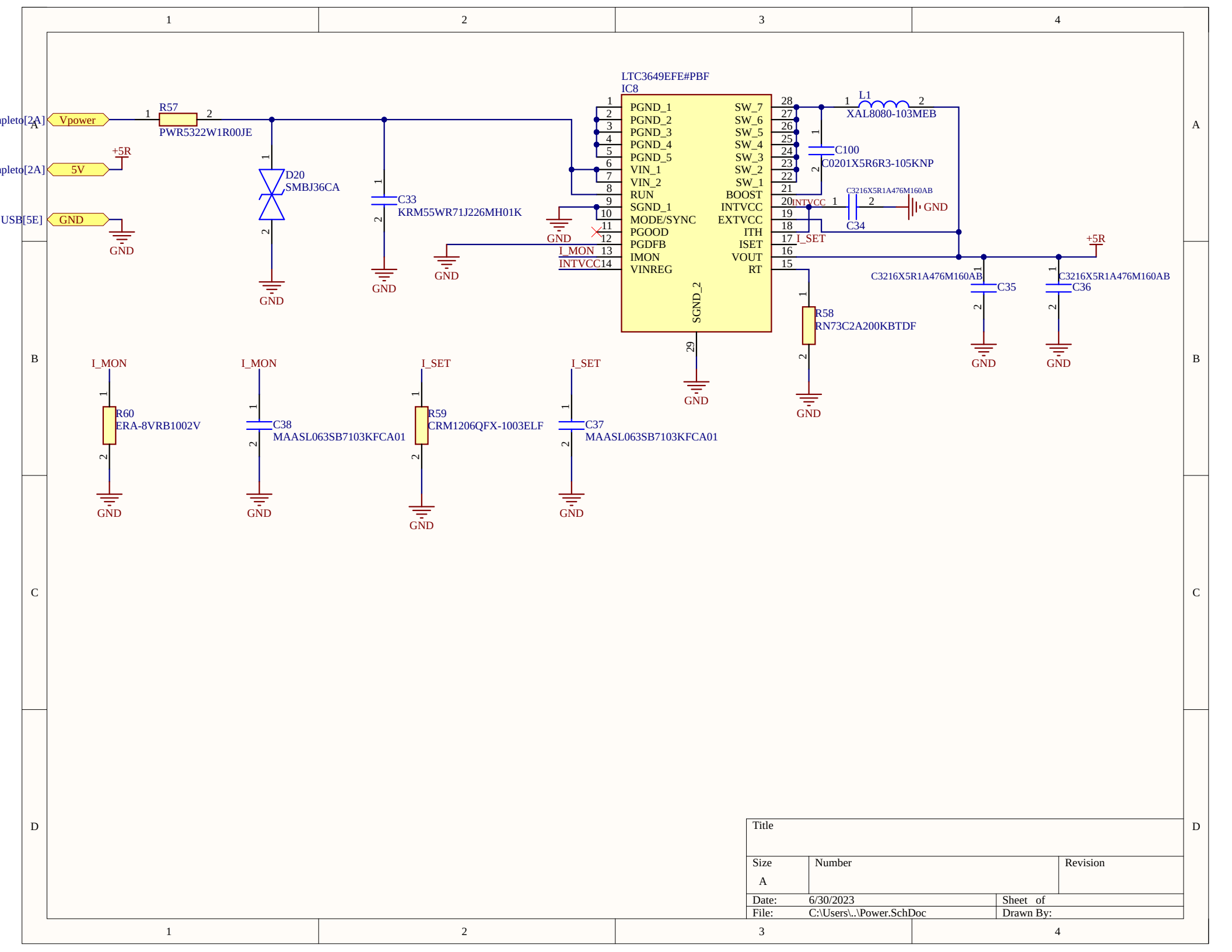
LTC3649EFE#PBF
IC8
PGND_1
PGND_2
PGND_3
PGND_4
PGND_5
VIN_1
VIN_2
RUN
SGND_1
MODE/SYNC
PGOOD
PGDFB
IMON
VINREG
SGND_2
SW_7
SW_6
SW_5
SW_4
SW_3
SW_2
SW_1
BOOST
INTVCC
EXTVCC
ITH
ISET
VOUT
RT
Vpower
R57
PWR5322W1R00JE
5V
+5R
GND
D20
SMBJ36CA
C33
KRM55WR71J226MH01K
I_MON
INTVCC
L1
XAL8080-103MEB
C100
C0201X5R6R3-105KNP
C34
C3216X5R1A476M160AB
I_SET
C35
C36
R58
RN73C2A200KBTDF
R60
ERA-8VRB1002V
C38
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R59
CRM1206QFX-1003ELF
C37
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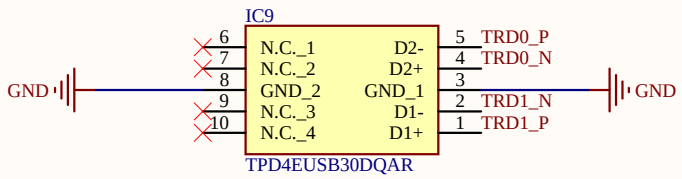
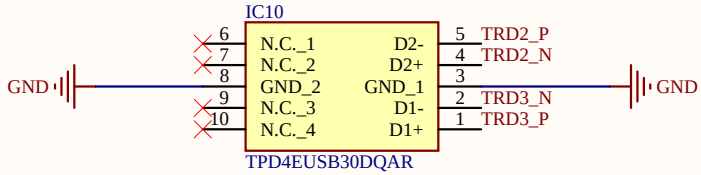
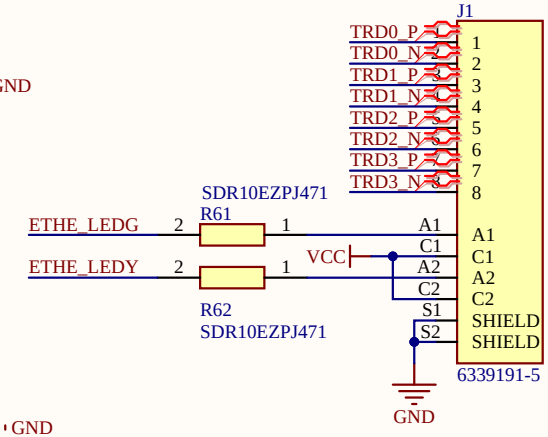
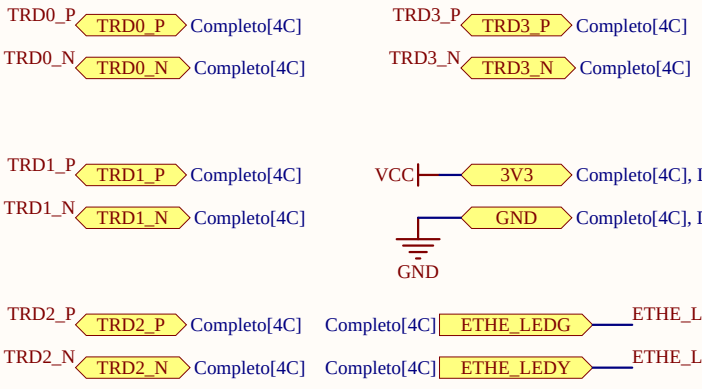
Number
Revision
Date:
6/30/2023
Sheet of
File:
C:\Users\..\Power.SchDoc
Drawn By:









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Date: 6/30/2023		Sheet of
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DWG. NO.	REV.	SHT.
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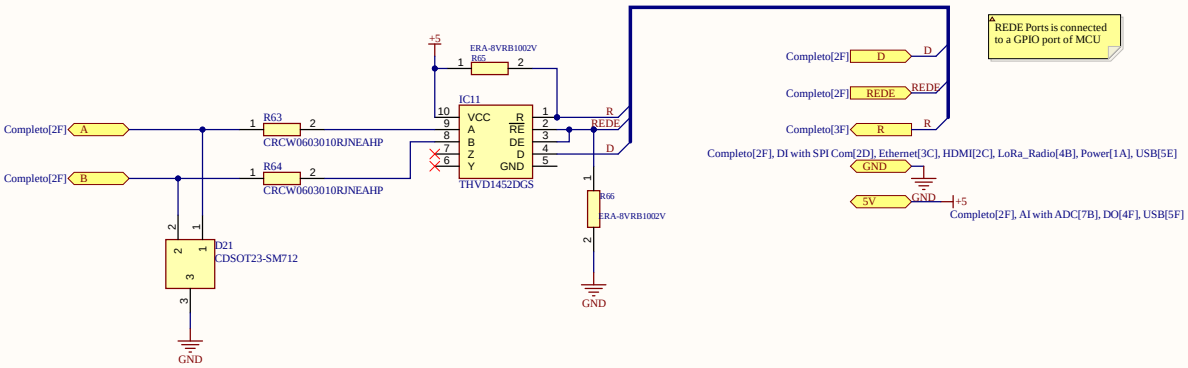
REVISION	DESCRIPTION	DATE	APPROVED



REDE Ports is connected to a GPIO port of MCU

Completo[2F] D D
Completo[2F] REDE REDE
Completo[3F] R R
Completo[2F], DI with SPI Com[2D], Ethernet[3C], HDMI[2C], LoRa_Radio[4B], Power[1A], USB[5E]
GND
5V GND +5
Completo[2F], AI with ADC[7B], DO[4F], USB[5F]

APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	
REFERENCE DOCUMENTS	
BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT *

PROJECT REVISION: DOCUMENT REVISION: RESOLUTION
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TITLE *

SIZE	CAGE CODE	DWG NO.	REV
B			

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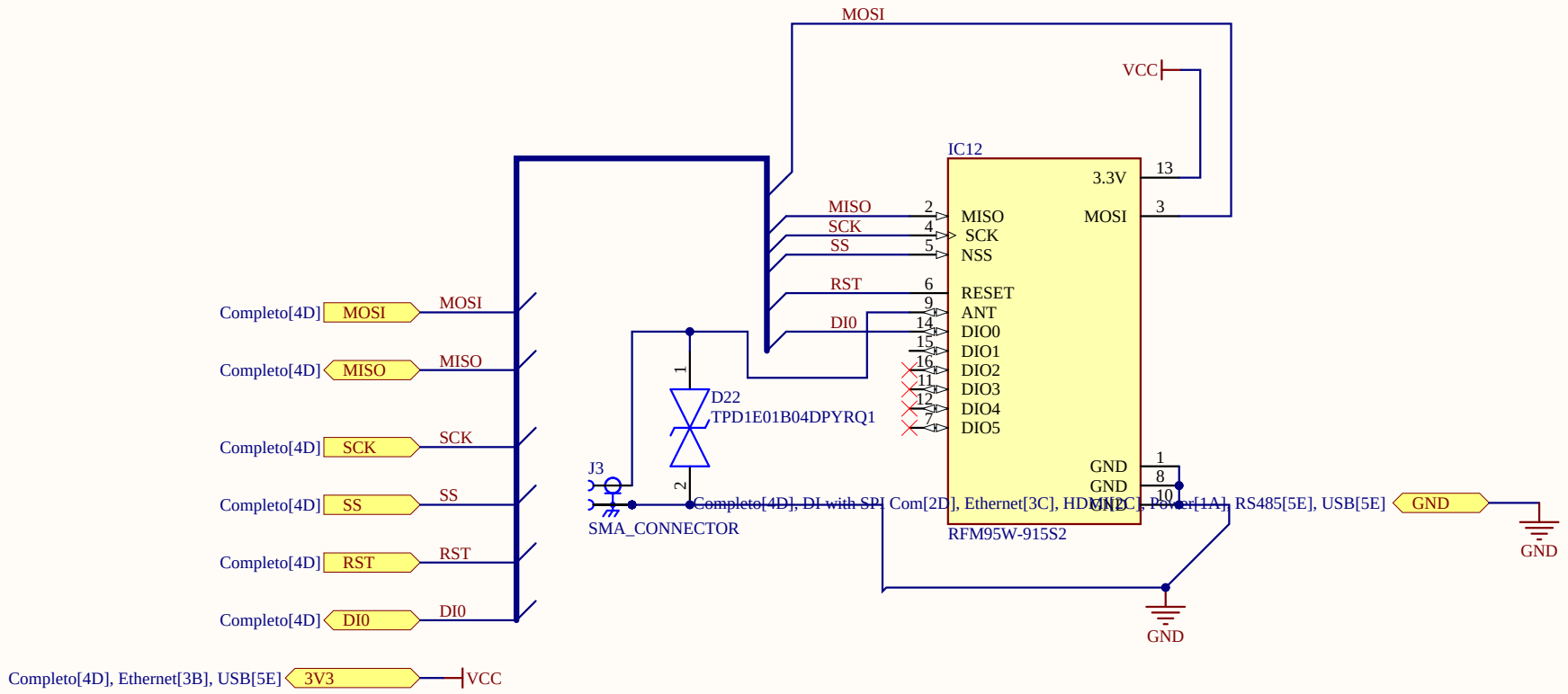

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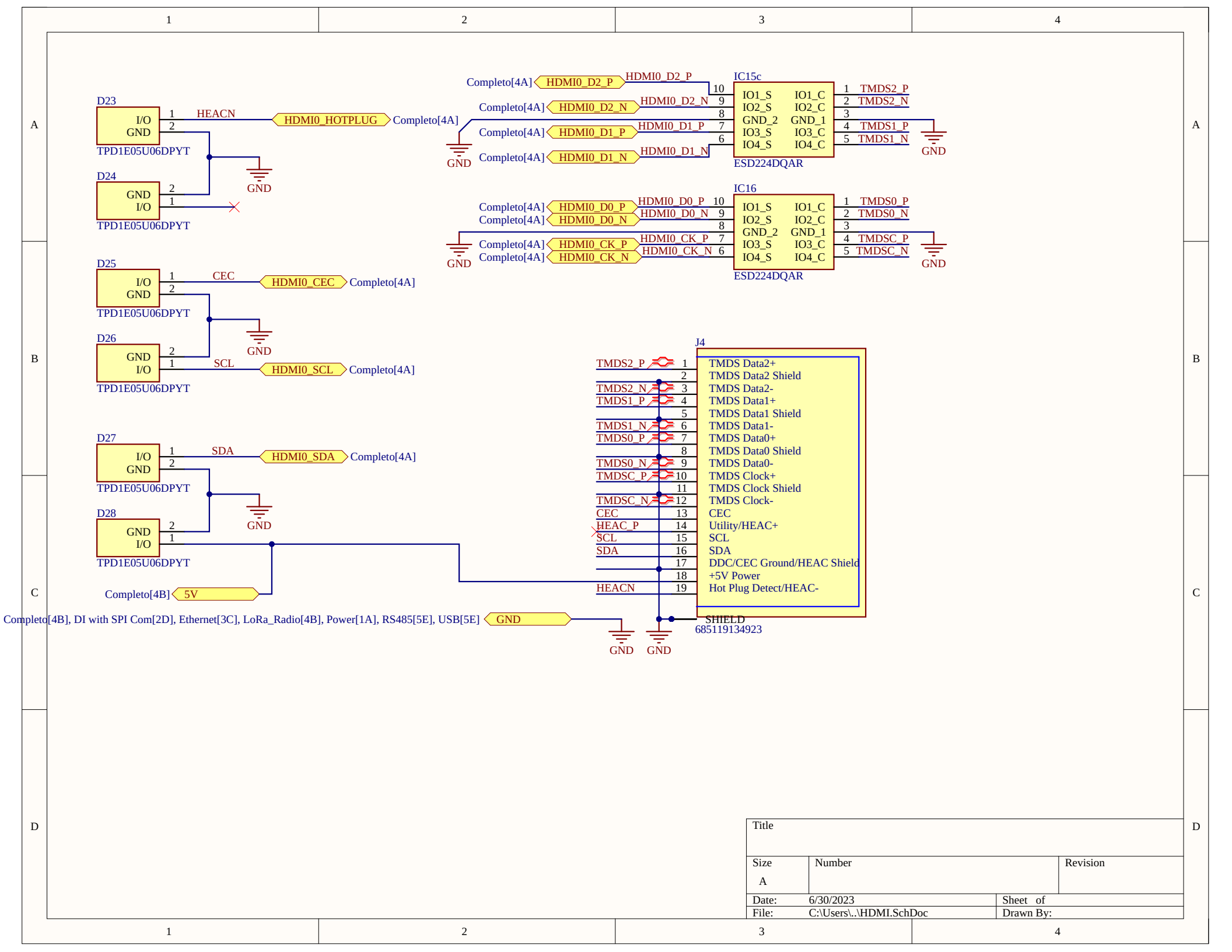
Date: 6/30/2023		Sheet of
File: C:\Users\..\LoRa_Radio.SchDoc		Drawn By:



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Date: 6/30/2023		Sheet of
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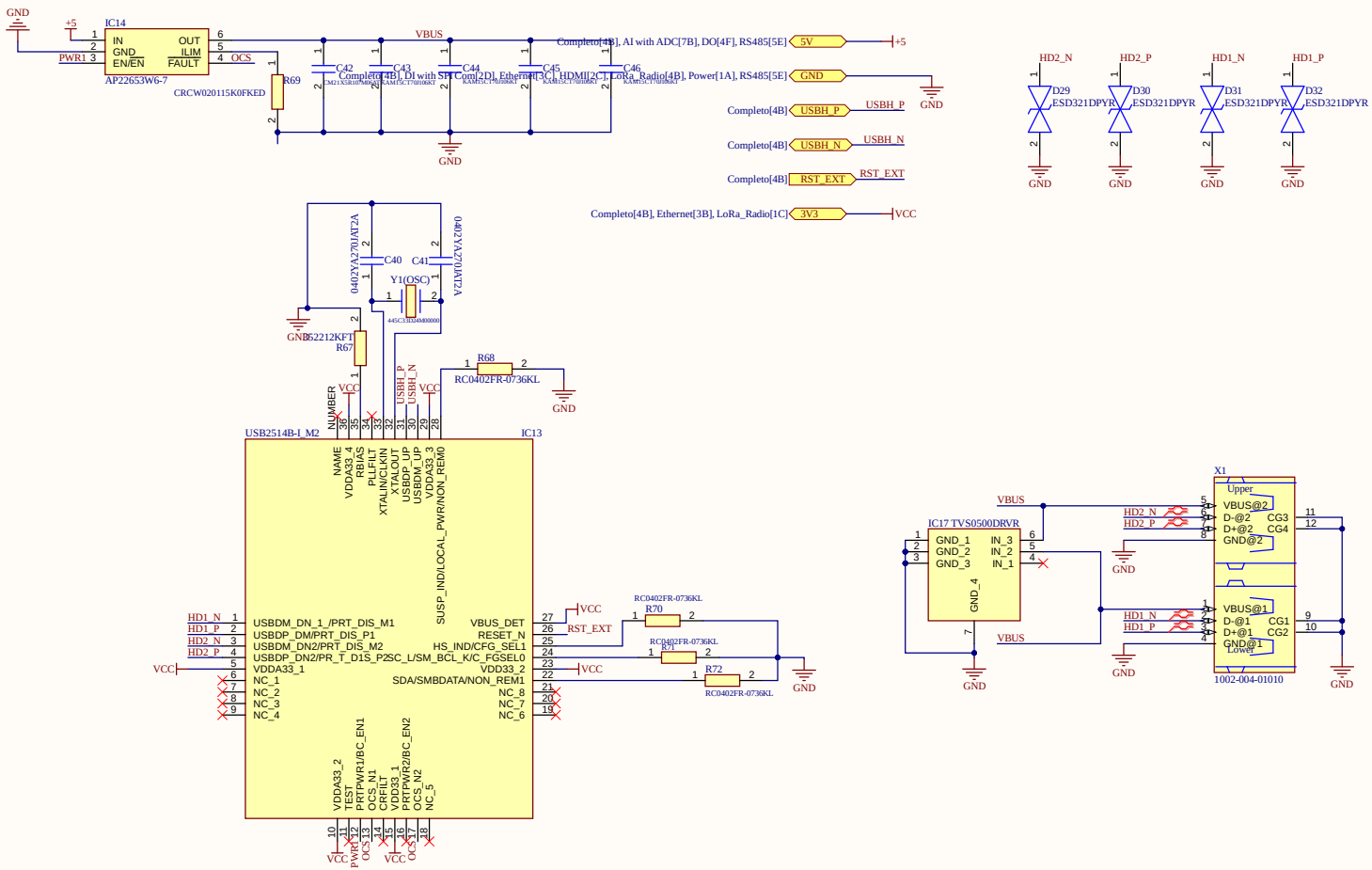
REVISION	DESCRIPTION	DATE	APPROVED



APPROVALS	DATE
ENG: *	
DSN: *	
CHK: *	
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BOM:	
ASSY DWG:	
FAB DWG:	
PCB DWG:	

PROJECT: Altium

PROJECT REVISION: DOCUMENT REVISION: DESIGN ITEM: 9cc7691d5a34db8bfc257[illegible]7067d2275eb6c792

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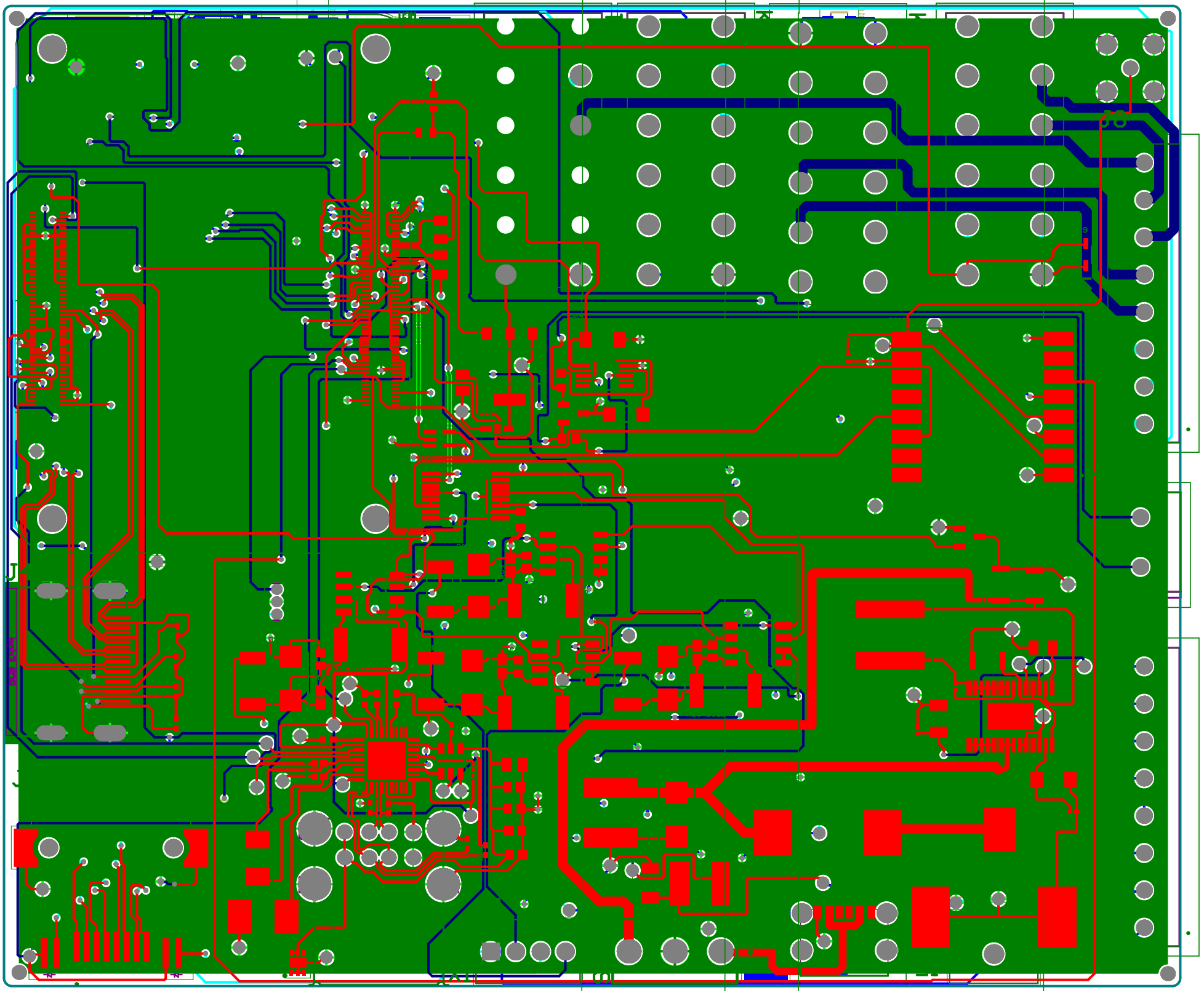
SIZE	CAGE CODE	DWG NO.	REV
B			

SCALE: FILE NAME: USB.SchDoc SHEET 10 OF 10



Board Stack Report