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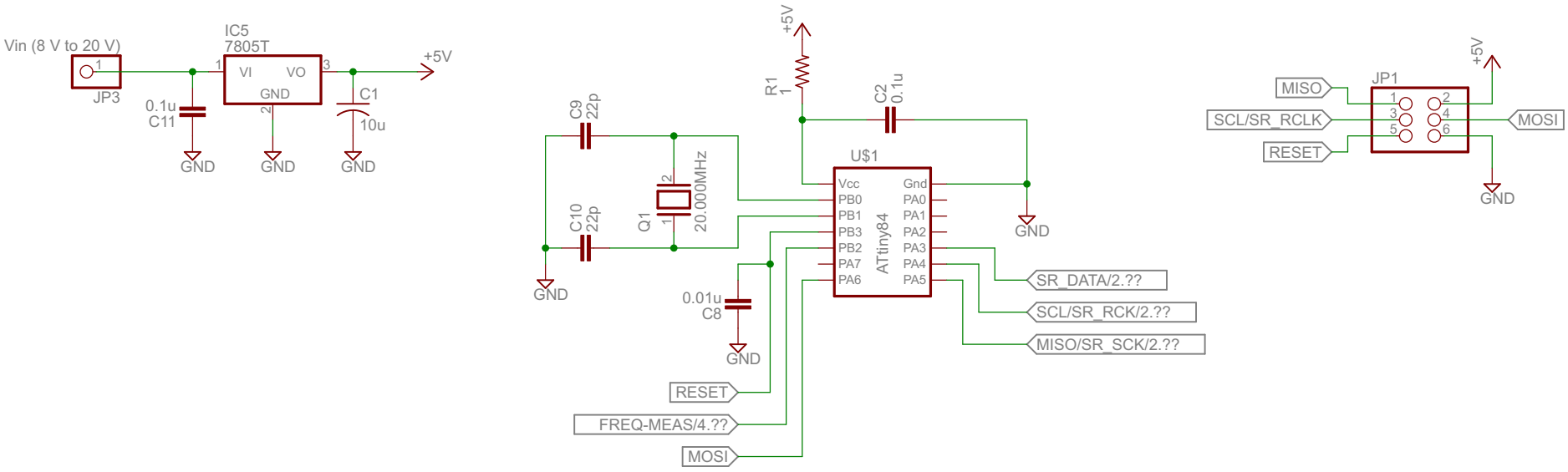
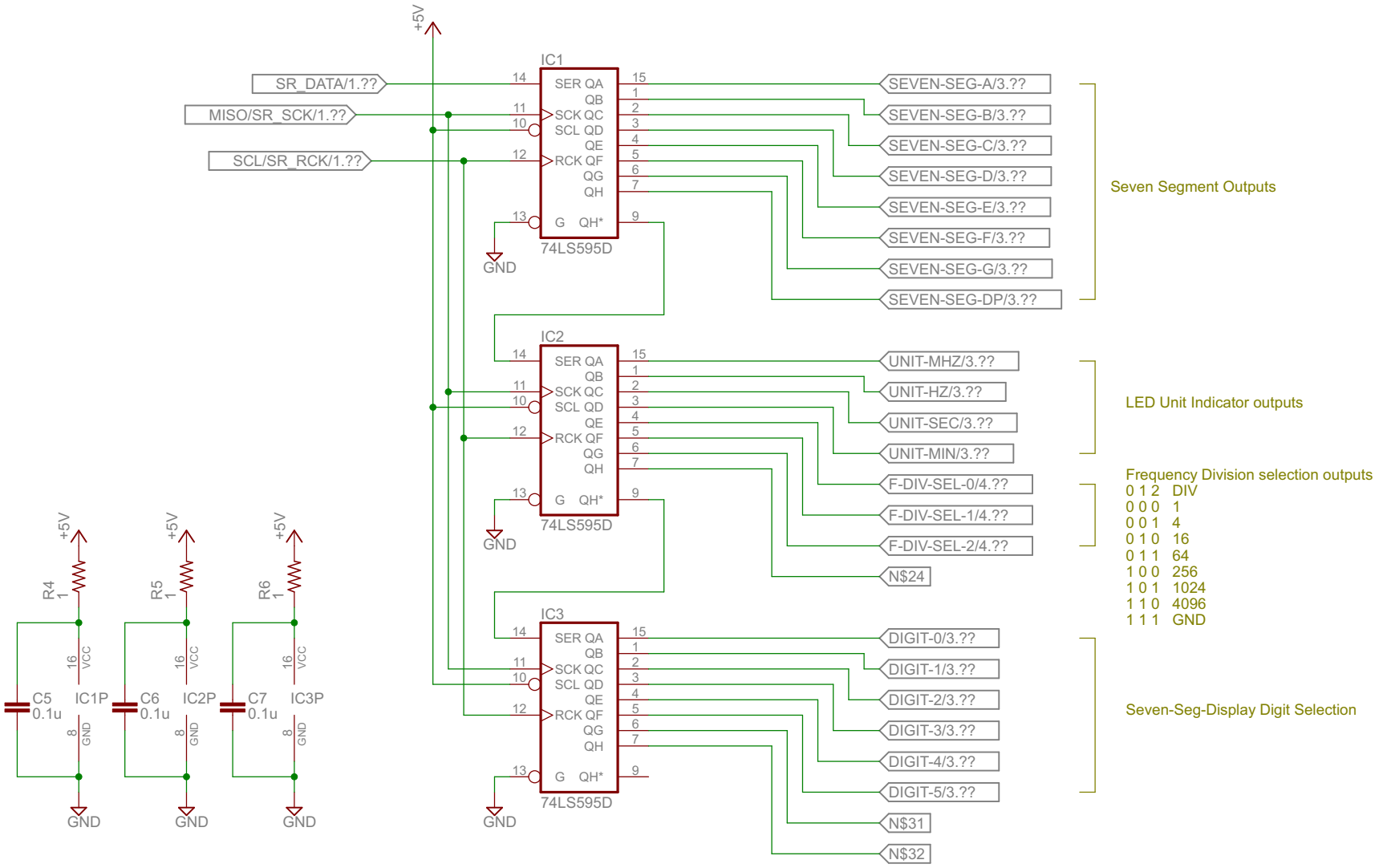
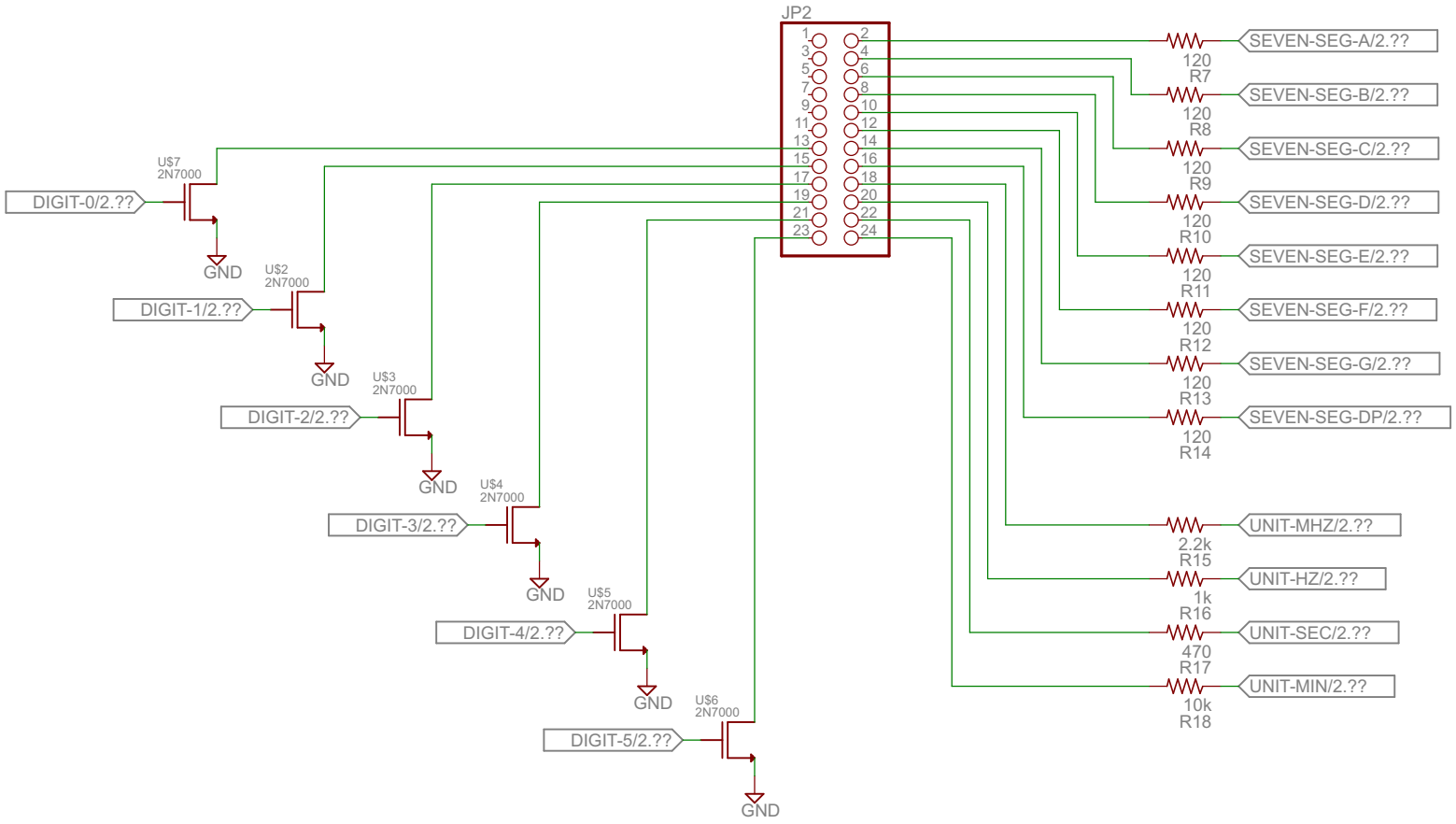
2016-April

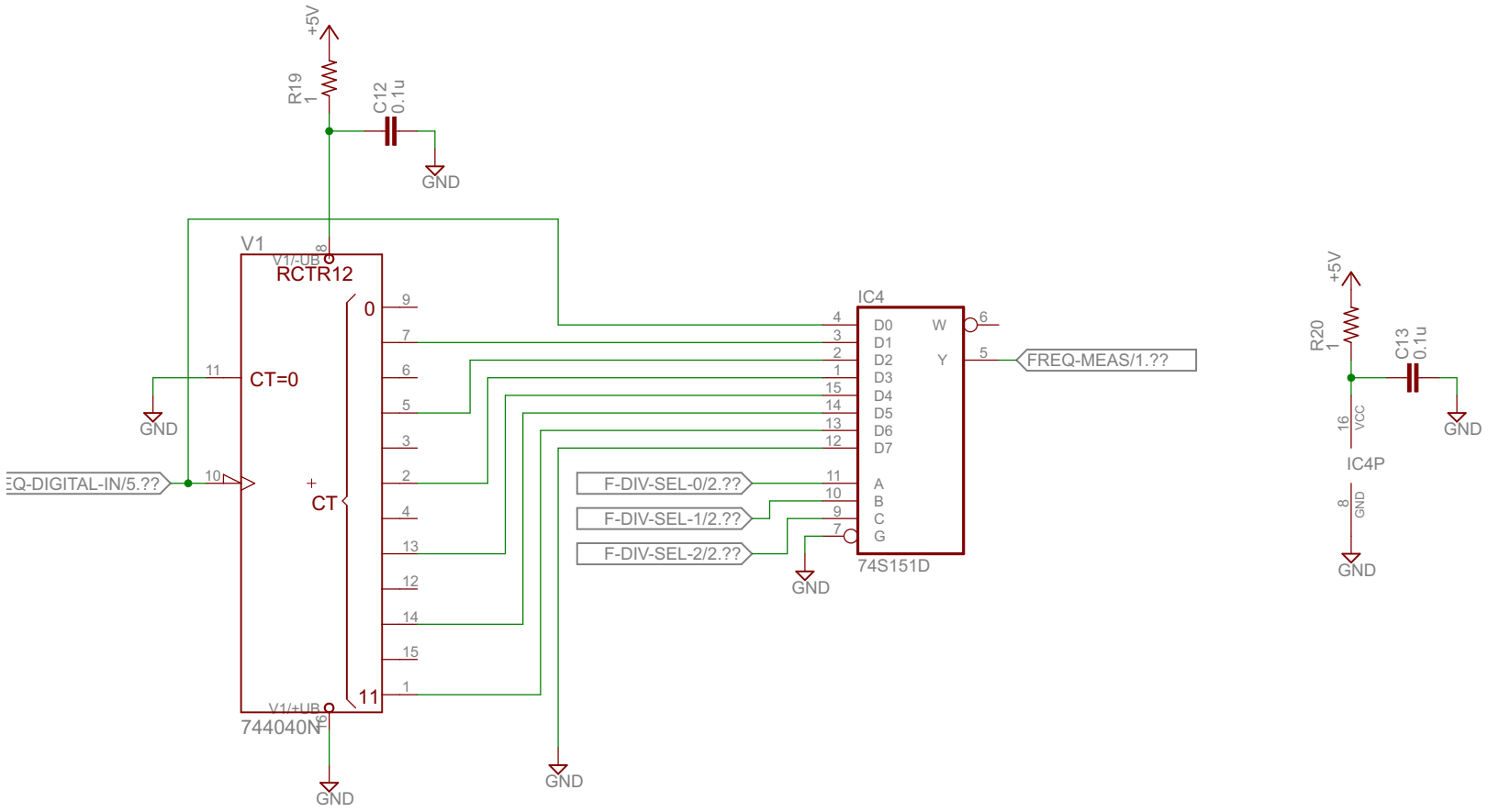
FreqCount84

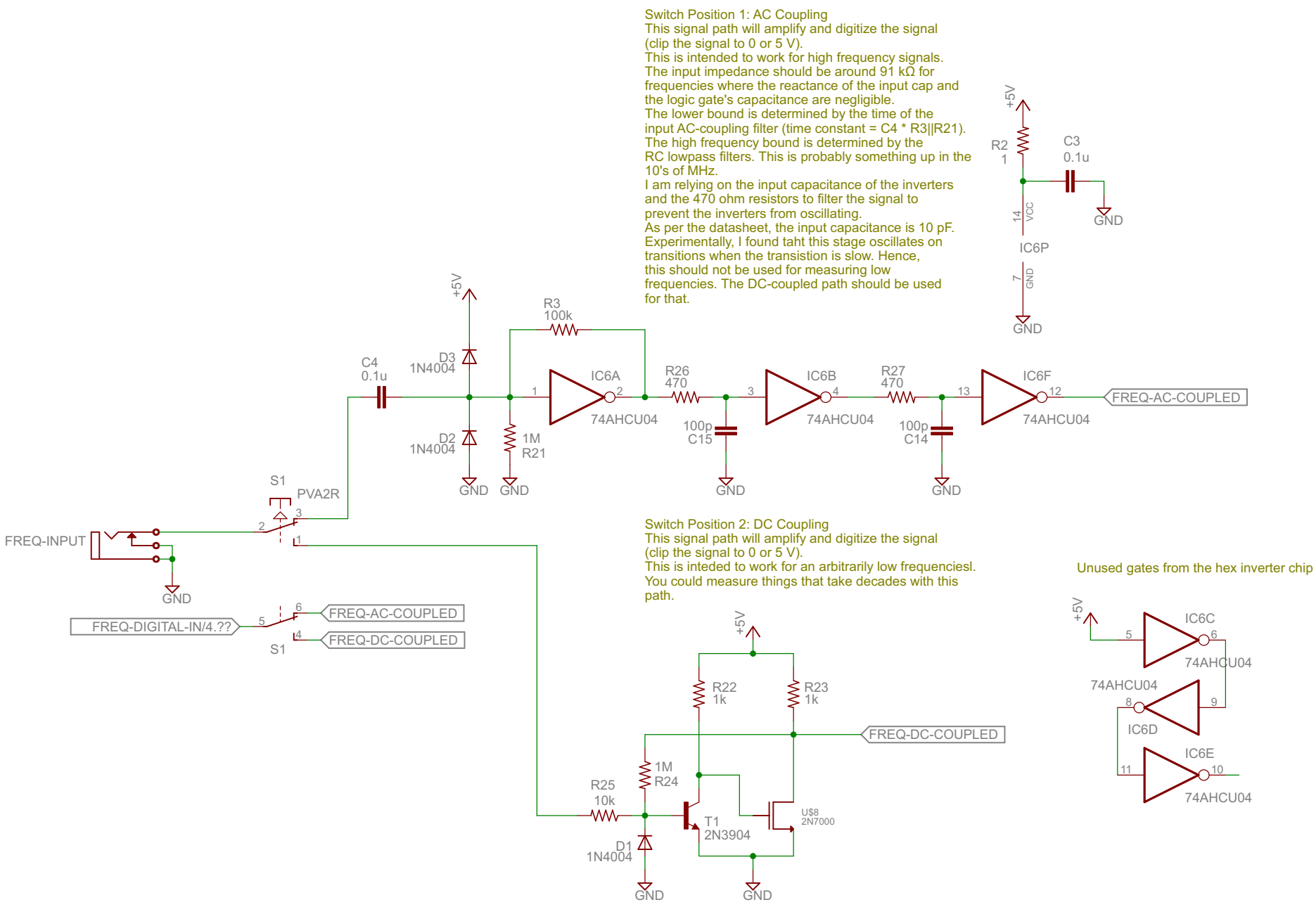
A frequency counter designed around the ATtiny84




+5V
IC1
SR_DATA/1.??
MISO/SR_SCK/1.??
SCL/SR_RCK/1.??
SER QA
QB
SCK QC
SCL QD
QE
RCK QF
QG
QH
G QH*
74LS595D
GND
SEVEN-SEG-A/3.??
SEVEN-SEG-B/3.??
SEVEN-SEG-C/3.??
SEVEN-SEG-D/3.??
SEVEN-SEG-E/3.??
SEVEN-SEG-F/3.??
SEVEN-SEG-G/3.??
SEVEN-SEG-DP/3.??
Seven Segment Outputs
IC2
UNIT-MHZ/3.??
UNIT-HZ/3.??
UNIT-SEC/3.??
UNIT-MIN/3.??
LED Unit Indicator outputs
F-DIV-SEL-0/4.??
F-DIV-SEL-1/4.??
F-DIV-SEL-2/4.??
N$24
Frequency Division selection outputs
0 1 2 DIV
0 0 0 1
0 0 1 4
0 1 0 16
0 1 1 64
1 0 0 256
1 0 1 1024
1 1 0 4096
1 1 1 GND
IC3
DIGIT-0/3.??
DIGIT-1/3.??
DIGIT-2/3.??
DIGIT-3/3.??
DIGIT-4/3.??
DIGIT-5/3.??
N$31
N$32
Seven-Seg-Display Digit Selection
R4 1
R5 1
R6 1
VCC
C5 0.1u
C6 0.1u
C7 0.1u
IC1P
IC2P
IC3P


JP2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
U$7
2N7000
U$2
2N7000
U$3
2N7000
U$4
2N7000
U$5
2N7000
U$6
2N7000
DIGIT-0/2.??
DIGIT-1/2.??
DIGIT-2/2.??
DIGIT-3/2.??
DIGIT-4/2.??
DIGIT-5/2.??
GND
GND
GND
GND
GND
GND
120
R7
120
R8
120
R9
120
R10
120
R11
120
R12
120
R13
120
R14
2.2k
R15
1k
R16
470
R17
10k
R18
SEVEN-SEG-A/2.??
SEVEN-SEG-B/2.??
SEVEN-SEG-C/2.??
SEVEN-SEG-D/2.??
SEVEN-SEG-E/2.??
SEVEN-SEG-F/2.??
SEVEN-SEG-G/2.??
SEVEN-SEG-DP/2.??
UNIT-MHZ/2.??
UNIT-HZ/2.??
UNIT-SEC/2.??
UNIT-MIN/2.??


+5V
R19
1
C12
0.1u
GND
V1
V1/-UB
8
RCTR12
0
9
7
6
5
3
2
4
13
12
14
15
1
11
CT=0
11
GND
10
CT
EQ-DIGITAL-IN/5.??
V1/+UB
16
744040N
GND
GND
IC4
D0
D1
D2
D3
D4
D5
D6
D7
A
B
C
G
W
Y
4
3
2
1
15
14
13
12
11
10
9
7
6
5
F-DIV-SEL-0/2.??
F-DIV-SEL-1/2.??
F-DIV-SEL-2/2.??
FREQ-MEAS/1.??
74S151D
GND
+5V
R20
1
C13
0.1u
16
VCC
IC4P
8
GND
GND


Switch Position 1: AC Coupling
This signal path will amplify and digitize the signal (clip the signal to 0 or 5 V).
This is intended to work for high frequency signals.
The input impedance should be around 91 kΩ for frequencies where the reactance of the input cap and the logic gate's capacitance are negligible.
The lower bound is determined by the time of the input AC-coupling filter (time constant = C4 * R3||R21).
The high frequency bound is determined by the RC lowpass filters. This is probably something up in the 10's of MHz.
I am relying on the input capacitance of the inverters and the 470 ohm resistors to filter the signal to prevent the inverters from oscillating.
As per the datasheet, the input capacitance is 10 pF.
Experimentally, I found taht this stage oscillates on transitions when the transistion is slow. Hence, this should not be used for measuring low frequencies. The DC-coupled path should be used for that.
+5V
R2
1
C3
0.1u
14
VCC
GND
IC6P
7
GND
GND
+5V
R3
100k
C4
0.1u
D3
1N4004
IC6A
R26
470
IC6B
R27
470
IC6F
FREQ-AC-COUPLED
74AHCU04
74AHCU04
74AHCU04
100p
C15
100p
C14
D2
1N4004
1M
R21
GND
GND
GND
GND
S1
PVA2R
FREQ-INPUT
GND
FREQ-DIGITAL-IN/4.??
FREQ-AC-COUPLED
FREQ-DC-COUPLED
S1
Switch Position 2: DC Coupling
This signal path will amplify and digitize the signal (clip the signal to 0 or 5 V).
This is inteded to work for an arbitrarily low frequenciesl. You could measure things that take decades with this path.
+5V
R22
1k
R23
1k
FREQ-DC-COUPLED
1M
R24
R25
10k
T1
2N3904
U$8
2N7000
D1
1N4004
GND
GND
Unused gates from the hex inverter chip
+5V
IC6C
74AHCU04
74AHCU04
IC6D
IC6E
74AHCU04