Properly Sizing MOSFETs for PWM Controllers

Fundamentals of Properly Sizing MOSFETs for Synchronous Buck Controllers and Their Effects on Efficiency

INTRODUCTION

Today's electronic designs are focusing more on optimizing efficiency in an attempt to minimize unnecessary power dissipation not only to maximize battery life in portable applications but to also assure that the application is running as "cool" as possible.

One of the challenges facing today's designers of synchronous buck PWM controllers is the proper selection of the external MOSFETs. Many designers are unaware that improper MOSFET selection can result in less than optimum efficiency and that proper selection becomes an even more prominent consideration as the conversion ratio increases (increasing input-to-output voltage ratios).

This application note first reviews the fundamentals of driving a MOSFET and then discusses the high-side and low-side MOSFET power losses. Efficiency versus load current data for a typical application circuit using the SP6133 synchronous buck PWM controller is then presented for several configurations of high-side and low-side MOSFETs to demonstrate the impact on efficiency for increasing conversion ratios.

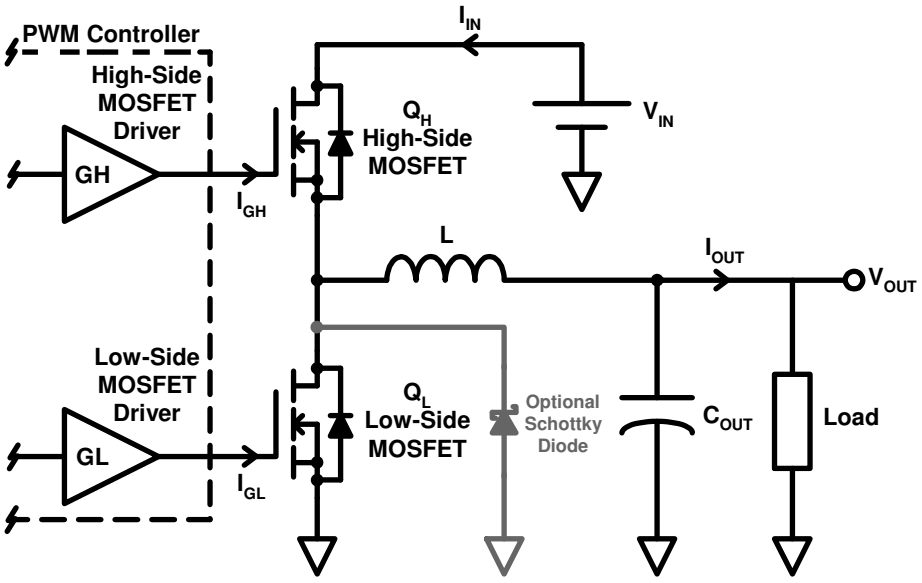


Figure 1: Simplified Synchronous Buck Converter Output Stage Diagram

FUNDAMENTALS OF DRIVING MOSFETS

Since a designer must select the external high-side and low-side MOSFETs required for synchronous PWM controllers, the fundamentals of driving these MOSFETs will be covered before discussing the power losses. Having a clearer understanding of the MOSFET driver and the load presented by the MOSFET will make the MOSFET selection process and the task of estimating their power losses less of a mystery.

A simplified synchronous buck converter diagram is shown in Figure 1. Notice that the gates of both the high-side and low-side MOSFETs are driven by independent MOSFET drivers which are contained within the PWM controller. The term "synchronous" is used to describe the process of turning "on" the low-side MOSFET when the high-side MOSFET is turned "off" (and visa versa). This results in higher efficiencies than those obtained by the classical non-synchronous converter that utilizes a Schottky diode in place of the low-side MOSFET. Sometimes this Schottky diode is included in synchronous designs and is placed in parallel with the low-side MOSFET to provide a momentary conduction path that is lower loss than the internal body diode of the low-side MOSFET before it is completely turned "on" by the low-side MOSFET driver.

A diagram illustrating the MOSFET driver/MOSFET interface is shown in Figure 2, and the resulting turn on and turn off switching waveforms are shown in Figure 3. The capacitances C_{GS}, C_{GD} and C_{DS} are used to model the capacitive loading effects of the MOSFET. The key MOSFET data sheet parameters for synchronous PWM buck controllers are the input capacitance C_{ISS}, the output capacitance C_{OSS}, the reverse capacitance C_{RSS}, the gate-to-source threshold voltage $V_{GS(TH)}$, the "Miller" gate plateau voltage V_{GP}, and the gate resistance R_G. Also, the key MOSFET driver data sheet parameter is the output impedance, R_O. The output current, I_G, (source or sink) of the MOSFET driver is limited by its output impedance R_O and is typically specified on the data sheet as R_O (high-level output impedance) and R_{OL} (low-level output impedance). It is important to understand these parameters and how they have an affect on the MOSFET switching transients and the resulting overall efficiency of the converter.

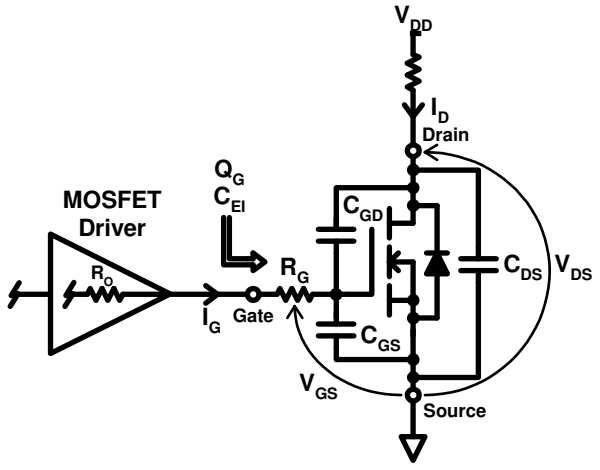
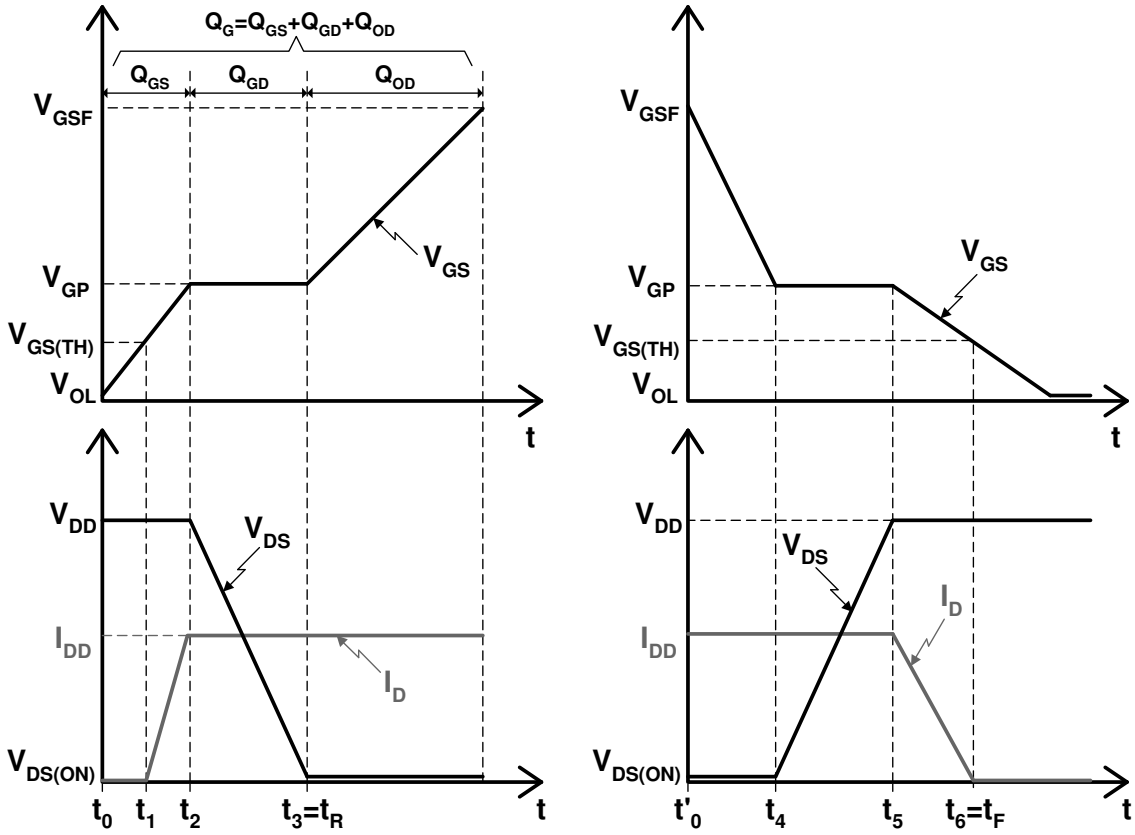


Figure 2: MOSFET Driver/MOSFET Interface.



Turn On Switching Waveforms **Turn Off Switching Waveforms**

Figure 3: Turn On & Turn Off Switching Waveforms

The variables in Figures 2 & 3 are defined and summarized in Table 2, and time events t_0 thru t_3 in Figure 3 are discussed in Table 1. When reviewing these switching waveforms and time events, keep in mind that the switching process happens rapidly (nano-seconds) and that the time events t_0 thru t_R and t_0 thru t_F are not intended to represent static states but rather key dynamic states that occur during the MOSFET switching process.

Time	Comment(s)
t_0	Output of MOSFET driver begins supplying gate charging current.
t_0 to t_1	The gate capacitance charges, and I_D=0 since $V_{GS}<V_{GS(TH)}$.
t_1	$V_{GS(TH)}$ is reached; therefore, channel enhancement begins, and $I_D>0$.
t_1 to t_0	The gate capacitance continues charging, and I_D increases due to increasing channel width.
t_2	The gate capacitance is fully charged, and $I_D=I_{DD}$.
t_2 to t_3	The MOSFET is operating in its "active" or "pinch off" region ($V_{GS}\geq V_{GS(TH)}$ and $V_{GD}\leq V_{GS(TH)}$), and C_{GD} discharges causing V_{DS} to decrease resulting in a "Miller" effect capacitance which steals current from the available gate charging current resulting in an approximate constant V_{GS} until C_{GD} has fully discharged. $I_D\cong I_{DD}$ (remains approximately at a constant value).
t_3	C_{GD} has fully discharged; therefore, V_{DS} is at a minimum, and the MOSFET is now operating in its "saturation" or "triode" region ($V_{GS}\geq V_{GS(TH)}$ and $V_{GD}\geq V_{GS(TH)}$).
t_3+	V_{GS} begins increasing again due to additional charging of the gate capacitance referred to as "overdrive" charging. The MOSFET Driver gate charging current is essentially zero once V_{GS} has reached its final value of V_{GSF}. At this point, the MOSFET's channel is fully enhanced.

Table 1: Discussion of Turn-On Time Events t_0 thru t_3 in Figure 3

Variable	Description	Units	Comment(s)
V_{GS}	Gate-to-Source Voltage	Volts	Instantaneous value
V_{GSF}	Final Gate-to-Source Voltage	Volts	$V_{GSF} >> V_{GS(TH)}$
$V_{GS(TH)}$	Gate-to-Source Threshold Voltage(Channel Enhancement Begins)	Volts	Obtained from MOSFET data sheet
V_{GP}	"Miller" Gate Plateau Voltage	Volts	Obtained from MOSFET data sheet
$V_{DS(ON)}$	"On" State Drain-to-Source Voltage	Volts	$V_{DS(ON)}=(I_D)(R_{DS(ON)})$ where $R_{DS(ON)}$ is the Drain-to-Source "On" state resistance of the MOSFET obtained from the data sheet
V_{DS}	Drain-to-Source Voltage	Volts	Instantaneous value
V_{DD}	Supply Voltage	Volts	Constant value
I_G	MOSFET Driver Output Current	Amps	Obtained from MOSFET driver/PWM controller data sheet
I_D	Drain Current	Amps	Instantaneous value
I_{DD}	Final Drain Current	Amps	Value of I_D when MOSFET channel is fully enhanced
Q_G	Total Gate Charge	Coulombs	$Q_G=Q_{GS}+Q_{GD}+Q_{OD}=(C_{EI})(V_{GSF})=(C_{EI})(V_{OH})$
Q_{GS}	Gate-to-Source Charge	Coulombs	-
Q_{GD}	Gate-to-Drain "Miller" Charge	Coulombs	-
Q_{OD}	Overdrive Charge After Charging "Miller" Capacitance	Coulombs	-
C_{GS}	Gate-to-Source Capacitance	Farads	$C_{ISS} = C_{GS} + C_{GD}$
C_{GD}	Gate-to-Drain Capacitance	Farads	$C_{RSS} = C_{GD}$
C_{DS}	Drain-to-Source Capacitance	Farads	$C_{OSS} = C_{GD} + C_{DS}$
C_{EI}	Equivalent Gate Capacitance	Farads	$C_{EI}=Q_G/V_{GSF}=Q_G/V_{OH}$
t_R	Rise Time	seconds	Majority of turn on switching losses occur during this time
t_F	Fall Time	seconds	Majority of turn off switching losses occur during this time
t	Time	seconds	-
R_G	Gate Resistance	Ohms	Obtained from MOSFET data sheet
R_O	MOSFET Driver Output Impedance (High-Level or Low-Level Output Impedance)	Ohms	$R_O=R_{OH}$ (High-Level Output Impedance) or R_{OL} (Low-Level Output Impedance). Obtained from MOSFET driver/PWM controller data sheet
$R_{DS(ON)}$	Drain-to-Source "On" State Resistance	Ohms	Obtained from MOSFET data sheet. Usually specified at one or more different gate-to-source voltages.

Table 2: Definition & Summary of Variables in Figures 2 & 3

The capacitances specified on most MOSFET data sheets are C_{iss} (input capacitance with V_{DS}=0V), C_{OSS} (output capacitance with V_{GS}=0V), and C_{RSS} (reverse capacitance with V_{GS}=0V). MOSFET manufacturers prefer to specify C_{RSS}, C_{OSS} and C_{RSS} instead of C_{GS}, C_{GD} and C_{DS} because they can be directly measured. The relationships between these capacitances are given by the following equations:

(1) $C_{ISS} = C_{GS} + C_{GD}$

(2) $C_{OSS} = C_{GD} + C_{DS}$

(3) $C_{RSS} = C_{GD}$

Since C_{ISS}, C_{OSS} and C_{RSS} can be obtained from the MOSFET's data sheet and $C_{RSS}=C_{GD}$, the other capacitances C_{GS} and C_{DS} can be easily obtained from these equations. It is common practice to assume that C_{GS} is a constant value and independent of the state of the MOSFET (values of V_{GS}, I_D, etc.). C_{GD} and C_{DS} on the other hand are both dependent on the value of V_{DS}; however, this relationship will be ignored to simplify the remainder of the discussion since we are primarily looking for approximate expressions for the turn on rise time and turn off fall time which can be used later to estimate the MOSFET switching losses .

The times t_1, t_2 and the time interval t_3-t_2 during the MOSFET turn "on" period are given by the following equations.

$$(4) \qquad t_1 = (R_{OH} + R_G)(C_{GS} + C_{GD}) \ln\left(\frac{1}{1 - \frac{V_{GS(TH)}}{V_{GSF}}}\right)$$

$$(5) \qquad t_2 = (R_{OH} + R_G)(C_{GS} + C_{GD}) \ln\left(\frac{1}{1 - \frac{V_{GP}}{V_{GSF}}}\right)$$

$$(6) \qquad t_3 - t_2 = \frac{(V_{DD} - V_{DS(ON)})(R_{OH} + R_G)(C_{GD})}{V_{GSF} - V_{GP}}$$

The majority of the turn-on switching losses in the MOSFET occur during the time frame t_3-t_1 which we will refer to as the rise time, t_R, and is approximately found from equations (1) thru (6) as

$$(7) \qquad t_R = \frac{(V_{DD})(C_{rss})(R_{OH} + R_G)}{V_{GSF} - V_{GP}} + (R_{OH} + R_G)(C_{iss}) \ln\left(\frac{V_{GSF} - V_{GS(TH)}}{V_{GSF} - V_{GP}}\right)$$

This expression will yield a fairly reasonable estimate for the turn-on switching rise time and will be utilized in the analysis of the high-side and low-side MOSFET power losses in the next section. As mentioned earlier, this expression for t_R assumes that C_{GD} and C_{DS} are both independent of the value of V_{DS}, and the value for $V_{DS(ON)}$ is assumed to be negligible. Also, the MOSFET package parasitic inductances were ignored in order to simplify the analysis. If these parasitics were taken into account, the rise time would be greater, so it is probably best to use the worst-case data sheet values for C_{RSS}, R_{OH}, R_G, C_{ISS}, etc that yield the largest rise time value in equation (7).

The time t_4, and the time intervals t_5-t_4 and t_6- t_5 during the MOSFET turn "off" period are given by the following equations.

$$(8) \qquad t_4 = (R_{OL} + R_G)(C_{GS} + C_{GD}) \ln\left(\frac{V_{GSF}}{V_{GP}}\right)$$

$$(9) \qquad t_5 - t_4 = (R_{OL} + R_G)(C_{GD})\left(\frac{V_{DD} - V_{DS(ON)}}{V_{GP}}\right)$$

$$(10) \qquad t_6 - t_5 = (R_{OL} + R_G)(C_{GS} + C_{GD})\left(\frac{V_{GP}}{V_{GS(TH)}}\right)$$

As with the calculation of turn-on switching losses, the majority of the turn-off switching losses in the MOSFET occur during the time frame t_6-t_4 which we will refer to as the fall time, t_F, and is approximately found from equations (1) thru (3) and (8) thru (9) as

$$(11) \qquad t_F = (R_{OL} + R_G)\left[C_{rss}\left(\frac{V_{DD}}{V_{GP}}\right) + C_{iss}\left(\frac{V_{GP}}{V_{GS(TH)}}\right)\right]$$

As with the turn-on switching rise time, this expression also yields a fairly reasonable estimate for the turn-off switching fall time and will be utilized in the analysis of the high-side and low-side MOSFET power losses in the next section.

Pertinent data sheet values used in the calculation of t_F and t_F using equations (7) and (8) are summarized in the following Table 3 for the **SP6133** synchronous buck (step-down) PWM controller driving the Vishay Siliconix Si4394DY and Si4320DY n-channel MOSFETs. For high conversion ratio buck converters, the Si4394DY is best used on the high-side, and the Si4320DY is best used on the low-side (more on this later).

	SP6133	Si4394DY	Si4320DY
V_{DD}	9V min, 12V typ, 15V max	-	-
V_{GSF}	5V typ	-	-
R_{OH}	2.5Ω typ, 3.9Ω max	-	-
R_{OL}	1.5Ω typ, 1.9Ω max	-	-
C_{ISS}	-	1900pF typ	6500pF typ
C_{OSS}	-	530pF typ	930pF typ
C_{RSS}	-	120pF typ	610pF typ
R_G	-	1.2Ω typ	1.1Ω typ
$R_{DS(ON)}$	-	7.7mΩ typ, 9.75mΩ max	3.2mΩ typ, 4mΩ max
$V_{GS(TH)}$	-	0.6V min, 1.8V max, 1.2V avg	1V min, 3V max, 2V avg
V_{GP}	-	2.0V typ	3.5V typ

Table 3: Pertinent Data Sheet Values for the SP6133, Si4394DY & Si4320DY

The minimum and maximum values for $V_{GS(TH)}$ were used to yield "average" values since typical values were not specified on the Si4394DY and Si4320DY data sheets.

The resulting values for t_R and t_F are summarized in Table 4 for several different values of the supply voltage V_{DD}.

	Si4394DY			Si4320DY		
V_{DD}	9V	12V	15V	9V	12V	15V
t_R	4.1ns	4.7ns	5.4ns	41ns	47ns	53ns
t_F	11.5ns	12.0ns	12.6ns	38.8ns	40.4ns	42.0ns

Table 4: t_R and t_F Estimates for the SP6133 Driving the Si4394DY & Si4320DY

Notice that the rise and fall time values for the Si4394DY are much smaller than those for the Si4320DY. This is a result of the Si4394DY's much smaller C_{ISS}, C_{OSS} and C_{RSS} capacitance values as summarized in Table 3. These rise and fall time values will be utilized in the next section when the high-side and low-side MOSFET power losses are investigated.

Another method commonly employed to provide rough estimates for the turn-on rise and turn-off fall times is to utilize the gate-to-source voltage (V_{GS}) versus total gate charge (Q_G) curve which is typically supplied on the MOSFET's data sheet. These curves for the Si4394DY and Si4320DY MOSFETs are shown in the following Figure 4.

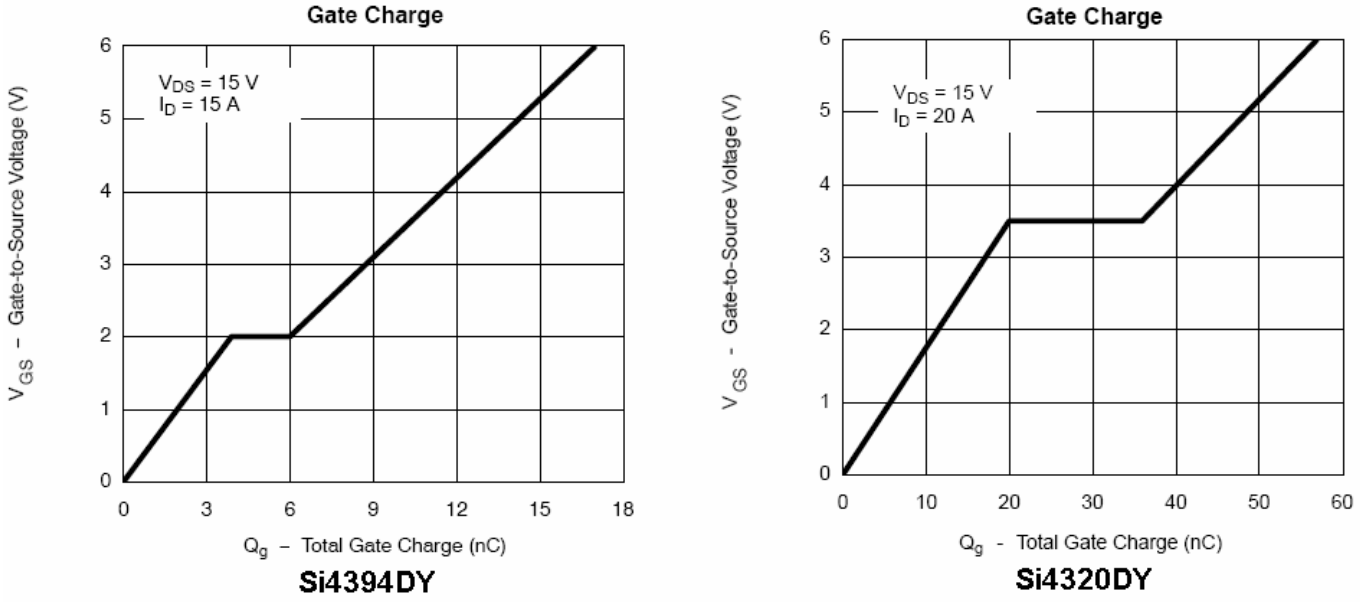


Figure 4: V_{GS} vs. Q_G Curves for the Si4394DY and Si4320DY MOSFETs

The final gate-to-source voltage, V_{GSF}, for the SP6133 was given earlier as 5V typ, so the total gate charge, Q_G, can be estimated from these curves as 14nC for the Si4394DY and 48nC for the Si4320DY. The MOSFET driver output current, I_G, is approximated for both the turn-on and turn-off switching time intervals as,

Si4394DY

$I_{G(ON)} \cong$ MOSFET Driver Turn-On Output Current (Source) $\cong V_{GSF}/(R_{OH} + R_{OH}) = 5V/(2.5\Omega + 1.2\Omega) = 1.35A$

$I_{G(OFF)} \cong$ MOSFET Driver Turn-Off Output Current (Sink) $\cong V_{GSF}/R_{OL} + R_G) = 5V/(1.5\Omega + 1.2\Omega) = 1.85A$

Si4320DY

$I_{G(ON)} \cong$ MOSFET Driver Turn-On Output Current (Source) $\cong V_{GSF}/(R_{OH} + R_G) = 5V/(2.5\Omega + 1.1\Omega) = 1.39A$

$I_{G(OFF)} \cong$ MOSFET Driver Turn-Off Output Current (Sink) $\cong V_{GSF}/R_{OL} + R_G) = 5V/(1.5\Omega + 1.1\Omega) = 1.92A$

This, of course, assumes that the MOSFET driver output current remains constant during the turn-on and turn-off switching transients which is not the case in reality. The turn-on rise and turn-off fall times can now be approximated for both MOSFETs as follows.

Si4394DY	Si4320DY
$t_R \cong Q_G/I_{G(ON)} = 14nC/1.35A = 10.4ns$	$t_R \cong Q_G/I_{G(ON)} = 48nC/1.39A = 34.5ns$
$t_F \cong Q_G/I_{G(OFF)} = 14nC/1.85A = 7.57ns$	$t_F \cong Q_G/I_{G(OFF)} = 48nC/1.92A = 25.0ns$

Keep in mind that these are simply quick estimates and that the results found earlier in Table 4 are going to be in better agreement with actual laboratory measurements.

HIGH-SIDE & LOW-SIDE MOSFET POWER LOSSES

For the simplified synchronous buck converter illustrated in Figure 1, the ratio of the input voltage to the output voltage is defined as the "conversion ratio" and is approximately equal to the inverse of the high-side MOSFET switch duty cycle. The high-side MOSFET duty cycle is defined as the ratio of its "on" time, t_{ON}, to the total switching frequency period which is constant for a fixed frequency PWM controller. The following equations summarize these relationships.

(12) $V_{OUT} < V_{IN}$

(13) $f_S \equiv$ *PWM Switching Frequency*

(14) $T \equiv$ *PWM Switching Frequency Period* $= 1/f_S$

(15) $D \equiv$ *Duty Cycle of High-Side MOSFET Switch* $\cong t_{ON}/T$

(16) $V_{IN}/V_{OUT} \equiv$ *Conversion Ratio* $\cong 1/D$

As can be seen from these relationships, buck converters with high conversion ratios create significant challenges for the PWM controller since the high-side MOSFET duty cycle decreases for increasing conversion ratios. Since high switching frequencies are generally employed in PWM controllers to reduce the size of the inductor and capacitors, very short duration high-side MOSFET pulses are required. For example, if V_{IN}=15V and V_{OUT}=1.8V, t_{ON} is found as 400ns for a PWM switching frequency of 300kHz, but is a mere 48ns for a PWM switching frequency of 2.5MHz. Producing PWM pulses this short in duration can prove to be challenging for most PWM controllers since it becomes taxing to fully turn the

MOSFET “on” before having to turn around and turn it back “off” again making it difficult to efficiently achieve high conversion ratios.

The power losses associated with the high-side and low-side MOSFETs are a combination of the conduction and switching losses. The conduction losses are a result of the I^2R losses in the MOSFET when it is fully enhanced and turned “on”, and the switching losses are a result of the MOSFET turn-on and turn-off transitions. The high-side MOSFET power losses, P_{QH}, and low-side MOSFET power losses, P_{QL}, can be approximated by the following equations.

$$(17) \quad P_{QH} = P_{QH(C)} + P_{QH(SW)} \cong I_{OUT}^2 R_{DS(ON)H} D + \left(\frac{t_{RH} + t_{FH}}{2} \right) V_{IN} I_{OUT} f_S$$

$$(18) \quad P_{QL} = P_{QL(C)} + P_{QL(SW)} \cong I_{OUT}^2 R_{DS(ON)L} (1 - D) + \left(\frac{t_{RL} + t_{FL}}{2} \right) V_{DIODEL} I_{OUT} f_S$$

Where,

$P_{QH(C)}$ ≡ High-Side MOSFET Conduction Losses
$P_{QH(SW)}$ ≡ High-Side MOSFET Switching Losses
$P_{QL(C)}$ ≡ Low-Side MOSFET Conduction Losses
$P_{QL(SW)}$ ≡ Low-Side MOSFET Switching Losses
$R_{DS(ON)H}$ ≡ High-Side MOSFET Drain-to-Source “On” State Resistance
$R_{DS(ON)L}$ ≡ Low-Side MOSFET Drain-to-Source “On” State Resistance
t_{RH} ≡ High-Side MOSFET Turn-On Rise Time
t_{RH} ≡ High-Side MOSFET Turn-Off Fall Time
t_{RL} ≡ Low-Side MOSFET Turn-On Rise Time
t_{FL} ≡ Low-Side MOSFET Turn-Off Fall Time
V_{DIODEL} ≡ Low-Side MOSFET Internal Body Diode Forward Voltage Drop

Approximate expressions for the turn-on rise and turn-off fall times were found in the previous section and can be utilized in equation (17) to approximate the switching power losses for the high-side and low-side MOSFETs. Keep in mind that a MOSFET with a lower $R_{DS(ON)}$ will result in lower conduction losses; however, it typically will have a higher Q_G resulting in higher switching losses, so a careful balance between these characteristics should be considered to maximize efficiency. Also, notice that the low-side MOSFET switching losses depends on the MOSFET’s own internal body diode since it limits the voltage drop across the MOSFET during switching transitions to about 1V for both the Si4394DY and Si4320DY. An external Schottky diode can be added in parallel with the low-side MOSFET to further reduce these switching losses since they typically have forward voltage drops of just a few tenths of a volt.

As can be seen upon examination of P_{QH}, the high-side MOSFET conduction losses increase as $R_{DS(ON)}$, I_{OUT} or D increase (or as the conversion ratio 1/D

decreases), and the switching losses increase as Q_G (and, therefore t_{RH} and t_{FH}), V_{IN}, I_{OUT} or f_T increase. A similar examination of P_{QL} shows the low-side MOSFET conduction losses also increase as $R_{DS(ON)}$, I_{OUT} or the conversion ratio 1/D increase (or as D decreases), and the switching losses also increase as Q_G (and, therefore t_{RL} and t_{RL}), I_{OUT} or f_S increase. Keep in mind that V_{DIODEL} will stay fairly constant for varying operational parameters such as I_{OUT}, V_{OUT}, D, etc. The entire term for $P_{QL(SW)}$ can become negligible in some cases if a low forward voltage drop Schottky diode is added in parallel with the low-side MOSFET making it a near zero-voltage-switched device.

As intuition might suggest, for a given PWM switching frequency the efficiency peaks where conduction losses in the high-side MOSFET are equal to its switching losses. Therefore, the high-side and low-side MOSFET selection procedure should begin by first identifying the nominal operational values for V_{IIN}, V_{OUT}, I_{OUT} and f_{OUT}. A reasonable attempt should then be made to identify a high-side MOSFET that has parameters resulting in approximately equal conduction and switching losses. The low-side MOSFET should then be selected that has the lowest possible $R_{DS(ON)}$ that is available in a small enough package that satisfies any space or cost constraints. Care must also be taken to assure that the maximum junction temperature is not exceeded for each MOSFET over the entire input voltage range at the maximum expected load current and ambient temperature.

APPLICATION CIRCUIT

The SP6133 is a synchronous buck (step-down) PWM controller and is designed to drive a pair of external, n-channel, enhancement mode MOSFETs at a fixed 300 kHz frequency. The part is designed for single supply operation at input voltages ranging from 5V up to 24V and can generate output voltages as low as 0.8V and up to 95% of the input voltage. The part's powerful internal MOSFET gate drivers can drive the gates of external MOSFETs capable of handling output currents as high 30A.

A schematic of the application circuit used to collect efficiency versus load current data can be seen in Figure 5. The circuit utilizes the SP6133 synchronous buck PWM controller. Several different MOSFET configurations were investigated using the Vishay Siliconix Si4320DY and Si4394DY n-channel MOSFETs. The input voltage, V_{IN}, was varied from 9V up to 15V while the output voltage, V_{OUT}, was held constant at 3.3V; therefore, as the input voltage is increased the conversion ratio increases. For each MOSFET configuration and input voltage, the load current was swept from 0A up to 10A using an electronic DC load.

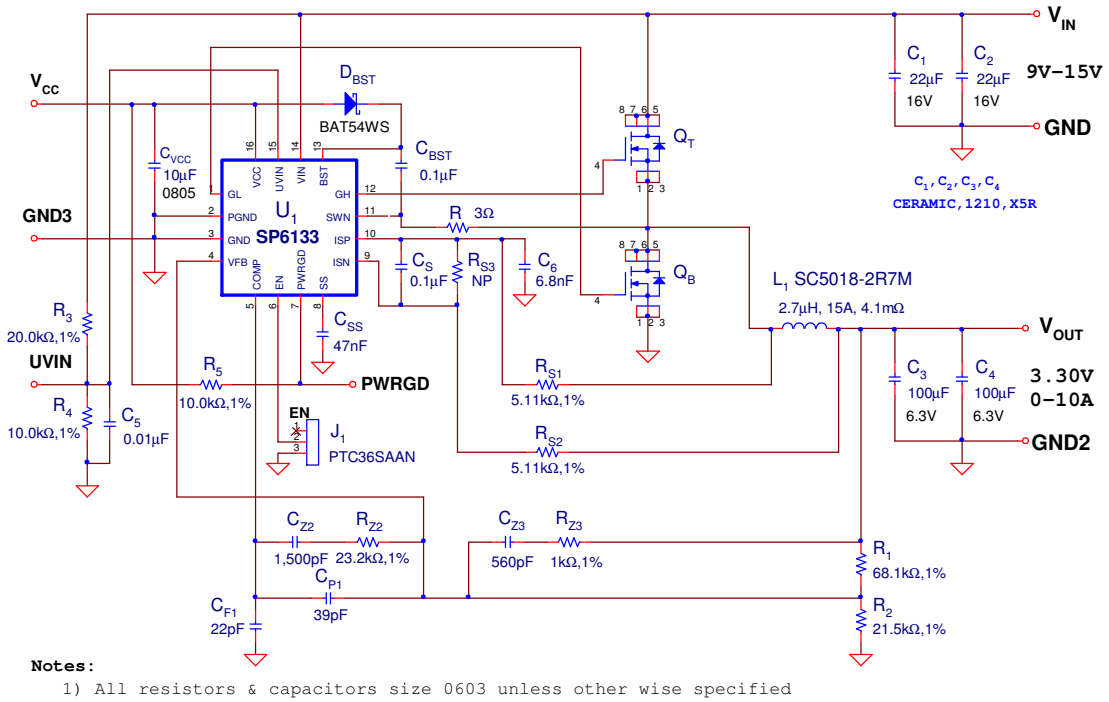


Figure 5: Application Circuit Schematic Using the SP6133

EFFICIENCY DATA

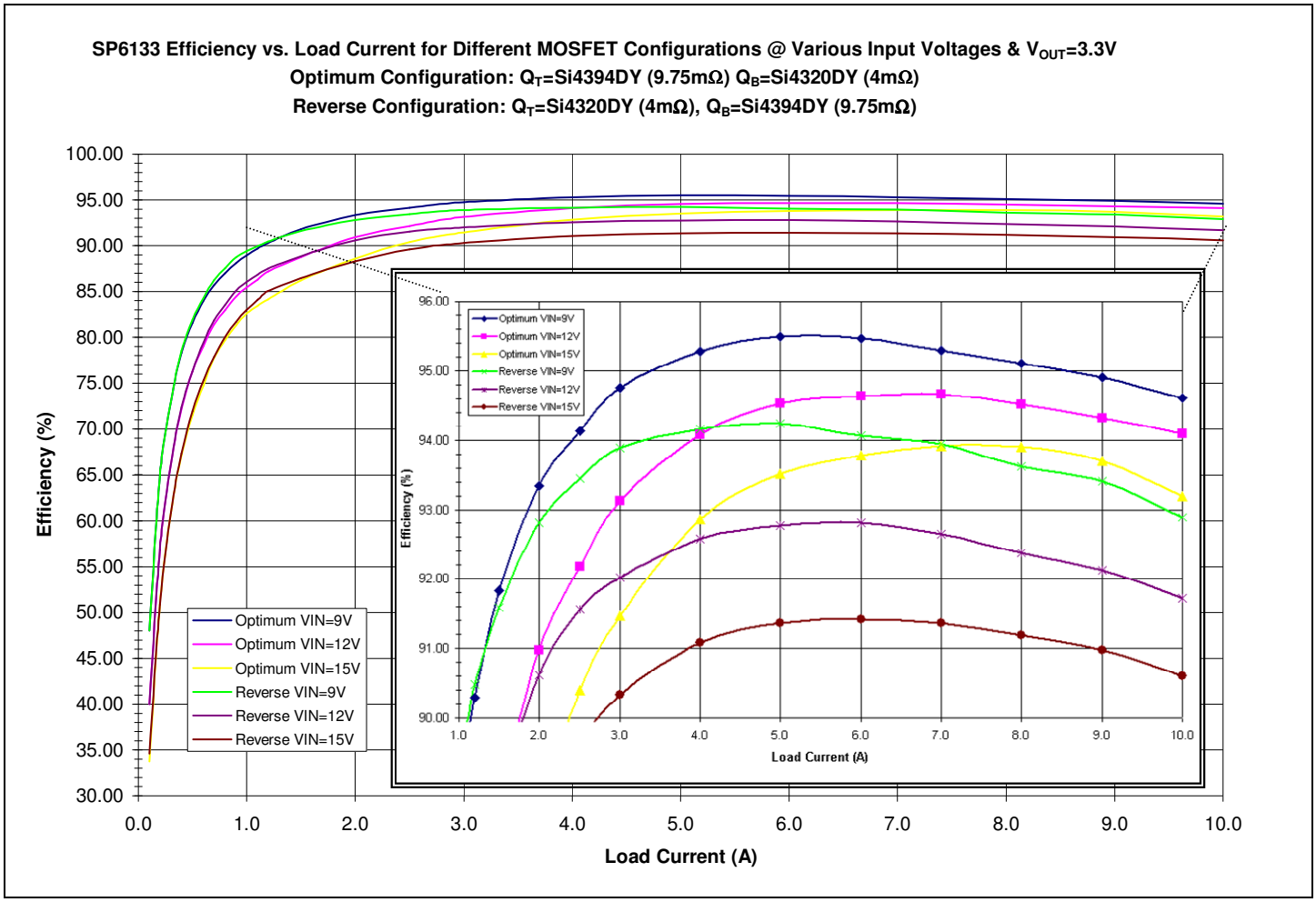
Efficiency versus load current data for the application circuit presented in Figure 5 was collected for several configurations of high-side (Q_T) and low-side (Q_B) MOSFETs in order to demonstrate the impact on the efficiency for increasing conversion ratios.

Three different input voltages were used to collect the data: 9V, 12V and 15V. The output voltage was held constant at 3.3V while the output current was swept from 0A up to 10A. Data was collected for several different MOSFET configurations as outlined in Table 5.

MOSFET Configuration	Q_T	Q_B	Comment
Optimum	Si4394DY (9.75mΩ)	Si4320DY (4mΩ)	Low Switching & Conduction Losses
Reverse	Si4320DY (4mΩ)	Si4394DY (9.75mΩ)	High Switching & Conduction Losses
High-Side Substitute	Si4320DY (4mΩ)	Si4320DY (4mΩ)	High Switching Losses
Low-Side Substitute	Si4394DY (9.75mΩ)	Si4394DY (9.75mΩ)	High Conduction Losses

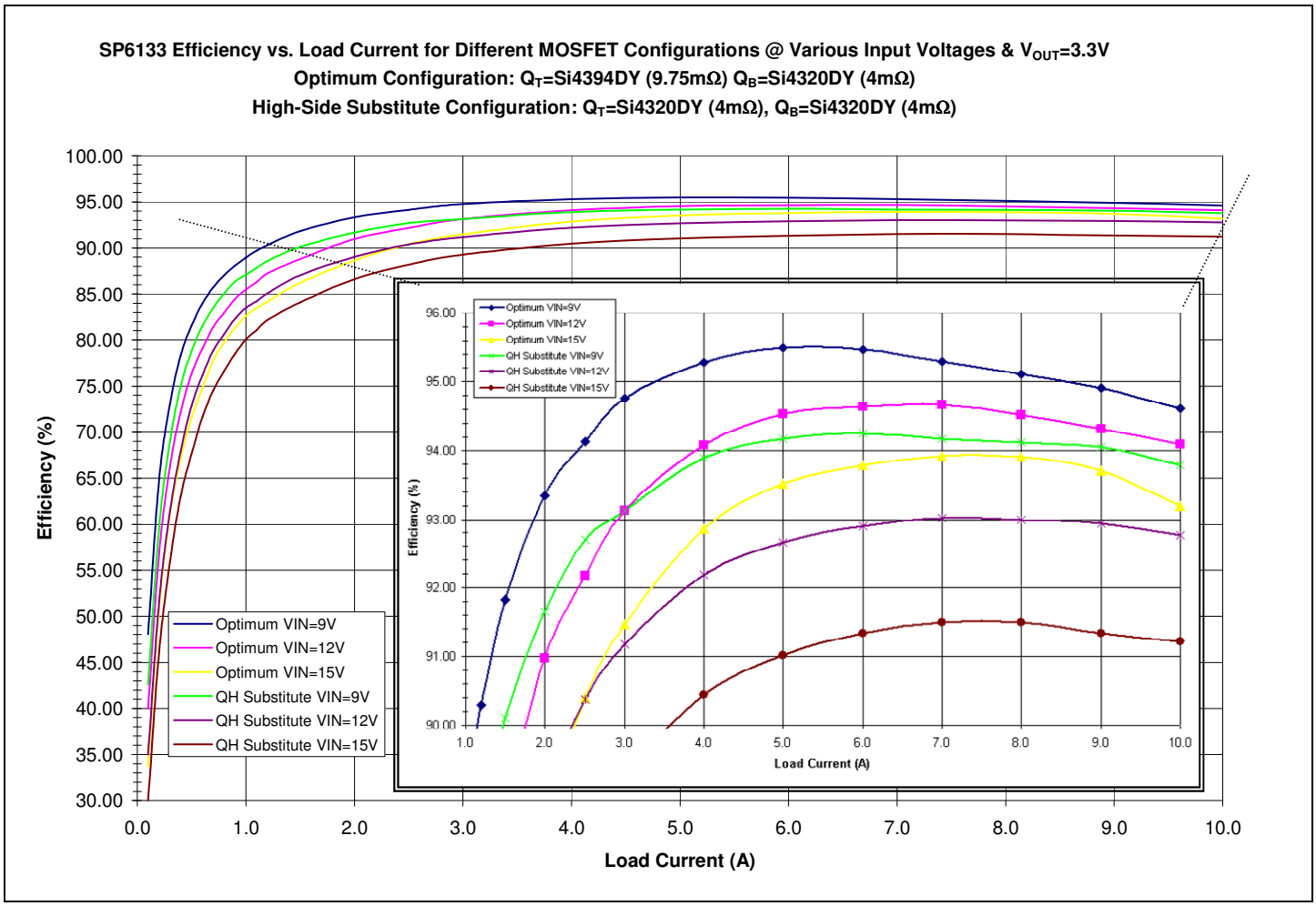
Table 5: MOSFET Configurations Used to Collect Efficiency vs. Load Current Data.

As can be seen in Plot 1 the efficiency data curves for both the optimum and reverse configurations almost overlay each other at each input voltage setting for load currents less than about 1.5A. For load currents greater than about 2.0A the efficiency data curves begin to diverge for each input voltage setting with the greatest spreads occurring at the higher input voltages of 12V and 15V (higher conversion ratios). This divergence is due to the increased conduction losses associated with the reversed low-side MOSFET.



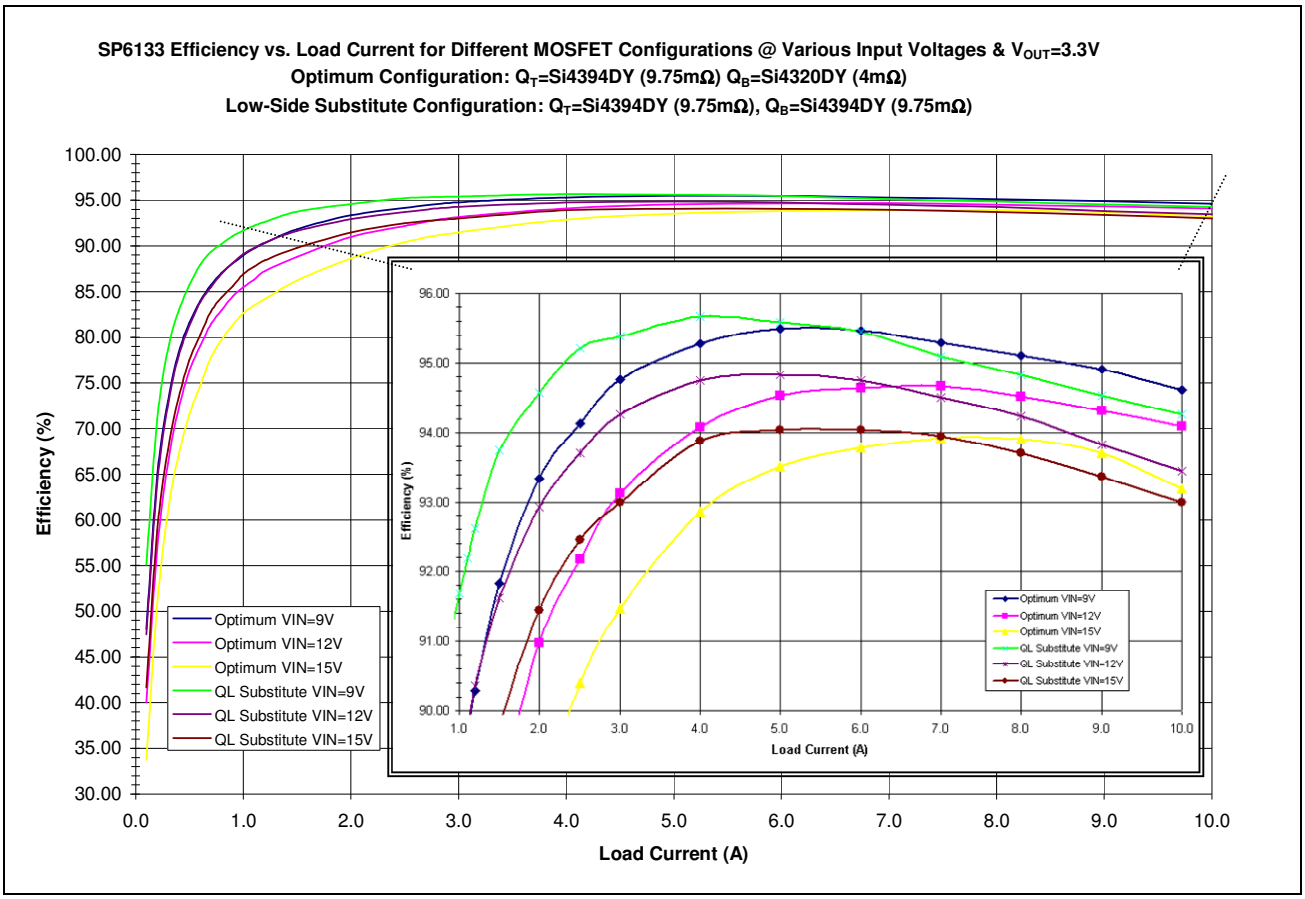
Plot 1: Efficiency vs. Load Current Data for Optimum & Reverse MOSFET Configurations.

Upon study of Plot 2, the greatest spread of efficiencies for the two configurations at each input voltage setting occurs at medium load currents with convergence occurring at the smaller and larger load currents.



Plot 2: Efficiency vs. Load Current Data for Optimum & High-Side Substitute MOSFET Configurations.

Plot 3 shows some interesting results. The efficiencies at medium and light load currents for each input voltage setting for the reverse configuration are significantly greater than they are for the optimum configuration. Only at the larger load currents does a reversal occur and even then, the differences in efficiencies are less than 1%.



Plot 3: Efficiency vs. Load Current Data for Optimum & Low-Side Substitute MOSFET Configurations.

The following Table 6 compares the peak efficiencies in addition to the efficiencies at load currents of 1A and 10A for the various MOSFET configurations at each input voltage setting.

MOSFET Configuration	Peak Efficiency (%)			Efficiency (%) @ 1A			Efficiency (%) @ 10A		
	9V	12V	15V	9V	12V	15V	9V	12V	15V
Optimum	95.5	94.7	93.9	89.0	85.5	82.6	94.6	94.1	93.2
Reverse	94.2	92.8	91.4	89.4	86.1	83.0	92.9	91.7	90.6
High-Side Substitute	94.3	93.0	91.5	87.1	83.5	80.1	93.8	92.8	91.2
Low-Side Substitute	95.7	94.8	94.0	91.7	89.1	86.9	94.3	93.5	93.0

Table 6: Efficiency Comparison for the Various MOSFET Configurations.

As can be seen from this table, the optimum configuration clearly dominates at the highest load current setting of 10A with the most pronounced exceptions occurring at medium and light load currents for the low-side substitute.

CONCLUSIONS

Proper selection of the high and low-side MOSFETs for synchronous buck PWM controllers clearly has an affect on the overall conversion efficiency with the effects becoming more pronounced at higher conversion ratios and load currents. Different high and low-side MOSFETs may sometimes be necessary in order to optimize the overall conversion efficiency; however, the additional cost and hassle associated with having to purchase and stock two separate parts may not justify the sometimes rather small gains in efficiency. This decision will ultimately be driven by cost structures and the overall system requirements.

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Live Technical Chat:	http://www.geolink-group.com/sipex/
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx

Sipex Corporation
Headquarters and
Sales Office
233 South Hillview Drive
Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600