Homework #4

108061127 電機 23 許澤群

Part I - 6-to-64 Decoder

1. Circuit design

Refer to the homework supplement, I design the 6-to-64 decoder by 3-bit pre-decoding. There is the top-level schematic and it consist of two 3-to-8 decoder, which are first stage, and eight NOR2x8, which are second stag e.

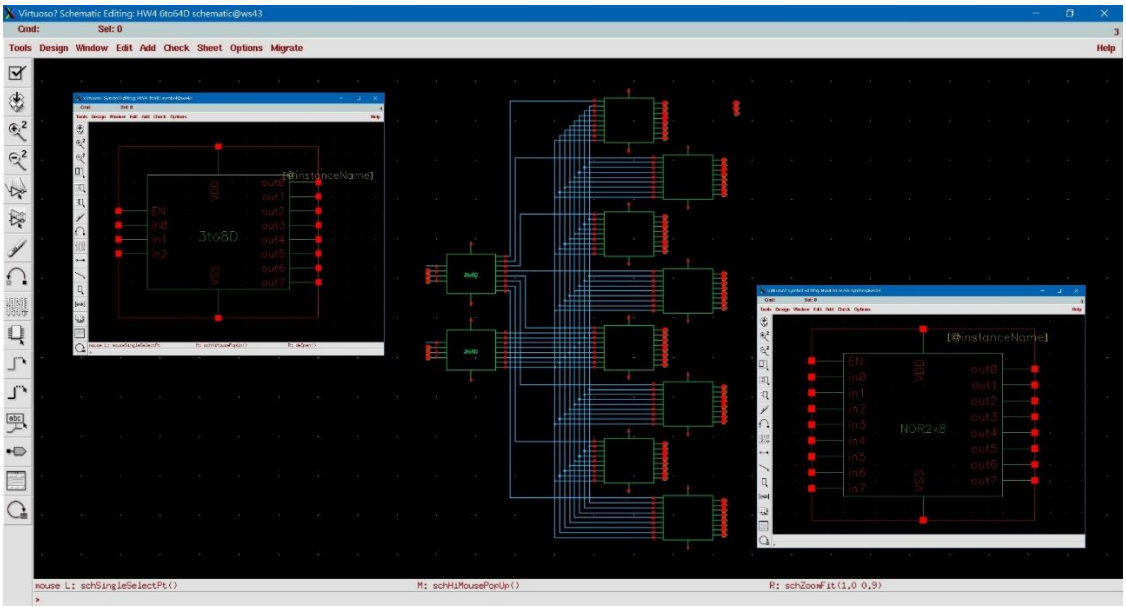


Fig.1 top-level of 6-to-64 decoder schematic

(1) 3-to-8 decoder

The 3-to-8 decoders are designed for pre-decoding. The input signals of 3-to-8 decoders are $in<2:0>$ and $in<5:3>$ respectively. Additionally, there is an enable signal for both decoders. Inside a 3-to-8 decoder, there are three inverters and eight NAND4. Since NAND4s output 0 only when all the input is 1, NAND4s can use for generating one-hot signal.

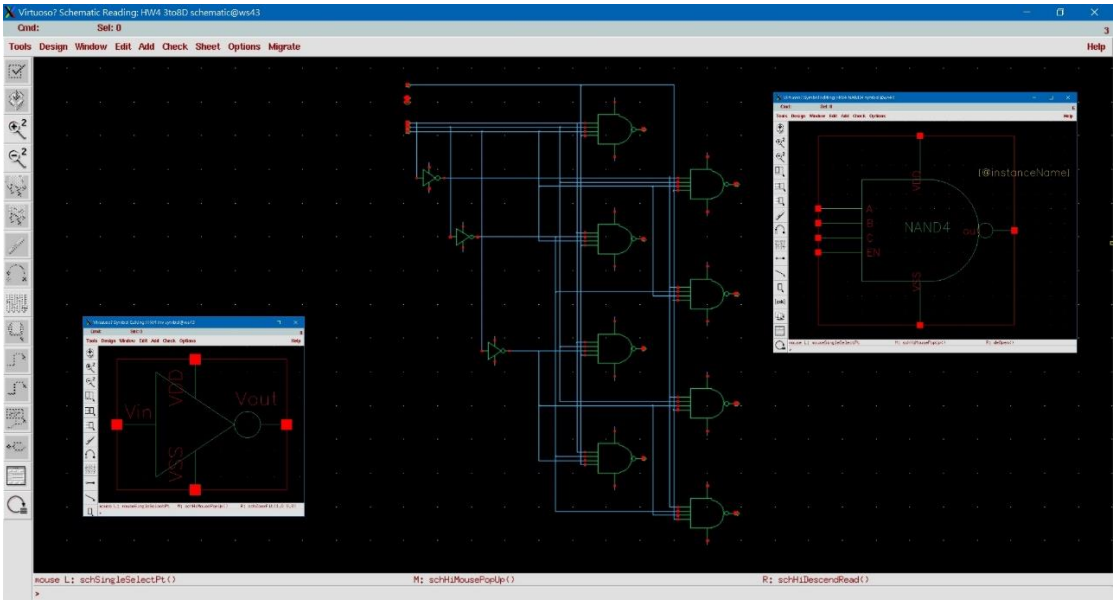


Fig.2 3-to-8 decoder schematic

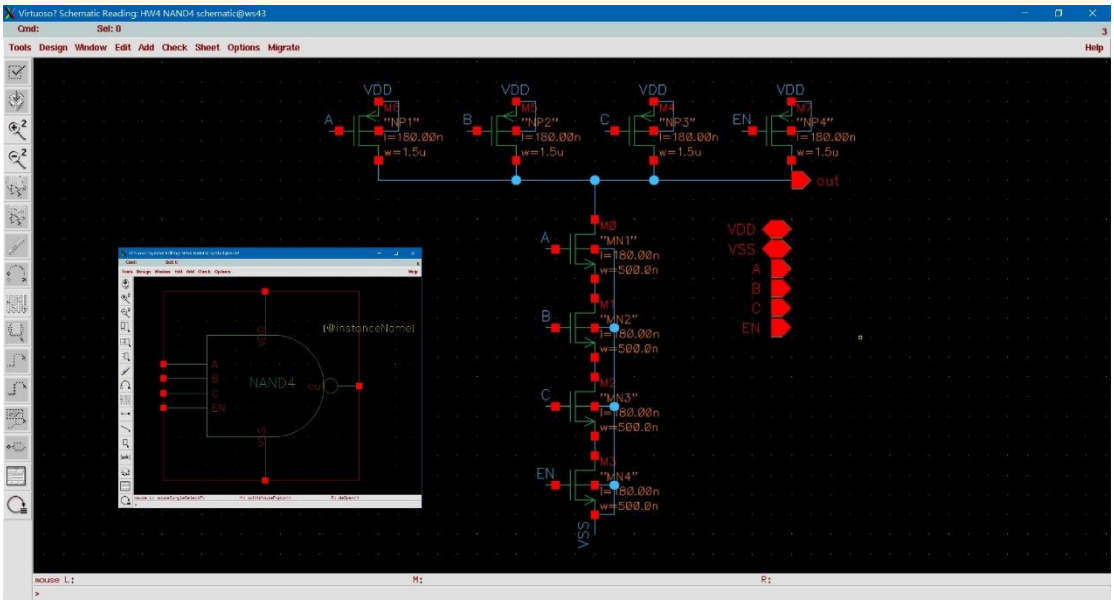


Fig.3 NAND4 schematic

(2) NOR2x8

The NOR2x8s are design for comparing and decoding any two signals form 3-to-8 decoders. Since there are eight output signals for each 3-to-8 decoder, there are totally sixty-four NOR2. To simplify the schematic, I packet every eight NOR2s as a module NOR2x8. Thus, each NOR2x8 contains eight NORs.

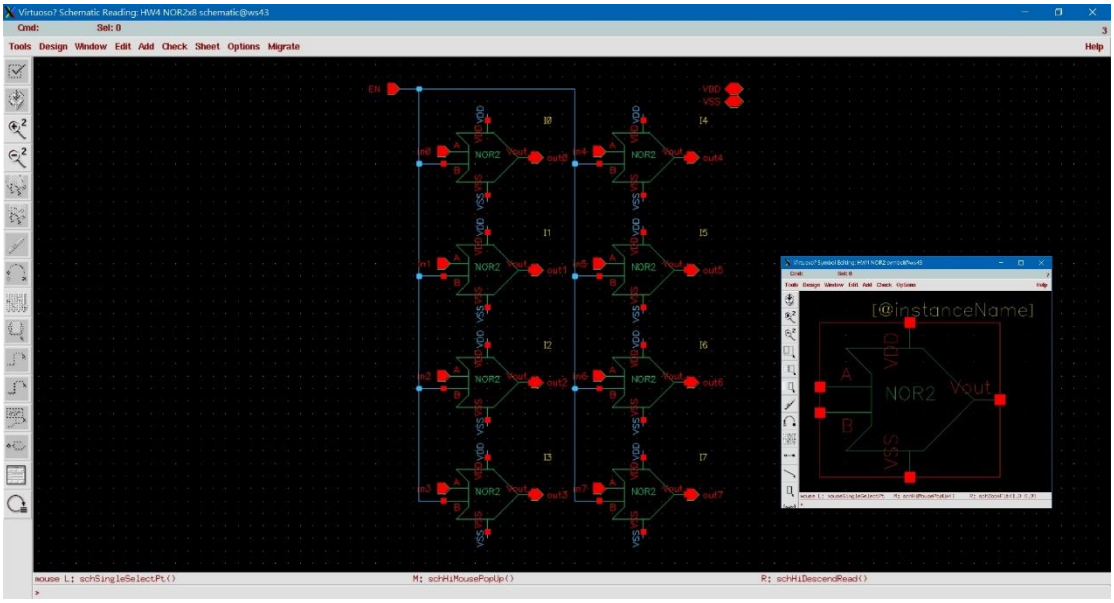


Fig.4 NOR2x8 schematic

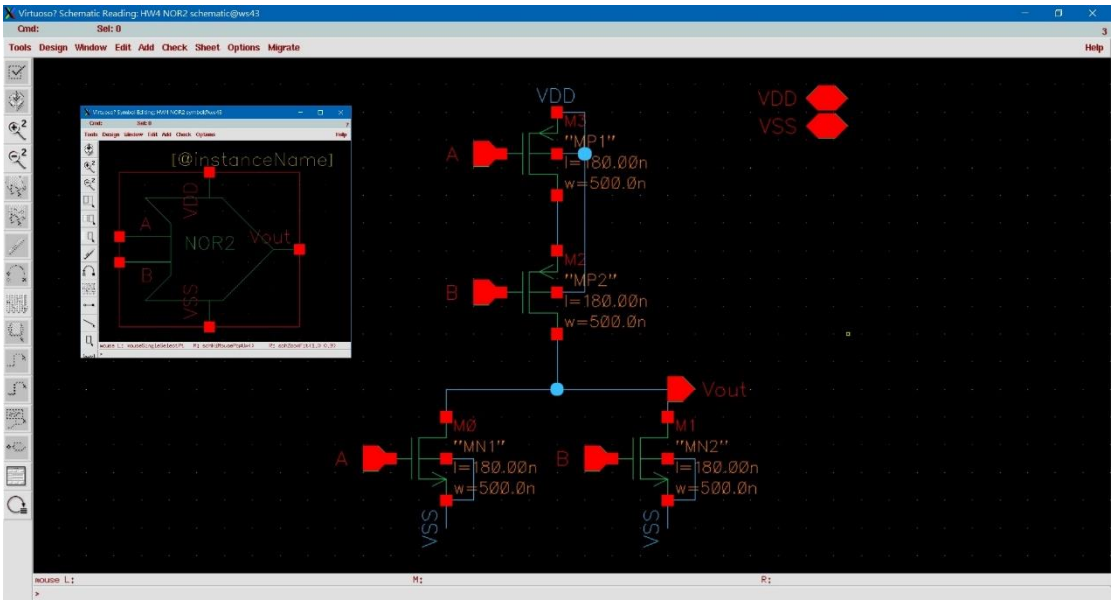


Fig.5 NOR2 schematic

2. Simulation waveforms

(1) delay

```
*hw4_6_t0_64_decoder_pre_sim

****** transient analysis tnom=  25.000 temp=  25.000 ******
tpr= 229.1441p  targ=  30.2791n   trig=  30.0500n
tpf=  63.9720p  targ=  35.2140n   trig=  35.1500n
tp= 146.5581p
```

Fig6. The delay of out< 5 >

(2) waveforms

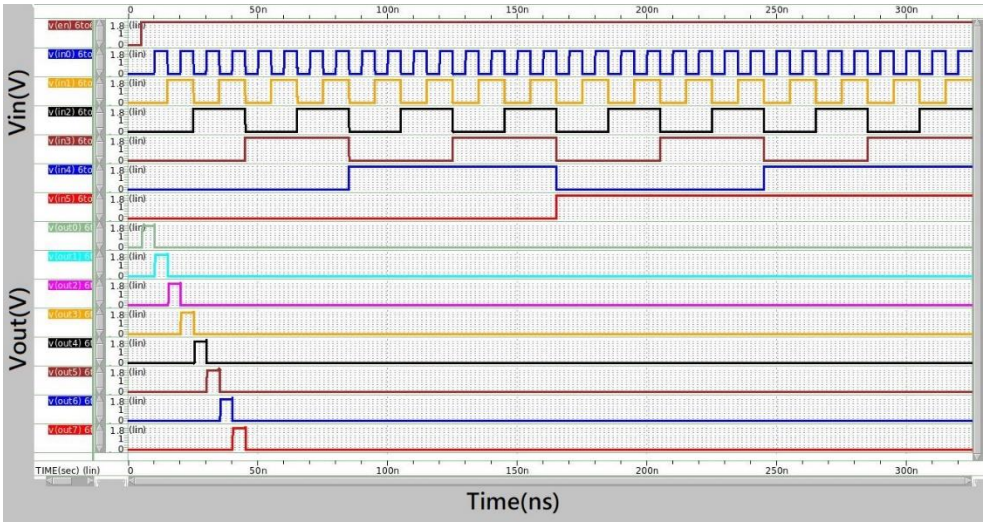


Fig.7 out< 7: 0 > v.s. time

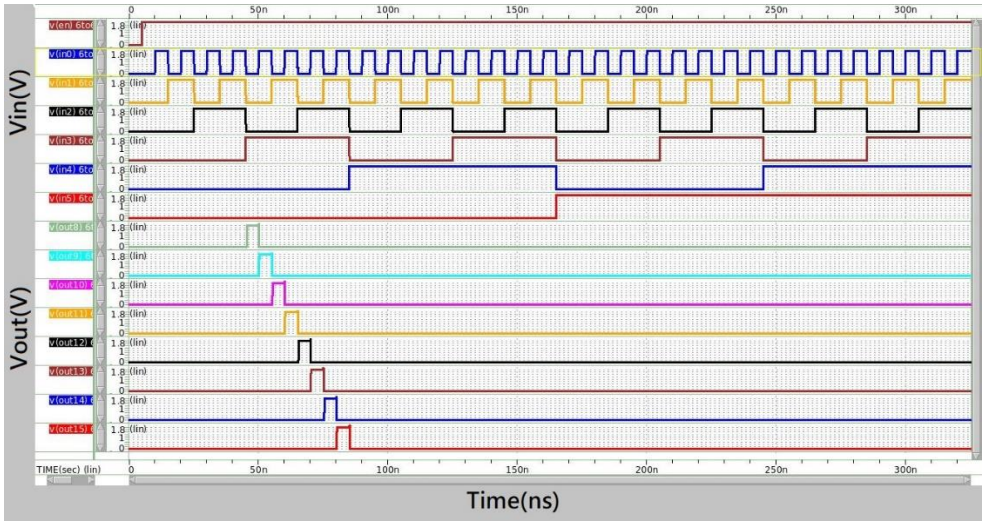


Fig.8 out< 15: 8 > v.s. time

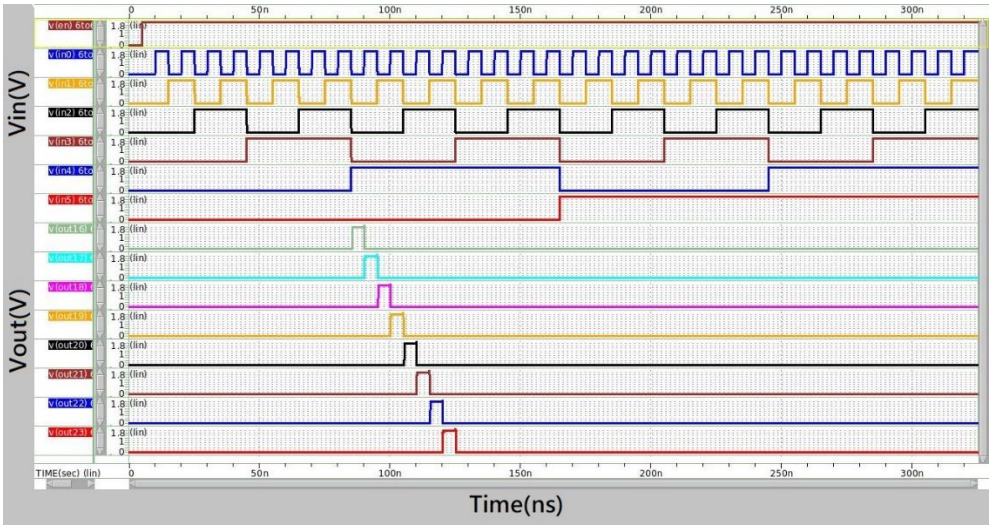


Fig.9 out< 23: 16 > v.s. time

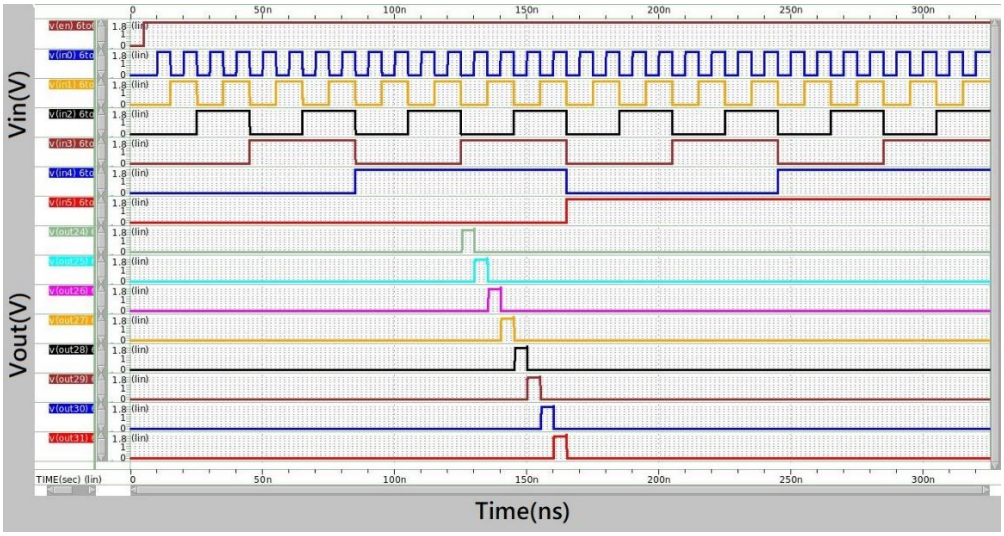


Fig.10 out< 31: 24 > v.s. time

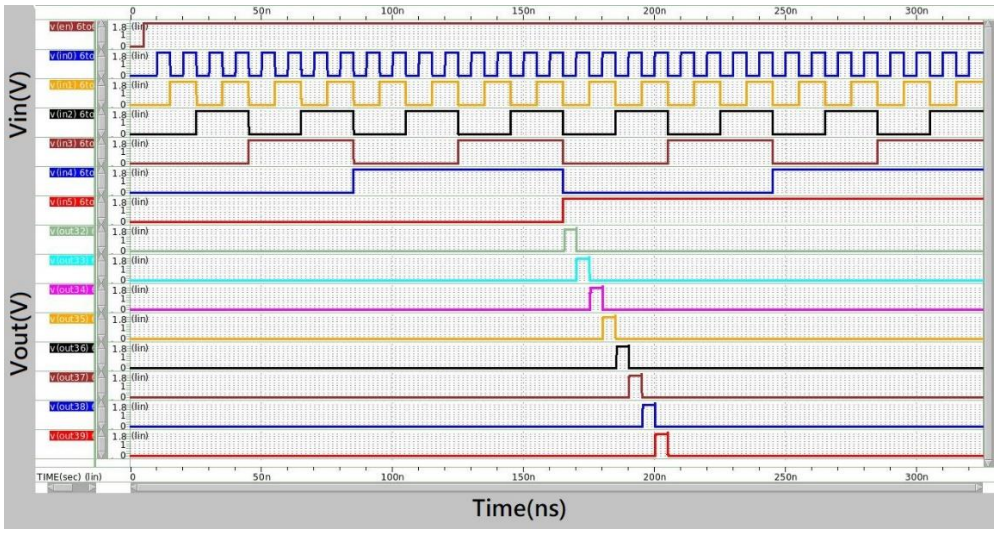


Fig.11 out< 39: 31 > v.s. time

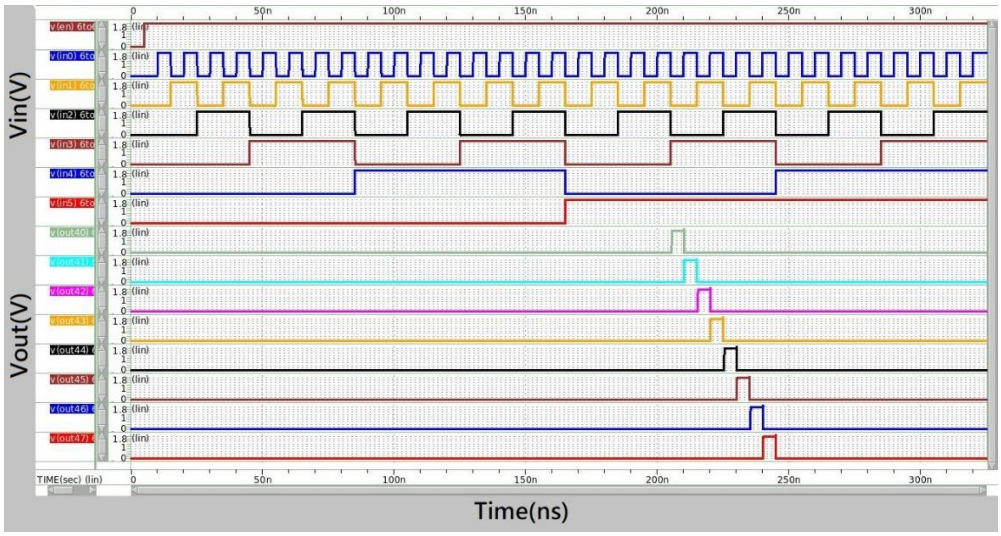


Fig.12 out< 47: 40 > v.s. time

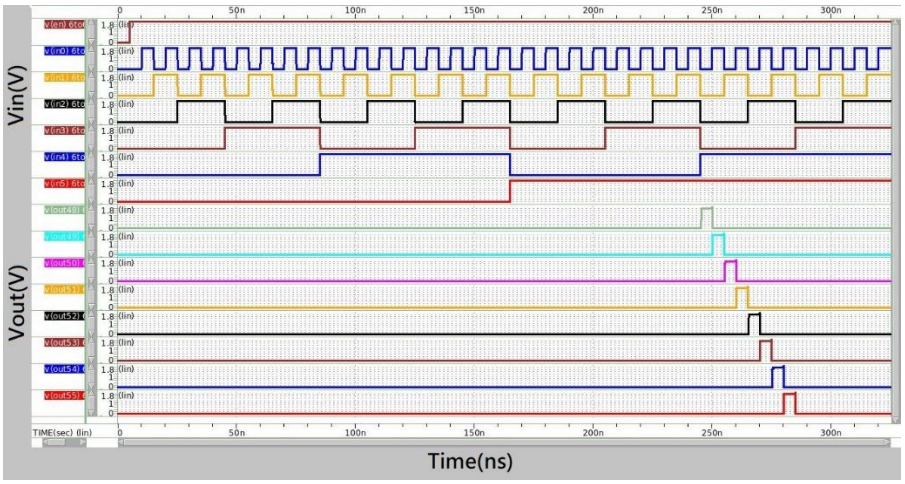


Fig.13 out< 55: 48 > v.s. time

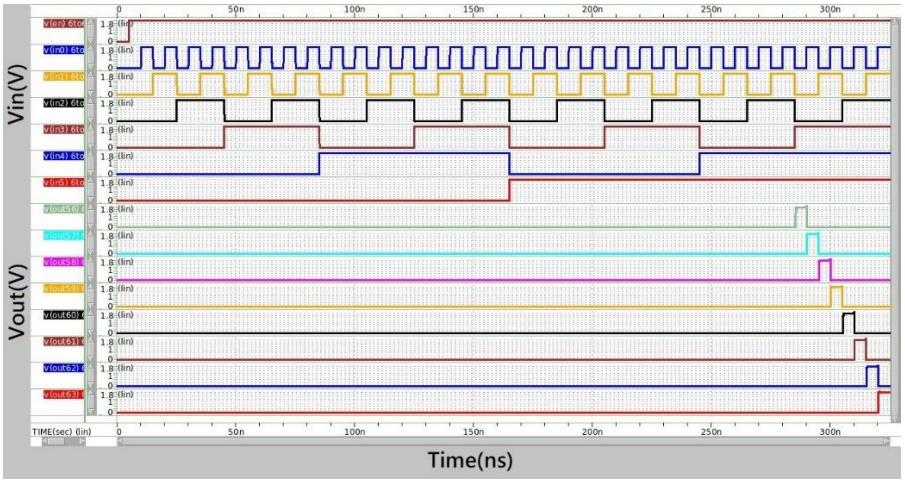


Fig.14 out< 63: 56 > v.s. time

3. Layout and post-sim

(1) Layout

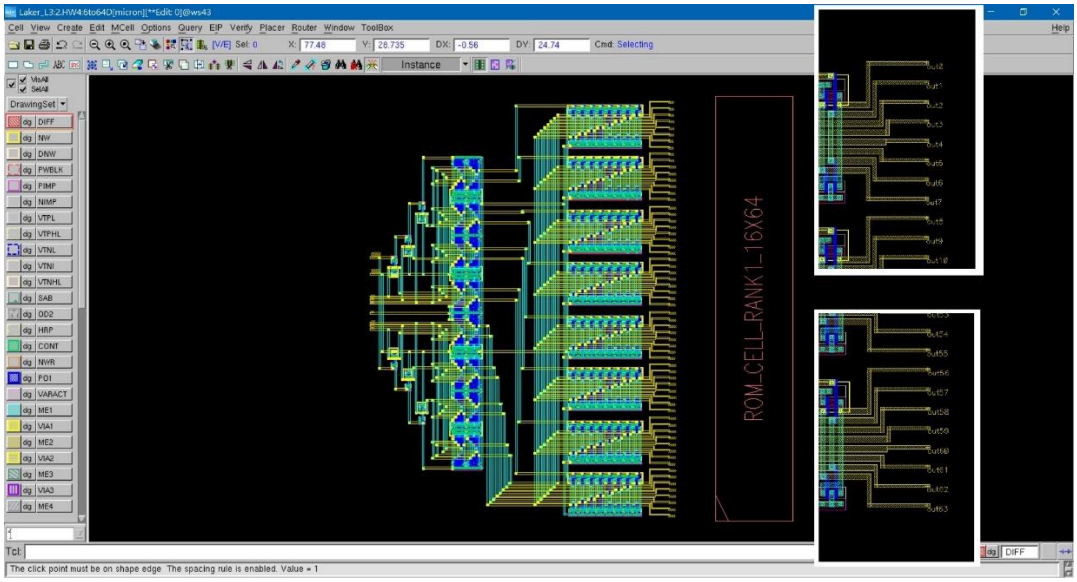


Fig. 6-to-64 decoder with ROM array layout

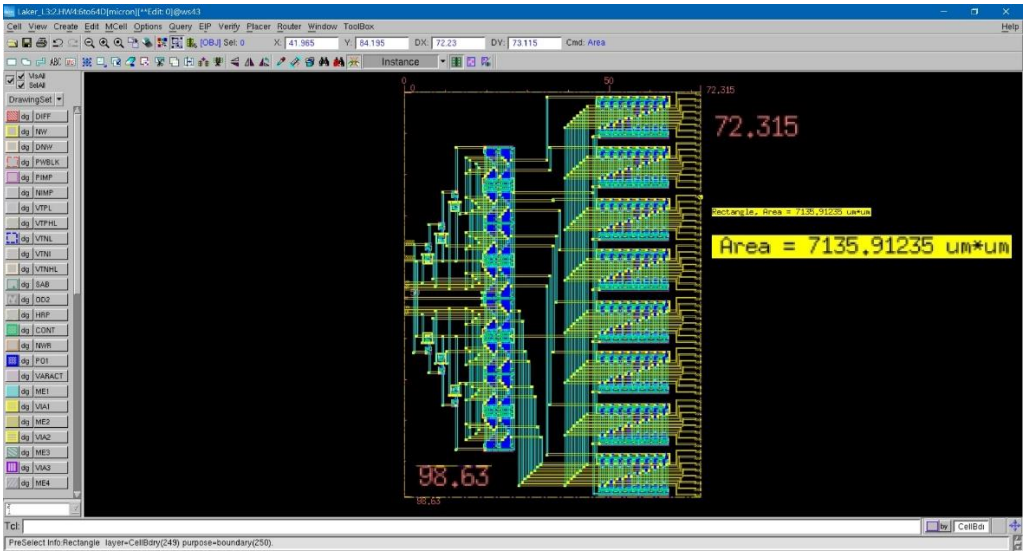


Fig. 6-to-64 decoder with marker array layout

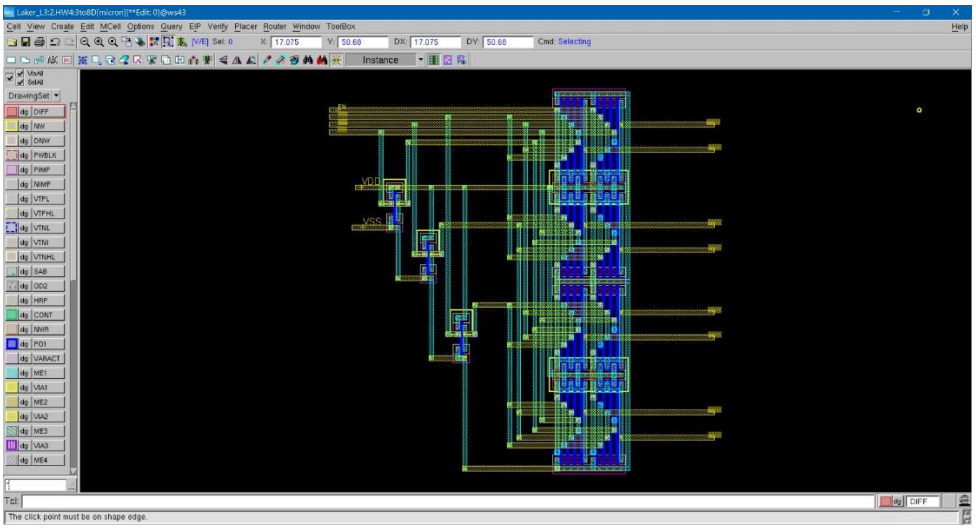


Fig. 3-to-8 decoder array layout

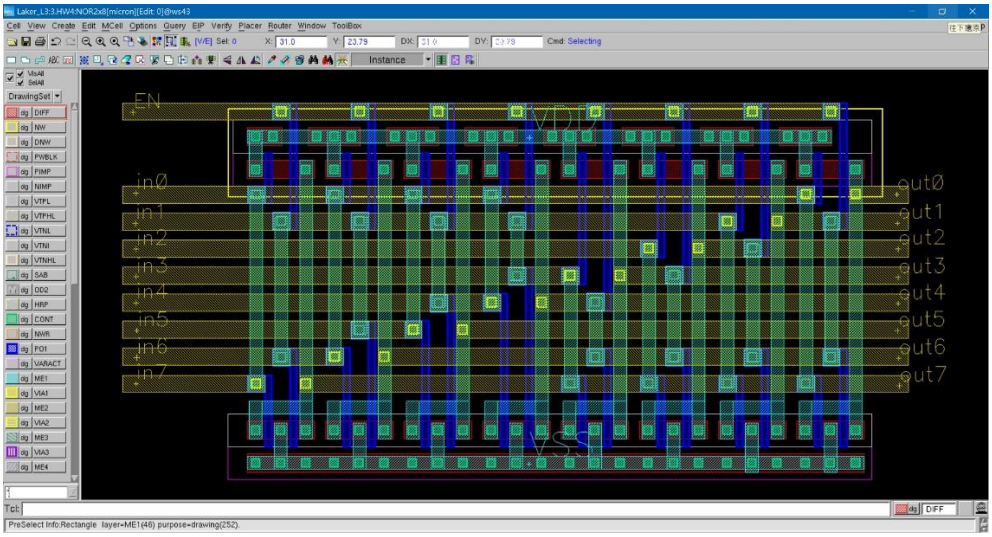
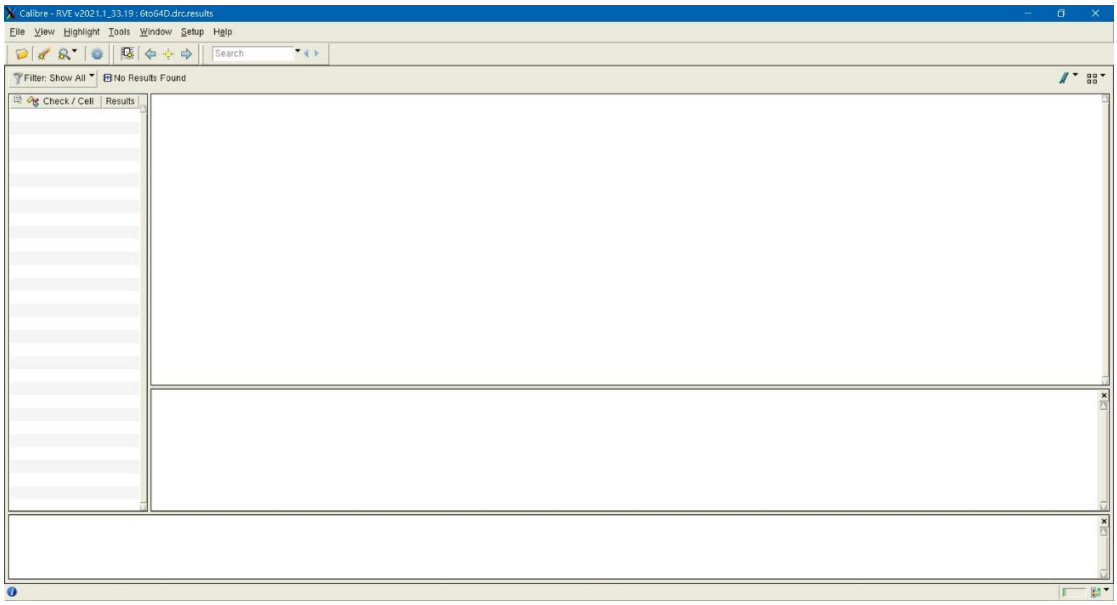
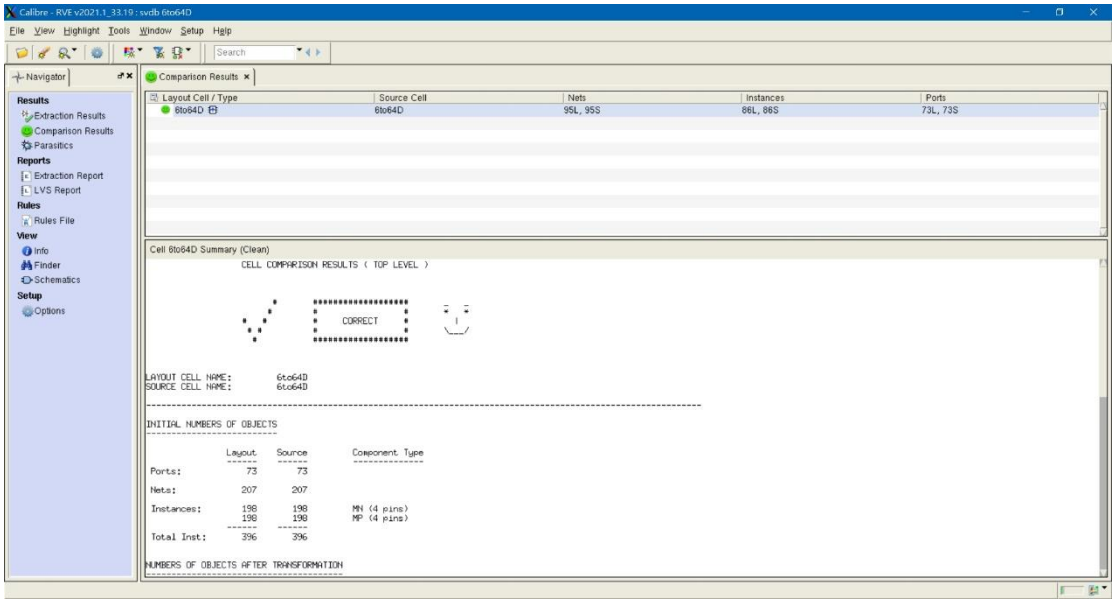


Fig. NOR2x8 decoder array layout

(2) DRC check



(3) LVS check



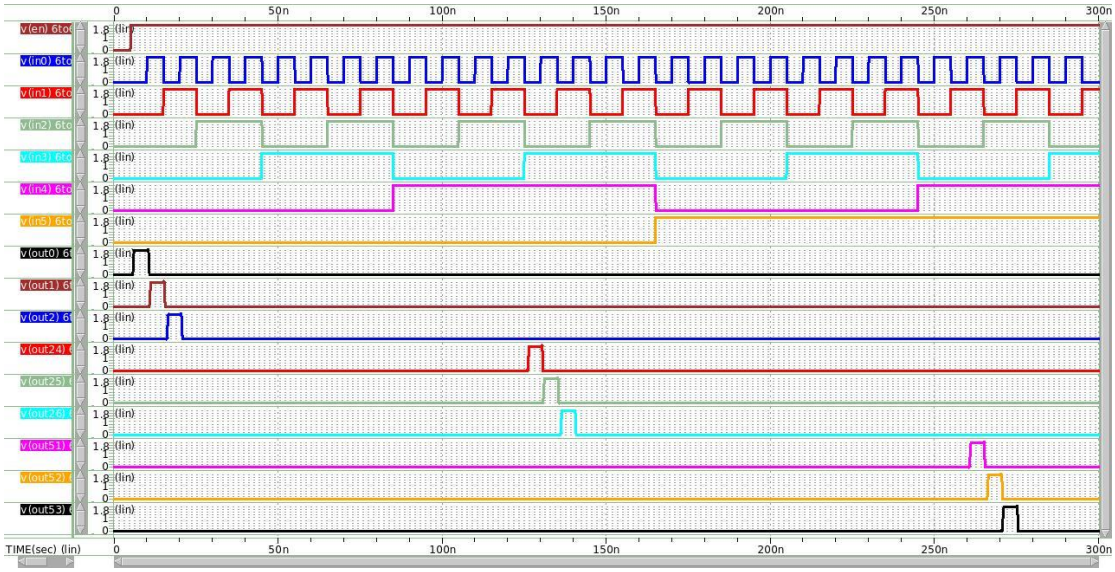
(4) Post_sim

```
*hw4_6_t0_64_decoder_post_sim

****** transient analysis tnom=  25.000 temp=  25.000 ******
tpr= 896.9697p  targ=  30.9470n   trig=  30.0500n
tpf= 356.9046p  targ=  35.5069n   trig=  35.1500n
tp= 626.9372p
```

The delay of post_sim difference= $\left|\frac{626.9372-146.5581}{146.5581}\right| = 327.77\%$, exceed three times larger than pre_sim. Since the amount of metals and MOSs used in this homework is large, leads to significant resistance and capacitance. Also, the large latency may result from the weak devices in first stage, since the width and length of

MOSs in both 3-to-8 decoder and NOR2x6 are deigned the same. Then, if the first stage cannot supply strong current, the MOS in second stage may be operated in linear region or even be cut off.



The post_sim waveforms are similarly to pre_sim. However, if took a close look to the output signal, it’s obviously that the voltage rising and falling slowly than pre_sim.