EE3230 VLSI Design, Fall 2021
Homework #2
Due Date : 2021/11/09

Note

1. Do the simulation and analysis with cic018.l.
2. Power supply (VDD) = 1.8V.
3. Use .tran 1p XXns for delay time. (XX is up to you)

Part I (Combinational Circuit) (50%)

1. Please design a NAND3 shown in Fig. 1 with minimum length (0.18μm) of NMOS and PMOS. Under the condition TT25℃, the logic circuit has the same output rise delay (t_{pLH}) and fall delay (t_{pHL}) as the inverter in HW1 Part-I with the following two input patterns. **(4%)**

   Note：Output loading C_{load} = 0.1pF (the same as HW1 Part I)

   Use pattern (A,B,C)=(1,1,1)→(0,1,1) to find the rise delay (t_{pLH}).
   Use pattern (A,B,C)=(0,1,1)→(1,1,1) to find the fall delay (t_{pHL}).

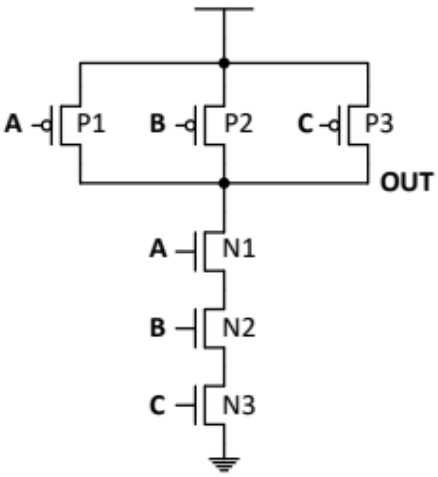

Fig. 1

2. Use the NAND3 designed above. Now, change one input from 0V to VDD at once and fix other inputs (see Table 1). Run simulation in different conditions and find output rise delay (t_{pLH}) and fall delay (t_{pHL}). Fill your results in Table 1. (**0.5%** for each gird, **6%** in total)

3. Comment what you have observed from Table 1 and give some discussion. **(5%) (As long as your discussions are reasonable, you can get all points)**

Table 1

	Input A	Input B	Input C	Condition	t_{pLH} (ps)	t_{pHL} (ps)
Case 1	pulse	1	1	SS 125℃		
				SF 25℃		
				TT 25℃		
				FS 25℃		
				FF -40℃		
Case 2	1	pulse	1	SS 125℃		
				SF 25℃		
				TT 25℃		
				FS 25℃		
				FF -40℃		
Case 3	1	1	pulse	SS 125℃		
				SF 25℃		
				TT 25℃		
				FS 25℃		
				FF -40℃		

4. Please design a logic circuit shown in Fig. 2 with minimum length (0.18μm) of NMOS and PMOS. Under the condition TT25℃, the logic circuit has the same output rise delay (t_{pLH}) and fall delay (t_{pHL}) as the inverter in HW1 Part-I with the following two input patterns. **(4%)**

   Note：Output loading C_{load} = 0.1pF (the same as HW1 Part I)

   Use pattern (A, B, C) = (1, 1, 0) → (0, 1, 0) to find the rise delay (t_{pLH}).
   Use pattern (A, B, C) = (0, 1, 0) → (1, 1, 0) to find the fall delay (t_{pHL}).

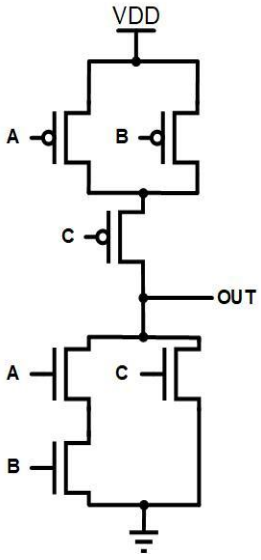

Fig. 2

5. Given the logic circuit in Fig. 2, please change one input from 0V to VDD at once and fix other inputs (see Table 2). Run simulation in different conditions and fined output rise delay (t_{pLH}) and fall delay (t_{pHL}). Please fill the simulation results in Table 2. (**0.5%** for each gird, **6%** in total)

6. Comment what you have observed from Table 2 and give some discussions. **(5%) (As long as your discussions are reasonable, you can get all points)**

Table 2

	Input A	Input B	Input C	Condition	t_{pLH} (ps)	t_{pHL} (ps)
Case 1	pulse	1	0	SS 125℃		
				SF 25℃		
				TT 25℃		
				FS 25℃		
				FF -40℃		
Case 2	1	pulse	0	SS 125℃		
				SF 25℃		
				TT 25℃		
				FS 25℃		
				FF -40℃		
Case 3	0	1	pulse	SS 125℃		
				SF 25℃		
				TT 25℃		
				FS 25℃		
				FF -40℃		

7. Complete the layout of Fig. 2. Show the figure of your layout and DRC/LVS report. **(10%)** and measure the area. **(5%)**
   Note: Area of the layout is the area of minimum single rectangle that can cover all circuits

8. Run post-sim (with R-C-CC extraction), compare the result and waveform with pre-sim. **(5%)**

Part II (Inverter chain) (50%)

1. Complete the layout of your inverter chain from HW1 Part II. Show the figure of your layout and DRC/LVS report. **(15%)** and measure the area. **(2.5%)** **(Output loading C_{load} = 10pF)**
   Bonus: FoM = delay * area (delay will get from post-sim)

2. Run post-sim (with R-C-CC extraction), compare the result and waveform with pre-sim from HW1 Part II. **(5%)**

3. Use different stage as branch to measure the propagation delay. The first half is your inverter chain in HW1 Part II and the last half is three kinds of inverter chain with different stage. **(5%) (Output loading C_{load} = 10pF)**
   Note : The size of first inverter in last half (where the red arrow points) of long inverter chain is fixed : $(W/L)_n$ = (0.5um/0.18um), $(W/L)_p$ = (1.85um/0.18um).

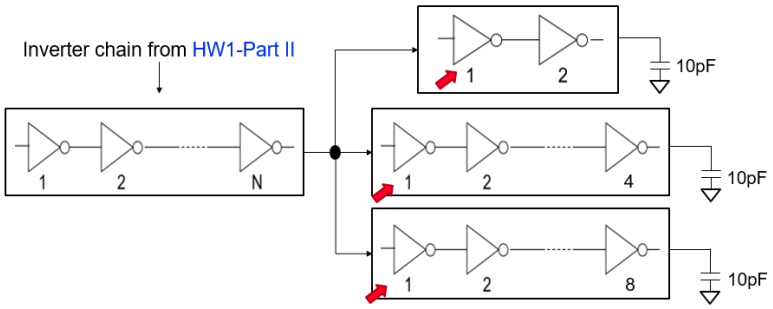

Fig. 3

4. Complete the layout of Fig. 3. Show the figure of your layout and DRC/LVS report. **(15%)** and measure the area. **(2.5%)**

5. Run post-sim (with R-C-CC extraction), compare the delay of three delay chain. **(5%)**

Bonus (FoM = delay * area)

1st		(10%)
2nd	~ 10th	(8%)
11th	~ 20th	(5%)
21th	~ 40th	(3%)

Note: The less, the better.

Submission

1. Report (HW2_StudentID_NAME.pdf)
   a. Picture of schematic
   b. Picture of waveform with cursor values
   c. Picture of area of the layout with markers
   d. Table 1,2 & Your comment
   e. Write down what you have learned in this HW (Not necessary)
2. Hspice code file (.sp)
3. Netlist files (.spi)
4. Gds files (.gds)