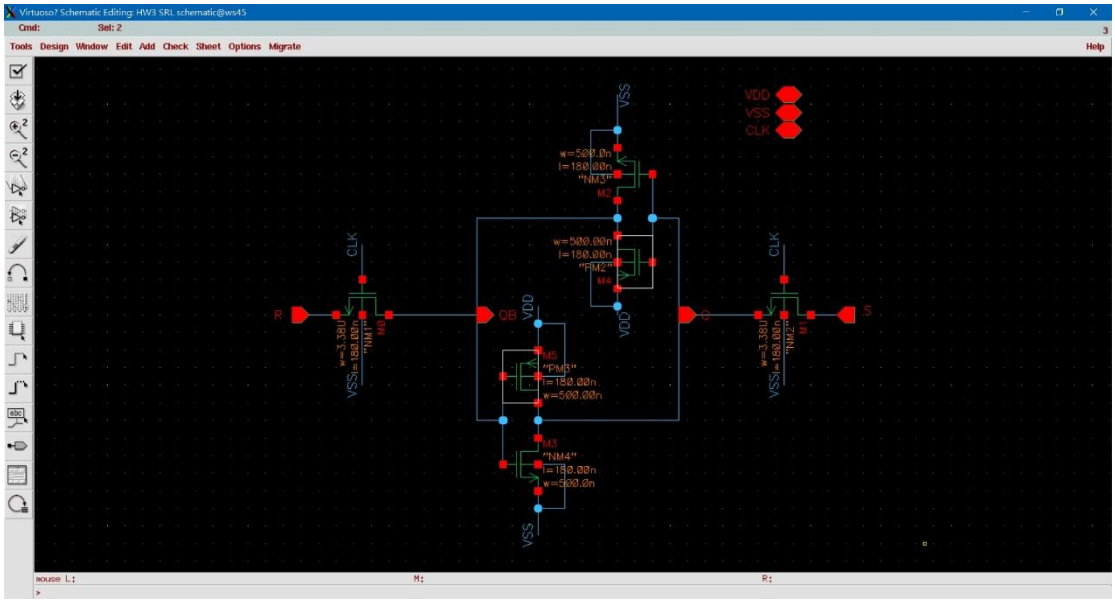
Homework #3

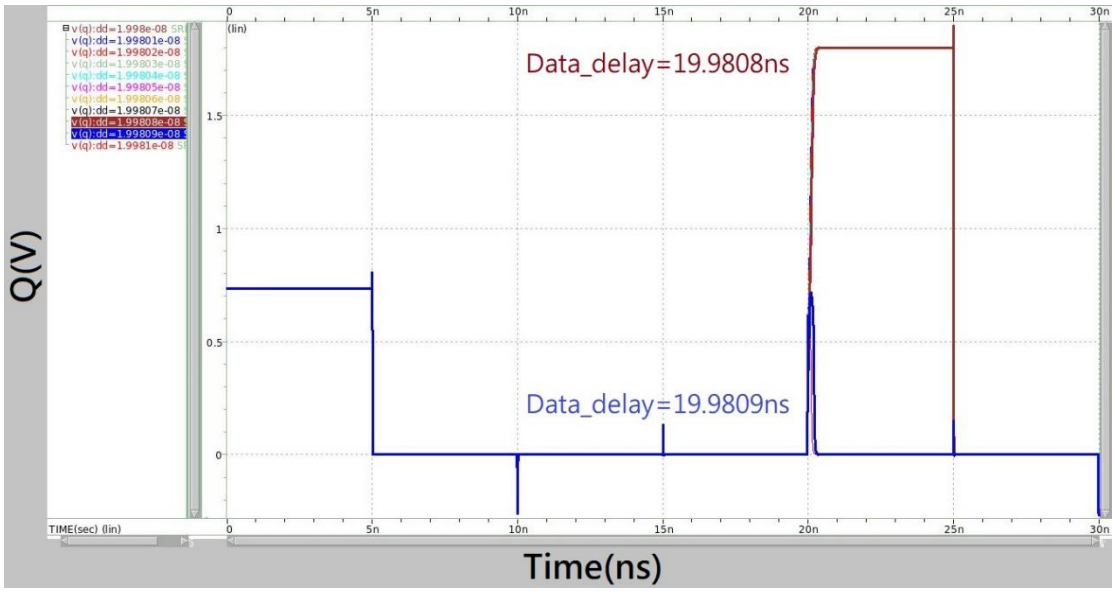
108061127 電機 23 許澤群

Part I-SR Latch

(1) Design

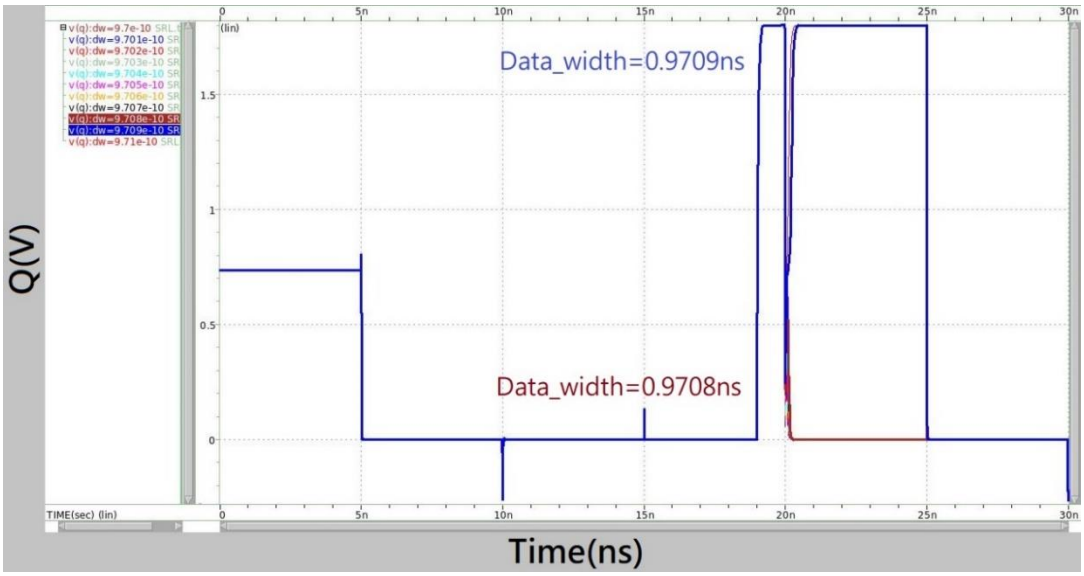


(2) Setup time



Setup time $= 20 - 19.9808 = 0.0192(ns)$

(3) Hold time



Hold time $= 0.9708 - 1 = -0.0292(ns)$

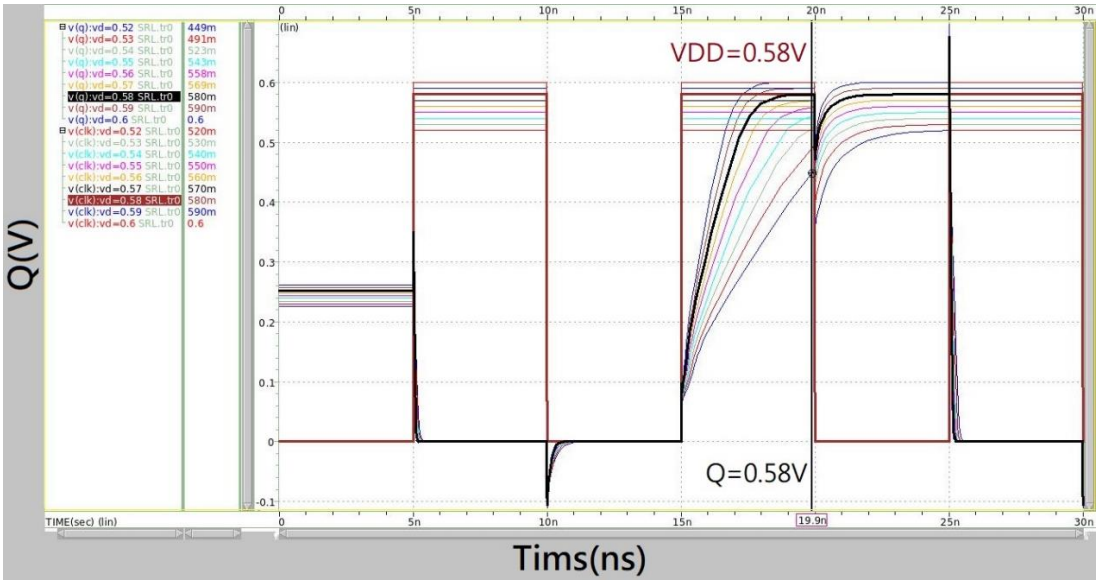
(4) S to Q delay

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tpr_sq=  11.5312p  targ=  16.0165n   trig=  16.0050n
tpr_rqb=  11.5187p  targ=  19.0265n   trig=  19.0150n
tpf_sq=   5.5215p  targ=  19.0205n   trig=  19.0150n
tpf_rqb=   5.5243p  targ=  16.0105n   trig=  16.0050n
tp_sq=   8.5264p
tp_rqb=   8.5215p
```

$t_{psq} = 8.5264(ps)$

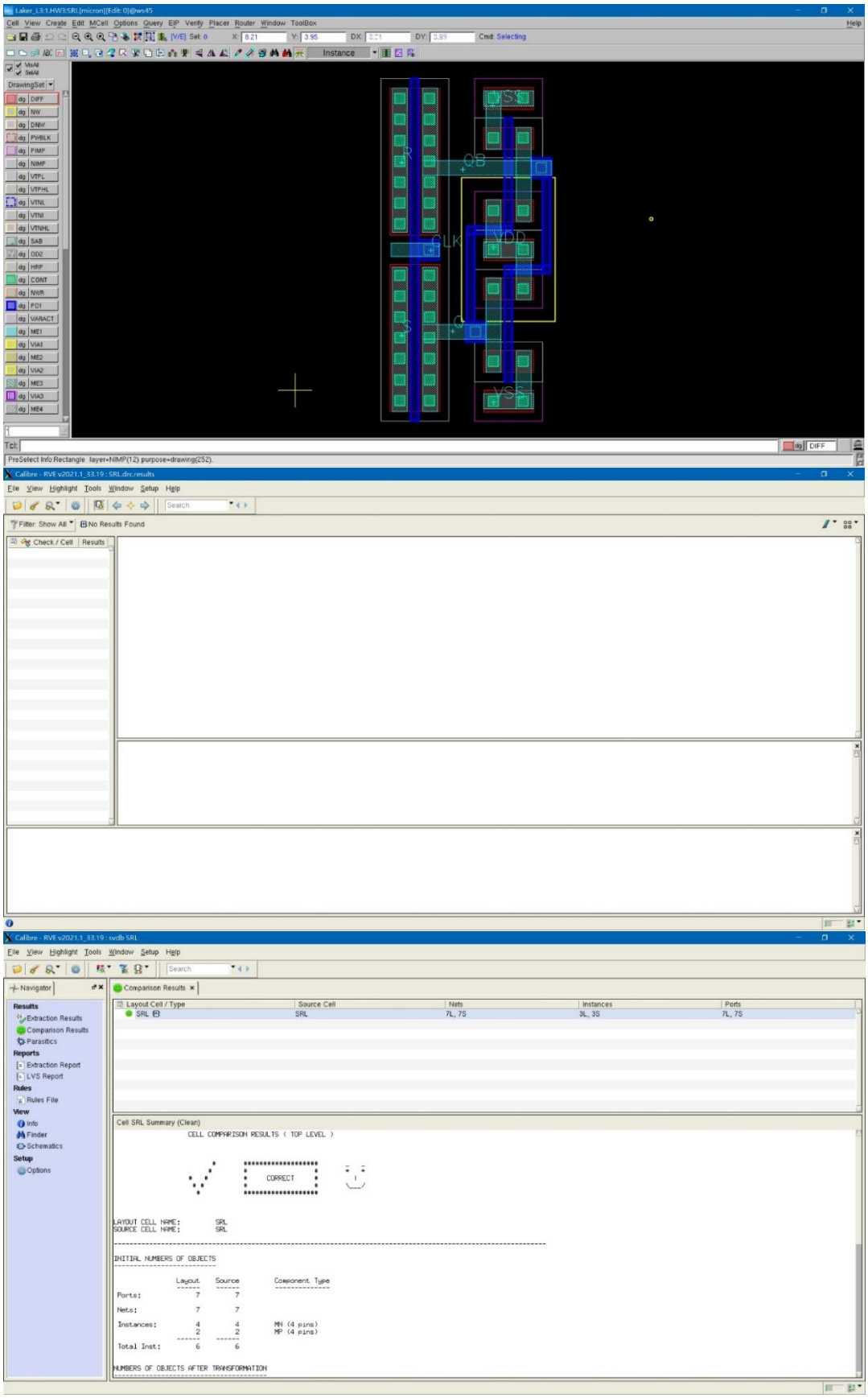
$t_{prqb} = 8.5215(ps)$

(5) Operation voltage



Operation voltage$= 0.58(V)$

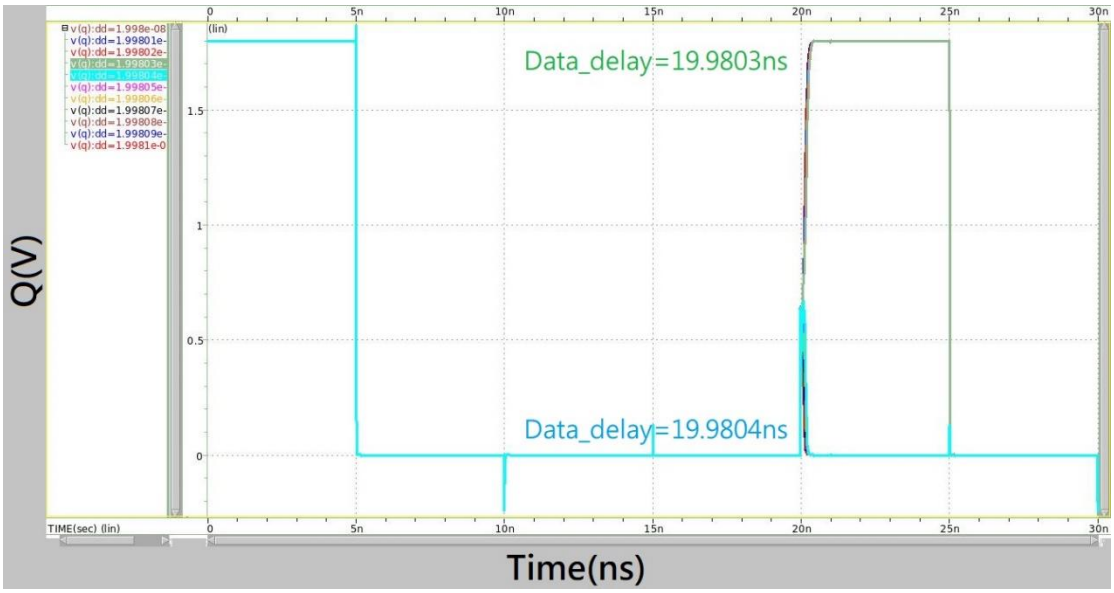
(6) Layout



$$\text{area} = 4.02 \times 7.88 = 31.6776(\mu m^2)$$

(7) Post-sim

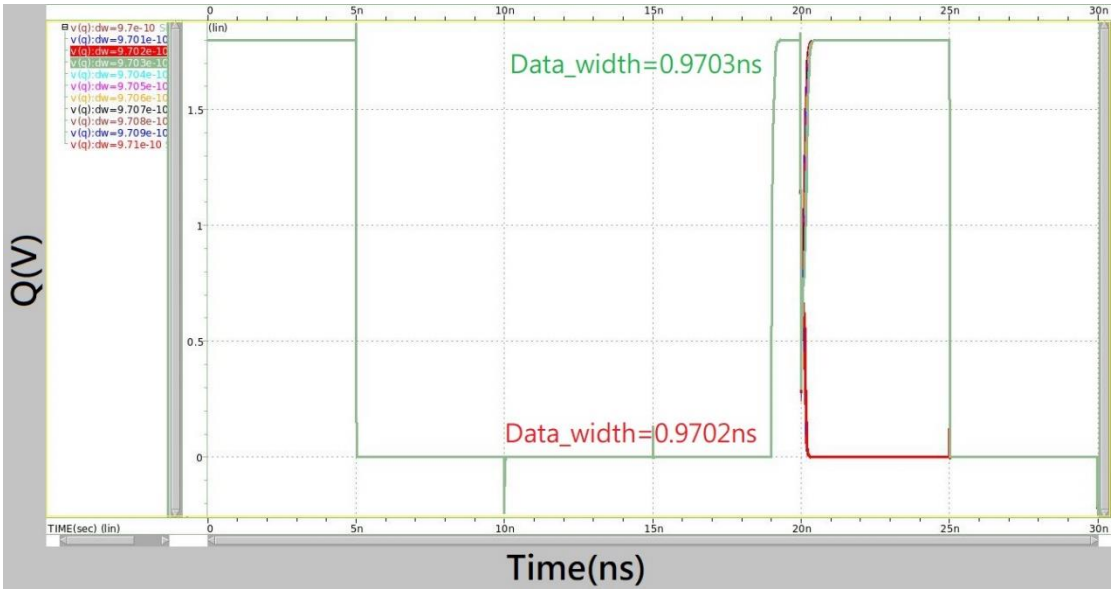
1.setup time



Setup time $= 20 - 19.9803 = 0.0197(ns)$

Difference $= 2.6041\%$

2.hold time



Hold time $= 0.9702 - 1 = -0.0298(ns)$

Difference $= 2.0547\%$

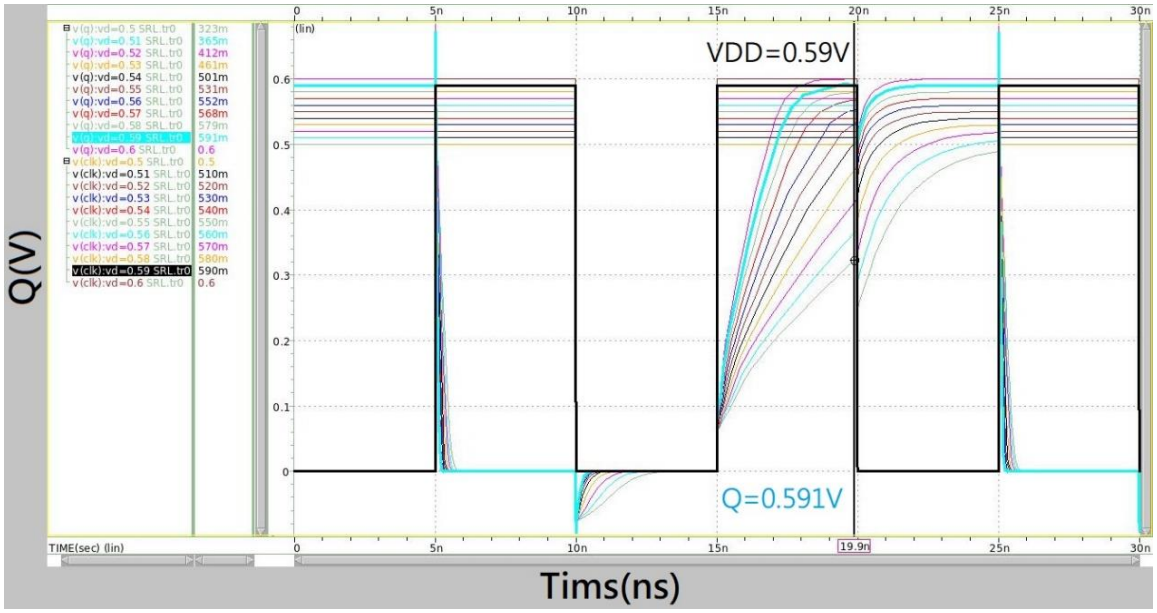
3.S to Q delay

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tpr_sq=  12.9081p  targ=  16.0179n   trig=  16.0050n
tpr_rqb=  12.9718p  targ=  19.0280n   trig=  19.0150n
tpf_sq=   6.4862p  targ=  19.0215n   trig=  19.0150n
tpf_rqb=   6.5709p  targ=  16.0116n   trig=  16.0050n
tp_sq=   9.6971p
tp_rqb=   9.7714p
```

$t_{psq} = 9.6971(ps)$, Difference $= 13.7302\%$

$t_{prqb} = 9.7714(ps)$, Difference $= 14.6676\%$

4.operation voltage



Operation voltage$= 0.59(V)$

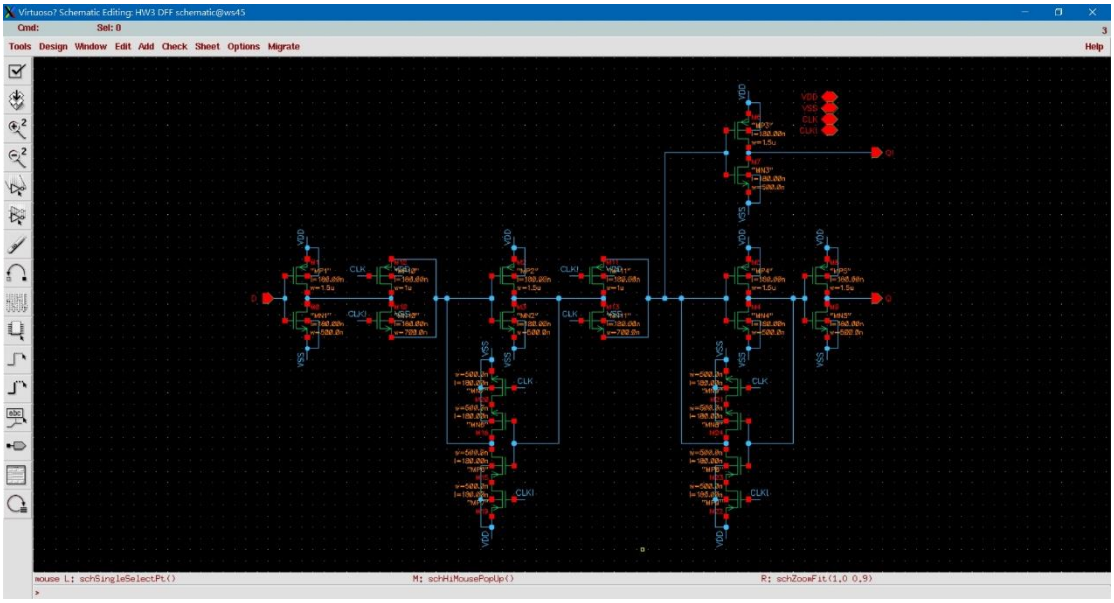
Difference $= 1.7241\%$

I defined operation voltage as the voltage of power supply that output voltage cannot reach steady state before clock falling edge. Since it cannot pass enough strong signal for next stage in single cycle and cause some problem when being operated in a sequential circuit.

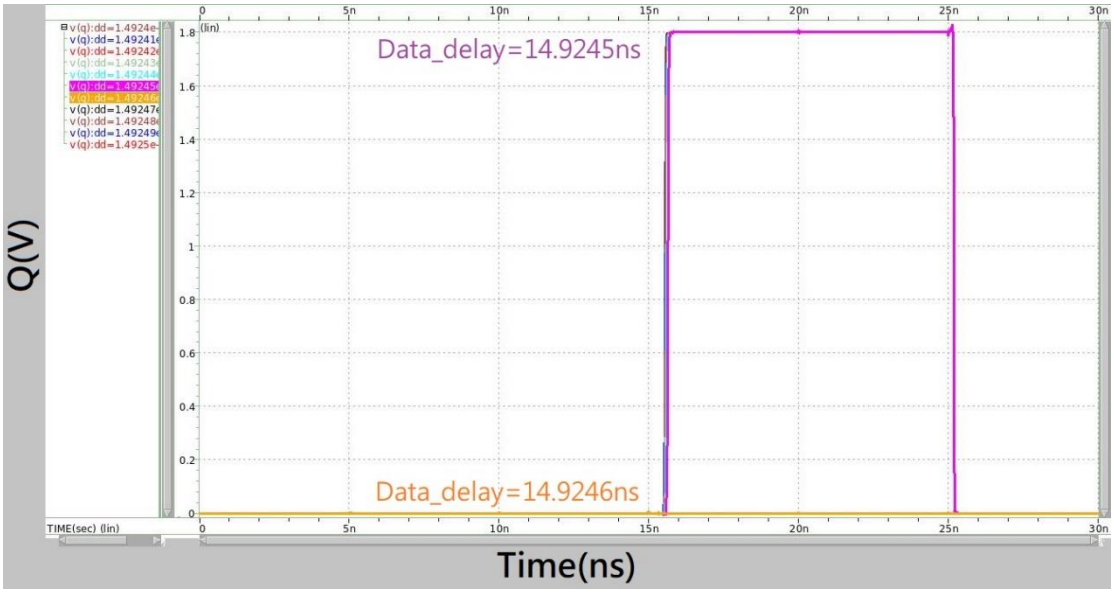
Then discuss the effect of different power supply voltage. Since MOSFET as transmission gate be turned on only when gate-source voltage is greater than threshold voltage, transmission never be turned on if the voltage of power supply smaller than threshold voltage. Also, since MOSFET as transmission gate be operated in saturation region when drain-source voltage is greater than overdrive voltage, transmission gate will be operated in triode region if the voltage of power supply is not large enough. Then, it took some delay to reach steady state.

Part II-D Flip Flop

(1) Design

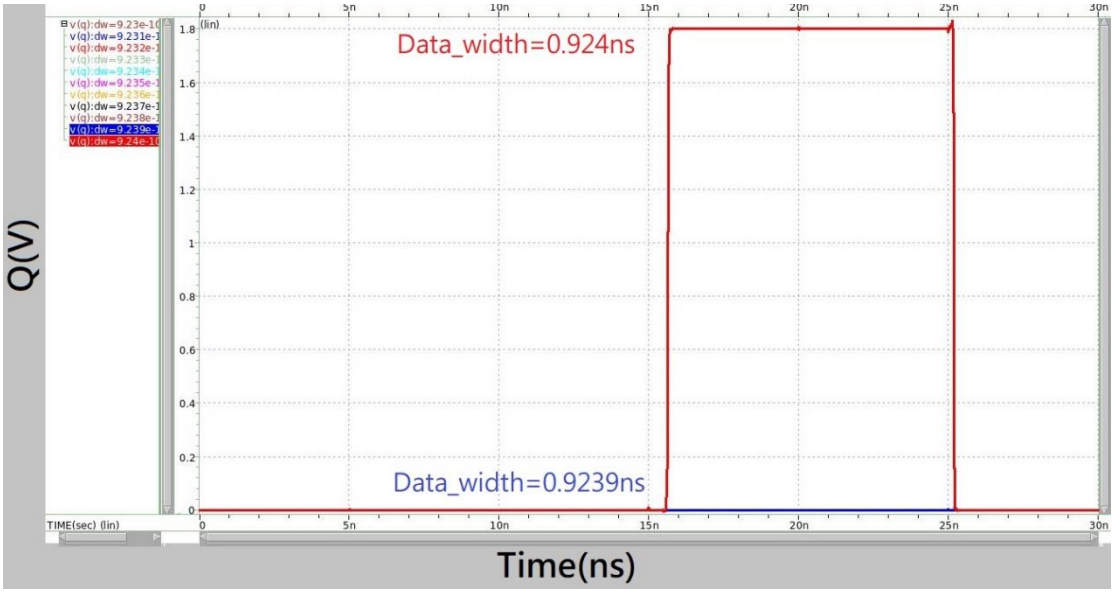


(2) Setup time



Setup time $= 15 - 14.9245 = 0.0755(ns)$

(3) Hold time



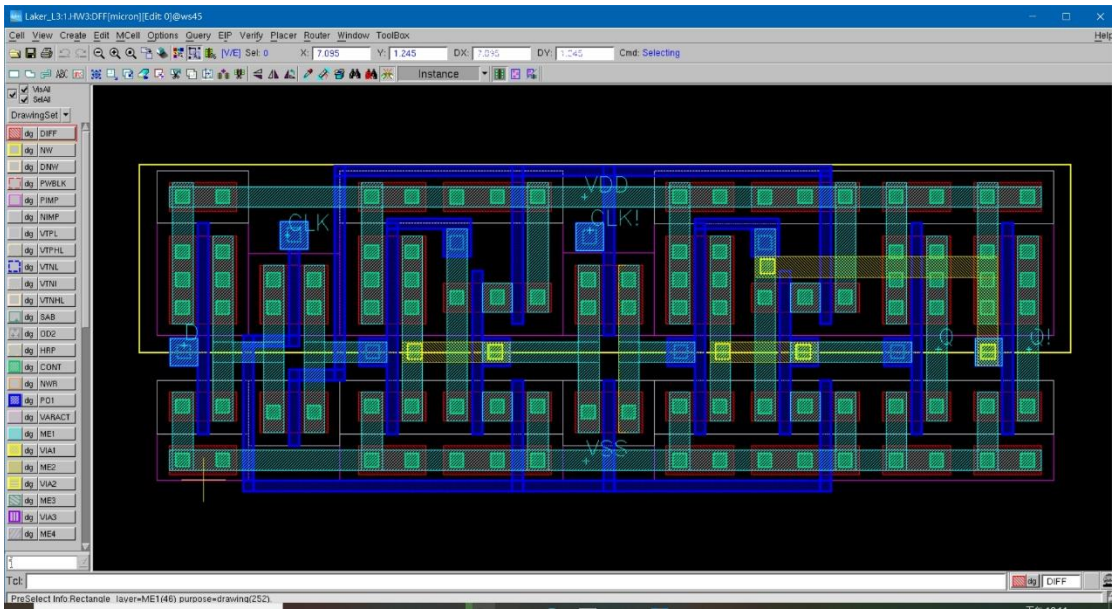
Hold time $= 0.9239 - 1 = -0.0761(ns)$

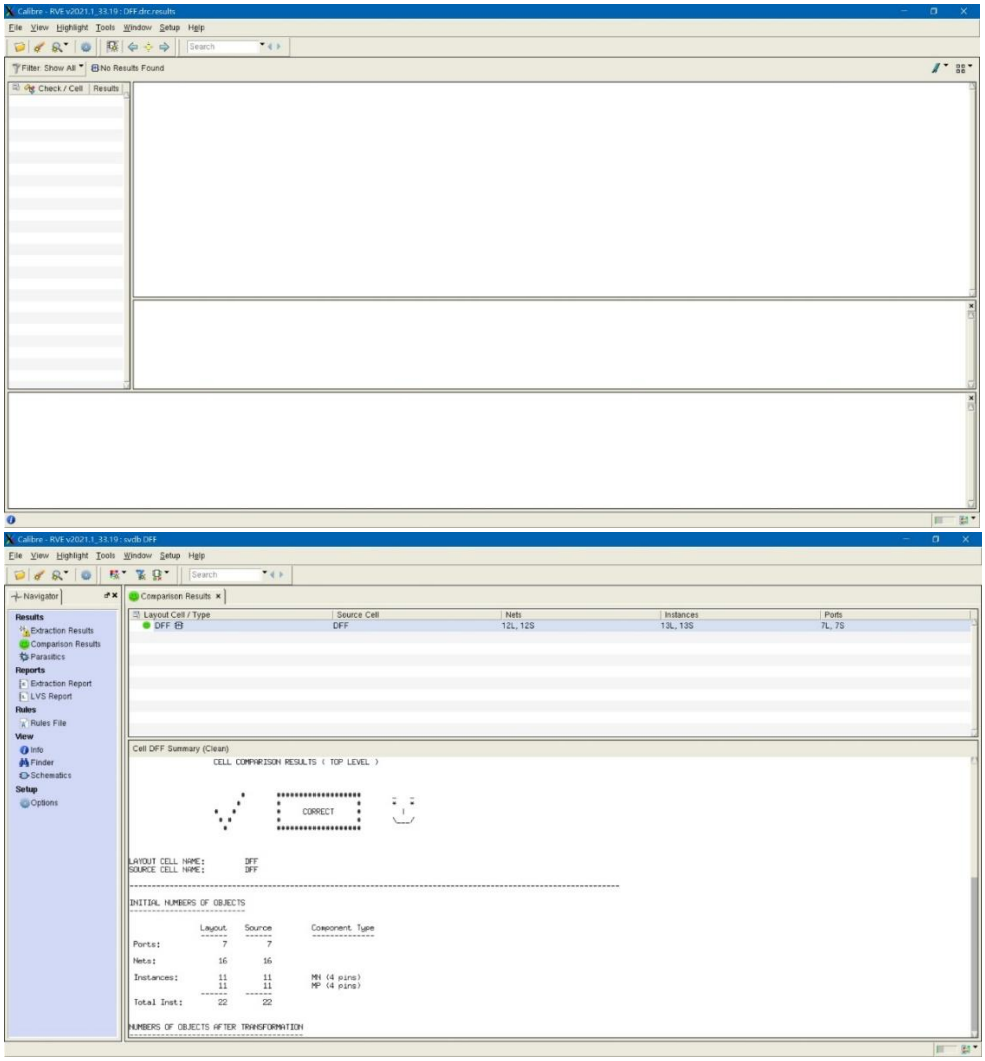
(4)

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tpr_cq= 356.2576p  targ=  15.3613n   trig=  15.0050n
tpf_cq= 199.1055p  targ=  25.2041n   trig=  25.0050n
tp_cq= 277.6816p
```

$t_{pcq} = 277.6816(ps)$

(5) Layout





area $= 15.94 \times 5.585 = 89.0249(\mu m^2)$

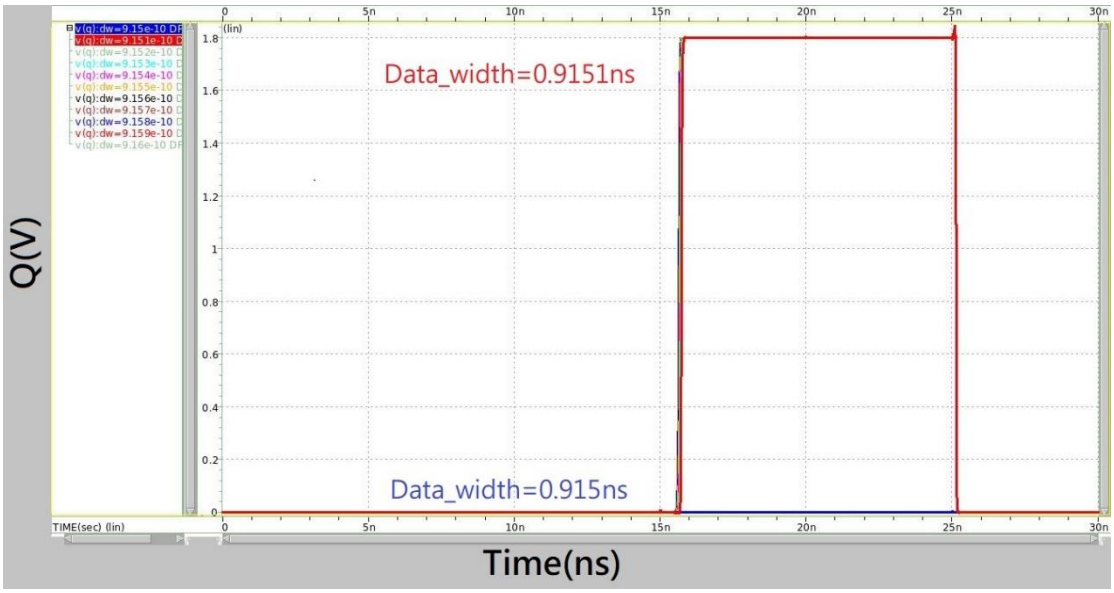
(6) Post-sim

1.setup time

Setup time $= 15 - 14.8949 = 0.1051(ns)$

Difference $= 39.2052\%$

2.hold time



Hold time $= 0.915 - 1 = -0.085(ns)$

Difference $= 11.6951\%$

3.CLK to Q delay

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tpr_cq= 403.4384p  targ=  15.4084n   trig=  15.0050n
tpf_cq= 145.1530p  targ=  25.1502n   trig=  25.0050n
tp_cq= 274.2957p
```

$t_{pcq} = 274.2957(ps)$

Difference $= -1.2193\%$

Part III-Comparison

(1) setup time and hold time

Both set up time and hold time of SR latch are much shorter than D flip flop because the difference of data path. For SR latch, the input signal goes through a transmission gate and arrive output node. Thus, the S to Q (or R to QB) delay is determined by the delay of transmission gate. While for D flip flop, when clock rise, the input signal from master latch goes through a transmission gate as well as inverters and arrive output node in slave latch. Thus, the clock to Q delay is determined by the sum of transmission gate and inverter delays, which is longer than SR latch.

(2) PMOS width of inverter

For SR latch, a shorter PMOS width result in smaller S to Q (or R to QB) delay. For D flip flop, it cannot work when PMOS width is too short. When the PMOS is long enough to let D flip flop work, a shorter PMOS width will not always result in smaller clock to D delay. The smallest delay happened when PMOS width is around $1.5\mu m$.

(3) difference between pre-sim and post-sim

For SR latch, both rising delay and falling delay increase in post-sim. For D flip flop, rising delay increase while falling delay decrease in post-sim. It may because the difference of ratio of PMOS width and NMOS width.