EE3230 Introduction to Integrated Circuit Design, Fall 2021
Homework #1
Due Date : 2021/10/26

Note

1. Do the simulation and analysis with cic018.l.
2. Power supply (VDD) = 1.8V.
3. The length of NMOS and PMOS is minimum length (0.18μm).
4. The rise time, fall time, and period of applied input pulse should be 1ns, 1ns, and 10ns respectively (see Fig. 1).
5. Try .meas, sweep, and .alter command in Hspice simulation.

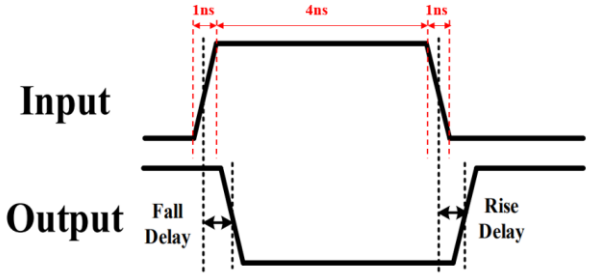


Fig. 1

Problem Defined

Part I (60%)

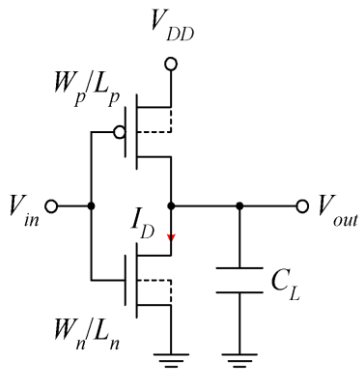
1. Please find the optimized width of NMOS and PMOS with minimum length (0.18μm) and C_{load} = 0.1pF under balanced trigger point (Vin = Vout = 0.5 x VDD) and @TT 25℃, which makes FoM < 8500 (FoM = Power x Delay, unit: μW x ps) (20%)

   Power consumption: measured in 1 cycle; Delay: $(t_{pLH}+ t_{pHL}) / 2$

   Given

   VVIN VIN 0 pulse 0 1.8 10n 1n 1n 4n 10n

   .tran 0.01ns XXns $ Transient precision should be 0.01ns



2. With minimum length (0.18μm), please use the NMOS width obtained in Q1 to find the PMOS width under balanced trigger point (Vin = Vout = 0.5 x VDD) at different corners and temperatures. Please fill the simulation results in Table 1. (10%)

Table 1

Corner	Temperature (°C)	NMOS width (μm)	PMOS width (μm)	Power (μW)	Delay (ps)	FoM (Power x Delay)
SS	-40					
	25					
	125					
SF	-40					
	25					
	125					
TT	-40					
	25					
	125					
FS	-40					
	25					
	125					
FF	-40					
	25					
	125					

3. Find the value of V_{IL},V_{IH},V_{OL},V_{OH}, and noise margin NM_L and NM_H @TT 25°C. (20%)

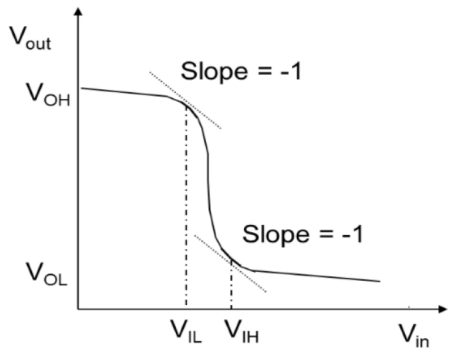


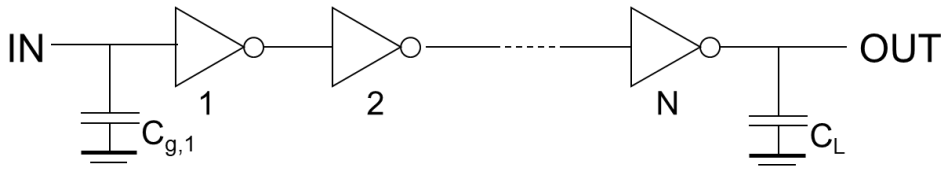
Fig. 2

4. Comment what you have observed from Table 1 and give some discussions. (10%)

Part II (40%)

1. Please design an inverter chain with odd stages and C_L = 10pF to reach propagation delay less than 1ns @TT 25℃. The first inverter, INV_1, is under balanced trigger point. NMOS size of INV_1 is fixed at $(W/L)_n$ = (0.5μm/0.18μm). Please show your waveform for each node and label the propagation delay. (20%)

   Given the estimated best umber of stages N, $N=\log_4 F$, $F=C_L/C_{g,1}$
   Given VVIN VIN 0 pulse 0 1.8 10n 1n 1n 4n 10n



2. According to the designed inverter chain in Q1, please fill the simulation results in Table 2 and give some observations and discussions. (20%)

Table 2.

Corner	Temperature (℃)	Delay (ns)
SS	-40	
	25	
	125	
SF	-40	
	25	
	125	
TT	-40	
	25	
	125	
FS	-40	
	25	
	125	
FF	-40	
	25	
	125	

Submission

1. Report (HW1_StudentID.pdf)
2. Hspice code file (.sp)
3. Waveform with cursor values