EE3230 Introduction to Integrated Circuit Design, Fall 2021

Homework #4

Due Date : 2021/12/14

Note

1. Do the simulation and analysis with cic018.l.
2. Power supply (VDD) = 1.8V.
3. No output loading is needed.
4. The input pulse has the rise and fall time of 0.1ns.
5. ROM array : ROM_CELL_RANK1_16X64.gds

Problem Defined

1. Design a 6-to-64 decoder. Use composer to construct your circuit.
   Show your top-level schematic and sub-circuits used. **(20%)**

2. Show your simulation waveforms. **(32%)**
   Fig. 1 use a 3-to-8 decoder as an example. Input pattern can be given by using different pulse widths and periods. Only one output signal is "high" at a time. In 6-to-64 decoder, please divide the results to print out in eight figures for readability, each figure includes 6 input signals and 8 output signals.

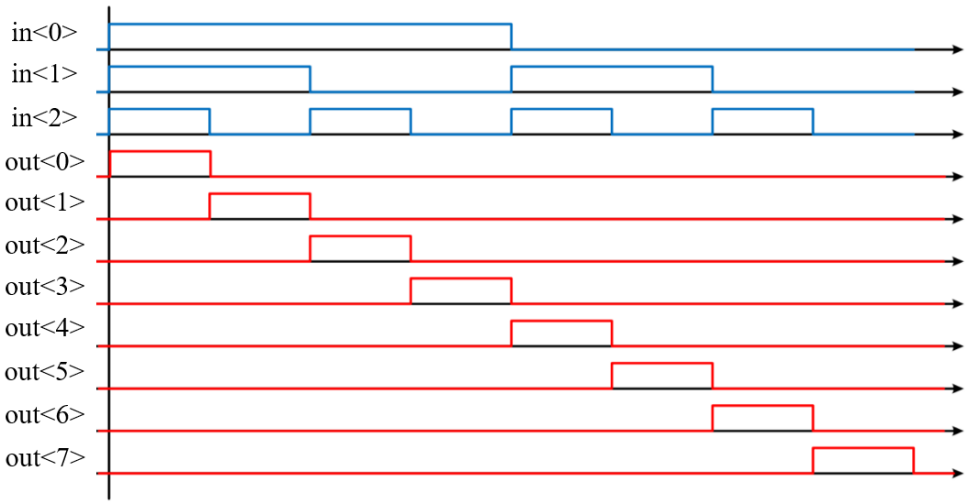

Fig. 1

3. Complete the layout of your 6-to-64 decoder that can match the pitch of given ROM array. That means the width of your layout should not exceed the width of the ROM array. The 64 outputs of the decoder correspond to the 64 WLs of the array respectively (see Fig. 2). Run DRC and LVS without ROM array.

Show your layout **(20%)**, area measured by marker **(4%)**, DRC **(12%)** and LVS **(12%)** reports.

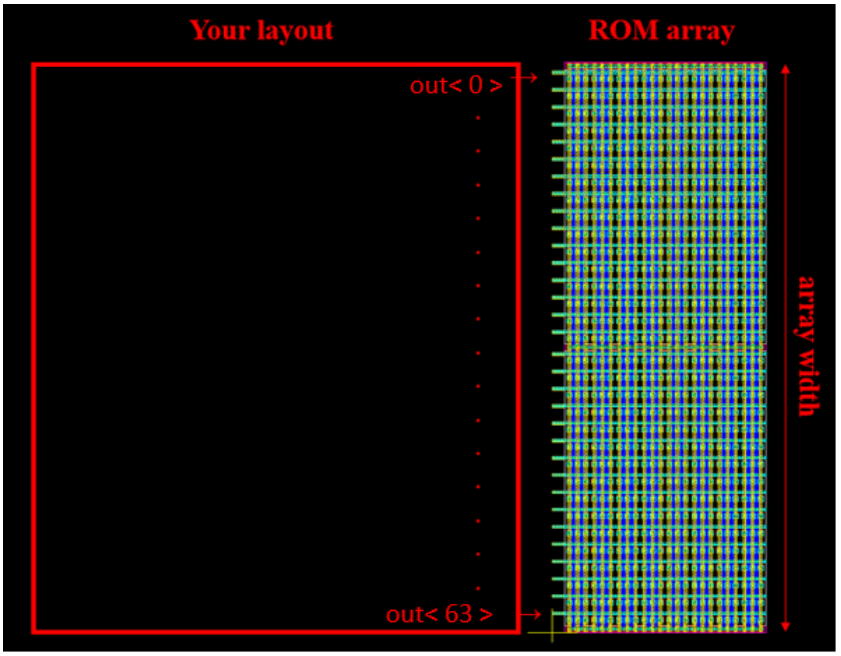

Fig. 2

Submission

1. Report (HW4_StudentID_Name.pdf)
2. Hspice code files (.sp)
3. Netlist files (.spi)
4. Gds files (.gds)

Do not zip these files !