Homework #2

108061127 電機 23 許澤群

Part I

(1)

HW1-part I: inverter

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  58.3432u  from=  20.0000n     to=  30.0000n
tphl= 163.3641p  targ=  10.6634n   trig=  10.5000n
tplh= 158.3998p  targ=  15.6584n   trig=  15.5000n
```

HW2-part I: NAND3

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
nmos_width=   6.0000u
pmos_width=  10.5000u
tphl= 174.7368p  targ=  10.6747n   trig=  10.5000n
tplh= 150.6130p  targ=  15.6506n   trig=  15.5000n
```

$t_{pHL} = 174.7368(\text{ps})$, error $= 6.51\%$

$t_{pLH} = 150.6130(\text{ps})$, error $= 5.17\%$

Delay $= (t_{pHL} + t_{pLH})/2 = 162.6749(\text{ps})$, error $= 1.1\%$

(2) **Table 1**

	Input A	Input B	Input C	Condition	t_{pLH}	t_{pHL}
Case 1	Pulse	1	1	SS 125℃	299.1857	391.6271
				SF 25℃	100.4889	347.7534
				TT 25℃	150.6130	174.7368
				FS 25℃	137.1688	201.7274
				FF -40℃	150.2583	133.1918
Case 2	1	Pulse	1	SS 125℃	333.0096	387.9231
				SF 25℃	123.6402	336.2180
				TT 25℃	164.0423	166.5003
				FS 25℃	165.7299	192.5866
				FF -40℃	169.9633	125.9891
Case 3	1	1	Pulse	SS 125℃	359.1181	377.6139
				SF 25℃	138.5815	317.1992
				TT 25℃	205.3032	148.8430
				FS 25℃	181.0238	173.1801
				FF -40℃	185.1672	110.3329

(3) Comment

First, discuss the results of same case with different conditions. We can observe that high temperature leads to large delay for both t_{pLH} and t_{pHL}. Then, t_{pHL} will be large if NMOS is processed in slow corner, since NMOS will be turned on and the worse carrier mobility increases the delay for the output voltage dropping from high to low. While t_{pLH} will be small if PMOS is processed in fast corner. However, the results FS corner seems not obey this rule. Although NMOS and PMOS are processed in fast corner and slow corner respectively, t_{pHL} is still larger and t_{pLH} is smaller than the result of TT corner.

Next, discuss the results of same condition in different cases. We can observe that for t_{pHL}, case1 $>$ case 2 $>$ case 3. While for t_{pLH}, case3 $>$ case 2 $>$ case 1. Since for NAND3, the source voltage of NMOS is different in each case. When input voltage grows from low to high, NMOS of A need longer time to get larger input voltage and be turned on, which results in larger delay for output voltage drops from high to low (t_{pHL}). Similarly, when input voltage drops from high to low, NMOS of A be turned off with larger input voltage in short time, which results in smaller delay for output voltage grows from low to high (t_{pLH}).

(4)

HW1-part I: inverter

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  58.3432u  from=  20.0000n     to=  30.0000n
tphl= 163.3641p  targ=  10.6634n   trig=  10.5000n
tplh= 158.3998p  targ=  15.6584n   trig=  15.5000n
```

HW2-part I: logic circuit !((A&B)|C)

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
nmos_width=   7.0000u
pmos_width=  15.5000u
tphl= 166.9055p  targ=  15.6669n   trig=  15.5000n
tplh= 167.7811p  targ=  10.6678n   trig=  10.5000n
```

$t_{pHL} = 166.9055(\text{ps})$, error $= 2.12\%$

$t_{pLH} = 167.7811(\text{ps})$, error $= 5.59\%$

Delay $= (t_{pHL} + t_{pLH})/2 = 167.3433(\text{ps})$, error $= 3.86\%$

(5) **Table 2**

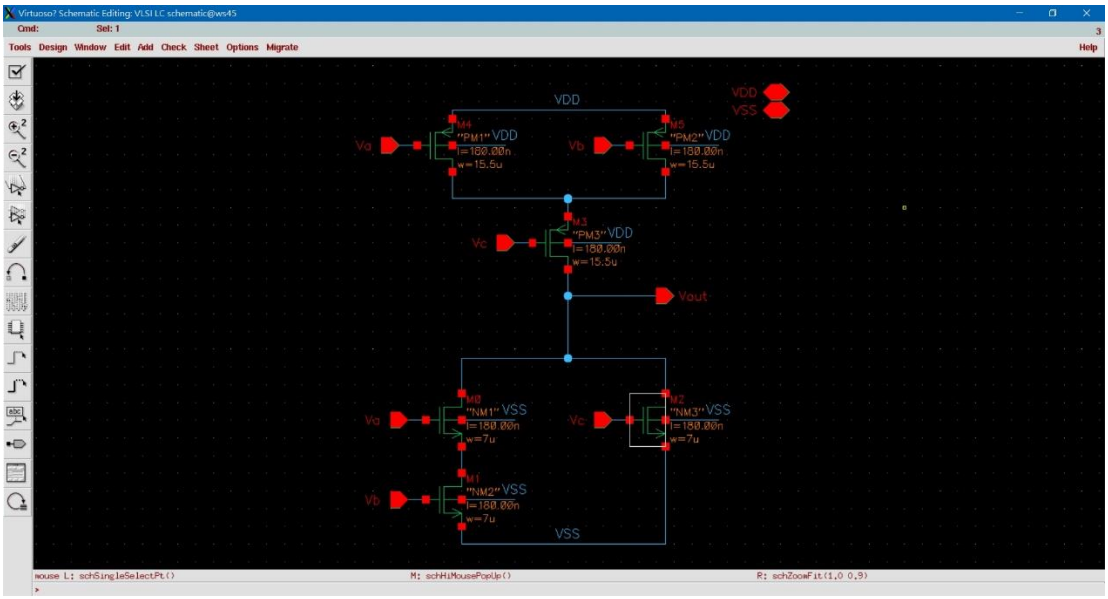
	Input A	Input B	Input C	Condition	t_{pLH}	t_{pHL}
Case 1	Pulse	1	0	SS 125℃	327.6543	374.1209
				SF 25℃	98.1781	336.6179
				TT 25℃	167.7811	166.9055
				FS 25℃	143.8298	194.5158
				FF -40℃	147.2202	129.2106
Case 2	1	Pulse	0	SS 125℃	365.9303	342.4127
				SF 25℃	121.2359	306.1783
				TT 25℃	189.1314	149.3834
				FS 25℃	164.0942	175.6655
				FF -40℃	164.8385	116.9597
Case 3	0	1	Pulse	SS 125℃	328.9584	211.7138
				SF 25℃	125.2743	215.5302
				TT 25℃	199.8671	86.9349
				FS 25℃	176.3105	110.5689
				FF -40℃	181.6741	59.7904

(6) Comment

First, discuss the results of same case with different conditions. The results are similar to NAND3, where high temperature leads to large delay for both t_{pLH} and t_{pHL}. And t_{pHL} is large when NMOS is processed in slow corner while t_{pH} is small when PMOS is processed in fast corner.

Next, discuss the results of same condition in different cases. The results are a little complex in this logic circuit, but they still follow the same rule. Comparing input A with input B, consider them as a NAND2, which is similar to NAND3, t_{pHL} is large but t_{pHL} is small for input A. Then for input C, with low source voltage of NMOS and high source voltage of PMOS, t_{pHL} and t_{pLH} of input C are both smaller than input A and input B.

(7) Layout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M4
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w=15.5u
M5
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l=180.00n
w=15.5u
Va
Vb
M3
"PM3" VDD
l=180.00n
w=15.5u
Vc
Vout
M0
"NM1" VSS
l=180.00n
w=7u
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M1
"NM2" VSS
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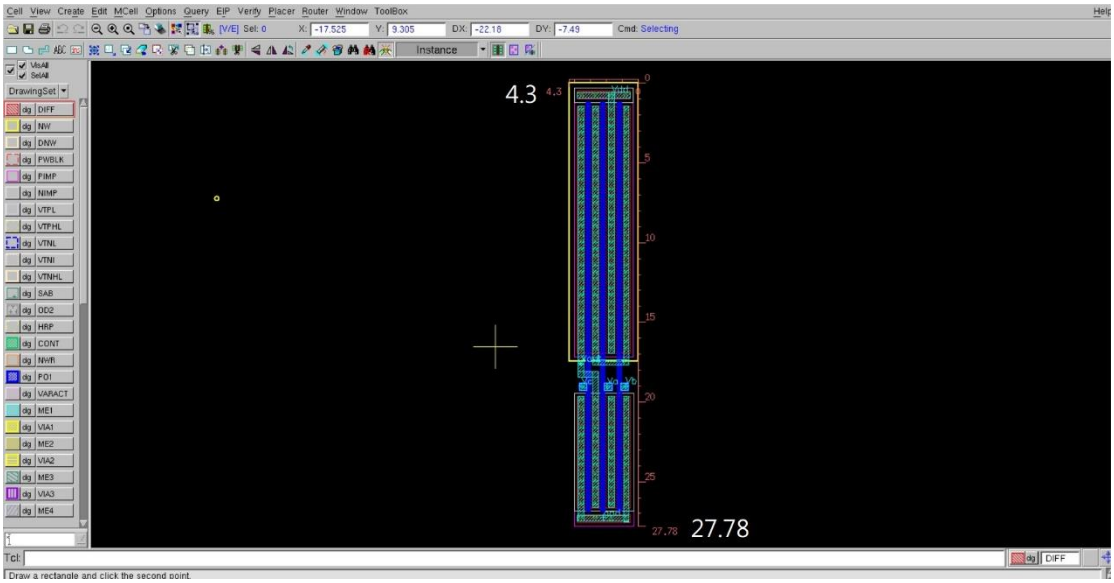
VSS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Instance
4.3
27.78
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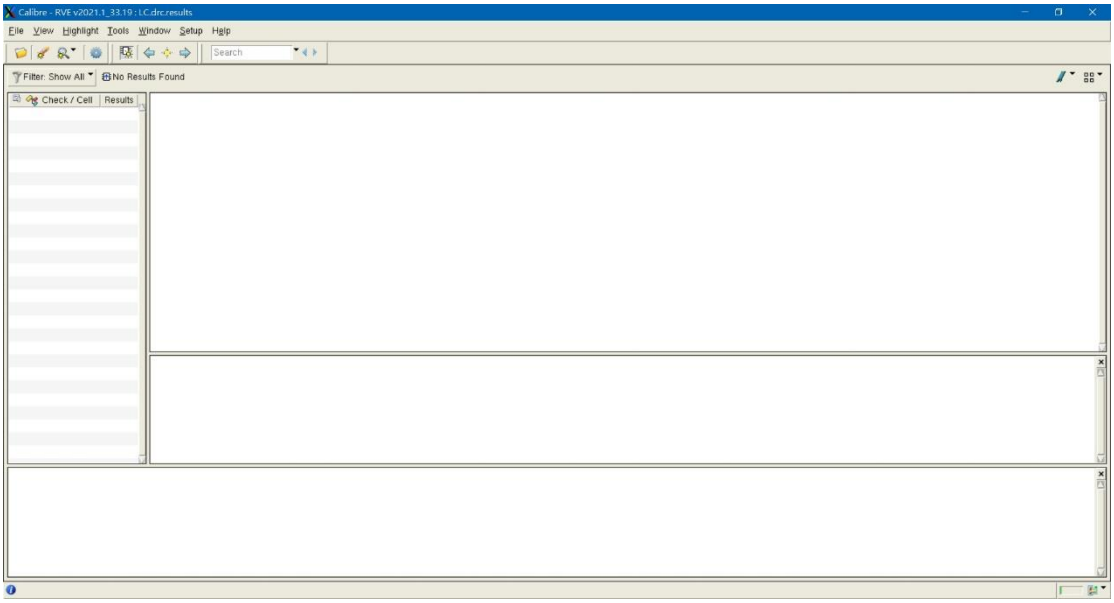
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File View Highlight Tools Window Setup Help
Filter: Show All
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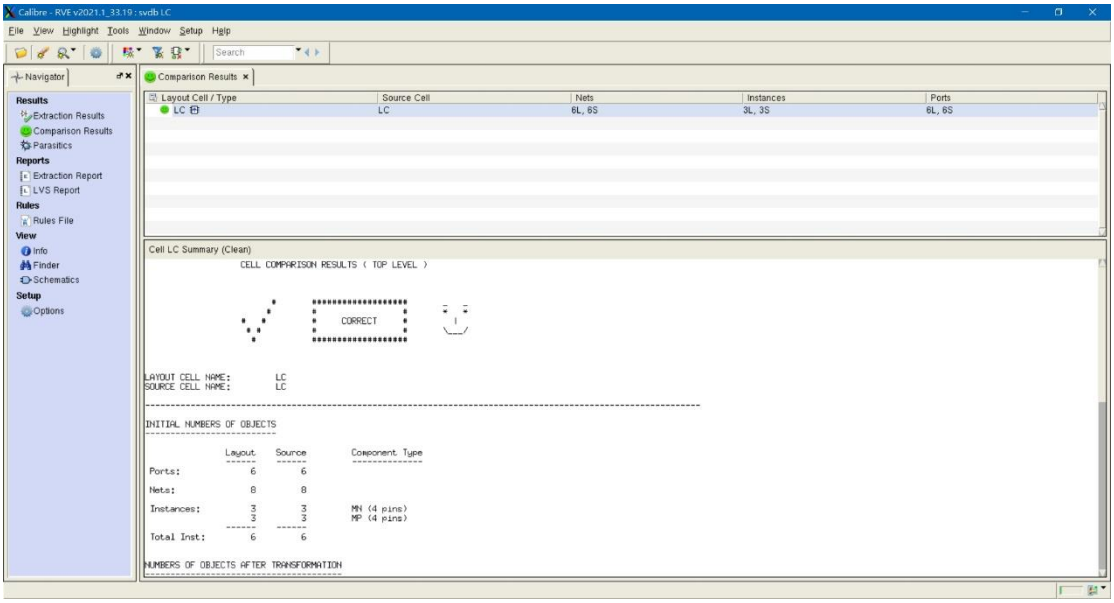
Check / Cell
Results



$\text{area} = 27.779 \times 4.296 = 119.3385(\mu m^2)$

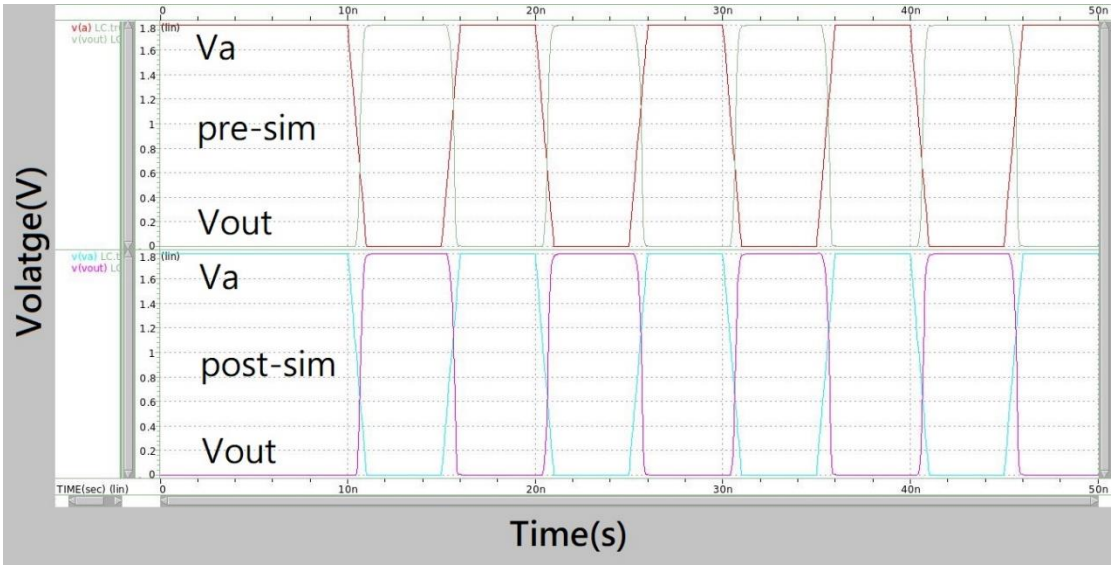
(8)

Pre-sim

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
nmos_width=   7.0000u
pmos_width=  15.5000u
tphl= 166.9055p  targ=  15.6669n   trig=  15.5000n
tplh= 167.7811p  targ=  10.6678n   trig=  10.5000n
```

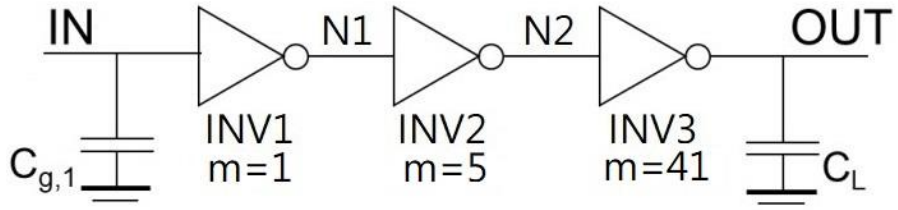
Post-sim

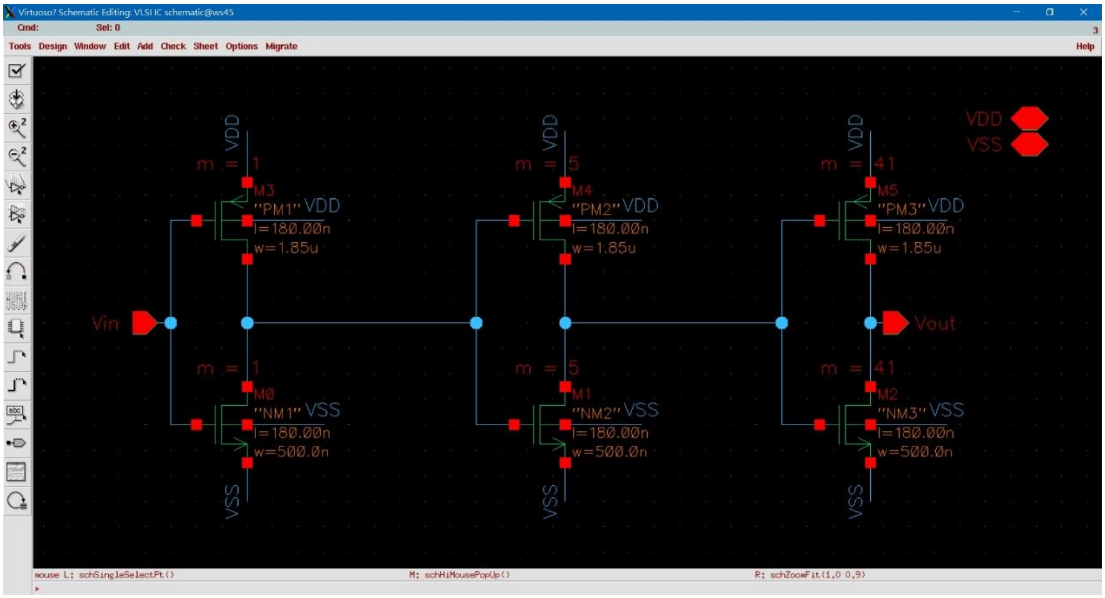
```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tphl= 176.4585p  targ=  15.6765n   trig=  15.5000n
tplh= 184.4437p  targ=  10.6844n   trig=  10.5000n
```



Part II

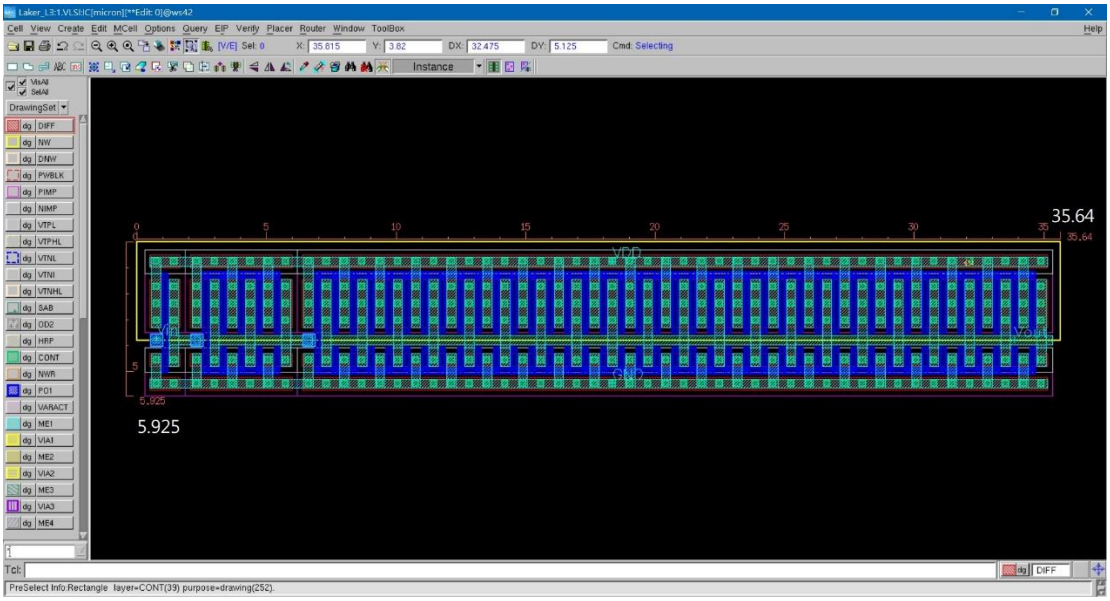
(1) Adjusting M of each stage from HW1.

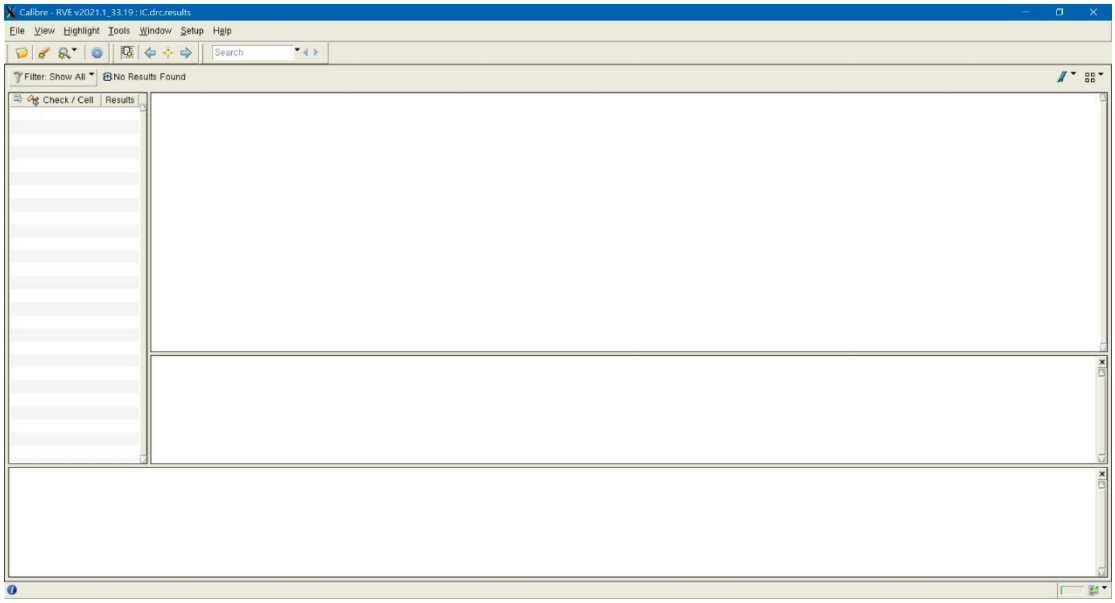


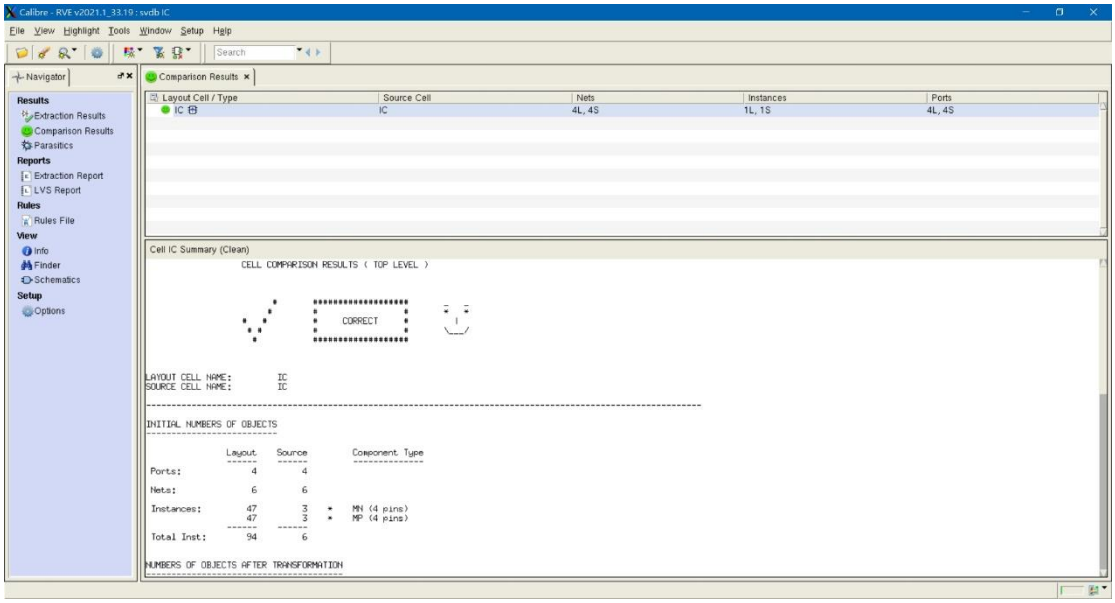



```
****** transient analysis tnom=  25.000 temp=  25.000 ******
nmos_width= 500.0000n
pmos_width=   1.8461u
tphl_vout=   1.0685n  targ=  11.5685n   trig=  10.5000n
tplh_vout= 922.0416p  targ=  16.4220n   trig=  15.5000n
```

Delay $= (t_{pHL} + t_{pLH})/2 = 995.458(ps)$







area $= 35.64 \times 5.926 = 211.2026(\mu m^2)$

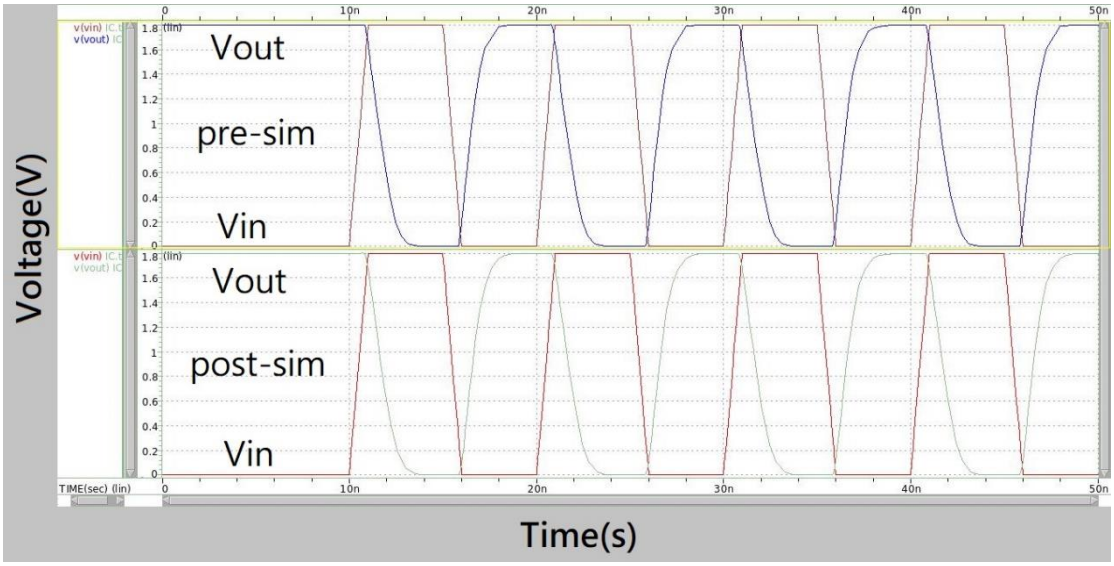
(2)

Pre-sim

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
nmos_width= 500.0000n
pmos_width=   1.8461u
tphl_vout=   1.0685n  targ=  11.5685n   trig=  10.5000n
tplh_vout= 922.0416p  targ=  16.4220n   trig=  15.5000n
```

Post-sim

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tphl_vout=   1.1286n  targ=  11.6286n   trig=  10.5000n
tplh_vout=   1.0480n  targ=  16.5480n   trig=  15.5000n
```



(3) Inverter Chain with Branches

subckt	xinv1	xinv1
element	1:mn	1:mp
model	0:n_18.1	0:p_18.1
region	Cutoff	Linear
id	20.0862p	-23.6865p
ibs	-9.839e-27	3.325e-27
ibd	-194.5080a	3.904e-24
vgs	0.	-1.8000
vds	1.8000	-31.2998n
vbs	0.	0.
vth	428.5764m	-538.9048m
vdsat	56.0137m	-963.8708m
vod	-428.5764m	-1.2611
beta	1.0154m	849.4318u
gam eff	507.4459m	557.0847m
gm	655.9143p	10.8629p
gds	16.9764p	758.0512u
gmb	85.8379p	5.9494p
cdtot	670.4137a	5.7044f
cgtot	566.8137a	4.1460f
cstot	918.3104a	5.5193f
cbtot	1.3789f	4.8751f
cgs	194.1562a	2.1046f
cgd	194.1500a	2.0242f

$C_{g,1} = C_{Ng,1} + C_{Pg,1} = 4.7128 \times 10^{-15}(F)$

$F = C_L / C_{g,1} = 2121.87(F/F)$

Branch A ($N = 2$): $f = \sqrt[2]{F} \approx 46$

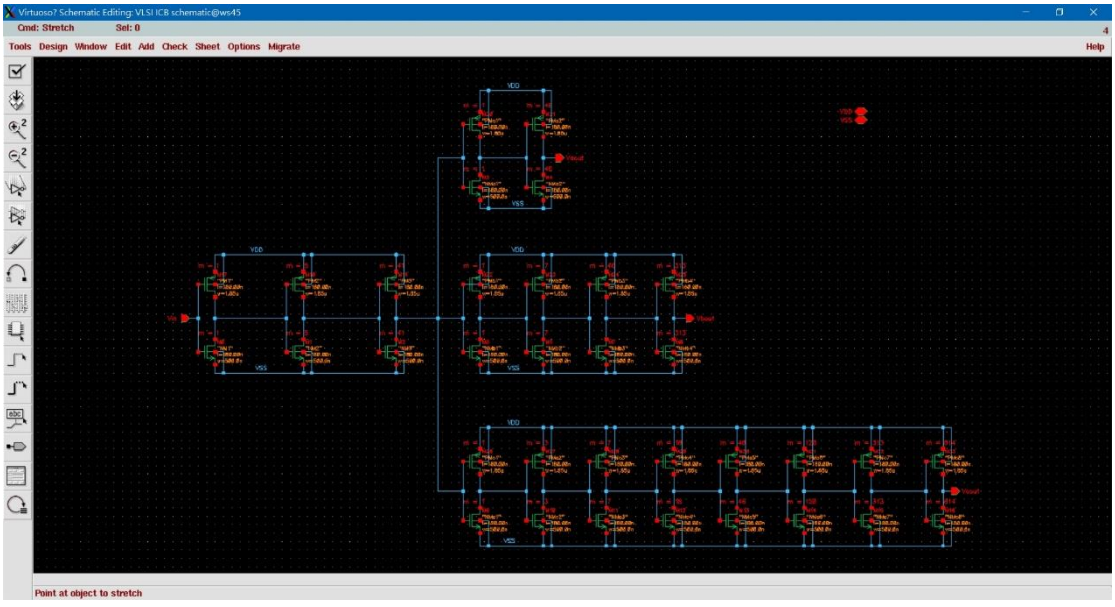
$1 \rightarrow 46$

Branch B ($N = 4$): $f = \sqrt[4]{F} \approx 6.78$

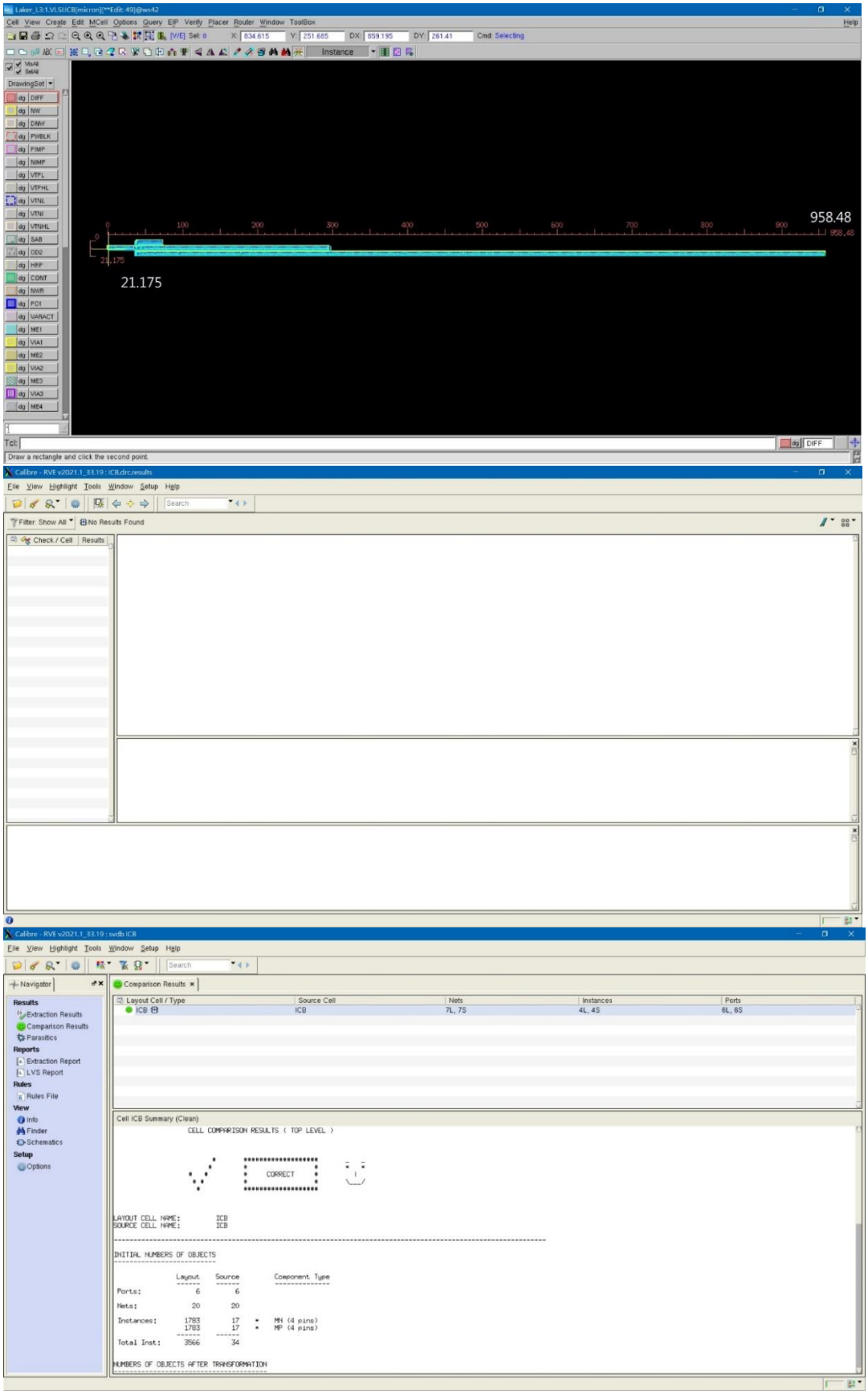
$1 \rightarrow 7 \rightarrow 46 \rightarrow 313$

Branch B ($N = 8$): $f = \sqrt[8]{F} \approx 2.6$

$1 \rightarrow 3 \rightarrow 7 \rightarrow 18 \rightarrow 46 \rightarrow 120 \rightarrow 313 \rightarrow 814$



(4)

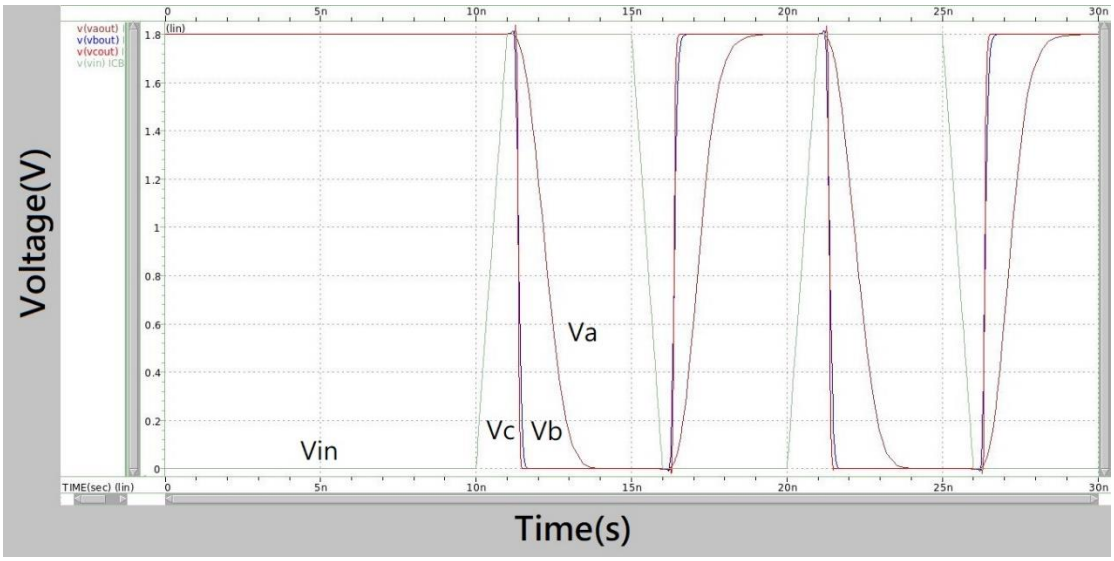


$$\text{area} = 21.178 \times 958.73 = 20.3039 \times 10^3 (\mu m^2)$$

(5)

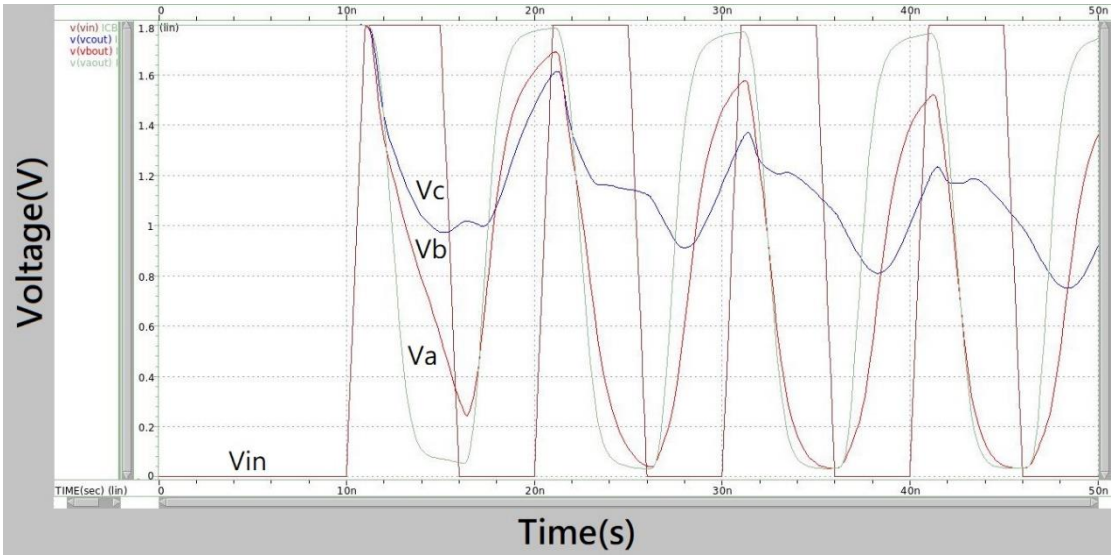
Pre-sim

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tphl_vaout=   1.7347n  targ=  12.2347n   trig=  10.5000n
tplh_vaout=   1.6857n  targ=  17.1857n   trig=  15.5000n
tphl_vbout= 879.5945p  targ=  11.3796n   trig=  10.5000n
tplh_vbout= 880.4408p  targ=  16.3804n   trig=  15.5000n
tpll_vcout= 862.5149p  targ=  11.3625n   trig=  10.5000n
tphh_vcout= 868.6918p  targ=  16.3687n   trig=  15.5000n
```



Post-sim

```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tphl_n2=    2.0249n  targ=  12.5249n   trig=  10.5000n
tplh_n2=    1.9465n  targ=  17.4465n   trig=  15.5000n
tphl_n4=    3.0195n  targ=  13.5195n   trig=  10.5000n
tplh_n4=    2.1882n  targ=  17.6882n   trig=  15.5000n
tpll_n8=   26.6423n  targ=  37.1423n   trig=  10.5000n
tphh_n8=   23.8892n  targ=  39.3892n   trig=  15.5000n
```



Discuss the post-sim result of inverter chain branch with 8 stage. From the waveform, it's obviously that the output voltage drops so slowly such that it cannot reach half of V_{DD} in a single input pulse cycle. Also, the output voltage cannot grow to V_{DD} in a single input pulse cycle. Therefore, it drops a little overall a single input pulse cycle and finally reach half of V_{DD} during the third input pulse cycle, resulting in the much large delay.

The unexpected result may come from the unproper design. Since $C_{g,1}$ used for design is measure from the first inverter of the branch without connecting with other inverters. However, when connect the branches to the inverter chain from HW1-part II and check out the simulation list after completed layout, the $C_{g,1}$ of the branches are not the same as the one used for design, which may lead to the unexpected result.

(6) What I have learned

From this homework, I have learned how to use the CAD tool as well as some sense of design circuit. For a combination logic circuit with PUN and PDN, how to determine the width of PMOS and NMOS is balance the total width of PUN and PDN. Usually, the width of PMOS is approximately 3 times larger than NMOS because of the difference of their carriers. For an inverter chain, the number of stages is determined according to $C_{g,1}$ and C_L. However, the area of circuit may be too large if we purchase the smallest delay. Therefore, the trade off between delay and area is something need to evaluate.