EE3230 VLSI Design, Fall 2021
Homework #5
Due Date : 2021/12/28

Note

1. Do the simulation and analysis with cic018.l.
2. Power supply (VDD) = 1.8V.
3. No output loading is needed.
4. Use .tran 0.01p XX for simulation

Description

Sense amplifier is a read circuitry used in memory chip. Its role is to sense the signal from memory cell that represents 1 or 0 and amplify the small signal swing to full swing so that the signal can be interpreted by other logics.

Fig 1. shows an example of latch-type amplifier. EN is the precharge signal used to reset the SA to the state that is prepared for working. INN and INP are signals came from memory cell which will presence a voltage difference when reading out the data. SO and SON are output signals, they are initially precharged to VDD, one will become VDD and the other GND after sensing.

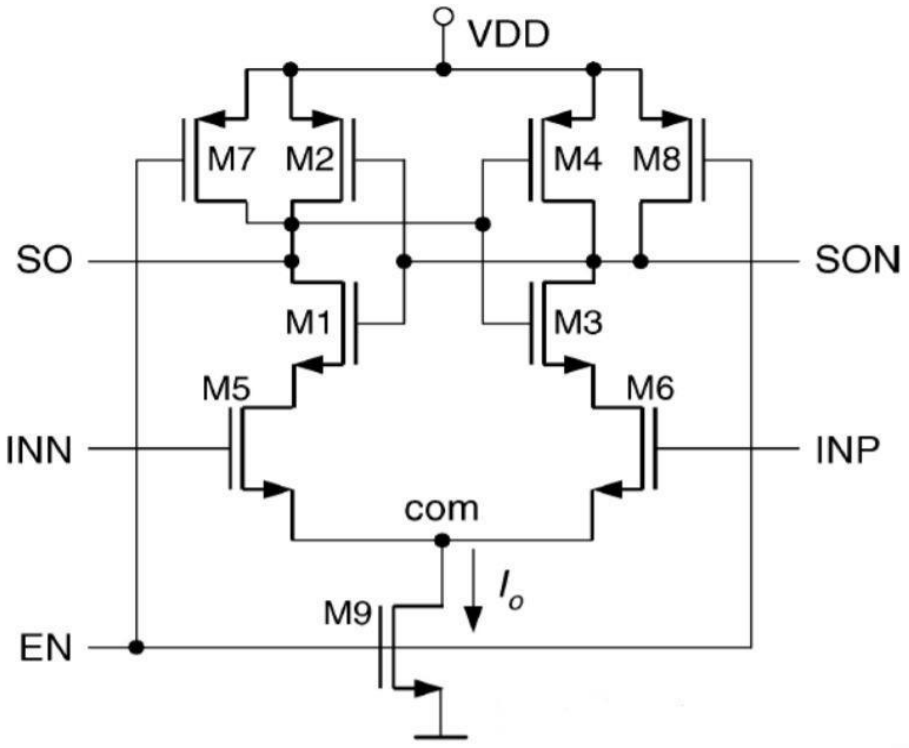

Fig 1.

Fig 2. Shows the transient behavior of the SA. In phase 1, EN goes high, drain current of M5 and M6 start to discharge SO and SON respectively. In phase 2, due to the

difference in drain current, M2 will be turned on before M4, strong positive feedback then enhances the output voltage difference. In phase 3, M1 turns off, latching complete.

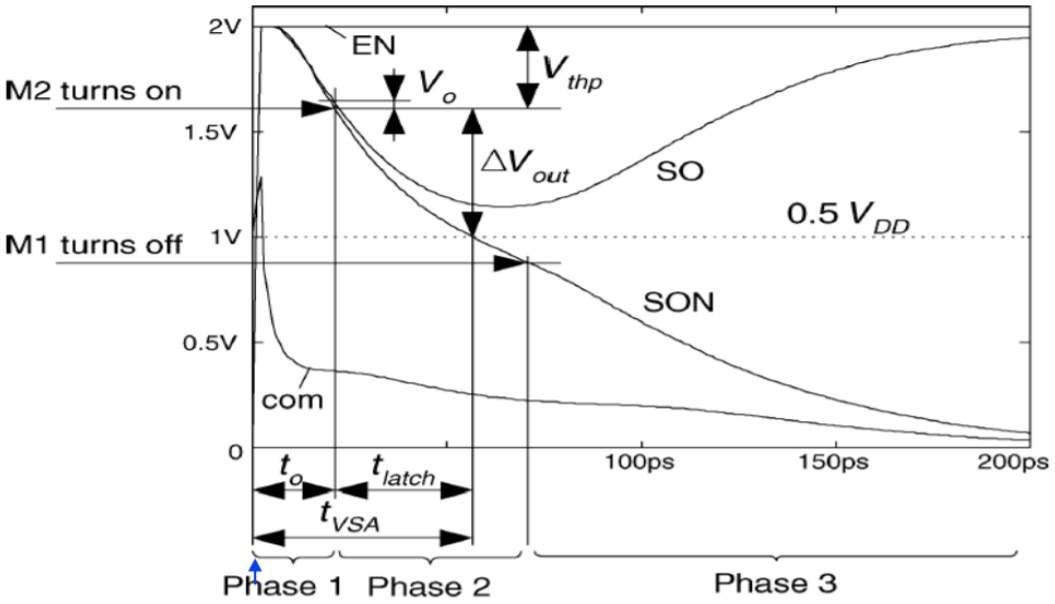

Fig 2.

Problem Defined

1. Design proper transistor sizing for the latch-type sense amplifier (SA) shown in Fig 1. (Symmetry MOS size and layout design is recommended).
Print out the **schematic** and comment how you design (you can run the pre-sim first to get better sensing time and power from sizing MOS). Fill in Table 1. **(10%)**
2. Run the pre-simulation with **Monte Carlo (1024 times)** for all transistors in SA and find sensing time and average power of your SA at **5 different corners**. Print out simulation waveforms at TT 25℃. **(10%)** Fill in Table 2. and give some discussion. **(40%)**

Note:

a. **EN** set as pulse (0 1.8 1n 0.1n 0.1n 0.9n 2n).
b. Define ***INP****=VDD,* ***INN****=VDD-Vin_offset*.
c. **Vin_offset** is defined as the minimum voltage difference between INP & INN with **99.9% yield** in Monte Carlo simulation.
d. For Monte Carlo set: .PARAM Vth=AGAUSS**(0,0.072,6)**
e. Take the results of Monte Carlo **without sensing fail**.
Sensing time (tp) is defined as *EN=0.5*VDD to SON=0.5*VDD*.
Average power for one EN cycle (2ns) (precharge + sensing).
(power negative means that devices are consuming and since supplies supply it, fill in Table with magnitude only.)

3. Complete the **layout** of your SA and pass DRC LVS. **(25%)**
Run **post-simulation** (with R-C-CC extraction) at TT 25℃ with Monte Carlo (1024 times) at condition (a) *INP=VDD, INN=VDD-Vin_offset* and (b)*INP=VDD-Vin_offset, INN=VDD.*
Compare the result and waveform with pre-simulation and give some discussion. **(15%)**

4. Fill in the google sheet with your post-simulation at TT 25℃ for ranking.
(Fill in Vin_offset with the bigger one at the condition (a) or (b).)
(Fill in Sensing Time and Power with M.C. average at the same condition as Vin_offset.)

$$FoM = \frac{1}{Vin_{offset}(mV) * tp(ps) * power(uW) * area(um^2)}$$

Bonus

1st (10%), 2nd ~ 10th (8%), 11th ~ 20th (5%), 21th ~ 40th (3%)
Note: The larger, the better.

MOS	Width(um)	Length(um)
M1		
M2		
M3		
M4		
M5		
M6		
M7		
M8		
M9		

Table 1. SA MOS size

Condition	Vin_offset (mV)	Sensing Time (ps)			Avg. Power (uW)		
		Max.	Min.	Avg.	Max.	Min.	Avg.
TT 25℃							
SF 25℃							
FS 25℃							
SS 125℃							
FF -40℃							

Table 2. Pre-sim. M.C. at 5 corners

Condition TT 25℃	Vin_offset (mV)	Sensing Time (ps)			Avg. Power (uW)		
		Max.	Min.	Avg.	Max.	Min.	Avg.
Pre-sim.							
Post-sim (a)							
Post-sim (b)							

Table 3. Post-sim. vs Pre-sim M.C.

Submission

Report (HW5_StudentID_Name.pdf)

(1) Picture of schematic, Table 1. and comment. (10%)

(2) Picture of pre-simulation waveforms at TT 25℃. (10%)

(3) Table 2. and discussion. (40%)

(4) Picture of area of the layout with markers. (15%)

(5) Picture of passing DRC, LVS. (10%)

(6) Picture of post-simulation waveforms compare with pre-simulation at TT 25℃, Table 3. and comment. (15%)

Hspice code files (HW5_studentID.sp)

Netlist files (HW5_studentID.spi)

Gds files (HW5_studentID.gds)

***** Please write your Report in the order above & Do not zip these files ! *****