

EE3230 VLSI Design, Fall 2021

Homework #3

Due Date : 2021/11/30

Note

1. Do the simulation and analysis with cic018.1.
2. Power supply (VDD) = 1.8V.
3. Use .tran 0.01p XX for simulation

Part I (42%)

1. Design a SR latch as shown in Fig. 1. Assume CLK=100MHz with $t_r=t_f=10ps$, duty cycle=50%. (7%)
2. Simulate and find the setup time of this latch. (7%)
Note1 : For a positive latch, setup time and hold time of this latch are defined as Fig. 2.
Note2 : Give $S \neq R$ for question 2., 3., 4. and 5.
3. Same as above, simulate and find the hold time of this latch. (7%)
4. Simulate the S to Q delay t_{psq} and R to QB delay t_{prqb} . (7%)
5. Sweep Vdd and find the operation voltage of this latch.
6. Complete the layout of this design. The layout should measure the area. (8%)
Note : Area of the layout is the area of the minimum single rectangle that can cover all circuits.
7. Run the post-layout simulation (post-sim) and compare it with pre-simulation(2., 3., 4. and 5.) (pre-sim) (7%)

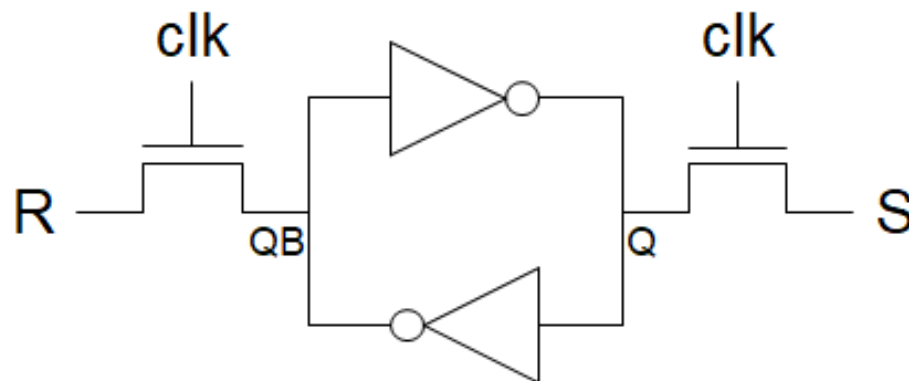


Fig. 1.

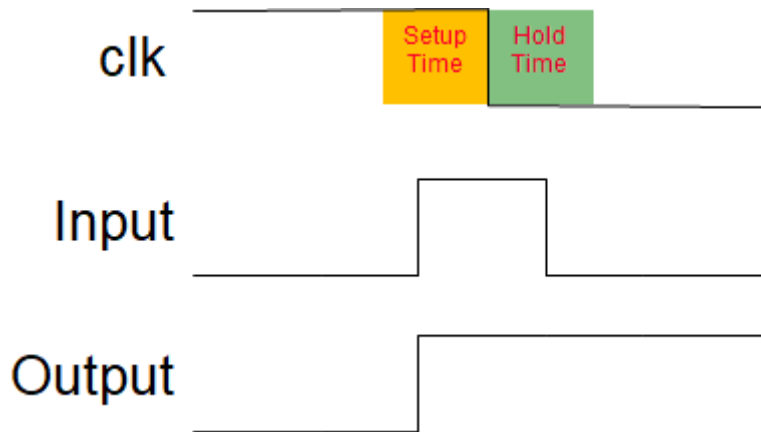


Fig. 2.

Part II (43%)

1. Design a master-slave positive-edge-triggered D flip-flop as shown in Fig. 3. Assume CLK(C)=100MHz with $t_r=t_f=10\text{ps}$, duty cycle=50%. (7%)
2. Simulate and find the setup time of this flip-flop. (7%)
3. Simulate and find the hold time of this flip-flop. (7%)
4. Simulate the clock to Q delay tpcq. (7%)
5. Complete the layout of this design. The layout should measure the area. (7%)
Note : Area of the layout is the area of the minimum single rectangle that can cover all circuits.
6. Run the post-layout simulation (post-sim) and compare it with pre simulation (2., 3. and 5.) (pre-sim) (7%)

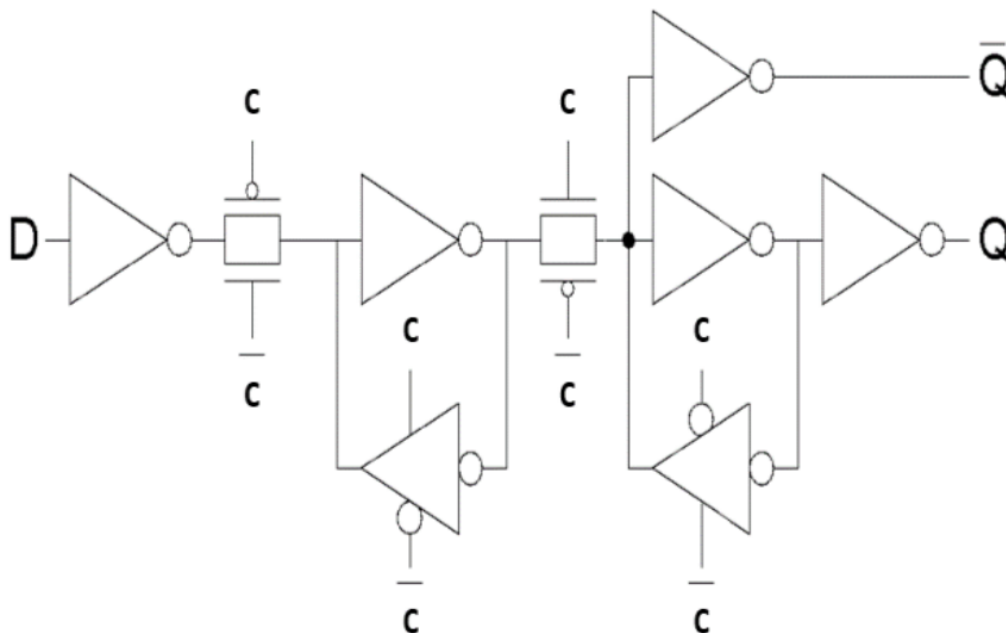


Fig. 3.

Part III (15%)

Comment and Compare between Latch in Part I and DFF in Part II . (at least three comparisons) (each for 5%)

Submission

1. Report (HW3_StudentID_NAME.pdf)
 - a. Picture of schematic
 - b. Picture of waveform with cursor values
 - c. Picture of area of the layout with markers
 - d. Your comment
2. Hspice code file (.sp)
3. Netlist files (.spi)
4. Gds files (.gds)