Homework #5

108061127 電機 23 許澤群

Part I – Sense Amplifier

1. Circuit design

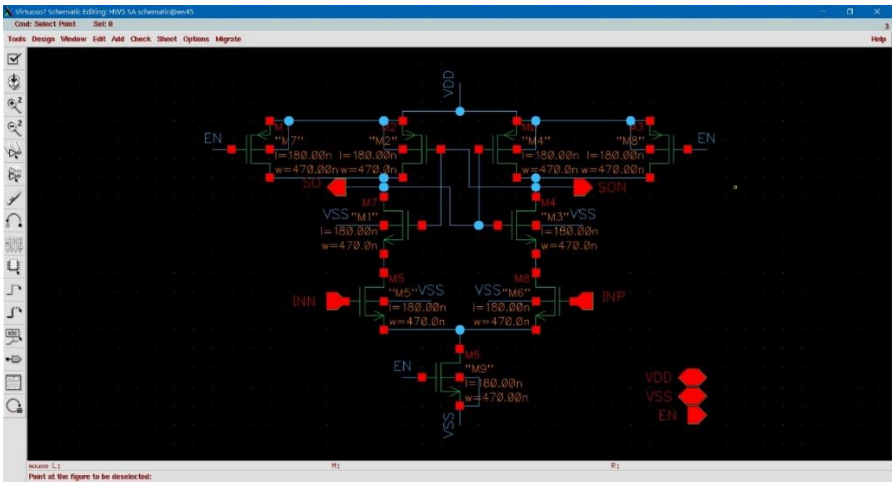


Fig.1 sense amplifier schematic

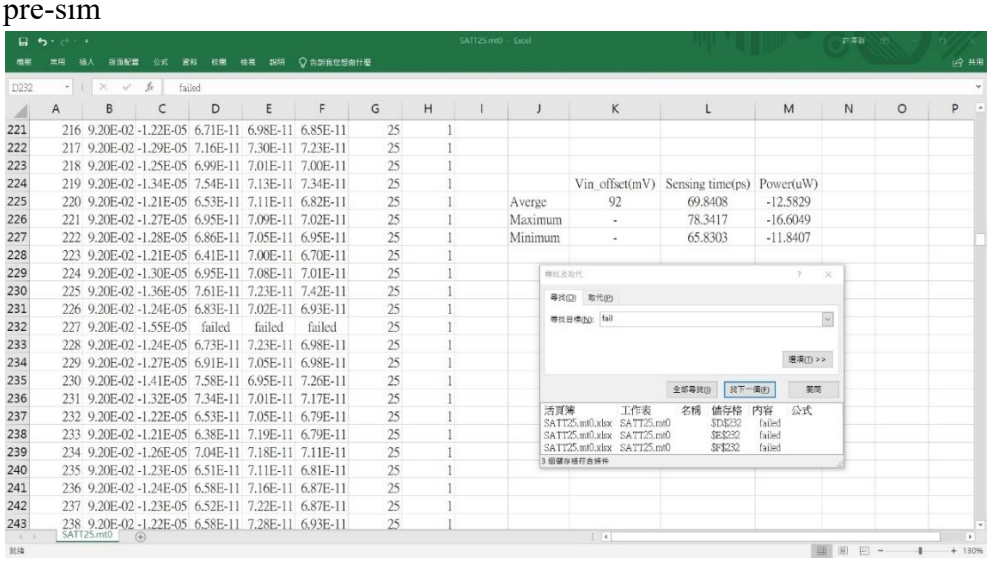
According the adjustment and simulation, I found that the sizes of M9, M7, M8 are negative correlated to the sensing time. Since the tail current dominated the drop of SON, a large M9 will decrease the sensing time. On the other hand, since a large M7 and M8 charge SO node quickly, SON discharge quickly, too. While large MOSFETs also increase the layout area as well as the current of device, which leads to a large power consumption. After comparison and trade-off, I design all MOS with minimum size W= 0.47(μm).

MOS	Width(um)	Length(um)
M1	0.47	0.18
M2	0.47	0.18
M3	0.47	0.18
M4	0.47	0.18
M5	0.47	0.18
M6	0.47	0.18
M7	0.47	0.18
M8	0.47	0.18
M9	0.47	0.18

Table 1. SA MOS size

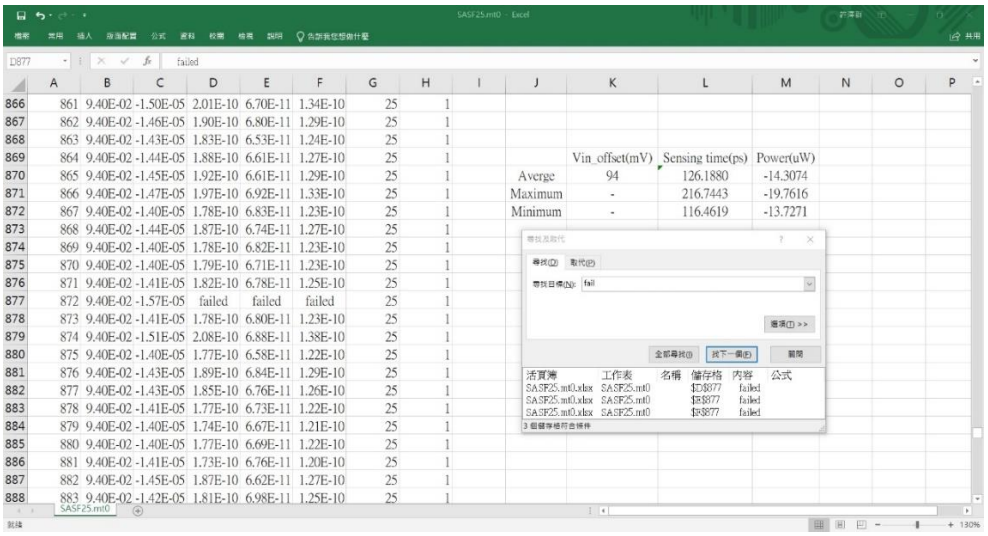
2. Pre-simulation with Monte Carlo

(1) pre-sim



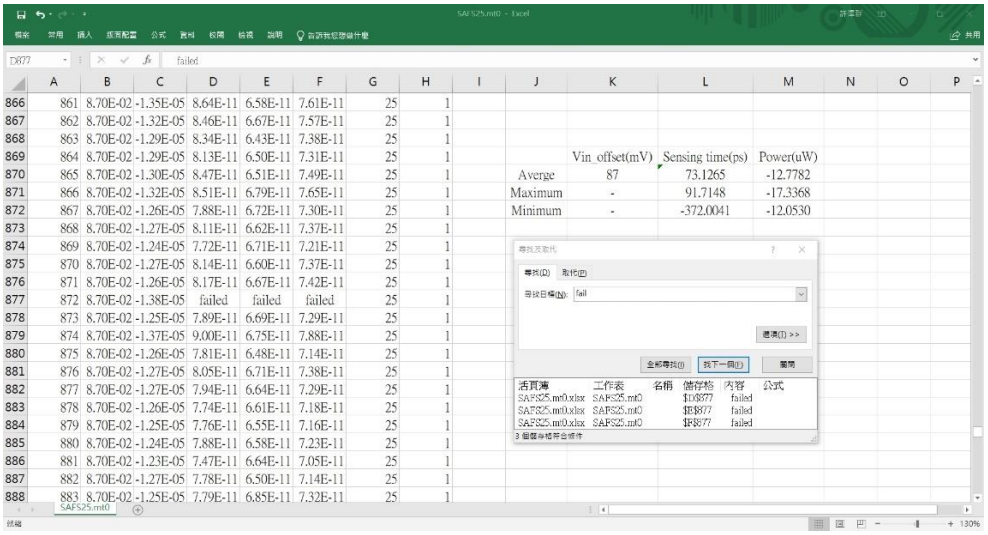
	Vin_offset(mV)	Sensing time(ps)	Power(uW)
Averge	92	69.8408	-12.5829
Maximum	-	78.3417	-16.6049
Minimum	-	65.8303	-11.8407

Fig.2 TT 25℃ pre-simulation



	Vin_offset(mV)	Sensing time(ps)	Power(uW)
Averge	94	126.1880	-14.3074
Maximum	-	216.7443	-19.7616
Minimum	-	116.4619	-13.7271

Fig.3 SF 25℃ pre-simulation



	Vin_offset(mV)	Sensing time(ps)	Power(uW)
Averge	87	73.1265	-12.7782
Maximum	-	91.7148	-17.3368
Minimum	-	-372.0041	-12.0530

Fig.4 FS 25℃ pre-simulation

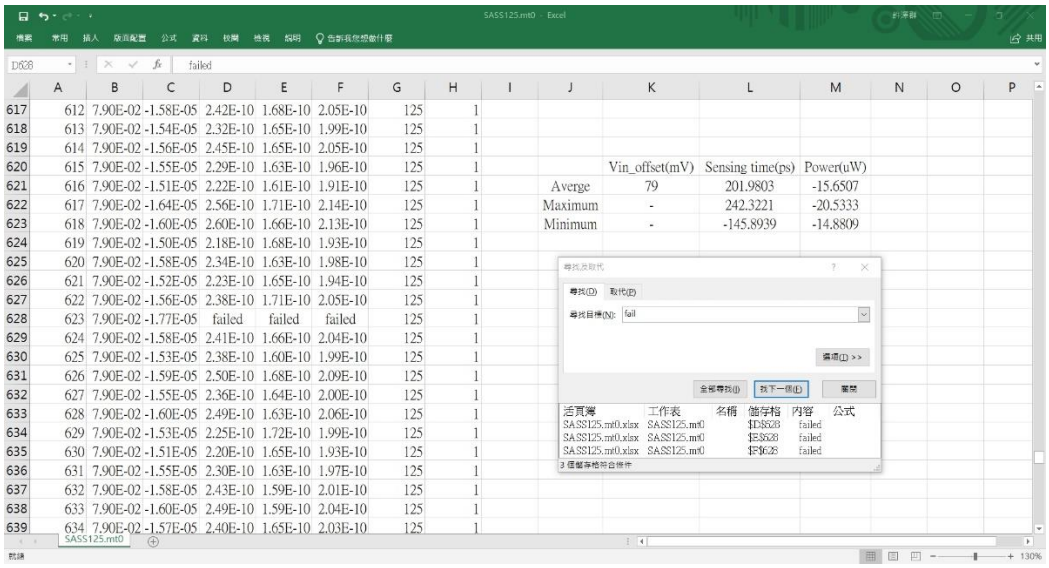


Fig.5 SS 125℃ pre-simulation

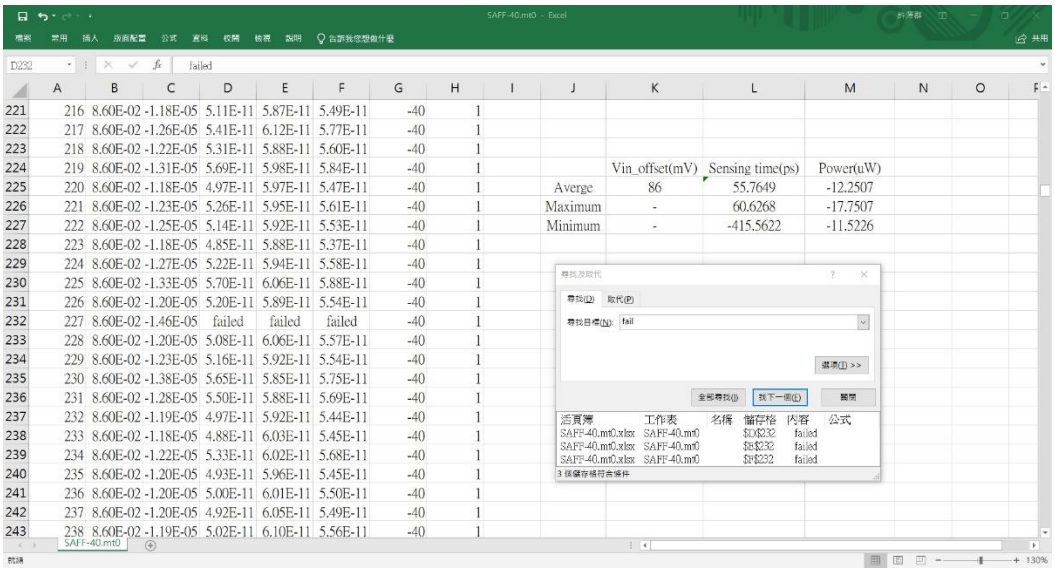


Fig.6 FF -40℃ pre-simulation

Condition	Vin_offset (mV)	Sensing Time (ps)			Avg. Power (mW)		
		Max.	Min.	Avg.	Max.	Min.	Avg.
TT 25℃	92	78.341	65.830	69.840	16.604	11.840	12.582
SF 25℃	94	216.74	116.46	126.18	19.761	13.727	14.307
FS 25℃	87	91.714	-372.00	73.126	17.336	12.053	12.778
SS 125℃	79	242.32	-145.89	201.98	20.533	14.880	15.650
FF -40℃	86	60.626	-415.56	55.764	17.750	11.522	12.250

Table 2. Pre-sim. with M.C. at 5 corners

For Vin_offset, the condition SS 125℃ is smaller than the others. It may because both carrier mobilities of NMOS and PMOS are slow, which let amplifier have enough time to sense the voltage difference from inputs.

For sensing time, the condition that NMOS operated in slow corner are larger than the other conditions. Since the signal SON is pulled down by NMOS, the lower carrier mobilities of NMOS will increase the sensing time.

For power consumption, the condition that operated in 125℃ is the largest, while the condition that operated in -40℃ is the smallest. It may because the temperature influences the leakage current, which cause more power consumption.

(2) waveforms

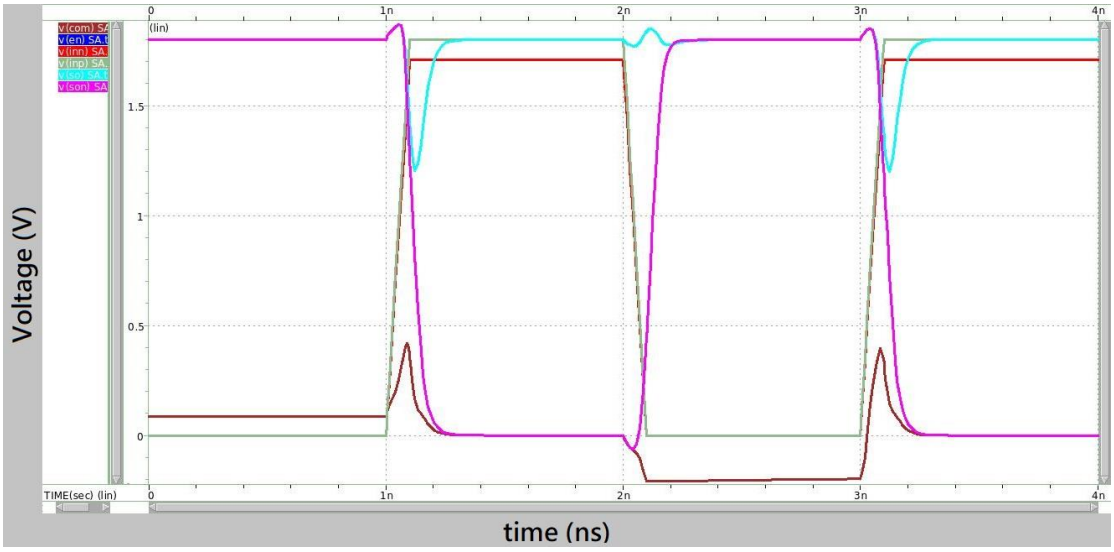


Fig.7 Pre-simulation waveform

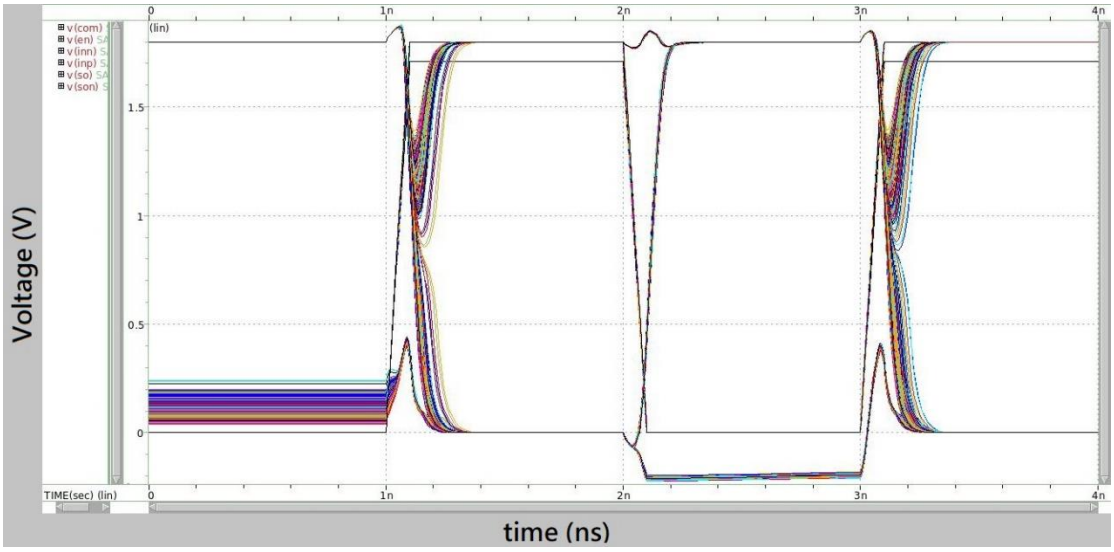


Fig.8 Pre-simulation waveform with Monte Carlo

3. Layout and post-sim

(1) Layout

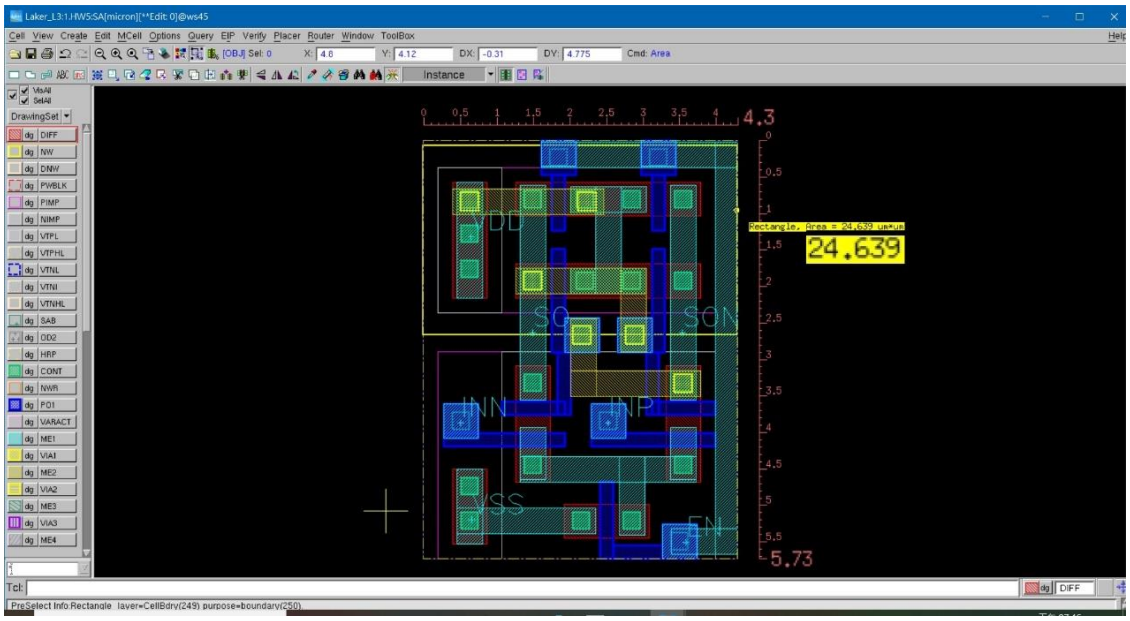


Fig.9 sense amplifier layout

device length= 5.73(μm)

device width= 4.3(μm)

device area= $5.73 \times 4.3 = 24.639(\mu m^2)$

(2) DRC check

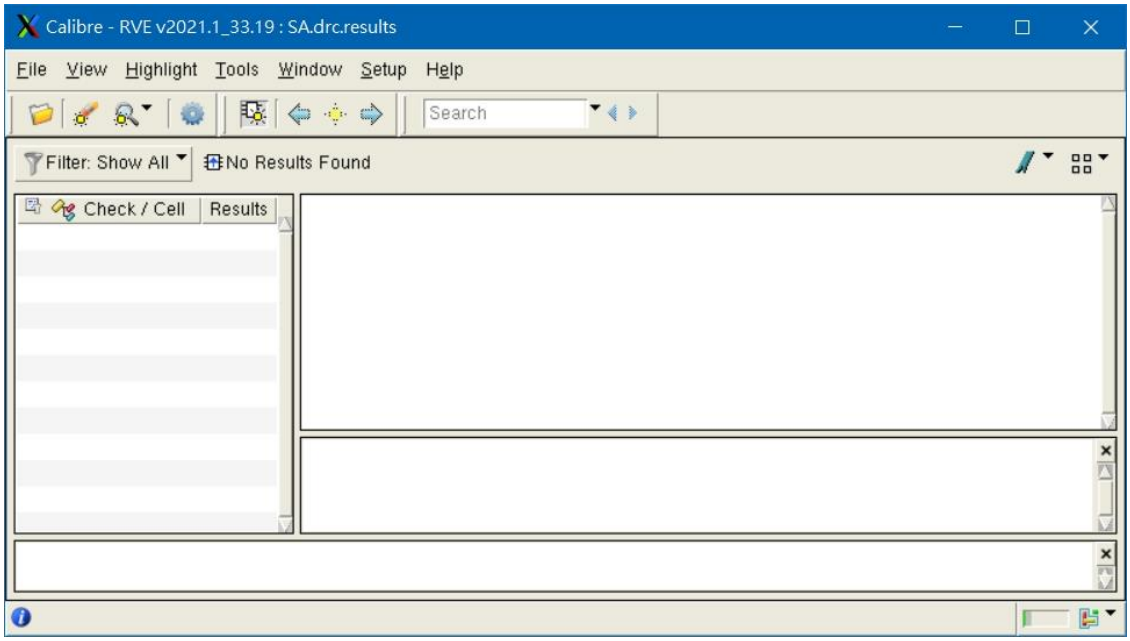


Fig.10 DRC passing results

(3) LVS check

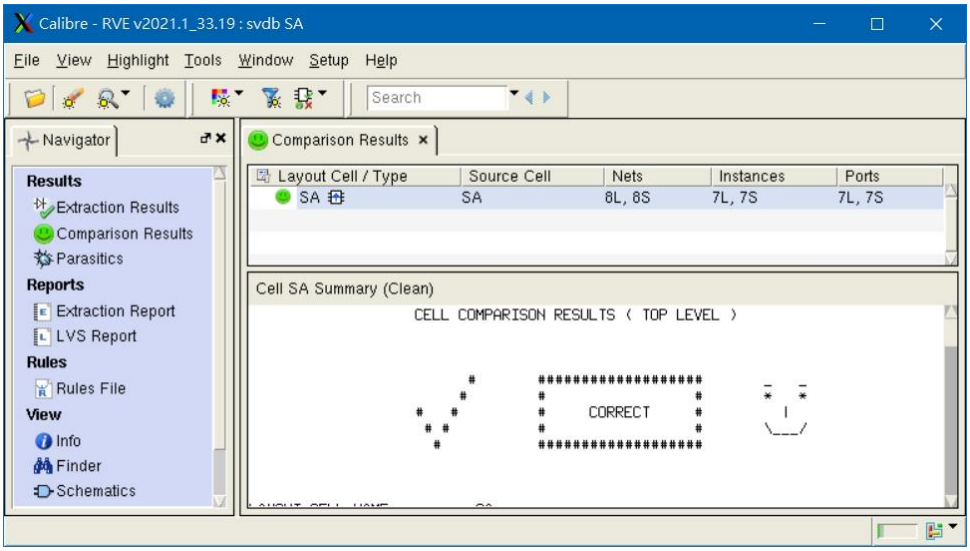


Fig.11 LVS passing results

(4) Post-sim

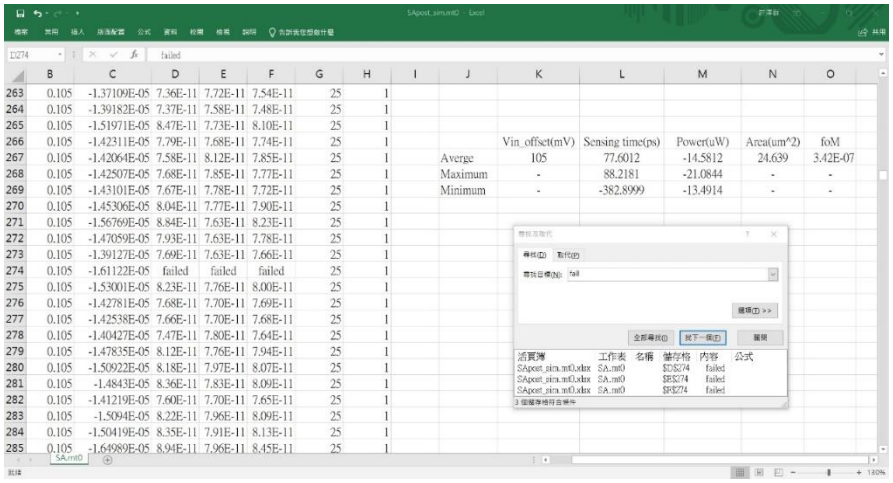


Fig.12 TT 25℃ post-simulation(a)

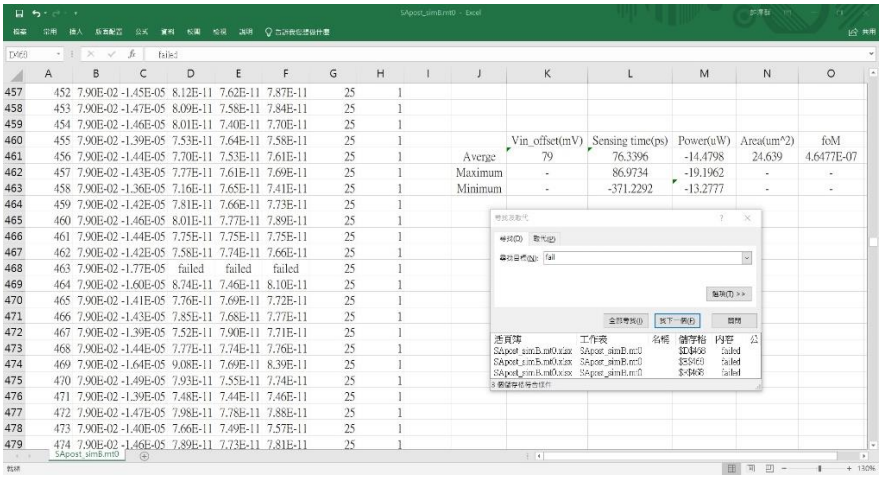


Fig.12 TT 25℃ post-simulation(b)

Condition TT 25℃	Vin_offset (mV)	Sensing Time (ps)			Avg. Power (mW)		
		Max.	Min.	Avg.	Max.	Min.	Avg.
Pre-sim.	92	78.341	65.830	69.840	16.604	11.840	12.582
Post-sim(a).	105	88.218	-382.89	77.601	21.084	13.491	14.581
Post-sim(b).	79	86.973	-371.22	76.339	19.196	13.277	14.479

Table 3. Post-sim. vs Pre-sim with M.C.

(5) Waveforms

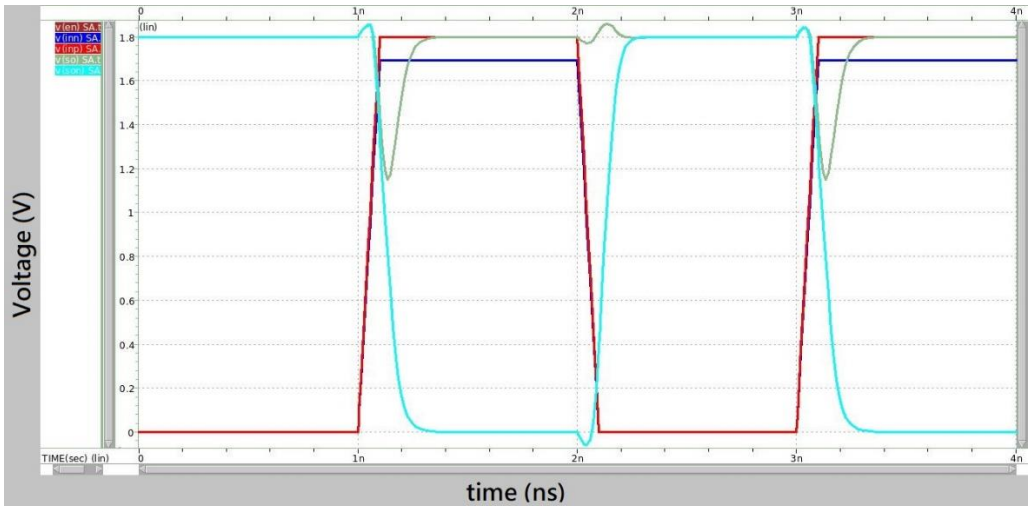


Fig.13 Post-simulation waveform

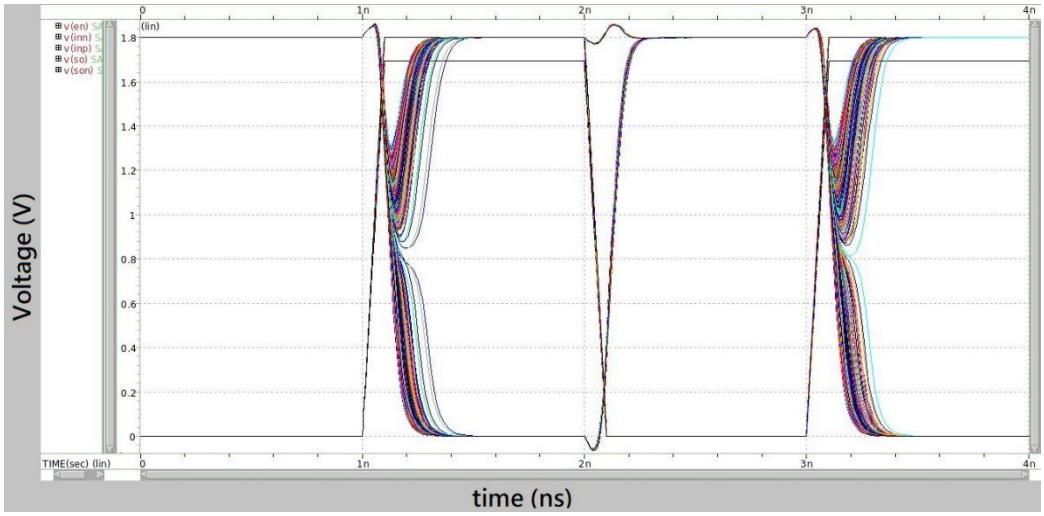


Fig.14 Post-simulation waveform with Monte Carlo

Compare post-simulation(a) with pre-simulation, the waveforms are closely while both sensing time and power consumption increase. It's because of the parasitic resistance and capacitance of device. Also, the Vin_offset increase, since the pair of MOSFET are not symmetry any more.