ROM MACRO DESIGN

***Abstract* - We propose a 1024 bits read only memory (ROM) with dynamic column sources, which enable us to achieve the high speed and the relative low power consumption. ROM macro using 180nm CMOS bulk technology realizes 0.814ns read access time at TT25 / 1.8V / 100MHz.**

I. INTRODUCTION

The macro consists of ROM, decoders, muxs, DFFs, SAs and the timing control. Its widths and lengths are very important. If we does not choose proper sizes, the circuit will not work.Finally, We simply use 11 inputs to produce wanted signals.

Due to regulations, the access time of the ROM Macro need to smaller than 5ns. The statistics of the access time in different corners are showed in the Table 1.Overall, the power supply is 1.8V and the macro size is 12355 um^2. We measure the power consumption and the delay time corresponding five corners at TT25°C, SF25°C, FS25°C, SS25°C and FF25°C respectively. Obviously, we statisfy the need.

TABLE I
THE STATISTICS OF MACRO

Process	180nm cmos
Macro size	12355 um
power_presim at TT25°C	586µw
power_postsim at TT25°C	945.7µw
access time_presim at TT25°C	2.576ns
access time_postsim at TT25°C	2.963ns
access time_presim at SF25°C	4.5316ns
access time_presim at FS25°C	2.267ns
access time_presim at SS25°C	3.392ns
access time_presim at FF25°C	2.628ns

A. The block diagram of ROM macro

The functional block diagram is shown in figure 1. Following function blocks contains : Timing control, Decoder, ROM, D flip-flop, Sense amplifier and additional output Latch.

(1)Timing Control: Making a pulse by differentiating the input into two inputs of a AND gate, one of which are connected to an inverter chain. While requiring two circuits above to make WL_EN and SA_EN, the adjustment of the delay and the width of the pulse results to the extra requirement of inverter chains.

(2)Decoders: Using a 6 to 64 decoder selects the rows of ROM and using two 8 to 1 mux selects the columns of ROM.That is, we can view the ROM as 1024-square division. Decoders choose a aquare from the ROM, which depends on the output of decoders.

(3)ROM: It contains datas which are setted in advance.

(4)MUX: Using two 8 to 1 mux selects the columns of ROM. Muxs are controlled by the 3 to 8 decoder.

(5)Sense Amplifier: Comparing the bit line voltage with Vref to sense the data.

(6)DFF: Sending the input A[8:0] to the X and Y decoder, which is controlled by the clock.

(7)Precharge: Precharge BL to VDD every cycle when clk is low level for avoiding read disturbs.

(8)Latch: Keep the output signal from sense amplifier to next CLK rising edge.

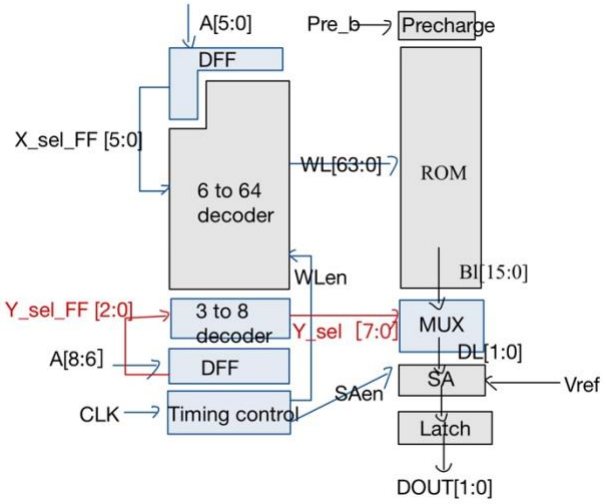


Fig. 1 ROM mcaro block diagram

B. schmaetics of each block

(1)Timing Control:

Total timing control circuit:

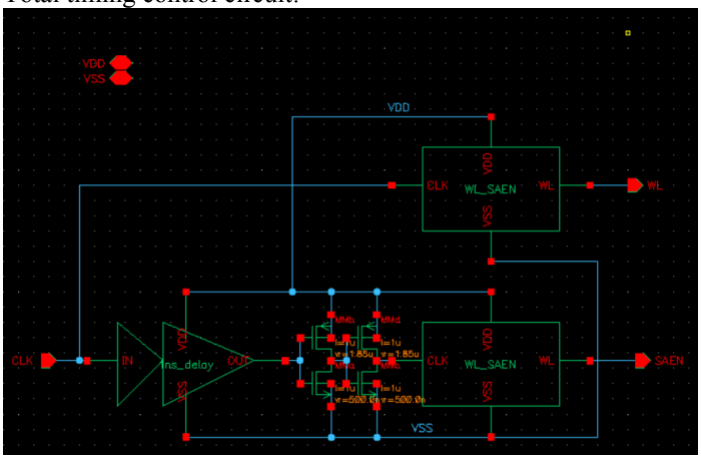


Fig. 2-1 Total timing control circuit

The WL_SAEN circuit

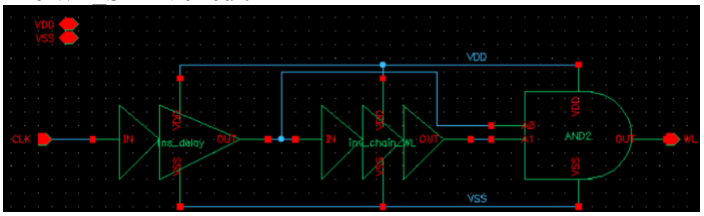


Fig. 2-2 The WL_SAEN circuit

Inverter chain in the WL_SAEN circuit:

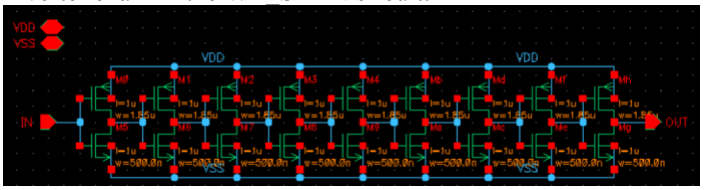


Fig. 2-3 Inverter chain in the WL_SAEN circuit

AND2:

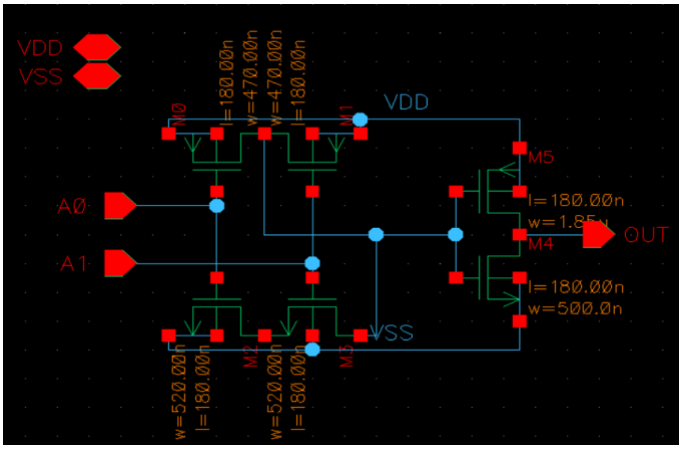
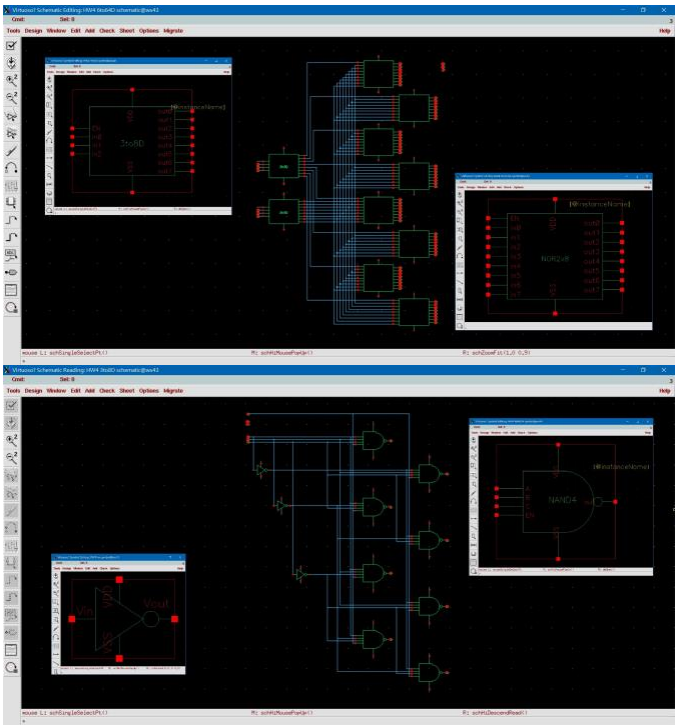


Fig. 2-4 AND2 gate

(2)Decoders:



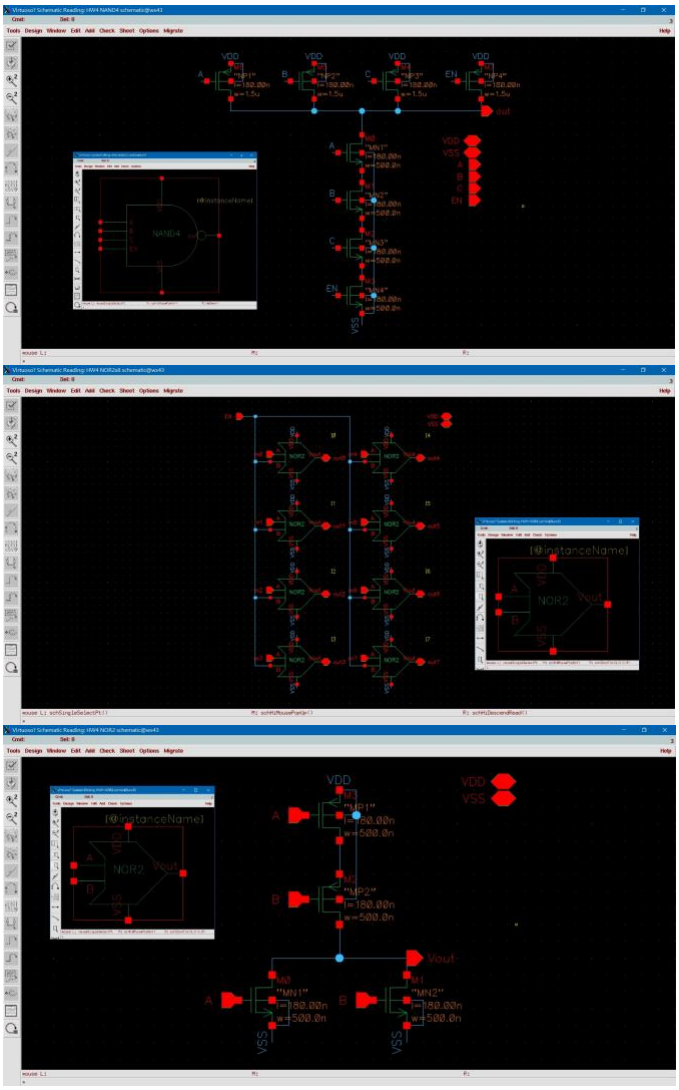


Fig. 2-5~2-9 Decoders

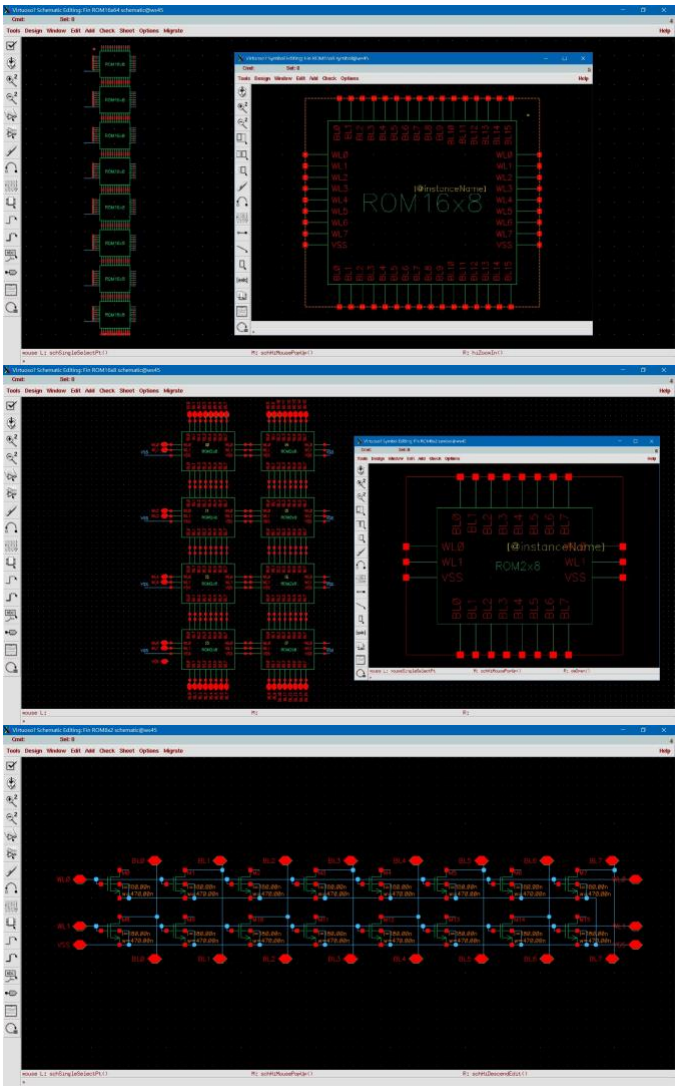
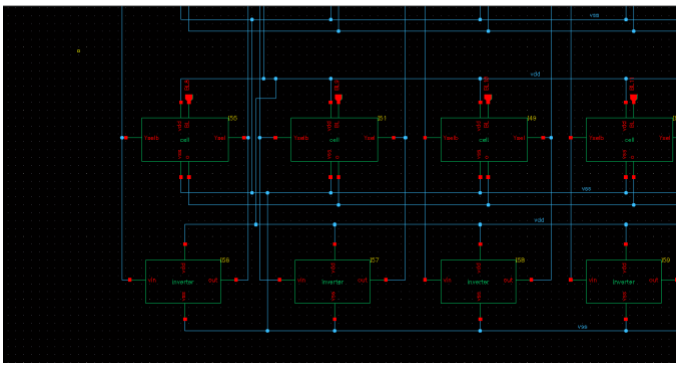


Fig. 2-10~2-12 ROM

(3)ROM:

(4)MUX:



cell:

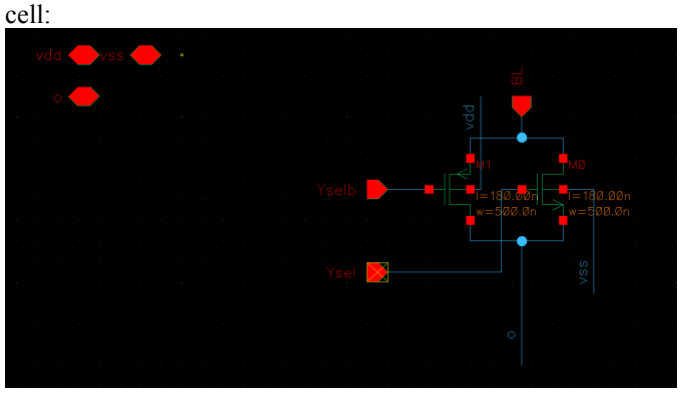


Fig. 2-13~2-14 MUX:

(5)Sense Amplifier:

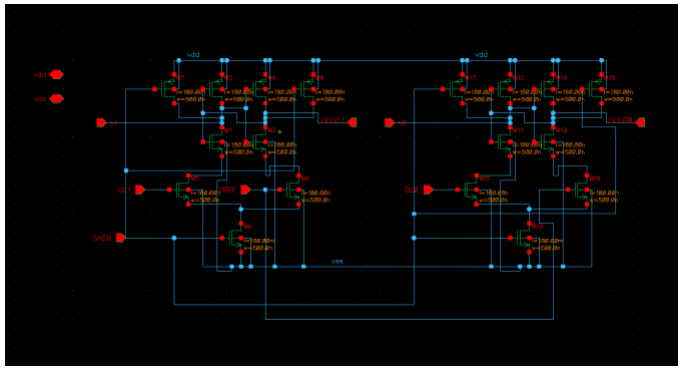


Fig. 2-15 Sense Amplifier

(6)DFF:

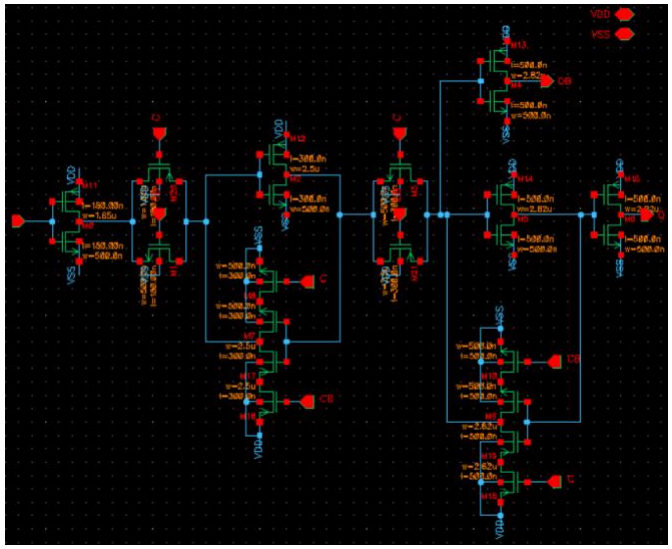


Fig. 2-16 DFF

(7)Precharge:

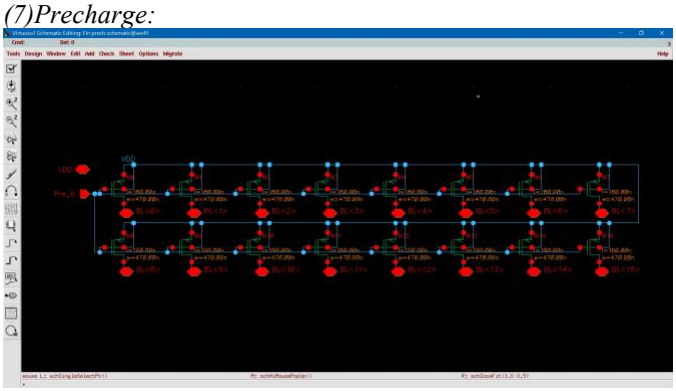


Fig. 2-17 Precharge

(8)Latch:

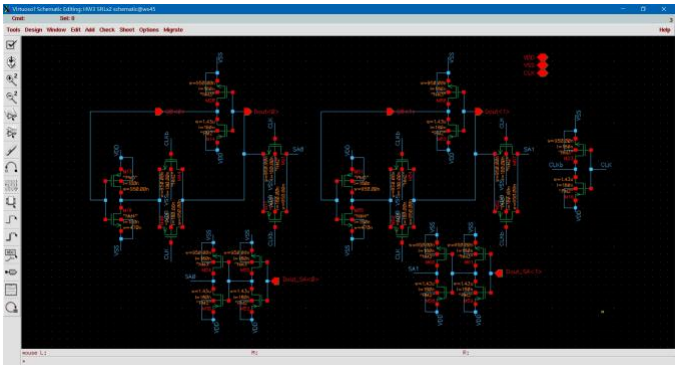


Fig. 2-18 Latch

However,we want to figure out the worst case so we need to run our circuits in different situations. Apparently, the worst case is in SS corner. Detailed statistics are showed in table2.

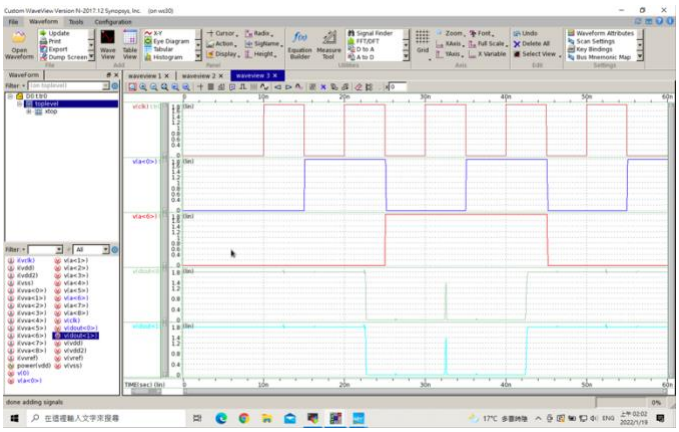


Fig. 3 The wavefrom of ROM mcaro in TT25°C

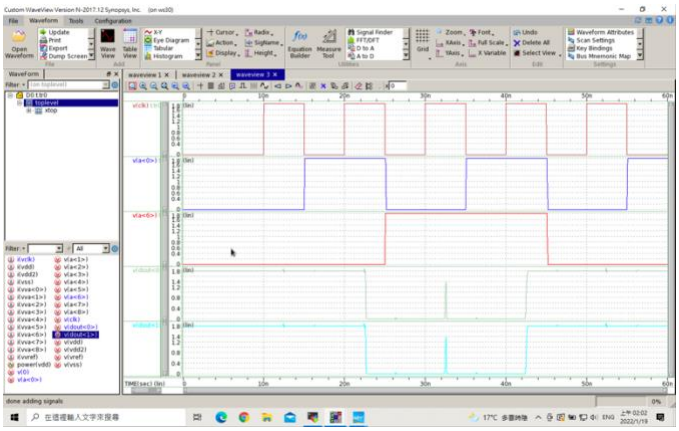


Fig. 3-1 The wavefrom of ROM mcaro in SS25°C

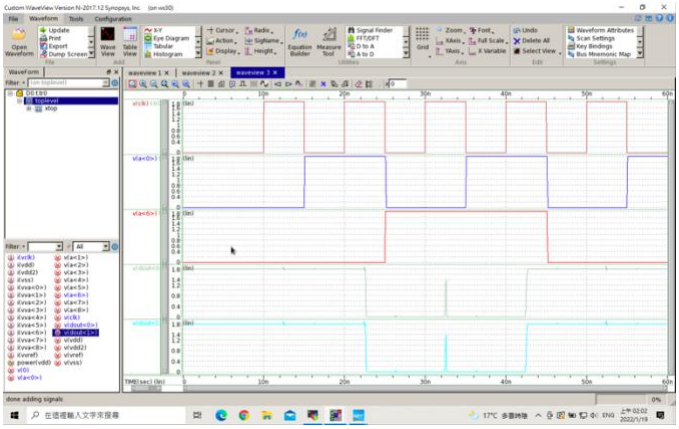


Fig. 3-2 The wavefrom of ROM mcaro in FF25°C

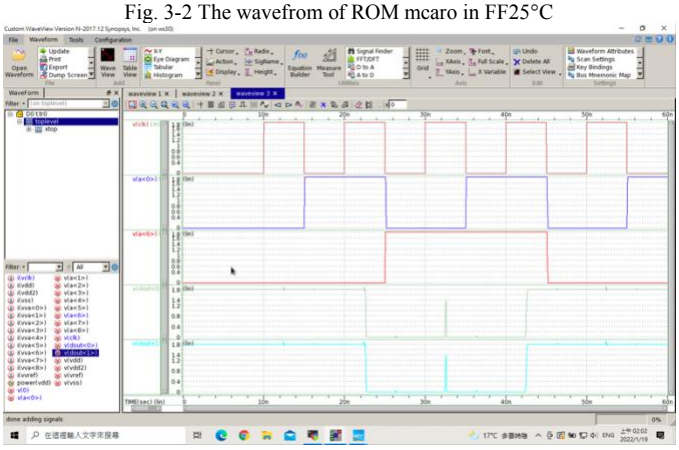


Fig. 3-3 The wavefrom of ROM mcaro in SF25°C

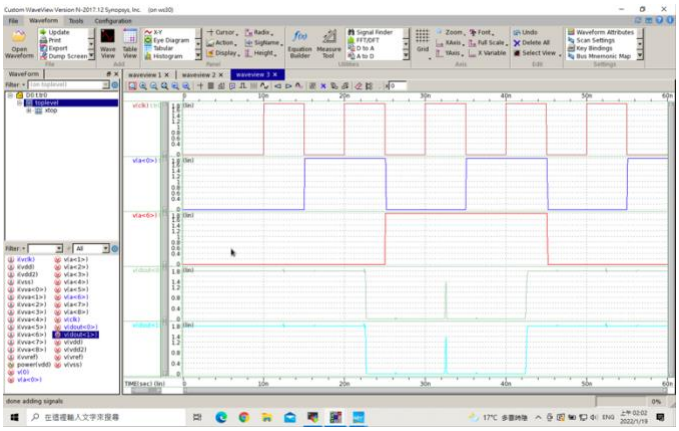


Fig. 3-4 The wavefrom of ROM mcaro in FS25°C

TABLE 2
THE STATISTCS OF MACRO

corners	average power	accees time
TT25°C	586μw	2.576ns
SS25°C	856.1μw	4.5316ns
FF25°C	612.94μw	2.267ns
SF25°C	719.7μw	3.392ns
FS25°C	578.9μw	2.628ns

II. IMPLEMENTATION

A. The layout of ROM macro

After running presim, we start to draw the layout of circuits. The figure4-1 is the completed layout.

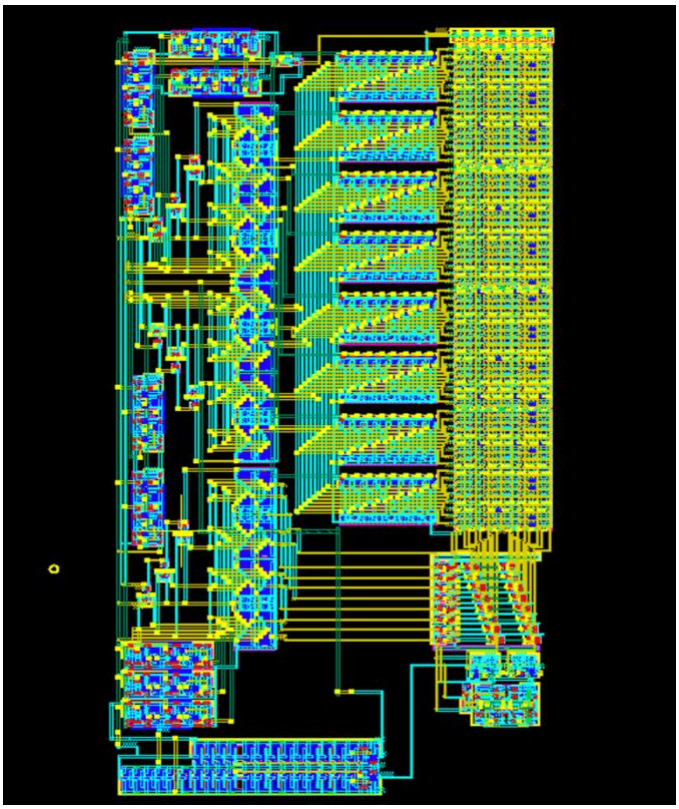


Fig. 4-1 The completed layout of ROM mcaro

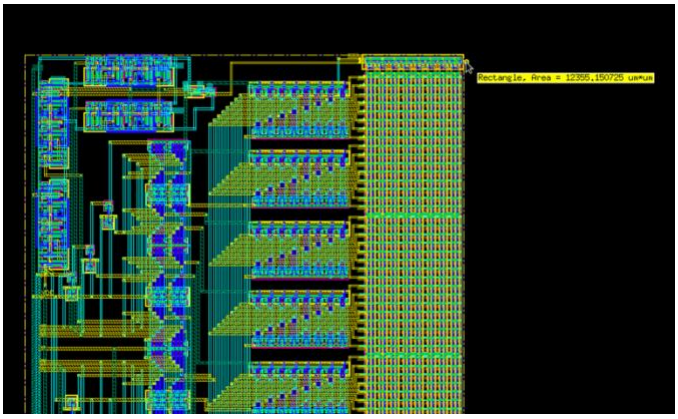


Fig. 4-2 The area of ROM mcaro

B. waveforms postsim in TT25°C

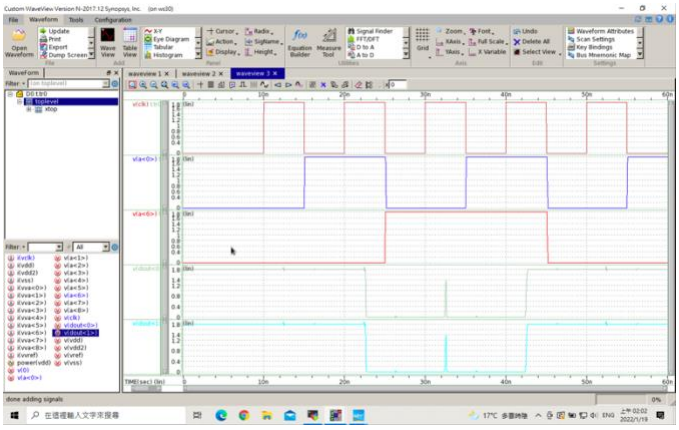


Fig. 5 The wavefrom of ROM mcaro in TT25°C

corners	average power	accees time
TT25°C	945.7μw	2.963ns

C. Compare the result of postsim with presim

The Average power or the access time, the statistics of postsim will bigger than presim. It makes sense because we use lots of metals when drawing the layout. Moreover, we can find that the waveform of presim is smooth than postsim. It is easy to understand because parasitic resistances and capacitances play a vital role in postsim.

IV. PROBIEMS HAVE CONQUERED

First of all, when we have to design the important part-Timing control, there are several problems such as the exactly delay time. If we does not choose proper sizes, the circuit will not work. As a result, the sizes of other parts are dertermined at first. Then, using unknown input signals such as wlen and saen perform to check whether the circuits will work or not.

The solution of the above problem is to adjust the length of inverter chain. However, when we do this, another problem has arisen. In TT corner, we can meet the spec but we can not meet in SS corner. It is because sense enable arrive sense amplifier earlier than data line, which leads to incorrect sensing. Therefore, we try to adjust the length of inverter chain to increase the delay of sense enable so that we can meet the spec.

REFERENCES

[1] *Yukiko Umemoto*, “28 nm 50% Power-Reducing Contacted Mask Read Only Memory Macro With 0.72-ns Read Access Time Using 2T Pair Bitcell and Dynamic Column Source Bias Control Technique” IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI)SYSTEMS, VOL. 22, NO. 3, MARCH 2014.