# EE3230 Introduction to Integrated Circuit Design, Fall 2021
# Final Project
### Due Date: 2022/01/18

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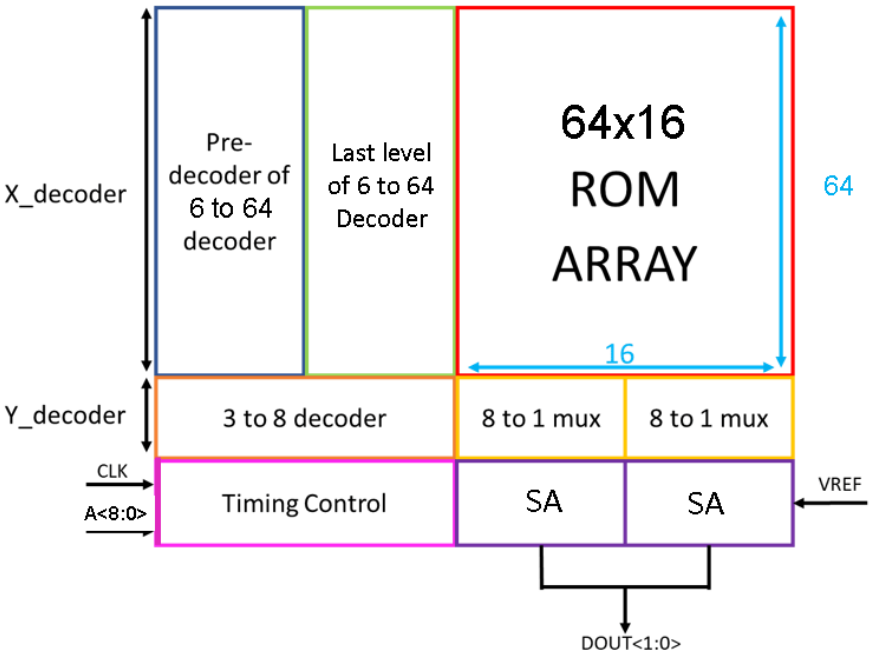
## Note

1. Do the simulation and analysis with cic018.l.
2. Power supply (VDD) = 1.8V.
3. Use .tran 1p XX for simulation

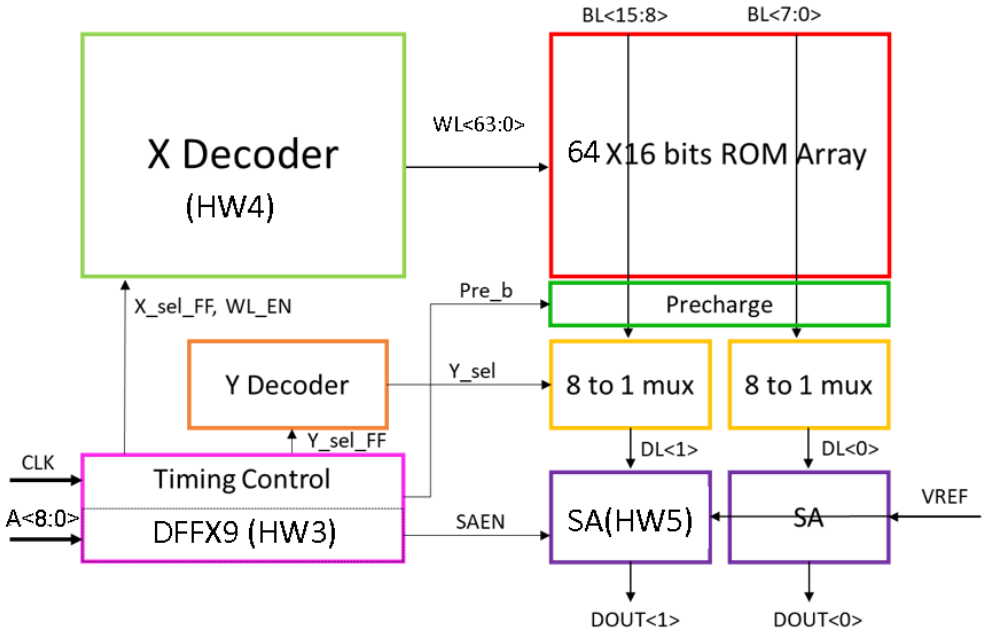
## Design Part

1. Please design a 1024 bits ROM macro with access time < 5ns, described as follows: **(40%)**
   A. 11-bit input: A<8:0>, CLK (100MHz, rise/fall time = 0.01ns), VREF.
   B. 2-bit output: DOUT<1:0> (Output loading is neglected)
   C. Pre-sim: TT25℃, SS25℃, FF25℃, SF25℃, FS25℃
   D. Post-sim: TT25℃
2. Print out your schematic and simulation waveforms with **5 corners**. Waveforms should show at least 2 cycles including read 0 and read 1, measure the average power and access time. **(10%)**
3. Complete the layout of your ROM macro and measure its area. **(30%)**
4. Run post-sim (with R-C-CC extraction) **at TT 25**℃, compare the result and waveform with pre-sim. **(10%)**
5. Fill in the google sheet with your post-simulation **at TT 25**℃ for ranking. **($FOM = access\ time^2 * power * area$)**
   *(access time^2*power) in FOM is also known as EDP(energy-delay product)
6. Describe how you design each block of the ROM macro. **(10%)**

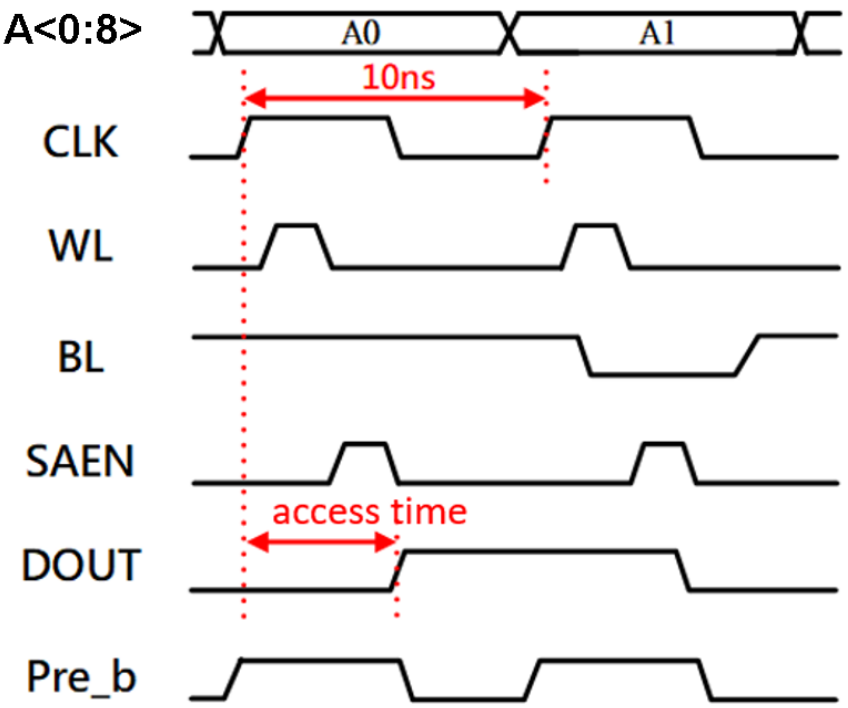
## Block Diagram Example



## Detail Block Diagram



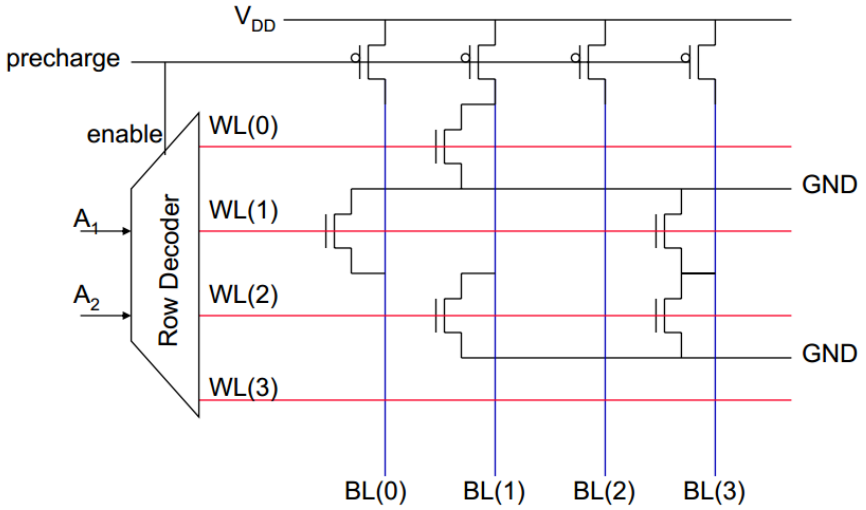

## Example Waveform



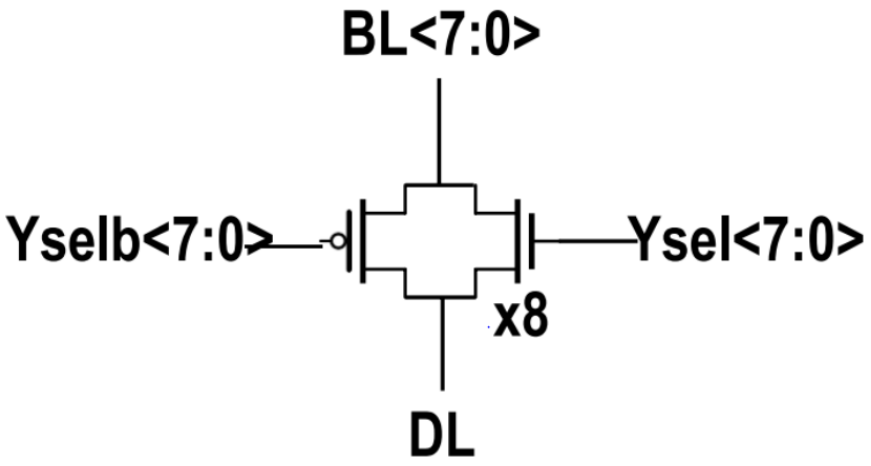
## Attached Information

1. ROM array (NOR Type ROM):

*ROM gds is attached in HW3. You should construct the schematic of ROM array by yourself.




2. YMUX_8_to_1: Select one of eight BLs and send it to the sense amplifier.




3. DFF: HW3
4. X_decoder: HW4
5. Sense amplifier: HW5
6. Timing Control: Use combinational logics to generate timing control signals SAEN, Pre_b, and WL_EN.

*You can redesign any circuit to get a better FOM except ROM array.

## Bonus ($access\ time^2 * power * area$)

1 st (10%)

2 nd ~ 10th (8%)

11th ~ 20th (5%)

21 th ~ 40 th (3%)

Note: The less, the better.

## Submission

1. IEEE format report (Final_TeamXX.pdf)
2. Hspice files (.sp/.spi)
3. Gds file (.gds)