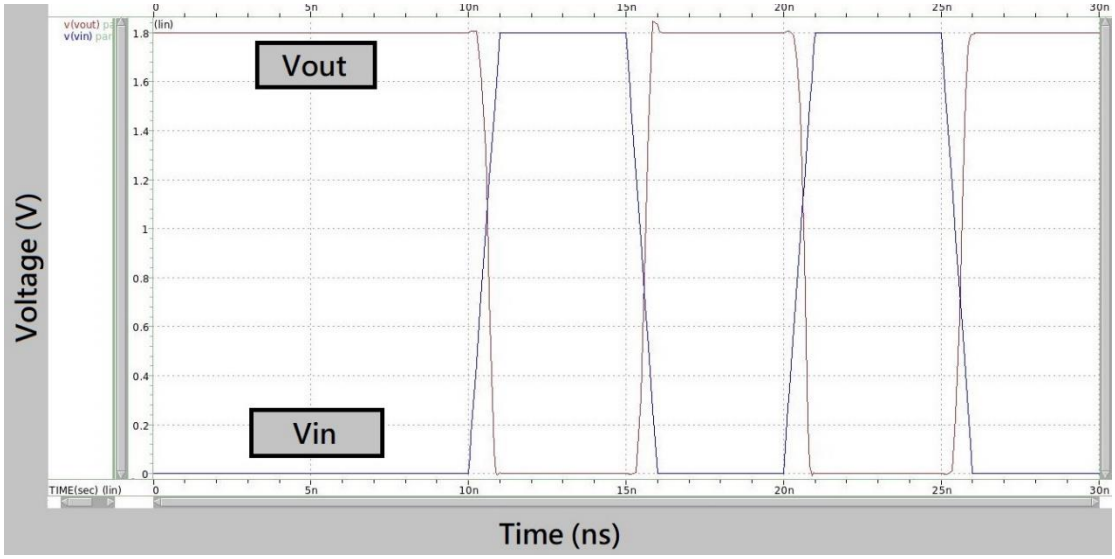
Homework #1

108061127 電機 23 許澤群

Part I

(1)

	NMOS	PMOS
W/L(μm/μm)	3μm/0.18μm	8.3626μm/0.18μm
M	1	1




```
****** transient analysis tnom=  25.000 temp=  25.000 ******
pwr=  61.6565u  from=  20.0000n     to=  30.0000n
tphl= 138.5298p  targ=  10.6385n   trig=  10.5000n
tplh= 114.6077p  targ=  15.6146n   trig=  15.5000n
```

Power consumption $=$ $61.6565(\mu W)$ in cycle between 20ns and 30ns

Delay $= (t_{pHL} + t_{pLH})/2 = 126.569(ps)$

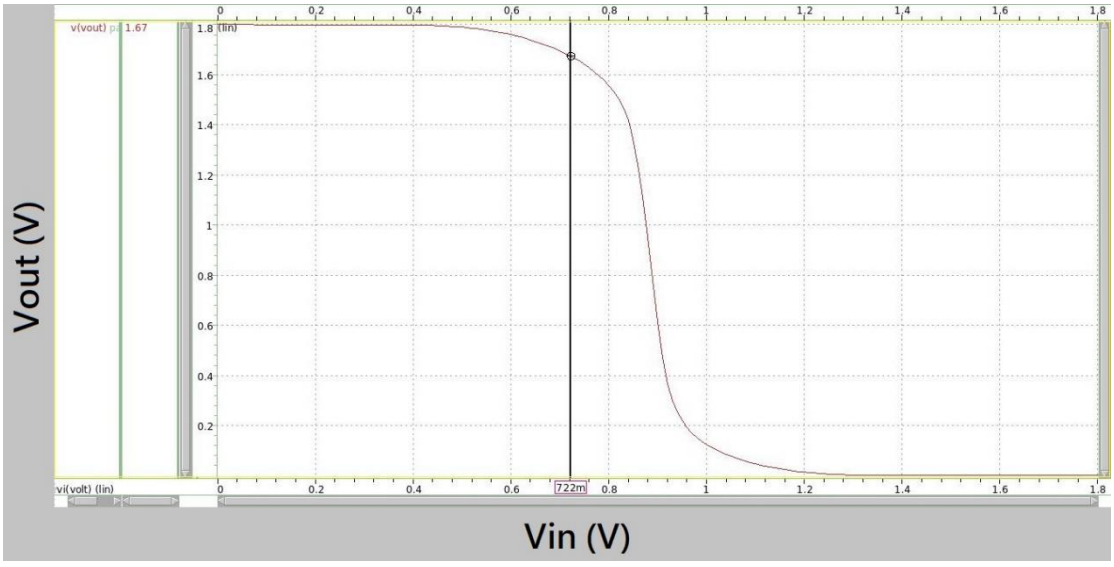
FoM$= 61.6565 \times 126.569 = 7803.8015(\mu W \times ps)$

(2)

Table 1

Corner	Temp (°C)	N_width (μm)	P_width (μm)	Power (μW)	Delay (ps)	FoM (μW×ps)
SS	-40	3	10.503	44.0447	239.249	10537.6
	25	3	8.9448	47.1051	239.516	11282.4
	120	3	7.4616	42.2985	272.758	11537.2
SF	-40	3	2.9425	39.7644	179.245	7127.57
	25	3	2.5229	44.1831	250.941	11087.3
	120	3	2.1168	39.2698	234.059	9191.45
TT	-40	3	9.32	59.435	141.462	8407.78
	25	3	8.3626	61.6565	126.569	7803.79
	120	3	7.3194	65.8523	165.864	10922.5
FS	-40	3	6.9204	52.1039	148.735	7749.65
	25	3	6.2791	56.4882	141.467	7991.21
	120	3	5.5612	55.3169	183.003	10123.2
FF	-40	3	8.8174	79.0178	117.813	9309.35
	25	3	7.9783	65.4281	130.714	8552.39
	120	3	7.0353	70.4523	148.347	10451.4

(3)



```
****** dc transfer curves tnom=  25.000 temp=  25.000 ******
vil= 722.3631m
vol=   1.6747
vih=   1.0253
voh=  98.1945m
```

$$V_{IL} = 0.7223(V) \qquad V_{OL} = 1.6747(V)$$
$$V_{IH} = 1.0253(V) \qquad V_{OH} = 0.0981(V)$$
$$NM_L = V_{IL} - V_{OL} = -0.9524(V)$$
$$NM_H = V_{OH} - V_{IH} = -0.9272(V)$$

(4)

(a) Effects of different temperature in the same corner

For the width of PMOS, it is negatively correlated to the temperature. Since the drain current I_D is reduced as the temperature increases, a longer width of MOS is required to remain the drain current to reach the balanced trigger point.

For the power consumption, we can observe that the largest powers are operated under 25℃ in SS, FS and FS corner, while under 120℃ in TT corner and under -40℃ in FF corner.

For the delay, it is smaller under -40℃ than under 120℃ in each corner. And the smallest delay is under 25℃ in TT corner.

For the FoM, it is smaller under -40℃ than under 120℃ in each corner. And the smallest FoM is under 25℃ in TT corner. The result is highly related to the result of delay.

(b) Effects of different corner under the same temperature

For the width of PMOS, it is much shorter in SF corner and a little shorter in FS corner than in the other corners, while they are closely in the range of 7μm to 10μm in TT, SS, FF corner.

For the power consumption, we can observe that the order from large to small is FF, TT, FS, SS, SF.

For the delay, consider the time delay from high to low and low to high. We can observe that t_{pHL} is smaller when NMOS is operated in fast corner such as FS and FF. Since the carrier mobilities are higher than normal in fast corner, the delay is negatively correlated to the speed of NMOS.

For the FoM, we can observe in average they are a little smaller in SF, TT, FS corner than in SS and FF corner.

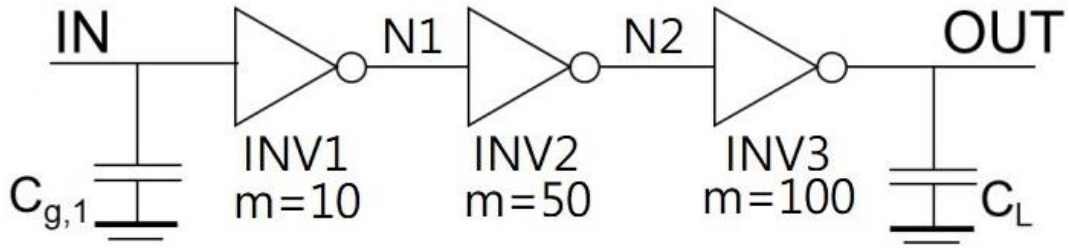
Part II

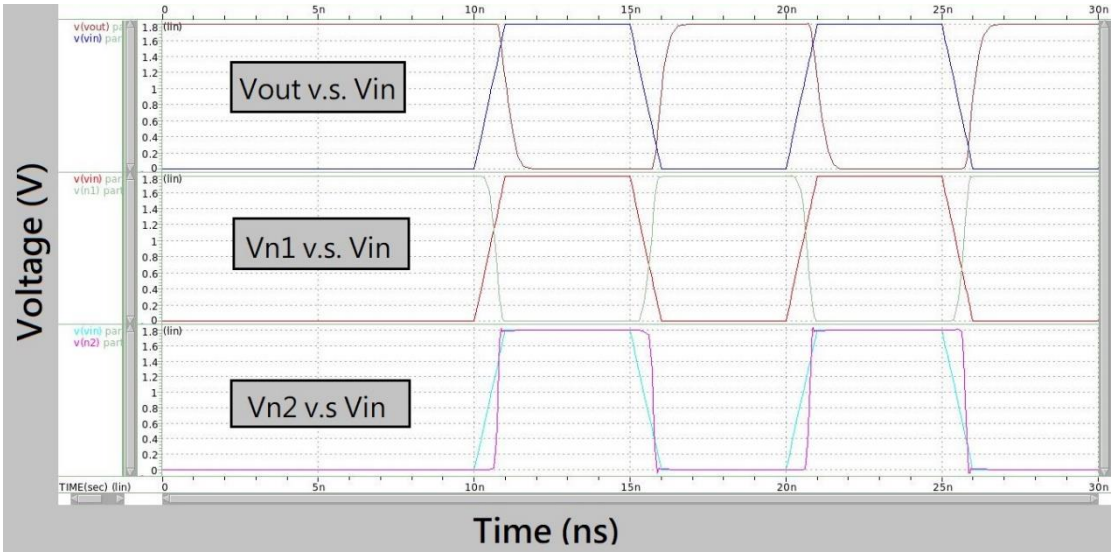
(1)

PMOS_width= 1.8461(μm)

$C_{g,1} = 0.1(pF)$

$N = \log_4(C_L/C_{g,1}) = 3.32 \rightarrow 3$






```
****** transient analysis tnom=  25.000 temp=  25.000 ******
tphl_vout= 571.1040p  targ=  11.0711n   trig=  10.5000n
tplh_vout= 489.2667p  targ=  15.9893n   trig=  15.5000n
tphl_n1= 178.0127p  targ=  10.6780n   trig=  10.5000n
tplh_n1= 161.9512p  targ=  15.6620n   trig=  15.5000n
tpll_n2= 256.0388p  targ=  10.7560n   trig=  10.5000n
tphh_n2= 245.1365p  targ=  15.7451n   trig=  15.5000n
```

Delay of Vout= 530.1838(ps)

Delay of node 1= 169.9819(ps)

Delay of node 2= 250.5876(ps)

(2)

Table 2

Corner	Temp (°C)	Delay (ns)
SS	-40	0.99703315
	25	1.10061885
	120	1.26995
SF	-40	0.71582025
	25	0.7882511
	120	0.92565045
TT	-40	0.50300405
	25	0.53018535
	120	0.59117265
FS	-40	0.50600155
	25	0.54659975
	120	0.6074559
FF	-40	0.42962195
	25	0.459573
	120	0.4973746

First, discuss the effects of different temperature in the same corner. We can observe that the delay is positively correlated to the temperature. Since the leakage current increased as the temperature rises, which may result in slowly voltage change and large delay.

Second, discuss the effects of different corner under the same temperature. We can observe that the delays in SS and SF corner is much larger than in the other corners. Since the carrier mobilities are lower than normal in slow corner, the delay will be large.