APPENDIX D

VERSAbus BACKPLANE EDGE CONNECTOR J1
AND
VERSAboard EDGE CONNECTOR P1
IDENTIFICATION

INTRODUCTION

This appendix identifies the VERSAbus backplane edge connector J1/P1 pin assignments. The following table lists the pin assignments by pin number order.

J1/P1 Pin Assignments

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
1	+5V	2	+5V
3	GND	4	GND
5	D00*	6	D01*
7	D02*	8	D03*
9	D04*	10	D05*
11	D06*	12	D07*
13	D08*	14	D09*
15	D10*	16	D11*
17	D12*	18	D13*
19	D14*	20	D15*
21	DPARITY0*	22	DPARITY1*
23	GND	24	GND
25	DS0*	26	DS1*
27	GND	28	GND
29	DTACK*	30	AS*
31	GND	32	GND
33	APARITY0*	34	WRITE*
35	LWORD*	36	A01*
37	A02*	38	A03*
39	A04*	40	A05*
41	A06*	42	A07*
43	A08*	44	A09*
45	A10*	46	A11*
47	A12*	48	A13*
49	A14*	50	A15*
51	A16*	52	A17*
53	A18*	54	A19*
55	A20*	56	A21*
57	A22*	58	A23*
59	AM4*	60	AM7*
61	GND	62	GND
63	AM3*	64	[RESERVED]
65	TEST0*	66	[RESERVED]

J1/P1 Pin Assignments (cont'd)

ODD PIN NUMBER (P1 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P1 SOLDER SIDE)	SIGNAL MNEMONIC
67	GND	68	GND
69	ACCLK	70	SYSCLK
71	GND	72	GND
73	[RESERVED]	74	SYSRESET*
75	[RESERVED]	76	[RESERVED]
77	[RESERVED]	78	ACFAIL*
79	TEST1*	80	SYSFAIL*
81	BERR*	82	[RESERVED]
83	AM0*	84	AM1*
85	AM2*	86	AM6*
87	IRQ1*	88	IRQ2*
89	IRQ3*	90	IRQ4*
91	IRQ5*	92	IRQ6*
93	IRQ7*	94	AM5*
95	ACKIN*	96	ACKOUT*
97	BGOIN*	98	BGOOUT*
99	BG1IN*	100	BG1OUT*
101	BG2IN*	102	BG2OUT*
103	BG3IN*	104	BG3OUT*
105	BG4IN*	106	BG4OUT*
107	BRO*	108	BR1*
109	BR2*	110	BR3*
111	BR4*	112	BBSY*
113	BCLR*	114	BREL*
115	[RESERVED]	116	[RESERVED]
117	APVAL*	118	DPVAL*
119	GND	120	GND
121	-12V	122	-12V
123	GND	124	GND
125	+12V	126	+12V
127	+12V	128	+12V
129	+5V	130	+5V
131	+5V	132	+5V
133	+5V STDBY	134	+5V STDBY
135	GND	136	GND
137	GND	138	GND
139	GND	140	GND

APPENDIX E

VERSAbus BACKPLANE EDGE CONNECTOR J2
AND
VERSAboard EDGE CONNECTOR P2
IDENTIFICATION

INTRODUCTION

This appendix identifies the VERSAbus backplane edge connector J2 pin assignments. Table 1 lists the J2/P2 pin assignments by pin number order for the expanded bus option. Table 2 lists the J2/P2 pin assignments for the non-expanded bus option.

TABLE 1. J2/P2 Pin Assignments for the Expanded Bus Option

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND ($\pm$ 15V)	14	GND ($\pm$ 15V)
15	-12V	16	-12V
17	[I/O PIN]	18	[I/O PIN]
19	[I/O PIN]	20	[I/O PIN]
21	[I/O PIN]	22	[I/O PIN]
23	[I/O PIN]	24	[I/O PIN]
25	[I/O PIN]	26	[I/O PIN]
27	[I/O PIN]	28	[I/O PIN]
29	[I/O PIN]	30	[I/O PIN]
31	[I/O PIN]	32	[I/O PIN]
33	[I/O PIN]	34	[I/O PIN]
35	[I/O PIN]	36	[I/O PIN]
37	[I/O PIN]	38	[I/O PIN]
39	[I/O PIN]	40	[I/O PIN]
41	[I/O PIN]	42	[I/O PIN]
43	[I/O PIN]	44	[I/O PIN]
45	[I/O PIN]	46	[I/O PIN]
47	[I/O PIN]	48	[I/O PIN]
49	[I/O PIN]	50	[I/O PIN]
51	[I/O PIN]	52	[I/O PIN]
53	[I/O PIN]	54	[I/O PIN]
55	[I/O PIN]	56	[I/O PIN]
57	[I/O PIN]	58	[I/O PIN]
59	[I/O PIN]	60	[I/O PIN]

TABLE 1. J2/P2 Pin Assignments for the Expanded Bus Option (cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
61	[I/O PIN]	62	[I/O PIN]
63	[I/O PIN]	64	[I/O PIN]
65	[I/O PIN]	66	[I/O PIN]
67	-15V	68	-15V
69	+15V	70	+15V
71	[RESERVED]	72	[RESERVED]
73	[RESERVED]	74	[RESERVED]
75	[RESERVED]	76	[RESERVED]
77	[RESERVED]	78	[RESERVED]
79	[RESERVED]	80	[RESERVED]
81	[RESERVED]	82	[RESERVED]
83	[RESERVED]	84	[RESERVED]
85	[RESERVED]	86	[RESERVED]
87	[RESERVED]	88	APARITY1*
89	A24*	90	A25*
91	A26*	92	A27*
93	A28*	94	A29*
95	A30*	96	A31*
97	GND	98	GND
99	[RESERVED]	100	[RESERVED]
101	GND	102	GND
103	DPARITY2*	104	DPARITY3*
105	D16*	106	D17*
107	D18*	108	D19*
109	D20*	110	D21*
111	D22*	112	D23*
113	D24*	114	D25*
115	D26*	116	D27*
117	D28*	118	D29*
119	D30*	120	D31*

NOTE: Pins 17 through 66 are not bussed together by the backplane.

TABLE 2. J2/P2 Pin Assignments for the Non-Expanded Bus Option

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
1	GND	2	GND
3	GND	4	GND
5	GND	6	GND
7	+5V	8	+5V
9	+5V	10	+5V
11	+12V	12	+12V
13	GND (± 15V)	14	GND (± 15V)
15	-12V	16	-12V
17	[I/O PIN]	18	[I/O PIN]
19	[I/O PIN]	20	[I/O PIN]
21	[I/O PIN]	22	[I/O PIN]
23	[I/O PIN]	24	[I/O PIN]
25	[I/O PIN]	26	[I/O PIN]
27	[I/O PIN]	28	[I/O PIN]
29	[I/O PIN]	30	[I/O PIN]
31	[I/O PIN]	32	[I/O PIN]
33	[I/O PIN]	34	[I/O PIN]
35	[I/O PIN]	36	[I/O PIN]
37	[I/O PIN]	38	[I/O PIN]
39	[I/O PIN]	40	[I/O PIN]
41	[I/O PIN]	42	[I/O PIN]
43	[I/O PIN]	44	[I/O PIN]
45	[I/O PIN]	46	[I/O PIN]
47	[I/O PIN]	48	[I/O PIN]
49	[I/O PIN]	50	[I/O PIN]
51	[I/O PIN]	52	[I/O PIN]
53	[I/O PIN]	54	[I/O PIN]
55	[I/O PIN]	56	[I/O PIN]
57	[I/O PIN]	58	[I/O PIN]
59	[I/O PIN]	60	[I/O PIN]
61	[I/O PIN]	62	[I/O PIN]
63	[I/O PIN]	64	[I/O PIN]
65	[I/O PIN]	66	[I/O PIN]
67	-15V	68	-15V
69	+15V	70	+15V
71	[I/O PIN]	72	[I/O PIN]
73	[I/O PIN]	74	[I/O PIN]
75	[I/O PIN]	76	[I/O PIN]
77	[I/O PIN]	78	[I/O PIN]
79	[I/O PIN]	80	[I/O PIN]
81	[I/O PIN]	82	[I/O PIN]
83	[I/O PIN]	84	[I/O PIN]
85	[I/O PIN]	86	[I/O PIN]
87	[I/O PIN]	88	[I/O PIN]
89	[I/O PIN]	90	[I/O PIN]
91	[I/O PIN]	92	[I/O PIN]
93	[I/O PIN]	94	[I/O PIN]
95	[I/O PIN]	96	[I/O PIN]

TABLE 2. J2/P2 Pin Assignments for the Non-Expanded Bus Option (cont'd)

ODD PIN NUMBER (P2 COMPONENT SIDE)	SIGNAL MNEMONIC	EVEN PIN NUMBER (P2 SOLDER SIDE)	SIGNAL MNEMONIC
97	[I/O PIN]	98	[I/O PIN]
99	[I/O PIN]	100	[I/O PIN]
101	[I/O PIN]	102	[I/O PIN]
103	[I/O PIN]	104	[I/O PIN]
105	[I/O PIN]	106	[I/O PIN]
107	[I/O PIN]	108	[I/O PIN]
109	[I/O PIN]	110	[I/O PIN]
111	[I/O PIN]	112	[I/O PIN]
113	[I/O PIN]	114	[I/O PIN]
115	[I/O PIN]	116	[I/O PIN]
117	[I/O PIN]	118	[I/O PIN]
119	[I/O PIN]	120	[I/O PIN]

NOTE: Pins 17 through 66 and pins 71 through 120 are not bussed together by the backplane.