WEITEK

INNOVATIONS IN MICROSYSTEM TECHNOLOGY

WTL1032 High-Speed 32-Bit IEEE Floating Point Multiplier
WTL1033 High-Speed 32-Bit IEEE Floating Point ALU

WTL 1032/1033
HIGH-SPEED 32-BIT IEEE FLOATING-POINT MULTIPLIER/ALU

Features

- A complete floating-point arithmetic solution for high-speed processors
- Full 32-bit floating-point conforming to the new IEEE Standard 754
- High Speed
  - 5 MEGAFLOPS in three stage pipeline mode
  - 1.1 MEGAFLOPS in low latency flowthrough mode
- Low power NMOS - 1.5 watts typical
- Fast
  - Two 16-bit data input and one data output operation every 100ns
  - Pipeline mode provides full 32 bit throughput every 200ns for ALU and Multiplier vector operation
  - Flowthrough mode provides full 32 bit delay time of 900ns for ALU and Multiplier scalar operation
- Full function
  - Add
  - Subtract
  - Multiply
  - Conversion to and from 24-bit fixed-point
  - Absolute value
- Flexible control interface
  - Single edge-trigger clock
  - Function control is included in three stage pipeline — no wasted cycles when changing function
  - Fully registered inputs and outputs with separate load and unload controls
  - Three-state TTL outputs with high drive capability
- Standard 64-pin DIP and 68-pin leadless packages with common pin-out for both ALU and multiplier

Description

The WTL1032 Multiplier and WTL1033 Arithmetic Logic Unit are designed to provide the essential 32-bit floating-point data path elements for high-speed processors. Their MOS VLSI design allows all of the functional elements to be combined on two low power chips, yet careful choice of input/output paths and flexible control signals permit their meeting the needs of a wide variety of applications.

The data format for the floating-point numbers conforms to the widely accepted IEEE Standard 754 including all rounding modes, infinity representations and treatment of exceptions such as underflow. This assures that systems can be built easily that will have the same numerical performance as much larger systems, providing complete software portability. Yet a fast mode of operation is included which removes the time penalty of underflow exception handling by zero substitution while retaining all other benefits of this high dynamic range format.

The arithmetic processing is inherently fast because of the state-of-the-art NMOS technology, both multiplier and ALU array times being under 600ns. This includes all denormalization, renormalization and exponent adjustments. Where even higher speeds are necessary, the array can be divided into 3 stages separated by pipeline registers. Thus, new operands can be entered and results removed every 200ns. This tripling of speed comes with only a small, one cycle increase in delay and no penalty in changing functions since the array instructions are pipelined also.

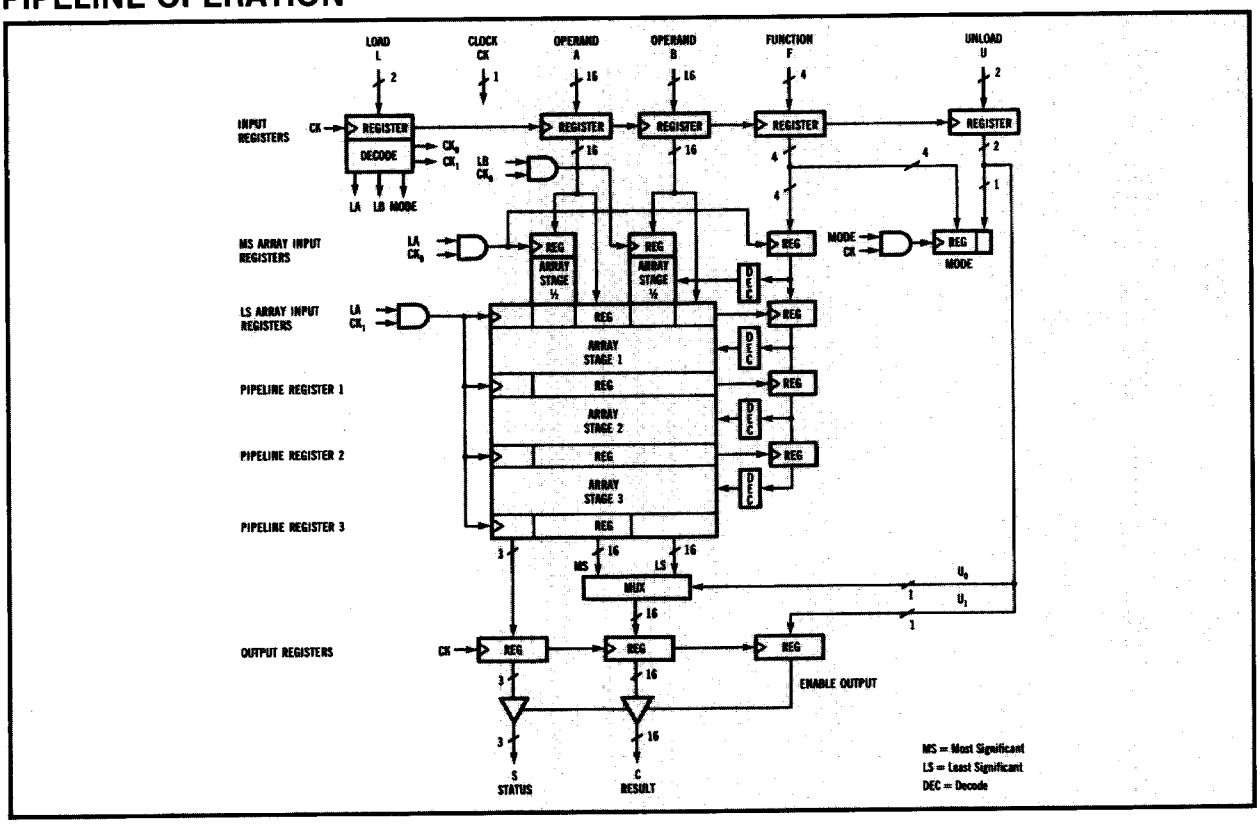
Data inputs and output transfer at twice the pipeline rate assuring that both 32-bit operands and the one result are not slowed getting on and off the chip through 16-bit busses. One operand can be stored internally, reducing external input bus transfers by two when repeated operations are performed with one constant. As shown in the block diagram, all inputs and outputs are registered. All are loaded on each positive going transition of the CLOCK. Transfers from input registers to the ALU or multiplier array and the MODE register are accomplished with LOAD instructions. UNLOAD instructions transfer from the array to the output registers and enable their outputs.

The MODE register determines the seldom changed options of the array and it is loaded through the FUNCTION and UNLOAD input registers. A MODE instruction can configure the array with the three pipeline registers as shown in the second block diagram.

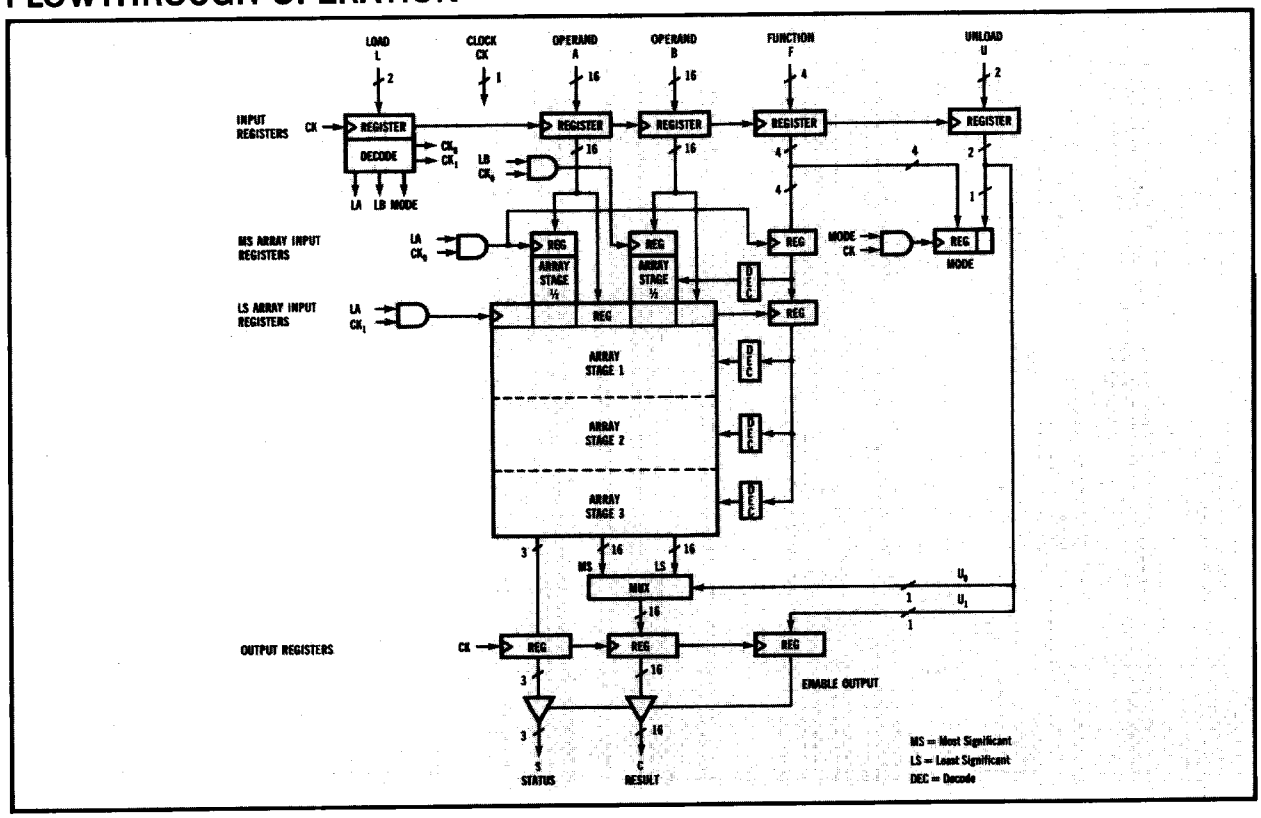
The arithmetic operation of the array is determined by the four-bit FUNCTION instruction which is transferred in with the operands. Three bits of STATUS record exception conditions in the array and they are output with the pertinent result. Input instructions and output status propagate with the applicable data for ease of design and programming. Timing diagrams show these relationships for both the pipeline and flow-through configuration of the array. Transfers proceed in a natural order of most significant 16-bit word on the first CLOCK (CK_0) and least significant on the second CLOCK (CK_1).

Block Diagrams

PIPELINE OPERATION



FLOWTHROUGH OPERATION



Specifications

Absolute Maximum Ratings (Above Which The Useful Life May Be Impaired)

Supply voltage ..... – 0.5 to 7.0V
Input voltage ..... – 0.5 to 5.5V
Output voltage ..... – 0.5 to 5.5V
Operating temperature range (T_{case}) .... – 55 °C to 125 °C
Storage temperature range ..... – 65 °C to 150 °C
Lead temperature
(10 seconds) ..... 300 °C
Junction temperature ..... 175 °C

Recommended Operating Conditions

PARAMETER	COMMERCIAL			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5.0	5.25	V
Operating temperature, $t_{Ambient}$	0		70	°C

DC Electrical Characteristics Over Recommended Temperature Range

(Except As Otherwise Noted)

PARAMETER	TEST CONDITIONS	COMMERCIAL			UNIT
		MIN	TYP*	MAX	
V_{IH} High-level input voltage	V_{CC} = MIN	2.4			V
V_{IL} Low-level input voltage	V_{CC} = MIN			0.8	V
V_{OH} High-level output voltage	V_{CC} = MIN, I_{OH} = – 1.0mA	2.8			V
V_{OL} Low-level output voltage	V_{CC} = MIN, I_{OL} = 5.0mA			0.4	V
I_{LI} Input leakage current	V_{CC} = MAX, V_{IN} = 0 – V_{CC}			10	μA
I_{LO} Output leakage current (output disabled)	V_{CC} = MAX, V_{OUT} = 0 – V_{CC}			10	μA
C_{IN} Input capacitance	V_{CC} = MAX, V_{IN} = 0 – V_{CC}			4	pF
C_{OUT} Output capacitance (output disabled)	V_{CC} = MAX, V_{OUT} = 0 – V_{CC}			8	pF
I_{CC} Supply current					
WTL1032 Floating Point Multiplier	V_{CC} = MAX		300	400	mA
WTL1033 Floating Point ALU	V_{CC} = MAX		300	400	mA

* T_A = 25 °C, V_{CC} = NOM

AC Electrical Characteristics Over Recommended Temperature Range

PARAMETER	TEST CONDITIONS (for all parameters)	COMMERCIAL			UNIT
		MIN	TYP*	MAX	
See Figure 1					
Clock cycle time, t_{CY}	V_{CC} = MIN	100		DC	nsec
Clock high time, t_{CH}	V_{IH} = 2.4V	40		DC	nsec
Clock low time, t_{CL}	V_{IL} = 0.8V	40		DC	nsec
Input setup time, t_S	V_{OH} = 2.8V, I_{OH} = – 1.0mA			35	nsec
Input hold time, t_H	V_{OL} = 0.4V, I_{OL} = 5.0mA	0			nsec
Output delay time, t_{DO}	C_{LOAD} = 40pF			50	nsec
Output valid time, t_{VO}		10			nsec
See Figure 2					
Flowthrough operation time, t_{OP}					
WTL1032 Floating Point Multiplier				600	nsec
WTL1033 Floating Point ALU				600	nsec
Total Latency, t_{LA}				900	nsec
See Figure 3					
Pipelined operation time per stage, t_{OP}					
WTL1032 Floating Point Multiplier				200	nsec
WTL1033 Floating Point ALU				200	nsec
Total Latency, t_{LA}				1100	nsec

* T_A = 25 °C, V_{CC} = NOM

Figure 1. Inputs and Output Timing

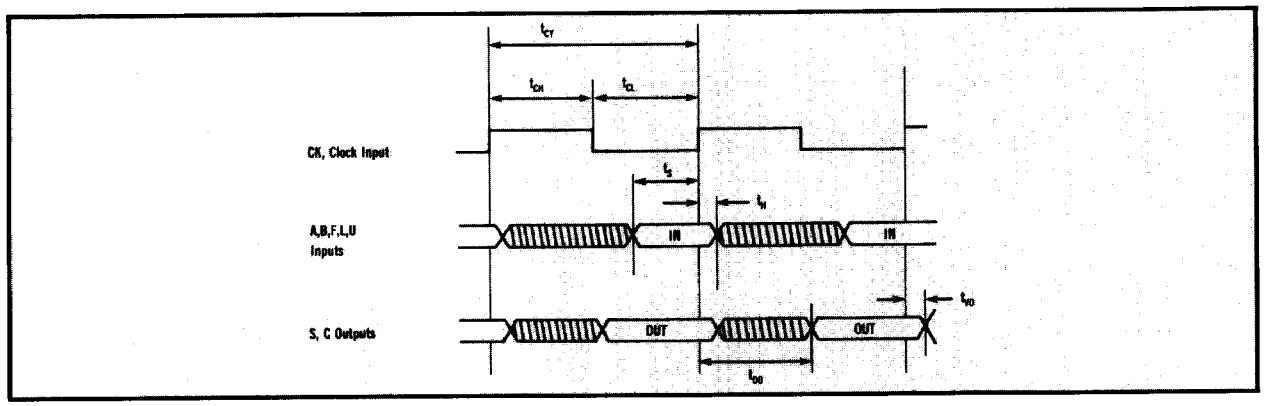


Figure 2. Flowthrough Operation Timing

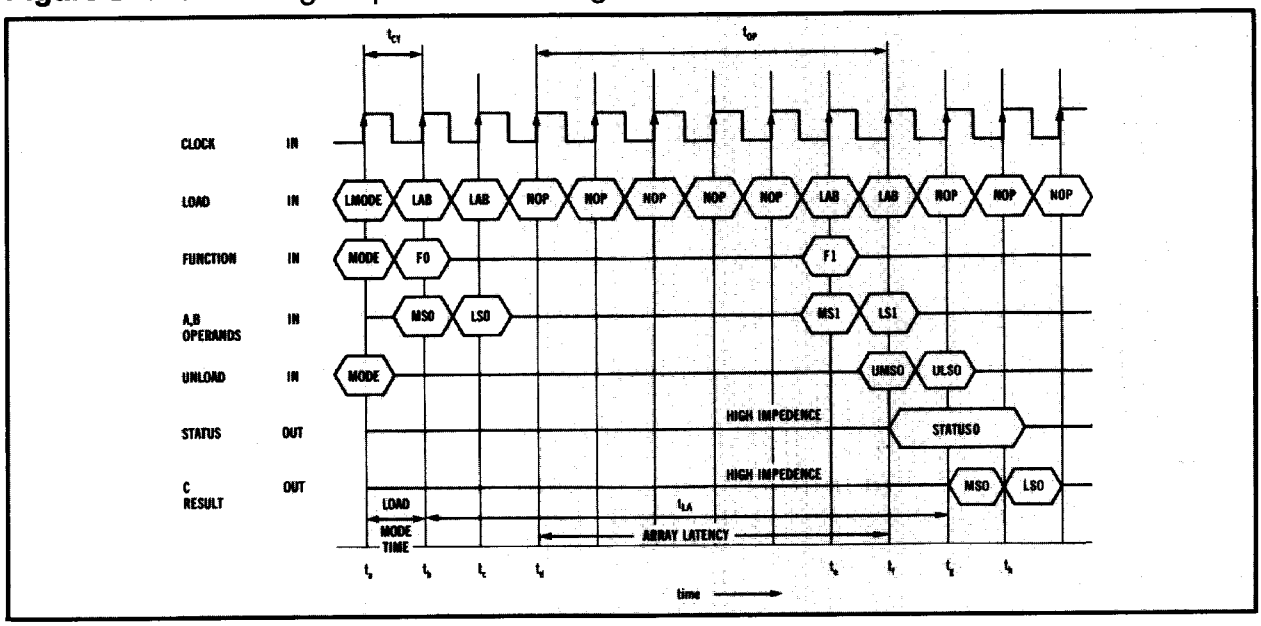
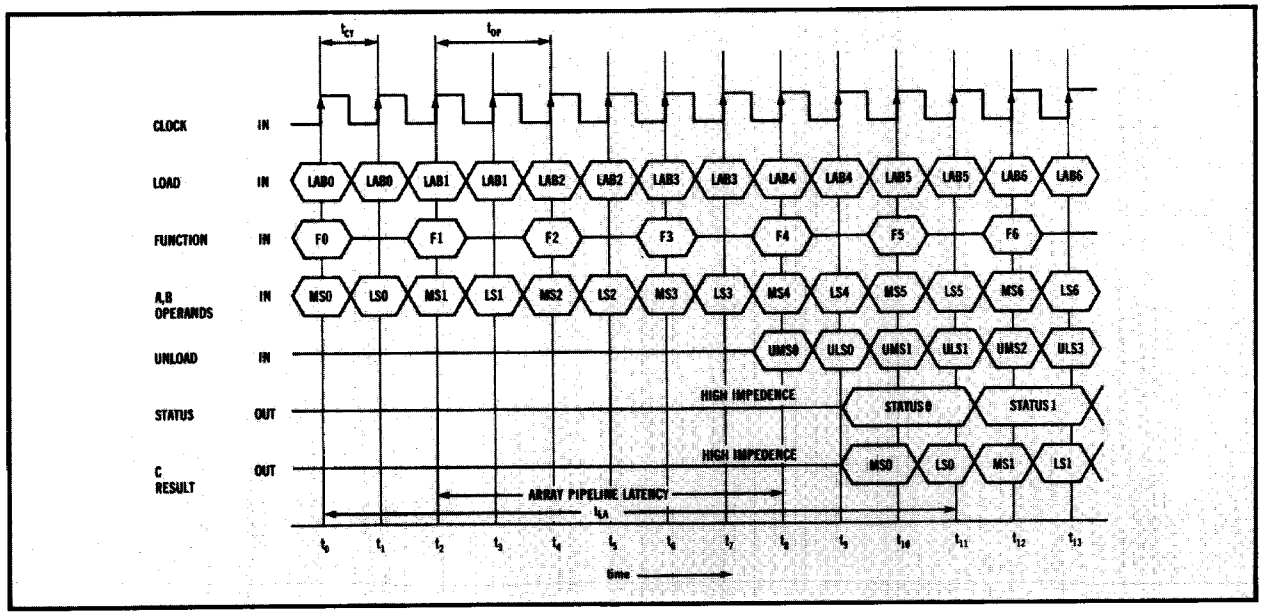


Figure 3. Pipelined Operation Timing



Signal Description/ Functional Operation

DATA INPUTS

A_0 — A_{15}

A inputs are 16-bit word portions of the 32-bit A OPERAND. Most significant word is selected by the load instruction, the least significant is loaded on the next CLOCK.

B_0 — B_{15}

B inputs are 16-bit word portions of the 32-bit B OPERAND. Most significant word is selected by the LOAD instruction, the least significant is loaded on the next CLOCK.

DATA OUTPUTS

C_0 — C_{15}

C outputs are 16-bit word portions of the 32-bit C RESULT. Most or least significant word is selected by the UNLOAD instruction.

CONTROL INPUTS

L_0, L_1

LOAD inputs control the transfer of data from the input registers for A, B, F, and U into registers that follow. All transfers take place on the next positive CLOCK transition following the loading of the LOAD instruction. Typical operations require that L_0 and L_1 be valid for two consecutive clock periods.

LOAD INSTRUCTIONS

L_1 L_0	MNEMONIC	OPERATION
0 0	NOP	No loading
0 1	LAB	Load operands A and B into array
1 0	LA	Load operand A only into array
1 1	LMODE	Load MODE register from F and U input registers

U_0, U_1

UNLOAD inputs control the transfer of data into the output registers and enable the three-state outputs of those registers. The data unloaded from the array is selected for the output register on the next positive CLOCK transition following the loading of the UNLOAD instruction. The three-state outputs are enabled after the transition that loads the output registers.

UNLOAD INSTRUCTIONS

U_1 U_0	MNEMONIC	OPERATION
1 X	DAB	Disable output register's three-state outputs to high impedence state
0 X	ENB	Enables output register's three-state outputs
X 0	UMS	Unload most significant word from array into output register
X 1	ULS	Unload least significant word from array into output register

F_0 — F_3

FUNCTION inputs control the operating MODES of the array and its arithmetic FUNCTION.

The operating MODE is entered in the F and U_0 input registers on the same positive CLOCK transition that loads an LMODE instruction. The new mode is effective after the next positive CLOCK transition.

MODE INSTRUCTIONS

F_3 F_2 F_1 F_0 U_0	MNEMONIC	OPERATION
X X X X 0	FLOW	Data flows through array without pipeline registers
X X X X 1	PIPE	Data is clocked through three pipeline registers in the array
X X 0 0 X	RN	Round to nearest number, or even number if a tie
X X 0 1 X	RZ	Round toward zero
X X 1 0 X	RP	Round toward positive infinity
X X 1 1 X	RM	Round toward minus infinity
X 0 X X X	AI	Affine infinity (sign preserved)
X 1 X X X	PI	Projective infinity (sign ignored)
0 X X X X	IEEE	Treats denormalized operands according to IEEE standard. WTL1032 only.
1 X X X X	FAST	Replaces denormalized operands with zero. WTL1032 only.

The arithmetic FUNCTION is entered in the F input register each positive CLOCK transition. This function is transferred to the array on the next CLOCK transition by a simultaneous LAB instruction on the LOAD input.

FUNCTION INSTRUCTIONS—WTL1033 FLOATING POINT ALU		
F_3 F_2 F_1 F_0	MNEMONIC	OPERATION
0 0 0 0	WRAP A	Conversion of a denormalized A operand to one normalized with negative (wrap-around) exponent
0 0 0 1	UNWRAP A	Conversion of a normalized A operand with negative exponent to a denormalized one
0 0 1 0	FLOAT A	Conversion of 24-bit integer to 32-bit normalized floating-point
0 0 1 1	FIX A	Conversion of 32-bit normalized floating-point to 24-bit integer
0 1 0 0	A+B	Floating-point addition of operands A plus B
0 1 0 1	A−B	Floating-point subtraction of operand A minus B
0 1 1 0	−A+B	Floating-point addition of operands minus A plus B
0 1 1 1	ABS A + ABS B	Floating-point addition of operands |A| plus |B|
1 0 0 0	ABS(A−B)	Absolute value of floating-point subtraction of operands A minus B
1 0 0 1	ABS(A+B)	Absolute value of floating-point addition of operands A plus B
1 0 1 0	—	Reserved
1 0 1 1	—	Reserved
1 1 0 0	—	Reserved
1 1 0 1	—	Unused
1 1 1 0	—	Unused
1 1 1 1	—	Unused

FUNCTION INSTRUCTIONS—WTL1032 FLOATING POINT MULTIPLIER		
F_3 F_2 F_1 F_0	MNEMONIC	OPERATION
0 0 0 0	A×B	Multiply normalized floating-point operands A times B
0 0 0 1	WA×B	Multiply wrapped (negative exponent) operand A times operand B
0 0 1 0	A×WB	Multiply operand A times wrapped operand B
0 0 1 1	WA×WB	Multiply wrapped operands A times B

The WTL1032 Floating-Point Multiplier operates on normalized operands. In the FAST MODE, denormalized operands are treated as zero and a zero result is given. In the IEEE MODE, the denormalized operand is detected in the multiplier by a DIN. This number must be sent to the WTL1033 Floating-Point ALU where the WRAP instruction normalizes the number by treating the exponent as a two's complement negative number. After the appropriate multiplication in the Multiplier, if the result has exponent underflow (UNF), then it may be returned to a denormalized number with the UNWRAP instruction in the ALU.

CK

CLOCK is the single initiator of transfers on the chip. The positive going transition loads all input and output registers and all array input and output, mode and function registers as selected by the LOAD, FUNCTION and UNLOAD instructions.

CONTROL OUTPUTS

S_0 — S_2

STATUS outputs indicate exception conditions in the array. They are held in an output register and pertain to the result word which is in the result output register. They remain the same while both the least and most significant words are unloaded.

STATUS		
S_2 S_1 S_0	MNEMONIC	EXCEPTIONS
0 0 0	—	No exceptions
0 0 1	INX	Inexact result
0 1 0	UF	Exponent underflow
0 1 1	UF + INX	Exponent underflow and inexact result
1 0 0	—	Unused
1 0 1	OF + INX	Exponent overflow and Inexact result
1 1 0	INV	Invalid operands
1 1 1	DIN	Denormalized operand in. WTL1032 only

POWER

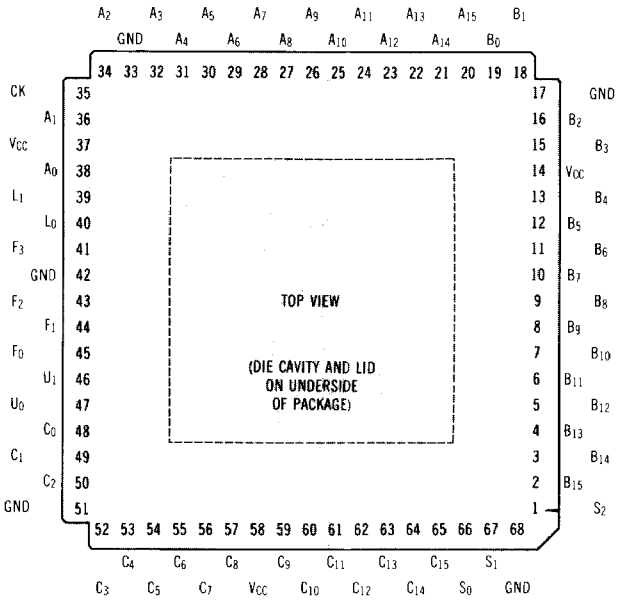
GND

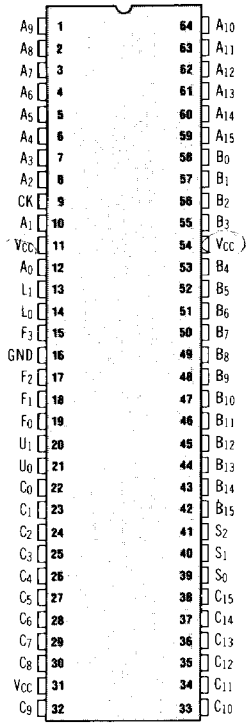
System ground of 0.0 volts. All GND pins must be connected.

V_{CC}

Supply voltage of +5.0 volts. All V_{CC} pins must be connected.

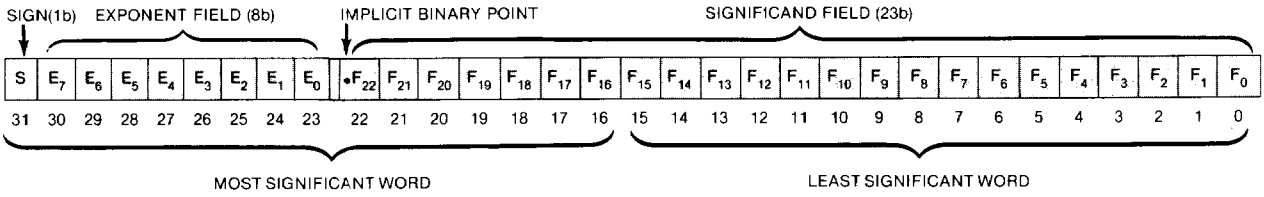
Pin Configuration





Data Formats

32-BIT FLOATING POINT (IEEE Standard)

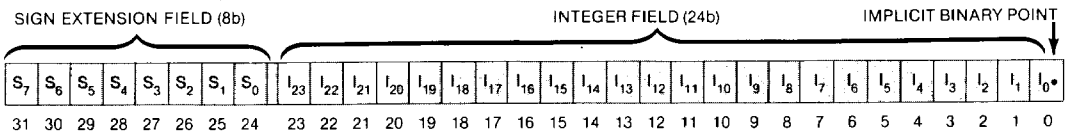


The value is determined by the following:

E	F	VALUE	NAME	MNEMONIC
255	Not all zeros	–	Not a number	NaN
255	All zeros	$(-1)^S$(Infinity)	Infinity	INF
1-254	Any	$(-1)^S(1.F)2^{E-127}$	Normalized number	NOR
0	Not all zeros	$(-1)^S(0.F)2^{-126}$	Denormalized number	DNOR
0	Zero	$(-1)^S0.0$	Zero	ZERO

Note that the F_{23} bit of the significand (the hidden bit) is always one except for zero and denormalized numbers, when it is zero.

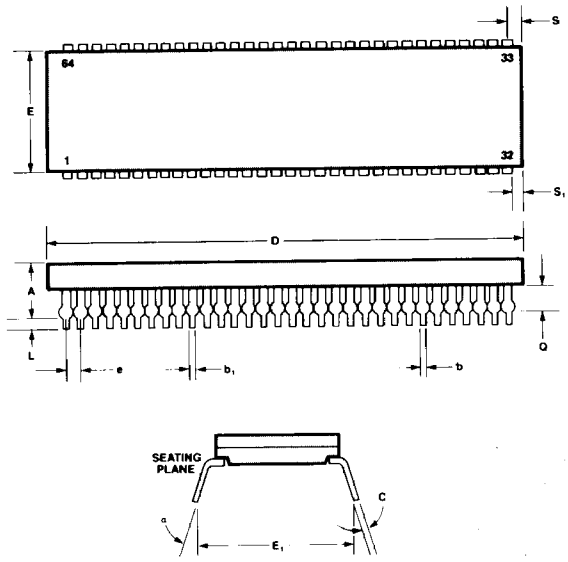
24-BIT FIXED POINT TWO'S COMPLEMENT



Note that the eight-bit sign extension field is a repeat of bit 23, the "sign" bit of the two's complement representation. Values can range between $+2^{23}-1$ and -2^{23}.

Physical Dimensions

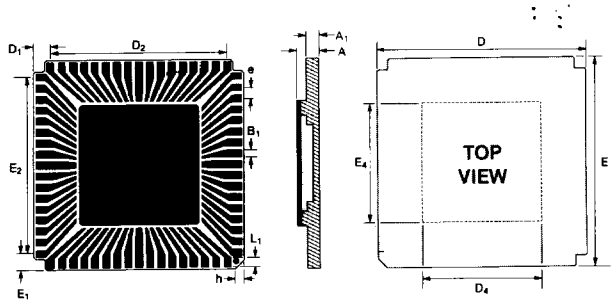
64-Pin Dual In-Line Package



Symbol	LIMITS			
	INCHES		MM	
	MIN	MAX	MIN	MAX
A	.135	.250	3.43	11.43
b	.015	.022	0.38	0.56
b_1	.030	.060	0.76	1.52
c	.008	.013	0.20	0.33
D	3.140	3.260	79.76	82.80
E	.775	.825	19.69	20.96
E_1	.880	.920	22.35	23.37
e	.090	.110	2.29	2.79
L	.120	.160	3.05	4.06
Q	.040	.100	1.02	2.54
α	0°	15°	0°	15°
S*		.098		2.49
S_1**	.005		1.27	

* From centerline of end lead
** From edge of end lead

68-Pin Leadless Chip Carrier (Type A)



Use 3M Textool socket # 268-5400 with flat plate lid # 268-5400-00

Symbol	LIMITS			
	INCHES		MM	
	MIN	MAX	MIN	MAX
A	.082	.120	2.08	3.05
A_1	.054	.065	1.37	1.65
B_1	.033	.04	0.84	1.0
D	.938	.962	23.83	24.43
D_1	.075 REF		1.91 REF	
D_2	.800 REF		20.32 REF	
D_4	—	.578	—	14.68
E	.938	.962	23.83	24.43
E_1	.075 REF		1.91 REF	
E_2	.800 REF		20.32 REF	
E_4	—	.578	—	14.68
e	.050 BSC		1.27 BSC	
h	.035	.058	0.89	1.47
L_1	.045	.055	1.14	1.40

Ordering Information

PACKAGE TYPE	TEMPERATURE RANGE	ORDER NUMBER
Hermetic DIP	T = 0 to + 70°C	WTL 1032JC/1033JC
Hermetic DIP	T = −55 to + 125°C	WTL 1032JM/1033JM
Leadless chip carrier	T = 0 + 70°C	WTL 1032LC/1033LC
Leadless chip carrier	T = −55 + 125°C	WTL 1032LM/1033LM

For flatpack or pingrid array call head office in Santa Clara for details.

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