



Spartan UltraScale+ Libraries Guide (UG1704)

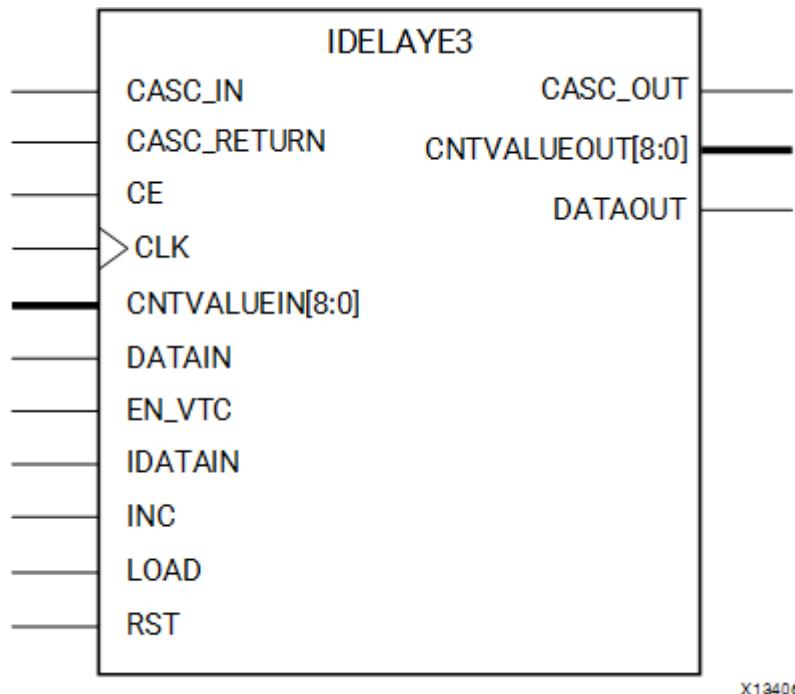
IDELAYE3

ODELAYE3

IDELAYE3

Primitive: Input Fixed or Variable Delay Element

- PRIMITIVE_GROUP: I/O
- PRIMITIVE_SUBGROUP: DELAY
- Families: UltraScale, UltraScale+



Introduction

In component mode, I/O blocks contain a programmable delay element called IDELAYE3. The IDELAYE3 can be connected to an input register/ISERDESE3 or driven directly into device logic. The IDELAYE3 is a 512-tap delay element with a calibrated tap resolution. Refer to the device Data Sheet for delay values. The IDELAYE3 allows incoming signals to be delayed on an individual basis.

Port Descriptions

Port	Direction	Width	Function
CASC_IN	Input	1	Cascade delay input from slave ODELAY CASCADE_OUT.
CASC_OUT	Output	1	Cascade delay output to ODELAY input cascade.

Port	DirectionWidth		Function
CASC_RETURN	Input	1	Cascade delay returning from slave ODELAY DATAOUT.
CE	Input	1	Active-High enable increment/decrement function.
CLK	Input	1	Clock Input
CNTVALUEIN<8:0>	Input	9	Counter value from device logic for dynamically loadable tap value input.
CNTVALUEOUT<8:0>	Output	9	The CNTVALUEOUT pins are used for reporting the dynamically switching value of the delay element. CNTVALUEOUT is only available when IDELAYE3 is in "VARIABLE" or "VAR_LOAD" mode.
DATAIN	Input	1	The DATAIN input is directly driven by the device logic providing a logic accessible delay line. The data is driven back into the device logic through the DATAOUT port with a delay set by the DELAY_VALUE.
DATAOUT	Output	1	Delayed data output from one of two data input ports (IDATAIN or DATAIN).
EN_VTC	Input	1	Keep delay constant over VT.
IDATAIN	Input	1	Data input for IDELAY from the IBUF.
INC	Input	1	Increment / Decrement tap delay input.

Port	DirectionWidth		Function
LOAD	Input	1	Loads the IDELAYE3 primitive to the pre-programmed value in VARIABLE mode. In VAR_LOAD mode, it load the value of CNTVALUEIN.
RST	Input	1	Asynchronous Reset to the DELAY_VALUE, active level based on IS_RST_INVERTED.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CASCADE	STRING	"NONE", "MASTER", "SLAVE_END", "SLAVE_MIDDLE"	"NONE"	Sets the location of the IDELAYE3 when it is used in a cascaded configuration.

Attribute	Type	Allowed Values	Default	Description
				<ul style="list-style-type: none"> • "NONE": Delay line is not cascaded. • "MASTER": Delay line is cascaded with another delay line. • "SLAVE_MIDDLE": Delay line is cascaded from adjacent delay line and also cascades to another delay line. • "SLAVE_END": Delay line is the last cascaded delay line.
DELAY_FORMAT	STRING	"TIME", "COUNT"	"TIME"	<p>Sets the units of DELAY_VALUE of the IDELAYE3. It is recommended to use TIME when DELAY_TYPE is FIXED and use COUNT when DELAY_TYPE is VARIABLE or VAR_LOAD.</p> <ul style="list-style-type: none"> • "TIME": IDELAYE3 DELAY_VALUE is specified in ps. • "COUNT": IDELAYE3 DELAY_VALUE is specified in taps.
DELAY_SRC	STRING	"IDATAIN", "DATAIN"	"IDATAIN"	Select the delay source input to the IDELAYE3.

Attribute	Type	Allowed Values	Default	Description
				<ul style="list-style-type: none"> • "DATAIN": IDELAYE3 chain input is DATAIN. • "IDATAIN": IDELAYE3 chain input is IDATAIN.
DELAY_TYPE	STRING	"FIXED", "VARIABLE", "VAR_LOAD"	"FIXED"	<p>Sets the type of tap delay line.</p> <ul style="list-style-type: none"> • "FIXED": Sets a static delay value. • "VARIABLE": Dynamically adjust (increment/decrement) delay value. • "VAR_LOAD": Dynamically loads tap values.
DELAY_VALUE	DECIMAL	0 to 1250	0	Specifies the fixed delay in ps in "FIXED" mode or the initial starting number of taps in "VARIABLE" mode or "VAR_LOAD" mode (input path).
IS_CLK_INVERT	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the CLK pin is active-High or active-Low.
IS_RST_INVERT	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the RST pin is active-High or active-Low.
REFCLK_FREQUENCY	FLOAT	200.0 to significant 300.0 digit	300.0	Sets the tap value (in MHz) used by the timing analyzer for static timing analysis

Attribute	Type	Allowed Values	Default	Description
				and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee performance.
SIM_DEVICE	STRING	"ULTRASCALE","ULTRASCALE_PLUS","ULTRASCALE_PLUS_ES1","ULTRASCALE_PLUS_ES2"	Set the device version for simulation	
UPDATE_MODE	STRING	"ASYNC", "MANUAL", "SYNC"	"ASYNC"	Determines when updates to the delay will take effect.

Attribute	Type	Allowed Values	Default	Description
				<ul style="list-style-type: none"> • "ASYNC": Updates are increments or decrements to the delay value independent of the data being received. • "SYNC": Updates require that DATAIN (or IDATAIN) transitions to synchronously update the delay with the DATAIN edges. • "MANUAL": Updates take effect when both LD and CE are asserted after the LD and CNTVALUEIN signals are used to load the new CNTVALUE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- IDELAYE3: Input Fixed or Variable Delay Element
--          Spartan UltraScale+
-- Xilinx HDL Language Template, version 2025.1
```

```

IDELEYE3_inst : IDELEYE3
generic map (
    CASCADE => "NONE",                      -- Cascade setting
(MASTER, NONE, SLAVE_END, SLAVE_MIDDLE)
    DELAY_FORMAT => "TIME",                  -- Units of the
DELAY_VALUE (COUNT, TIME)
    DELAY_SRC => "IDATAIN",                 -- Delay input (DATAIN,
IDATAIN)
    DELAY_TYPE => "FIXED",                  -- Set the type of tap
delay line (FIXED, VARIABLE, VAR_LOAD)
    DELAY_VALUE => 0,                      -- Input delay value
setting
    IS_CLK_INVERTED => '0',                -- Optional inversion for
CLK
    IS_RST_INVERTED => '0',                -- Optional inversion for
RST
    REFCLK_FREQUENCY => 300.0,              -- IDELAYCTRL clock input
frequency in MHz (200.0-800.0)
    SIM_DEVICE => "ULTRASCALE_PLUS",      -- Set the device version
for simulation functionality (ULTRASCALE, ULTRASCALE_PLUS,
ULTRASCALE_PLUS_ES1,
                                         -- ULTRASCALE_PLUS_ES2)
    UPDATE_MODE => "ASYNC"                 -- Determines when
updates to the delay will take effect (ASYNC, MANUAL, SYNC)
)
port map (
    CASC_OUT => CASC_OUT,                  -- 1-bit output: Cascade delay
output to ODELAY input cascade
    CNTVALUEOUT => CNTVALUEOUT,           -- 9-bit output: Counter value
output
    DATAOUT => DATAOUT,                   -- 1-bit output: Delayed data
output
    CASC_IN => CASC_IN,                   -- 1-bit input: Cascade delay
input from slave ODELAY CASCADE_OUT
    CASC_RETURN => CASC_RETURN,           -- 1-bit input: Cascade delay
returning from slave ODELAY DATAOUT
    CE => CE,                          -- 1-bit input: Active-High
enable increment/decrement input
    CLK => CLK,                         -- 1-bit input: Clock input
    CNTVALUEIN => CNTVALUEIN,            -- 9-bit input: Counter value
input
    DATAIN => DATAIN,                   -- 1-bit input: Data input
from the logic
    EN_VTC => EN_VTC,                  -- 1-bit input: Keep delay
constant over VT

```

```

IDATAIN => IDATAIN,           -- 1-bit input: Data input
from the IOBUF
INC => INC,                  -- 1-bit input: Increment /
Decrement tap delay input
LOAD => LOAD,                -- 1-bit input: Load
DELAY_VALUE input
RST => RST,                  -- 1-bit input: Asynchronous
Reset to the DELAY_VALUE
);

-- End of IDELAYE3_inst instantiation

```

Verilog Instantiation Template

```

// IDELAYE3: Input Fixed or Variable Delay Element
//          Spartan UltraScale+
// Xilinx HDL Language Template, version 2025.1

IDELEYE3 #(
    .CASCADE("NONE"),           // Cascade setting
    (MASTER, NONE, SLAVE_END, SLAVE_MIDDLE)
    .DELAY_FORMAT("TIME"),       // Units of the
    DELAY_VALUE (COUNT, TIME)
    .DELAY_SRC("IDATAIN"),      // Delay input (DATAIN,
    IDATAIN)
    .DELAY_TYPE("FIXED"),        // Set the type of tap
    delay line (FIXED, VARIABLE, VAR_LOAD)
    .DELAY_VALUE(0),            // Input delay value
    setting
    .IS_CLK_INVERTED(1'b0),     // Optional inversion for
    CLK
    .IS_RST_INVERTED(1'b0),     // Optional inversion for
    RST
    .REFCLK_FREQUENCY(300.0),   // IDELAYCTRL clock input
    frequency in MHz (200.0-800.0)
    .SIM_DEVICE("ULTRASCALE_PLUS"), // Set the device version
    for simulation functionality (ULTRASCALE, ULTRASCALE_PLUS,
    ULTRASCALE_PLUS_ES1,
                                         // ULTRASCALE_PLUS_ES2)
    .UPDATE_MODE("ASYNC")        // Determines when updates
    to the delay will take effect (ASYNC, MANUAL, SYNC)
)
IDELEYE3_inst (
    .CASC_OUT(CASC_OUT),        // 1-bit output: Cascade delay

```

```

output to ODELAY input cascade
    .CNTVALUEOUT(CNTVALUEOUT), // 9-bit output: Counter value
output
    .DATAOUT(DATAOUT),           // 1-bit output: Delayed data
output
    .CASC_IN(CASC_IN),          // 1-bit input: Cascade delay
input from slave ODELAY CASCADE_OUT
    .CASC_RETURN(CASC_RETURN), // 1-bit input: Cascade delay
returning from slave ODELAY DATAOUT
    .CE(CE),                  // 1-bit input: Active-High
enable increment/decrement input
    .CLK(CLK),                // 1-bit input: Clock input
    .CNTVALUEIN(CNTVALUEIN),   // 9-bit input: Counter value
input
    .DATAIN(DATAIN),           // 1-bit input: Data input from
the logic
    .EN_VTC(EN_VTC),          // 1-bit input: Keep delay
constant over VT
    .IDATAIN(IDATAIN),        // 1-bit input: Data input from
the IOBUF
    .INC(INC),                // 1-bit input: Increment /
Decrement tap delay input
    .LOAD(LOAD),               // 1-bit input: Load
DELAY_VALUE input
    .RST(RST)                 // 1-bit input: Asynchronous
Reset to the DELAY_VALUE
);

// End of IDELAYE3_inst instantiation

```

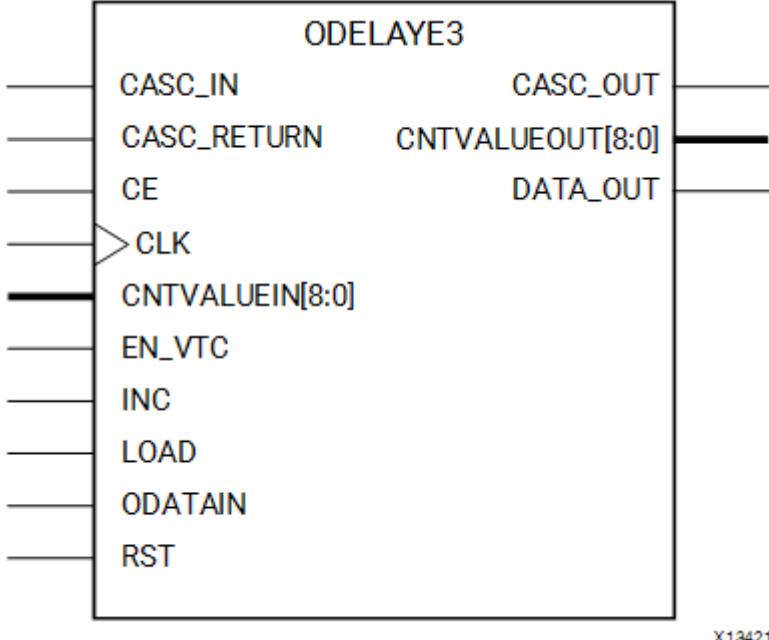
Related Information

- *UltraScale Architecture SelectIO Resources User Guide (UG571)*

ODELAYE3

Primitive: Output Fixed or Variable Delay Element

- PRIMITIVE_GROUP: I/O
- PRIMITIVE_SUBGROUP: DELAY
- Families: UltraScale, UltraScale+



X13421

Introduction

In component mode, I/O blocks contain a programmable delay element called ODELAYE3. The ODELAYE3 can be connected to an output register/OSERDESE3 or driven directly by device logic. The ODELAYE3 is a 512-tap delay element with a calibrated delay. The ODELAYE3 allows signals to be delayed on an individual basis.

Port Descriptions

Port	Direction	Width	Function
CASC_IN	Input	1	Cascade delay input from slave IDELAY CASCADE_OUT.
CASC_OUT	Output	1	Cascade delay output to IDELAY input cascade.
CASC_RETURN	Input	1	Cascade delay returning from slave IDELAY DATAOUT.
CE	Input	1	Active-High enable increment/decrement function.
CLK	Input	1	Clock input
CNTVALUEIN<8:0>	Input	9	Counter value from device logic for dynamically loadable tap value input.

Port	Direction	Width	Function
CNTVALUEOUT<8:0>	Output	9	The CNTVALUEOUT pins are used for reporting the dynamically switching value of the delay element. CNTVALUEOUT is only available when ODELAYE3 is in "VARIABLE" or "VAR_LOAD" mode.
DATAOUT	Output	1	Delayed data from ODATAIN input port.
EN_VTC	Input	1	Keep delay constant over VT.
INC	Input	1	Increment/Decrement tap delay input.
LOAD	Input	1	Loads the ODELAY primitive to the pre-programmed value in VARIABLE mode. In VAR_LOAD mode, it loads the value of CNTVALUEIN.
ODATAIN	Input	1	Data input for ODELAYE3 from OSERDES or programmable logic.
RST	Input	1	Asynchronous Reset to the DELAY_VALUE, active level based on IS_RST_INVERTED.

Design Entry Method

Instantiation	Yes
Inference	No
IP and IP Integrator Catalog	Yes

Available Attributes

Attribute	Type	Allowed Values	Default	Description
CASCADE	STRING	"NONE",	"NONE"	Set the location of

Attribute	Type	Allowed Value	Default	Description
		"MASTER", "SLAVE_END", "SLAVE_MIDDLE"		<p>the ODELAYE3 when it is used in a cascaded configuration.</p> <ul style="list-style-type: none"> • "NONE": Delay line is not cascaded. • "MASTER": Delay line is cascaded with another delay line. • "SLAVE_MIDDLE": Delay line is cascaded from adjacent delay line and also cascades to another delay line. • "SLAVE_END": Delay line is the last cascaded delay line.
DELAY_FORMAT	STRING	"TIME", "COUNT"	"TIME"	Sets the units of DELAY_VALUE of the ODELAYE3. It is recommended to use TIME when DELAY_TYPE is FIXED and use COUNT when DELAY_TYPE is VARIABLE or VAR_LOAD.

Attribute	Type	Allowed Value	Default	Description
				<ul style="list-style-type: none"> • "TIME": ODELAYE3 DELAY_VALUE is specified in ps. • "COUNT": ODELAYE3 DELAY_VALUE is specified in taps.
DELAY_TYPE	STRING	"FIXED", "VARIABLE", "VAR_LOAD"	"FIXED"	<p>Sets the type of tap delay line.</p> <ul style="list-style-type: none"> • "FIXED": Sets a static delay value. • "VARIABLE": Dynamically adjust (increment/decrement) delay value. • "VAR_LOAD": Dynamically loads tap values.
DELAY_VALUE	DECIMAL	0 to 1250	0	Specifies the fixed delay in ps in "FIXED" mode or the initial starting number of taps in "VARIABLE" mode or "VAR_LOAD" mode (input path).
IS_CLK_INVERT	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the CLK pin is active-High or active-Low.
IS_RST_INVERT	BINARY	1'b0 to 1'b1	1'b0	Specifies whether the RST pin is active-High or active-Low.

Attribute	Type	Allowed Values	Default	Description
REFCLK_FREQUENCY	FLOAT	200.0 to 800.0 significant digit	300.0	Sets the tap value (in MHz) used by the timing analyzer for static timing analysis and functional/timing simulation. The frequency of REFCLK must be within the given datasheet range to guarantee performance.
SIM_DEVICE	STRING	"ULTRASCALE", "ULTRASCALE_PLUS", "ULTRASCALE_PLUS_ES1", "ULTRASCALE_PLUS_ES2"	Set	Set the device version for simulation functionality.
UPDATE_MODE	STRING	"ASYNC", "MANUAL", "SYNC"	"ASYNC"	Determines when updates to the delay will take effect.

Attribute	Type	Allowed Value	Default	Description
				<ul style="list-style-type: none"> • "ASYNC": Updates are increments or decrements to the delay value independent of the data being received. • "SYNC": Updates require that ODATAIN transitions to synchronously update the delay with the ODATAIN edges. • "MANUAL": Updates take effect when both LD and CE are asserted after the LD and CNTVALUEIN signals are used to load the new CNTVALUE.

VHDL Instantiation Template

Unless they already exist, copy the following two statements and paste them before the entity declaration.

```
Library UNISIM;
use UNISIM.vcomponents.all;
```

```
-- ODELAYE3: Output Fixed or Variable Delay Element
--          Spartan UltraScale+
-- Xilinx HDL Language Template, version 2025.1
```

```

ODELAYE3_inst : ODELAYE3
generic map (
    CASCADE => "NONE",                      -- Cascade setting
    (MASTER, NONE, SLAVE_END, SLAVE_MIDDLE)
    DELAY_FORMAT => "TIME",                   -- (COUNT, TIME)
    DELAY_TYPE => "FIXED",                   -- Set the type of tap
    delay line (FIXED, VARIABLE, VAR_LOAD)
    DELAY_VALUE => 0,                        -- Output delay tap
    setting
    IS_CLK_INVERTED => '0',                -- Optional inversion for
    CLK
    IS_RST_INVERTED => '0',                -- Optional inversion for
    RST
    REFCLK_FREQUENCY => 300.0,              -- IDELAYCTRL clock input
    frequency in MHz (200.0-800.0).
    SIM_DEVICE => "ULTRASCALE_PLUS",        -- Set the device version
    for simulation functionality (ULTRASCALE, ULTRASCALE_PLUS,
    ULTRASCALE_PLUS_ES1,                     -- ULTRASCALE_PLUS_ES2)
    UPDATE_MODE => "ASYNC"                  -- Determines when
    updates to the delay will take effect (ASYNC, MANUAL, SYNC)
)
port map (
    CASC_OUT => CASC_OUT,                  -- 1-bit output: Cascade delay
    output to IDELAY input cascade
    CNTVALUEOUT => CNTVALUEOUT,           -- 9-bit output: Counter value
    output
    DATAOUT => DATAOUT,                  -- 1-bit output: Delayed data
    from ODATAIN input port
    CASC_IN => CASC_IN,                  -- 1-bit input: Cascade delay
    input from slave IDELAY CASCADE_OUT
    CASC_RETURN => CASC_RETURN,           -- 1-bit input: Cascade delay
    returning from slave IDELAY DATAOUT
    CE => CE,                          -- 1-bit input: Active-High
    enable increment/decrement input
    CLK => CLK,                         -- 1-bit input: Clock input
    CNTVALUEIN => CNTVALUEIN,           -- 9-bit input: Counter value
    input
    EN_VTC => EN_VTC,                  -- 1-bit input: Keep delay
    constant over VT
    INC => INC,                        -- 1-bit input: Increment/
    Decrement tap delay input
    LOAD => LOAD,                       -- 1-bit input: Load
    DELAY_VALUE input
    ODATAIN => ODATAIN,                -- 1-bit input: Data input

```

```

RST => RST           -- 1-bit input: Asynchronous
Reset to the DELAY_VALUE
);

-- End of ODELAYE3_inst instantiation

```

Verilog Instantiation Template

```

// ODELAYE3: Output Fixed or Variable Delay Element
//           Spartan UltraScale+
// Xilinx HDL Language Template, version 2025.1

ODELAYE3 #(
    .CASCADE("NONE"),           // Cascade setting
    (MASTER, NONE, SLAVE_END, SLAVE_MIDDLE)
    .DELAY_FORMAT("TIME"),       // (COUNT, TIME)
    .DELAY_TYPE("FIXED"),        // Set the type of tap
    delay line (FIXED, VARIABLE, VAR_LOAD)
    .DELAY_VALUE(0),            // Output delay tap
    setting
    .IS_CLK_INVERTED(1'b0),     // Optional inversion for
    CLK
    .IS_RST_INVERTED(1'b0),     // Optional inversion for
    RST
    .REFCLK_FREQUENCY(300.0),    // IDELAYCTRL clock input
    frequency in MHz (200.0-800.0).
    .SIM_DEVICE("ULTRASCALE_PLUS"), // Set the device version
    for simulation functionality (ULTRASCALE, ULTRASCALE_PLUS,
    ULTRASCALE_PLUS_ES1,
                                         // ULTRASCALE_PLUS_ES2)
    .UPDATE_MODE("ASYNC")        // Determines when updates
    to the delay will take effect (ASYNC, MANUAL, SYNC)
)
ODELAYE3_inst (
    .CASC_OUT(CASC_OUT),        // 1-bit output: Cascade delay
    output to IDELAY input cascade
    .CNTVALUEOUT(CNTVALUEOUT),   // 9-bit output: Counter value
    output
    .DATAOUT(DATAOUT),          // 1-bit output: Delayed data
    from ODATAIN input port
    .CASC_IN(CASC_IN),          // 1-bit input: Cascade delay
    input from slave IDELAY CASCADE_OUT
    .CASC_RETURN(CASC_RETURN),   // 1-bit input: Cascade delay
    returning from slave IDELAY DATAOUT

```

```
.CE(CE),                                // 1-bit input: Active-High
enable increment/decrement input
.CLK(CLK),                                // 1-bit input: Clock input
.CNTVALUEIN(CNTVALUEIN),      // 9-bit input: Counter value
input
.EN_VTC(EN_VTC),                         // 1-bit input: Keep delay
constant over VT
.INC(INC),                                // 1-bit input: Increment/
Decrement tap delay input
.LOAD(LOAD),                                // 1-bit input: Load
DELAY_VALUE input
.ODATAIN(ODATAIN),                         // 1-bit input: Data input
.RST(RST)                                  // 1-bit input: Asynchronous
Reset to the DELAY_VALUE
);

// End of ODELAYE3_inst instantiation
```

Related Information

- *UltraScale Architecture SelectIO Resources User Guide (UG571)*