Course: Computer Organization & Architecture   **Course Code: 21VMC0C105**

Assignment: 1   **Full Marks:30**

Subjective Section

Instructions :

- This section is of 20 marks. Each question carries 5 marks.
- Submission of the assignment
  - Format: PDF with proper question numbers and subsections
  - Handwritten solutions will not be accepted
- Due Date
  - You have three weeks to complete this assignment. The solution must be submitted on or before 26 December, 11:59 pm.
- Step marks will also be awarded, in case the final answer is incorrect or if the answer is incomplete

All the questions are mandatory

Question 1

(a) Design a Common Bus System using MUX which consists of 8 registers & each register consists of 4 Bits. (2.5 marks)
(b) Also explain the working of the Common Bus System using an appropriate example. (2.5 mark)

Question 2

Register A holds the 8 bit Binary value 11011001. Determine the B operand & the logic micro operation to be performed in order to change the value in A to :-

(a) 01101101 (2.5 marks)
(b) 11111101 (2.5 marks)

Question 3

A two word instruction is stored in memory at an address designated by symbol W. The address field of the instruction(stored at W+1) is designated by symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from other addresses if the addressing mode of the instruction is :-

(a) Direct (1 mark)
(b) Indirect (1 mark)
(c) Relative (1 mark)
(d) Indexed (2 marks)

Question 4

    (a) 16k x 8 RAM Chips are used to construct 64k x 16 RAM. Find how many Chips will be needed. (2 marks)

    (b) Draw a block diagram showing connections of chips to address lines. (3 marks)