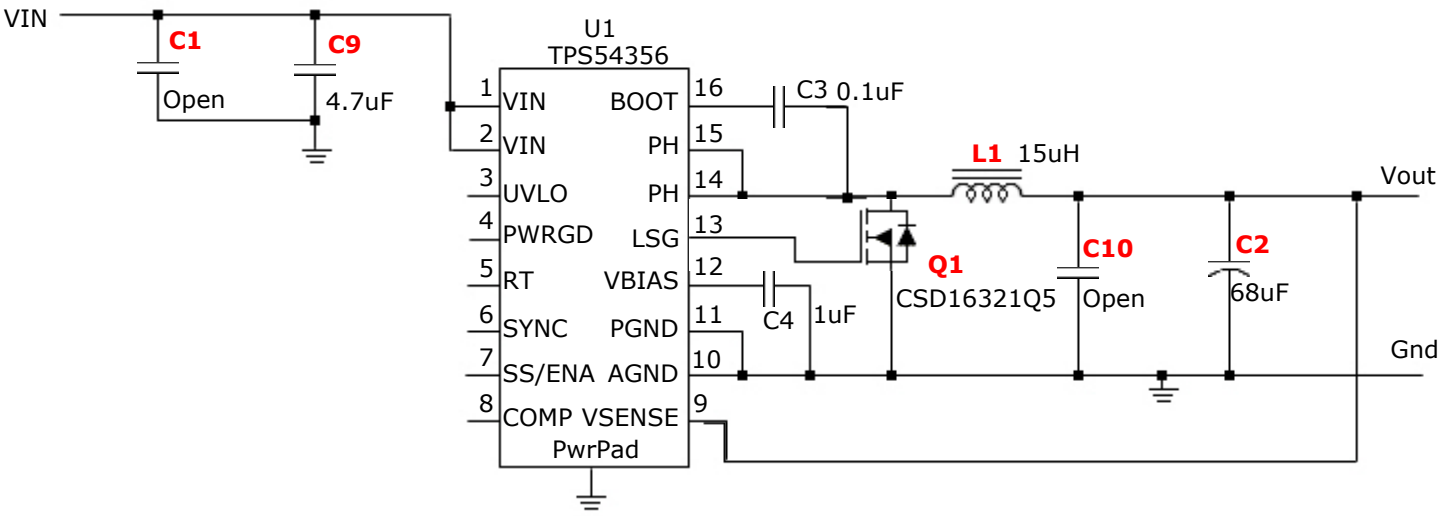
SwitcherPro Design Report
Schematic

Design Name: Quadrotor supply **Part:** TPS54356

VinMin: 6V **VinMax:** 10V **Vout:** 3.3V **Iout:** 2A



SwitcherPro Design Report
Analysis - Main

Design Name: Quadrotor supply **Part:** TPS54356

VinMin: 6V **VinMax:** 10V **Vout:** 3.3V **Iout:** 2A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	6.00	-	10.00	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	200	-	-	270.3
UVLO(Start) Volts - V	-	-	-	-	-	-	-	-	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	-	-
Switching Frequency KHz - KHz	-	-	-	-	500	-	-	-	-
Slow Start ms - ms	-	-	-	-	4.00	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	413	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	4

SwitcherPro Design Report
Analysis - Output1

Design Name: Quadrotor supply **Part:** TPS54356

VinMin: 6V **VinMax:** 10V **Vout:** 3.3V **Iout:** 2A

Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	3.300	-	-	-	-	3.291	-	3.309
Output Ripple mVp-p - mVp-p	-	-	-	-	-	66	-	-	3.5
Output Current Amps - A	-	-	2.000	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.259	-	0.380
Current Limit Threshold Amps - A	-	-	-	-	3.000	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-16	-
Phase Margin Deg. - Deg.	-	-	-	60	-	-	-	56	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	111	-	142
Lower FET RDSon mOhms - mΩ	-	-	-	-	-	-	2	-	2
Duty Cycle % - %	-	-	-	-	-	-	34.3	-	58.6
On Time Min (switch) ns - ns	-	-	-	-	-	-	571.4	-	1465.7
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	26	-

SwitcherPro Design Report
Stress Results

Design Name: Quadrotor supply **Part:** TPS54356

VinMin: 6V **VinMax:** 10V **Vout:** 3.3V **Iout:** 2A

Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	25V	10V	3.5A	1A	-	2mW	-
C2 (Bulk Output Cap)	6.3V	3.32V	3A	0.11A	-	108uW	-
L1 (Output Inductor)	-	-	3.1A	2A	-	100mW	-
Q1 (Sync. Rectifier)	25V	10V	100A	1.62A	-	128mW	30°C
U1 (Converter)	21V	10V	6.5A	1.53A	-	877mW	62°C

SwitcherPro Design Report

Efficiency

Design Name: Quadrotor supply **Part:** TPS54356

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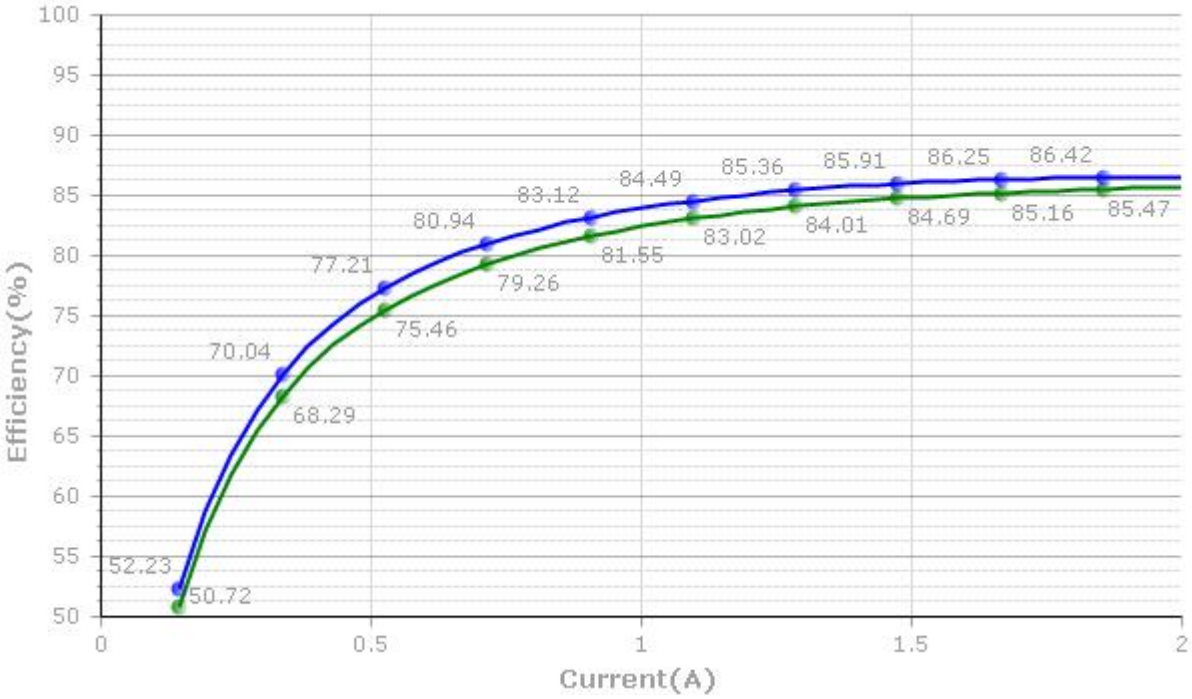
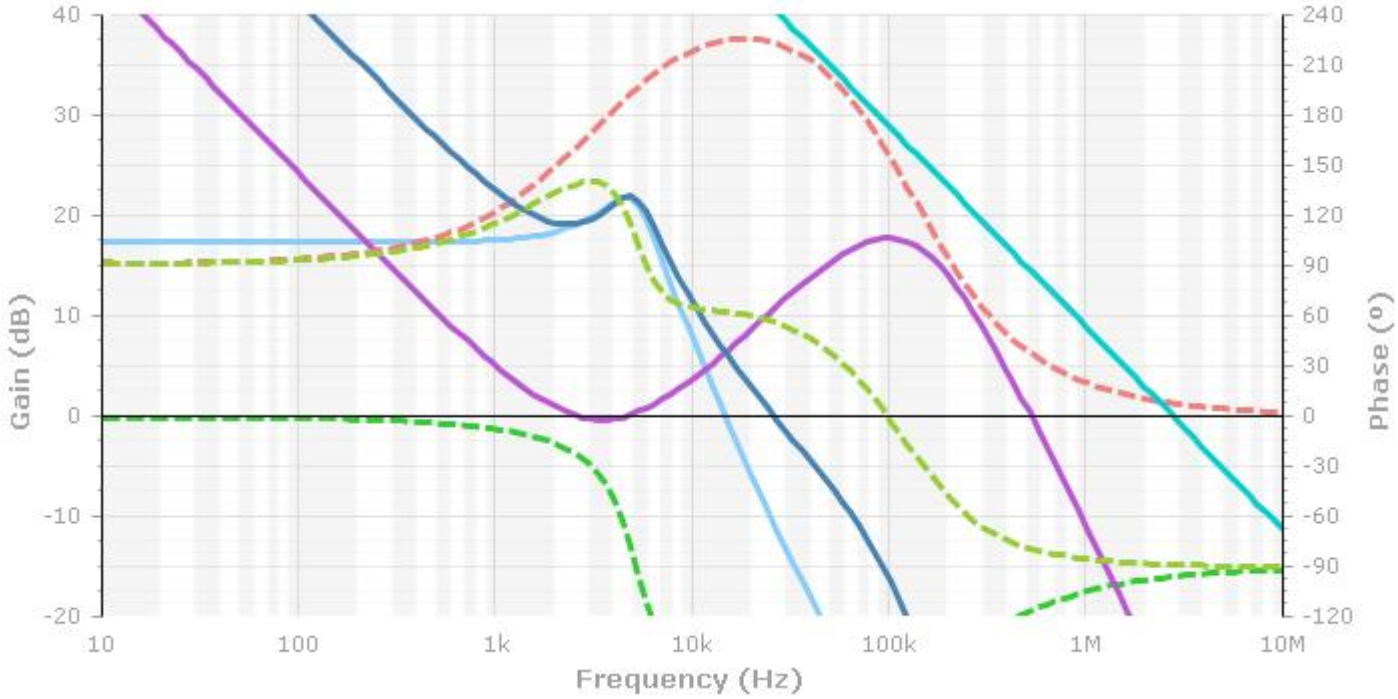


Efficiency For Vin Max
Efficiency For Vin Min

SwitcherPro Design Report
Loop Response

Design Name: Quadrotor supply **Part:** TPS54356

VinMin: 6V **VinMax:** 10V **Vout:** 3.3V **Iout:** 2A



This graph was generated using the following conditions: Nominal Switching Freq, Minimum Vin, Maximum Load,and Maximum Capacitor ESR. To customize conditions use the 'What If Analysis' form

- Power Stage Gain
- Power Stage Phase
- Compensation Gain
- Compensation Phase
- Error Amp Gain
- Total Gain
- Total Phase

SwitcherPro Design Report
Bill of Materials

Design Name: Quadrotor supply **Part:** TPS54356

VinMin: 6V **VinMax:** 10V **Vout:** 3.3V **Iout:** 2A

Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C2	1	EEFSX0J680R	Capacitor, NA, 68uF, 6.3V, 20%	Panasonic	EEFSX0	32	1
C3	1	Standard	Capacitor, Ceramic, 0.1uF, 20V, 1%	Standard	0805	3	1
C4	1	Standard	Capacitor, Ceramic, 1uF, 20V, 1%	Standard	0805	3	1
C9	1	GRM21BR61E475MA12L	Capacitor, Ceramic, 4.7uF, 25V, 20%	muRata	0805	2.5	1.25
L1	1	ELLCTV150M	Inductor, 15uH, 3.1A, 25mΩ	Panasonic	ELLATV	111	4
Q1	1	CSD16321Q5	Transistor, NFET, 25V, 100A, 3mΩ	Texas Instruments, Inc.	QFN 5x6	31	1
R15	1	Standard	Resistor, SurfaceMount, 0.0Ω, 100mW, 1%	Standard	0603	2	1
R7	1	Standard	Resistor, SurfaceMount, 0.0Ω, 100mW, 1%	Standard	0603	2	1
U1	1	TPS54356	IC, Converter, 16 pins	Texas Instruments, Inc.	HTSSOP-Power PAD	34	2

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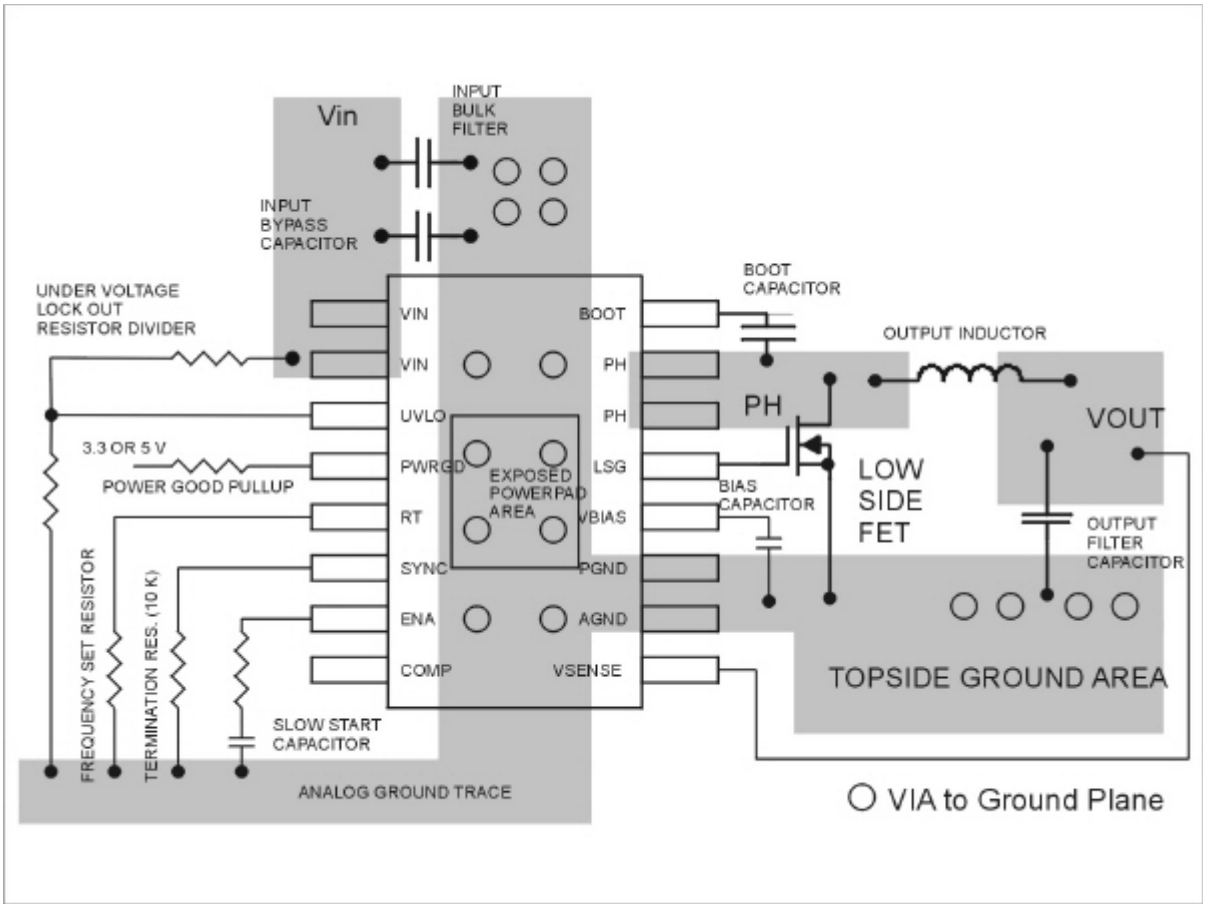

TPS5435x

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54350 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the AGND and PGND pins. See Figure 21 for an example of a board layout. The AGND and PGND pins should be tied to the PCB ground plane at the pins of the IC. The source of the low-side MOSFET and the anode of the Schottky diode should be connected directly to the PCB ground plane. The PH pins should be tied together and routed to the drain of the low-side MOSFET or to the cathode of the external Schottky diode. Since the PH connection is the switching node, the MOSFET (or diode) should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The recommended conductor width from pins 14 and 15 is 0.050 inch to 0.075 inch of 1-ounce copper. The length of the copper land pattern should be no more than 0.2 inch.

For operation at full rated load, the analog ground plane must provide adequate heat dissipating area. A 3-inch by 3-inch plane of copper is recommended, though not mandatory, dependent on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the bottom or top layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013-inch diameter vias to avoid solder wicking through the vias. Four vias should be in the PowerPAD area with four additional vias outside the pad area and underneath the package. Additional vias beyond those recommended to enhance thermal performance should be included in areas not under the device package.