Señal	direccion	Pin FPGA	I/O bank	I/O standard
clk	Input	M8	2	2.5-V
rst_n	Input	H21	6	1.5-V Scmitt Trigger
SPC	output	B5	8	1.2-V
SDO	Inout	C6	8	1.2-V
SDI	Inout	D5	8	1.2-V
nCS	Output	E9	8	1.2-V
Display Y[7]	Output	V10	3	3.3-V LVTTL
Display Y[6]	Output	AA6	3	3.3-V LVTTL
Display Y[5]	Output	AB6	3	3.3-V LVTTL
Display Y[4]	Output	R11	3	3.3-V LVTTL
Display Y[3]	Output	AB8	3	3.3-V LVTTL
Display Y[2]	Output	W8	3	3.3-V LVTTL
Display Y[1]	Output	W6	3	3.3-V LVTTL
Display Y[0]	Output	Y5	3	3.3-V LVTTL
Leds_X[7]	Output	C5	8	1.2-V
Leds_X[6]	Output	B4	8	1.2-V
Leds_X[5]	Output	A5	8	1.2-V
Leds_X[4]	Output	C4	8	1.2-V
Leds_X[3]	Output	В7	8	1.2-V
Leds_X[2]	Output	A6	8	1.2-V
Leds_X[1]	Output	C8	8	1.2-V
Leds_X[0]	Output	C7	8	1.2-V
G GPIO0_D17)	Output	W16	4	3.3-V LVTTL
F (GPIO0_D28)	Output	AB11	4	3.3-V LVTT
E (GPIO0_D19)	Output	W15	4	3.3-V LVTTL
D GPIO0_D38)	Output	AB10	4	3.3-V LVTTL
C (GPIO0_D21)	Output	AA15	4	3.3-V LVTTL
B (GPIO0_D34)	Output	W12	4	3.3-V LVTTL
A GPIO0_D25)	Output	AA13	4	3.3-V LVTTL