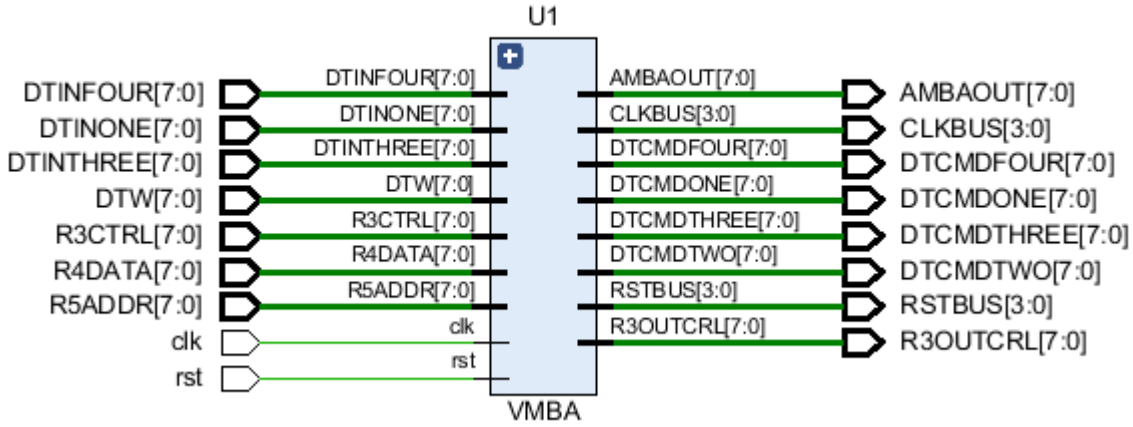
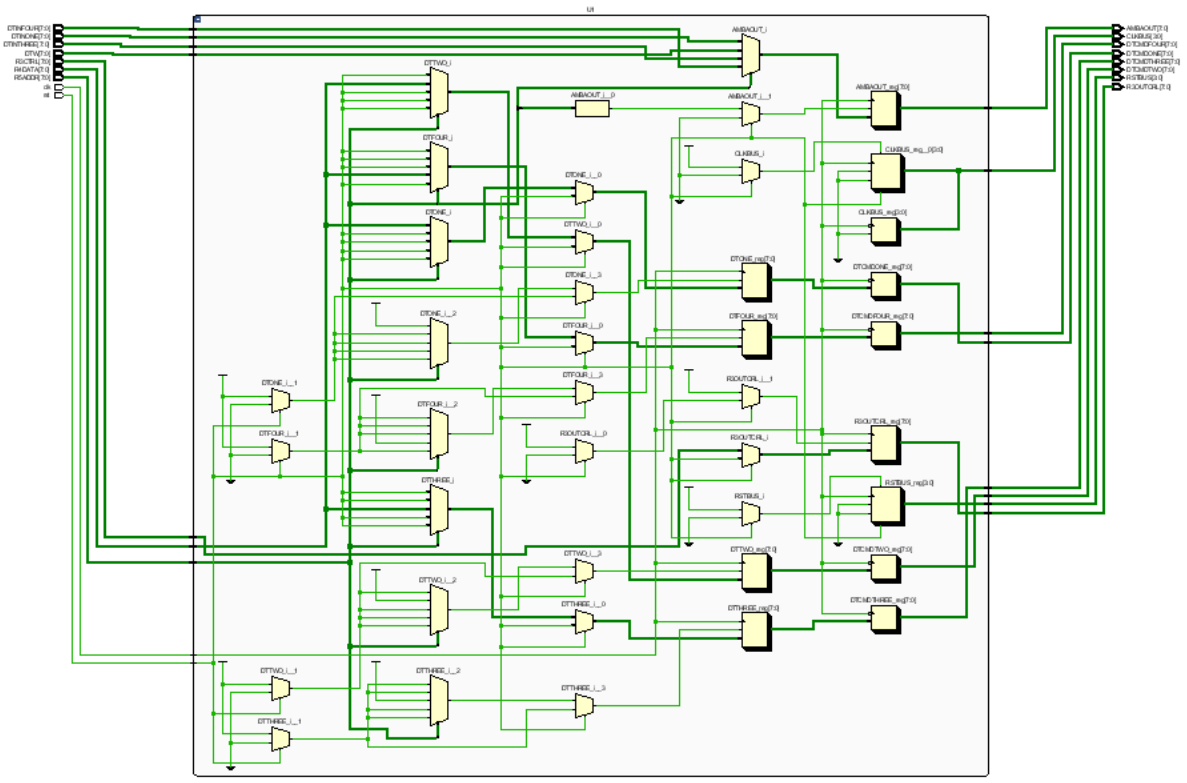
Virtual Advance Machine Bus Peripheral

Functional Block Diagram



Internal structure



Virtual Advance Machine Bus Peripheral

Description	Input/Output	Size	Purpose
Main	Input - R3CNTRL	8 bits	Control Lines from uP
	Output – R3OUTCRL	8 bits	Control Line to PPI
	Input – R4DATA	8 bits input to DEMUX	Data Input for Devices
	Input – R5ADDR[3:0]	4 bits DEMUX Controller	0 – D1Input<-R4DATA
			1 – D2Input<-R4DATA
			2 – D3Input<-R4DATA
			3 – D4Input<-R4DATA
	Input – R5ADDR[7:4]	4 bits MUX Controller	0 AMBAOUT<-D1OUT
			1 AMBAOUT<-D2OUT
			2 AMBAOUT<-D3OUT
			3 AMBAOUT<-D4OUT
	Input CLK	1 bit	Master Clock Signal
	Input RST	1 bit	Master Reset Signal
Device 1	Output CLKBUS[0]	1 bit	Clock Signal Device 1
	Output RSTBUS[0]	1 bit	Reset Signal Line Device 1
	Output - DTCMDONE	8 bit	Data Input to Device 1 Command/Address
	Input – DTINONE	8 bit	Data Output from Device 1
	Output R3OUTCRL[1:0]	2 bits	OE/LD or RS/RW
Device 2	Output CLKBUS[1]	1 bit	Clock Signal Device 2
	Output RSTBUS[1]	1 bit	Reset Signal Line Device 2
	Output - DTCMDONE	8 bit	Data Input to Device 2 Command/Address
	Input – DTINONE	8 bit	Data Output from Device 2
	Output R3OUTCRL[3:2]	2 bits	OE/LD or RS/RW
Device 3	Output CLKBUS[2]	1 bit	Clock Signal Device 3
	Output RSTBUS[2]	1 bit	Reset Signal Line Device 3
	Output – DTCMDONE	8 bit	Data Input to Device 3 Command/Address
	Input – DTINONE	8 bit	Data Output from Device 3
	Output R3OUTCRL[5:4]	2 bits	OE/LD or RS/RW
Device 4	Output CLKBUS[3]	1 bit	Clock Signal Device 4
	Output RSTBUS[3]	1 bit	Reset Signal Line Device 4
	Output – DTCMDONE	8 bit	Data Input to Device 4 Command/Address
	Input – DTINONE	8 bit	Data Output from Device 4
	Output R3OUTCRL[7:6]	2 bits	OE/LD or RS/RW