Instruction Set

Nomenclature

Registers and Operands

- **Rd** Destination (and source) register
- **Rr** Source register
- **K** Constant data
- **k** Constant address

Status Register

- **C** Carry Flag
- **N** Negative Flag
- **O** Signed Overflow Flag
- **Z** Zero Flag

Instruction Set Summary

Mnemonic	Operands	Operation	Flags	Cycles	Description
ADD	Rd, Rr	Rd ← Rd + Rr	C, N, O, Z	6	Add
AND	Rd, Rr	Rd ← Rd • Rr	N, Z	6	Logical AND
DEC	Rd	Rd ← Rd - 1	C, N, Z	6	Decrement
HLT			None	-	Halt Processor
INC	Rd	Rd ← Rd + 1	C, N, Z	6	Increment
JCA	k	PC ← k	None	2	Branch if Carry Set
JEZ	k	PC ← k	None	2	Branch if Zero Set
JGZ	k	PC ← k	None	2	Branch if Positive
JLZ	k	PC ← k	None	2	Branch if Negative
JMP	k	PC ← k	None	2	Jump
JNZ	k	PC ← k	None	2	Branch if Zero Cleared
JOV	k	PC ← k	None	2	Branch if Overflow Set
LDI	Rd, K	Rd ← K	None	3	Load Immediate
LDR	Rd, k	Rd ← (k)	None	4	Load Indirect
MOV	Rd, Rr	Rd ← Rr	None	3	Copy Register
NEG	Rd	Rd ← – Rd	N, Z	6	Negate
NOP			None	1	No Operation
NOT	Rd	Rd ← ~ Rd	N, Z	6	Logical NOT
OR	Rd, Rr	Rd ← Rd v Rr	N, Z	6	Logical OR
STR	Rr, k	(k) ← Rr	None	3	Store Indirect
SUB	Rd, Rr	Rd ← Rd - Rr	C, N, O, Z	6	Subtract