

COMPILE_ULTRA SETUP		
Report	Parameter	NLDM
report_cell	Top Module cells	8905
get_cells -hierarchical	Total Cells	12509
report_reference	No of References	71
	Levels of Logic	19.00
	Critical Path Length	2.52
report_qor	Critical Path Slack	-2.17
	Total Negative Slack	-1530.18
	No. of Violating Paths	1673.00
	Combinational Area	30519.899043
report_area	Sequential Area	3735.662681
	Buf/Inv Area	10868.468492
	Net Interconnect Area	11089.324808
	Total area (μm^2)	52477.692343
	Internal Power (μW)	1.0597E+04
report_power	Switching Power (μW)	94.9999
	Total Dynamic Power (mW)	10.6916
	Leakage Power (pW)	4.5923E+09
	Total Power (μW)	1.5284E+04
	SETUP	
report_timing	Data Required Time	0.35
	Data Arrival Time	-2.52
	Slack(max) - Setup	-2.17
	HOLD	
	Data Required Time	-0.01
	Data Arrival Time	-0.21
	Slack(min) - Hold	0.22
	HVT	
report_threshold_voltage_group	Cell Count	7 (0.06%)
	Area	8.90 (0.02%)
	Leakage (μW)	27.551nW (0.00%)
	LVT	
	Cell Count	12488 (99.89%)
	Area	41360.16 (99.93%)
	Leakage (μW)	4.592mW (99.99%)
	RVT	
	Cell Count	7 (0.06%)
	Area	19.31 (0.05%)
	Leakage (μW)	613.411nW (0.01%)
report_clock_tree	No of Sinks	1582
	Clock Global Skew	0.000
	Longest Path Delay	0.000
	Shortest Path Delay	0.000

COMPILE_ULTRA

Clk Period: 0.44

WNS: 2.17

TNS: 1530.18

COMPILE_ULTRA HOLD		
Report	Parameter	NLDM
report_cell	Top Module cells	10759
get_cells -hierarchical	Total Cells	14980
report_reference	No of References	114
report_qor	Levels of Logic	17.00
	Critical Path Length	12.91
	Critical Path Slack	-12.49
	Total Negative Slack	-17368.03
	No. of Violating Paths	1803.00
report_area	Combinational Area	32523.061963
	Sequential Area	6949.822004
	Buf/Inv Area	10881.683977
	Net Interconnect Area	8838.696960
	Total area (μm^2)	52243.442900
report_power	Internal Power (μW)	-2.3650E+05
	Switching Power (μW)	265.2399
	Total Dynamic Power (mW)	-236.2357
	Leakage Power (pW)	2.0831E+11
	Total Power (μW)	-2.7922E+04
report_timing	SETUP	
	Data Required Time	0.41
	Data Arrival Time	-12.91
	Slack(max) - Setup	-12.49
	HOLD	
report_threshold_voltage_group	Data Required Time	0.02
	Data Arrival Time	-0.07
	Slack(min) - Hold	0.05
	HVT	
	Cell Count	11410 (76.95%)
report_clock_tree	Area	30005.26(-69.13%)
	Leakage (μW)	7.618mW -3.66%
	LVT	
	Cell Count	2954 (19.92%)
	Area	12440.35 -28.66%
report_clock_tree	Leakage (μW)	199.092mW -95.57%
	RVT	
	Cell Count	463 (3.12%)
	Area	959.14. -2.21%
	Leakage (μW)	1.604mW -0.77%
report_clock_tree	No of Sinks	1582
	Clock Global Skew	0.000
	Longest Path Delay	1524247040.000
	Shortest Path Delay	1524247040.000

COMPILE_ULTRA
Clk Period: 0.44
WNS: 0.00
TNS: 0.00