After Elobrate

Report_Cells

S.No	Cell Name/Refernece	Cell Count	Library	Area	Attributes
1	**GTECH_BUF**	124	Gtech	0	C,u
2	**GTECH_AND2**	387	Gtech	0	C,u
3	**GTECH_OR2**	919	Gtech	0	C,u
4	**GTECH_NOT**	373	Gtech	0	C,u
5	**GTECH_XOR2**	32	Gtech	0	C,u
6	**GTECH_AND3**	4	Gtech	0	U
7	**GTECH_AND4**	12	Gtech	0	U
8	**GTECH_AND5**	4	Gtech	0	U
9	**SEQGEN**	1616		0	N,u
10	**MULT_UNS_OP_3_1_3**	1		0	N,u
11	**LT_TC_OP_32_32_1**	1		0	S,u
12	**LT_UNS_OP_32_32_1**	1		0	S,u
13	**ASH_UNS_UNS_OP**	2		0	S,u
14	**ASHR_TC_UNS_OP**	1		0	S,u
15	**SUB_UNS_OP**	6		0	S,u
16	**LT_TC_OP**	1		0	S,u
17	**LT_UNS_OP**	1		0	S,u
18	**EQ_UNS_OP**	2		0	S,u
19	**SELECT_OP_2**	199		0	S,u
20	**SELECT_OP_3**	35		0	S,u
21	**SELECT_OP_4**	24		0	S,u
22	**SELECT_OP_5**	9		0	S,u
23	**SELECT_OP_6**	5		0	S,u
24	**SELECT_OP_7**	2		0	S,u
25	**SELECT_OP_9**	29		0	S,u
26	**SELECT_OP_11**	8		0	S,u
27	**ADD_UNS_OP**	10		0	S,u
	Total No.of Cells	**3808**		**0**	

Report_Area

S.No	Number of	Count	AREA
1	**Ports**	4129	0
2	**Nets**	15050	0
3	**Cells**	8326	0
4	**combinational cells**	6177	0
5	**sequential cells**	2076	0
6	**macros/black boxes**	0	0
7	**buf/inv**	870	0
8	**references:**	63	0
9	**Net Interconnect**		7809.67614
		TOTAL CELL AREA	**0**
		TOTAL AREA	**7809.67614**

Report_hierarchical

Captured with Xnip

```
picorv32a
   *ADD_UNS_OP_32_3_32
      DW01_add_width32
         GTECH_ADD_ABC                gtech
   *ADD_UNS_OP_32_32_32
      DW01_add_width32
         GTECH_ADD_ABC                gtech
   *ADD_UNS_OP_64_1_64
      DW01_inc_width64
         GTECH_ADD_AB                 gtech
         GTECH_NOT                    gtech
         GTECH_XOR2                   gtech
   *ASHR_TC_UNS_OP_33_5_33
      DW_rightsh                                r
         GTECH_AND2                   gtech
         GTECH_BUF                    gtech
         GTECH_MUX2                   gtech
   *ASH_UNS_UNS_OP_4_2_4
      DW_leftsh                                 r
         GTECH_AND2                   gtech
         GTECH_BUF                    gtech
         GTECH_NOT                    gtech
         GTECH_OR2                    gtech
   *ASH_UNS_UNS_OP_32_5_32
      DW_leftsh                                 r
         GTECH_AND_NOT                gtech
         GTECH_MUX2                   gtech
   *EQ_UNS_OP_32_1_1
      DW01_cmp6_width32
         GTECH_AND_NOT                gtech
         GTECH_NAND2                  gtech
         GTECH_NOR2                   gtech
         GTECH_NOT                    gtech
         GTECH_OR_NOT                 gtech
         GTECH_XNOR2                  gtech
         GTECH_XOR2                   gtech
   *EQ_UNS_OP_32_32_1
      DW01_cmp6_width32
         GTECH_AND_NOT                gtech
         GTECH_NAND2                  gtech
         GTECH_NOR2                   gtech
         GTECH_NOT                    gtech
         GTECH_OR_NOT                 gtech
         GTECH_XNOR2                  gtech
         GTECH_XOR2                   gtech
   *LT_TC_OP_32_32_1
      DW01_cmp2_width32
         GTECH_NAND2                  gtech
         GTECH_NOT                    gtech
         GTECH_OR_NOT                 gtech
         GTECH_XNOR2                  gtech
         GTECH_XOR2                   gtech
   *LT_UNS_OP_32_32_1
      DW01_cmp2_width32
         GTECH_NAND2                  gtech
         GTECH_NOT                    gtech
         GTECH_OR_NOT                 gtech
         GTECH_XNOR2                  gtech
         GTECH_XOR2                   gtech
   *MULT_UNS_OP_3_1_3                               r
      DW02_mult
         GTECH_ADD_ABC                gtech
         GTECH_AND2                   gtech
         GTECH_NOR2                   gtech
         GTECH_NOT                    gtech
         GTECH_OR2                    gtech
         GTECH_XNOR2                  gtech
         GTECH_XOR2                   gtech
   *SUB_UNS_OP_4_1_4
      DW01_dec_width4
         GTECH_OR2                    gtech
         GTECH_XNOR2                  gtech
         GTECH_ZERO                   gtech
   *SUB_UNS_OP_5_1_5
      DW01_dec_width5
         GTECH_OR2                    gtech
         GTECH_XNOR2                  gtech
         GTECH_ZERO                   gtech
   *SUB_UNS_OP_5_3_5
      DW01_sub_width5
         GTECH_ADD_ABC                gtech
         GTECH_NOT                    gtech
   *SUB_UNS_OP_32_1_32
      DW01_dec_width32
         GTECH_OR2                    gtech
         GTECH_XNOR2                  gtech
         GTECH_ZERO                   gtech
   *SUB_UNS_OP_32_32_32
      DW01_sub_width32
         GTECH_ADD_ABC                gtech
         GTECH_NOT                    gtech
   GTECH_AND2                         gtech
   GTECH_AND3                         gtech
   GTECH_AND4                         gtech
   GTECH_AND5                         gtech
   GTECH_BUF                          gtech
   GTECH_NOT                          gtech
   GTECH_OR2                          gtech
   GTECH_XOR2                         gtech
   picorv32_pcpi_fast_mul
      *MULT_TC_OP_33_33_64                          r
         DW02_mult
            GTECH_ADD_AB              gtech
            GTECH_ADD_ABC             gtech
            GTECH_AND2                gtech
            GTECH_BUF                 gtech
            GTECH_NOR2                gtech
            GTECH_NOT                 gtech
            GTECH_OR2                 gtech
            GTECH_XNOR2               gtech
            GTECH_XOR2                gtech
            GTECH_XOR3                gtech
      GTECH_AND2                      gtech
      GTECH_BUF                       gtech
      GTECH_NOT                       gtech
      GTECH_OR2                       gtech
1
```

Report_power -1

S.No	Design	Wire Load Model	Library
1	**picorv32a**	ForQA	saed32rvt_tt0p78vn40c
2	**picorv32_pcpi_fast_mul**	ForQA	saed32rvt_tt0p78vn40c
3	**ASH_UNS_UNS_OP_4_2_4**	ForQA	saed32rvt_tt0p78vn40c
4	**DW_leftsh**	ForQA	saed32rvt_tt0p78vn40c
5	***SUB_UNS_OP_32_32_32**	ForQA	saed32rvt_tt0p78vn40c
6	**DW01_sub_width32**	ForQA	saed32rvt_tt0p78vn40c
7	**ADD_UNS_OP_32_32_32**	ForQA	saed32rvt_tt0p78vn40c
8	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
9	**EQ_UNS_OP_32_32_1**	ForQA	saed32rvt_tt0p78vn40c
10	**DW01_cmp6_width32**	ForQA	saed32rvt_tt0p78vn40c
11	**LT_TC_OP_32_32_1**	ForQA	saed32rvt_tt0p78vn40c
12	**DW01_cmp2_width32**	ForQA	saed32rvt_tt0p78vn40c
13	**LT_UNS_OP_32_32_1**	ForQA	saed32rvt_tt0p78vn40c
14	**DW01_cmp2_width32**	ForQA	saed32rvt_tt0p78vn40c
15	***ASH_UNS_UNS_OP_32_5_32**	ForQA	saed32rvt_tt0p78vn40c
16	**DW_leftsh**	ForQA	saed32rvt_tt0p78vn40c
17	***ASHR_TC_UNS_OP_33_5_33**	ForQA	saed32rvt_tt0p78vn40c
18	**DW_rightsh**	ForQA	saed32rvt_tt0p78vn40c
19	***ADD_UNS_OP_32_3_32**	ForQA	saed32rvt_tt0p78vn40c
20	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
21	***SUB_UNS_OP_4_1_4**	ForQA	saed32rvt_tt0p78vn40c
22	**DW01_dec_width4**	ForQA	saed32rvt_tt0p78vn40c
23	***ADD_UNS_OP_64_1_64**	ForQA	saed32rvt_tt0p78vn40c
24	**DW01_inc_width64**	ForQA	saed32rvt_tt0p78vn40c
25	***SUB_UNS_OP_32_1_32**	ForQA	saed32rvt_tt0p78vn40c
26	**DW01_dec_width32**	ForQA	saed32rvt_tt0p78vn40c
27	***EQ_UNS_OP_32_1_1**	ForQA	saed32rvt_tt0p78vn40c
28	**DW01_cmp6_width32**	ForQA	saed32rvt_tt0p78vn40c
29	**DW01_dec_width32**	ForQA	saed32rvt_tt0p78vn40c
30	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
31	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
32	**DW01_inc_width64**	ForQA	saed32rvt_tt0p78vn40c
33	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
34	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
35	***SUB_UNS_OP_5_3_5**	ForQA	saed32rvt_tt0p78vn40c
36	**DW01_sub_width5**	ForQA	saed32rvt_tt0p78vn40c
37	***SUB_UNS_OP_5_1_5**	ForQA	saed32rvt_tt0p78vn40c
38	**DW01_dec_width5**	ForQA	saed32rvt_tt0p78vn40c
39	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
40	**DW01_add_width32**	ForQA	saed32rvt_tt0p78vn40c
41	***MULT_UNS_OP_3_1_3**	ForQA	saed32rvt_tt0p78vn40c
42	**DW02_mult**	ForQA	saed32rvt_tt0p78vn40c
43	***MULT_TC_OP_33_33_64**	ForQA	saed32rvt_tt0p78vn40c
44	**DW02_mult**	ForQA	saed32rvt_tt0p78vn40c
		ENCLOSED	

Operating Conditions: tt0p78vn40c

Report Power-2

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
io_pad	0.0000	0.0000	0.0000	0.0000	0.00%	
memory	0.0000	0.0000	0.0000	0.0000	0.00%	
black_box	0.0000	0.0000	0.0000	0.0000	0.00%	
clock_network	0.0000	0.0000	0.0000	0.0000	0.00%	I
register	0.0000	0.0000	0.0000	0.0000	0.00%	
sequential	0.0000	1.5485	0.0000	1.5485	9.66%	
combinational	0.0000	14.4761	0.0000	14.4761	90.34%	
Total		**16.0246**	**0.0000**	**16.0246**	**100.00%**	

Report-Wire load Model -1

Wire load model	**ForQA**
Location	**picorv32a (design)**
Resistance	**0.002067**
Capacitance	**0.026724**
Area	**0.01**
Slope	**30.2854**

Report-Wire load Model -2

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	8.28				
2	2	18.49				
3	3	29.35				
4	4	40.92				
5	5	53.23				
6	6	66.36				
7	7	80.36				
8	8	95.27				
9	9	111.17				
10	10	128.09				
11	11	146.10				
12	12	165.26				
13	13	185.61				
14	14	207.22				
15	15	230.13				
16	16	254.41				
17	17	280.11				
18	18	307.28				
19	19	335.98				
20	20	366.27				
	Total Length	**3109.89**				

Report- Threshold Voltage Group

S.No	Vth Group Name->	undefined
2	**All Cells**	6504 (100.00%)
3	**Blackbox Cells**	0 (0.00%)
4	**Non-Blackbox cells**	6504 (100.00%)
5	**All Cells Area**	0 (0.00%)
6	**Blackbox Cells area**	0 (0.00%)
7	**Non-Blackbox cells area**	0 (0.00%)
8	**All Cells leakage**	0 (0.00%)
9	**Blackbox Cells leakage**	0 (0.00%)
10	**Non-Blackbox cells leakage**	0 (0.00%)

Report-qor

S.No		
	Timing Path Group (none)	
1	Levels of Logic:	0.00
2	Critical Path Length:	0.04
3	Critical Path Slack:	uninit
4	Critical Path Clk Period:	n/a
5	Total Negative Slack:	0.00
6	No. of Violating Paths:	0.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	51
11	Hierarchical Port Count:	3720
12	Leaf Cell Count:	8253
13	Buf/Inv Cell Count:	870
14	Buf Cell Count:	345
15	Inv Cell Count:	525
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	6504
	Area	
18	Combinational Area:	0.000000
19	Noncombinational Area:	0.000000
20	Total Inverter Area:	0.000000
21	Macro/Black Box Area:	0.000000
22	Net Area	7809.676140
	Cell Area:	**0.000000**
	Design Area:	**7809.676140**
	Design Rules	
	Total Number of Nets:	11380
	Nets With Violations:	0
	Max Trans Violations:	0
	Max Cap Violations:	0

After read.sdc

Report_clock

S.No	Clock	Period	Waveform	Attr	Source
1	Clk	6	{0,3}		{clk}

Report_timing - 1

S.No		
	Startpoint:	resetn (input port clocked by clk)
	Endpoint:	mem_la_write (output port clocked by clk)
	Path Group:	Clk
	Path Type:	max

Report_timing-2

Des/Clust/Port	Wire Load Model	Library
picorv32a	ForQA	saed32rvt_tt0p78vn40c

Report_timing -3

S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	1.00	1.00	
3	input external delay	1.30	2.30	r
4	resetn (in)	0.00	2.30	r
5	C12644/Z (GTECH_AND2)	0.01	2.31	r
6	C12643/Z (GTECH_AND2)	0.00	2.32	r
7	mem_la_write (out)	0.01	2.33	r
8	data arrival time		2.33	
9	clock clk (rise edge)	6.00	6.00	
10	clock network delay (ideal)	1.00	7.00	
11	clock uncertainty	-1.00	6.00	
12	output external delay	-1.30	4.70	
13	data required time		4.70	
14	clock clk (rise edge)	0.00	0.00	
15	clock network delay (ideal)	1.00	1.00	
	clock uncertainty	-1.00	6.00	
	output external delay	-1.30	4.70	
	data required time		4.70	
	data required time	4.70		
	data arrival time	-2.33		
	slack (MET)	2.37		

Report_clock_tree Global Skew Report

S.No		
1	Clock Tree Name	"clk"
2	Clock Period	6.00000
3	Clock Tree root pin	"clk"
4	Number of Levels	1
5	Number of Sinks	1681
6	Number of CT Buffers	0
7	Number of CTS added gates	0
8	Number of Preexisting Gates	0
9	Number of Preexisting Buf/Inv	0
10	Total Number of Clock Cells	0
11	Total Area of CT Buffers	0.00000
12	Total Area of CT cells	0.00000
13	Max Global Skew	0.00000
14	Number of MaxTran Violators	0
15	Number of MaxCap Violators	1
16	Number of MaxFanout Violators	0
17	Clock Tree Name	"clk"
18	Clock Period	6.00000
19	Clock Tree root pin	"clk"
20	Number of Levels	1
21	Number of Sinks	1681
1	Operating Condition	worst
2	Clock global Skew	0.000
3	Longest path delay	0.050
4	Shortest path delay	0.050

The longest path delay end pin: genblk1.pcpi_mul/rd_reg[63]/clocked_on
The shortest path delay end pin: genblk1.pcpi_mul/rd_reg[63]/clocked_on

Clock_tree Longest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001802.875	1681	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/clocked_on	1001802.875	0	0	0.050	0.050	r
	Clock Delay					0.05	

Clock_tree Shortest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001802.875	1681	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/clocked_on	1001802.875	0	0	0.050	0.050	r
	Clock Delay					0.05	

After Compile

Report_cell (compile)

S.No	Reference	Cell Count	Library	Area	Total Area For Each cell	Attributes
1	AND2X1_RVT	234	saed32rvt_tt0p78vn40c	2.033152	475.757568	
2	AND2X2_RVT	5	saed32rvt_tt0p78vn40c	2.287296	11.43648	
3	AND2X4_RVT	6	saed32rvt_tt0p78vn40c	2.795584	16.773504	
4	AND3X1_RVT	37	saed32rvt_tt0p78vn40c	2.287296	84.629952	
5	AND4X1_RVT	27	saed32rvt_tt0p78vn40c	2.541440	68.61888	
6	AO21X1_RVT	105	saed32rvt_tt0p78vn40c	2.541440	266.8512	
7	AO221X1_RVT	221	saed32rvt_tt0p78vn40c	3.049728	673.989888	
8	AO221X2_RVT	8	saed32rvt_tt0p78vn40c	3.303872	26.430976	
9	AO222X1_RVT	200	saed32rvt_tt0p78vn40c	3.303872	660.7744	
10	AO22X1_RVT	1034	saed32rvt_tt0p78vn40c	2.541440	2627.84896	
11	AO22X2_RVT	82	saed32rvt_tt0p78vn40c	2.795584	229.237888	
12	AO31X1_RVT	8	saed32rvt_tt0p78vn40c	3.049728	24.397824	
13	AOI221X1_RVT	27	saed32rvt_tt0p78vn40c	3.558016	96.066432	
14	AOI222X1_RVT	28	saed32rvt_tt0p78vn40c	3.812160	106.74048	
15	decoder_pseudo_trigger_reg	1		6.607744	6.607744	n
16	DELLN3X2_RVT	2	saed32rvt_tt0p78vn40c	9.657472	19.314944	
17	DFFX1_RVT	1432	saed32rvt_tt0p78vn40c	6.607744	9462.289408	n
18	DFFX2_RVT	34	saed32rvt_tt0p78vn40c	7.116032	241.945088	n
19	IBUFFX16_RVT	2	saed32rvt_tt0p78vn40c	6.607744	13.215488	
20	IBUFFX2_RVT	3	saed32rvt_tt0p78vn40c	2.541440	7.62432	
21	INVX0_RVT	40	saed32rvt_tt0p78vn40c	1.270720	50.8288	
22	INVX1_RVT	465	saed32rvt_tt0p78vn40c	1.270720	590.8848	
23	INVX2_RVT	65	saed32rvt_tt0p78vn40c	1.524864	99.11616	
24	INVX4_RVT	44	saed32rvt_tt0p78vn40c	2.033152	89.458688	
25	INVX8_RVT	1	saed32rvt_tt0p78vn40c	3.049728	3.049728	
26	is_beq_bne_blt_bge_bltu_bgeu_reg	1		6.607744	6.607744	n
27	is_jalr_addi_slti_sltiu_xori_ori_andi_reg	1		6.607744	6.607744	n
28	is_lui_auipc_jal_jalr_addi_add_sub_reg	1		6.607744	6.607744	n
29	LATCHX1_RVT	68	saed32rvt_tt0p78vn40c	5.082880	345.63584	
30	MUX21X1_RVT	297	saed32rvt_tt0p78vn40c	3.303872	981.249984	
31	MUX21X2_RVT	1	saed32rvt_tt0p78vn40c	3.558016	3.558016	
32	NAND2X0_RVT	189	saed32rvt_tt0p78vn40c	1.524864	288.199296	
33	NAND3X0_RVT	69	saed32rvt_tt0p78vn40c	1.779008	122.751552	
34	NAND3X2_RVT	3	saed32rvt_tt0p78vn40c	3.049728	9.149184	
35	NAND4X0_RVT	120	saed32rvt_tt0p78vn40c	2.033152	243.97824	
36	NBUFFX2_RVT	130	saed32rvt_tt0p78vn40c	2.033152	264.30976	
37	NBUFFX4_RVT	2	saed32rvt_tt0p78vn40c	2.541440	5.08288	
38	NBUFFX8_RVT	1	saed32rvt_tt0p78vn40c	3.812160	3.81216	
39	NOR2X0_RVT	4	saed32rvt_tt0p78vn40c	2.541440	10.16576	
40	NOR3X0_RVT	5	saed32rvt_tt0p78vn40c	2.795584	13.97792	
41	NOR4X1_RVT	13	saed32rvt_tt0p78vn40c	3.049728	39.646464	
42	OA21X1_RVT	11	saed32rvt_tt0p78vn40c	2.541440	27.95584	
43	OA221X1_RVT	170	saed32rvt_tt0p78vn40c	3.049728	518.45376	
44	OA222X1_RVT	145	saed32rvt_tt0p78vn40c	3.303872	479.06144	
45	OA22X1_RVT	54	saed32rvt_tt0p78vn40c	2.541440	137.23776	
46	OAI21X1_RVT	36	saed32rvt_tt0p78vn40c	3.049728	109.790208	
47	OAI221X1_RVT	2	saed32rvt_tt0p78vn40c	3.558016	7.116032	
48	OAI222X1_RVT	8	saed32rvt_tt0p78vn40c	3.812160	30.49728	
49	OAI22X1_RVT	15	saed32rvt_tt0p78vn40c	3.049728	45.74592	
50	OR2X1_RVT	23	saed32rvt_tt0p78vn40c	2.033152	46.762496	
51	OR2X2_RVT	1	saed32rvt_tt0p78vn40c	2.287296	2.287296	
52	OR2X4_RVT	1	saed32rvt_tt0p78vn40c	2.795584	2.795584	
53	OR3X1_RVT	6	saed32rvt_tt0p78vn40c	2.541440	15.24864	
54	OR4X1_RVT	21	saed32rvt_tt0p78vn40c	3.558016	74.718336	
55	pcpi_timeout_counter_reg[0]	1		6.607744	6.607744	n
56	pcpi_timeout_counter_reg[1]	1		6.607744	6.607744	n
57	pcpi_timeout_counter_reg[2]	1		6.607744	6.607744	n
58	pcpi_timeout_counter_reg[3]	1		6.607744	6.607744	n
59	picorv32_pcpi_fast_mul	1		9382.742271	9382.742271	h,n
60	picorv32a_DW_cmp_0	1		242.961665	242.961665	BO,h
61	picorv32a_DW01_add_5	1		158.585851	158.585851	BO,h
62	picorv32a_DW01_cmp6_0	1		198.994753	198.994753	BO,h
63	picorv32a_DW01_dec_0_DW01_dec_1	1		181.458819	181.458819	BO,h
64	picorv32a_DW01_sub_0	1		200.011323	200.011323	n
	Total Cells = 5058	**5519**			**30194.086138**	

Report_Area

S.No	Number of	Count	Area
1	**Number of ports:**	1919	
2	**Number of nets:**	12431	
3	**Number of cells:**	9037	
4	**Number of combinational cells:**	7797	
5	**Number of sequential cells:**	1667	
6	**Number of macros/black boxes:**	0	
7	**Number of buf/inv:**	1458	
8	**Number of references:**	69	
9	**Combinational area:**		21094.460267
10	**Buf/Inv area:**		2076.356500
11	**Noncombinational area:**		10929.208921
12	**Macro/Black Box area:**		0.000000
13	**Net Interconnect area:**		4328.556079
	Total Cell Area		**32023.669188**
	Total Area		**36352.225267**

Report_power-1

S.No	Design	Wire Load Model	Library
1	**picorv32a**	ForQA	saed32rvt_tt0p78vn40c
2	**picorv32_pcpi_fast_mul**	ForQA	saed32rvt_tt0p78vn40c
3	**picorv32a_DW01_add_0**	ForQA	saed32rvt_tt0p78vn40c
4	**picorv32a_DW01_add_1**	ForQA	saed32rvt_tt0p78vn40c
5	**picorv32a_DW01_add_2**	ForQA	saed32rvt_tt0p78vn40c
6	**picorv32a_DW01_add_3**	ForQA	saed32rvt_tt0p78vn40c
7	**picorv32a_DW_cmp_0**	8000	saed32rvt_tt0p78vn40c
8	**picorv32a_DW01_add_4**	ForQA	saed32rvt_tt0p78vn40c
9	**picorv32a_DW01_sub_0**	ForQA	saed32rvt_tt0p78vn40c
10	**picorv32a_DW01_add_5**	ForQA	saed32rvt_tt0p78vn40c
11	**picorv32a**	ForQA	saed32rvt_tt0p78vn40c
12	**picorv32a_DW01_dec_0_DW01_dec_1**	ForQA	saed32rvt_tt0p78vn40c
13	**picorv32a_DW01_cmp6_0**	ForQA	saed32rvt_tt0p78vn40c
14	**picorv32a_DW01_add_6**	ForQA	saed32rvt_tt0p78vn40c
15	**picorv32_pcpi_fast_mul_DW_mult_tc_1**	16000	saed32rvt_tt0p78vn40c
16	**picorv32a_DW01_inc_2**	8000	saed32rvt_tt0p78vn40c
17	**picorv32a_DW01_inc_3**	8000	saed32rvt_tt0p78vn40c

Cell Internal Power = 984.6401 uW (99%)
Net Switching Power = 10.8277 uW (1%)

Total Dynamic Power = 995.4677 uW (100%)
Cell Leakage Power = 56.1337 uW

Report-power-2

S.No	Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
1	**io_pad**	0.0000	0.0000	0.0000	0.0000	0.00%	
2	**memory**	0.0000	0.0000	0.0000	0.0000	0.00%	
3	**black_box**	0.0000	0.0000	0.0000	0.0000	0.00%	
4	**clock_network**	972.4143	0.0000	0.0000	972.4143	-92.47%	i
5	**register**	4.6282	1.7049	3.0705E-07	37.0496	-3.52%	
6	**sequential**	0.6379	0.1417	1.1301E-06	1.9096	-0.18%	
7	**combinational**	6.9592	8.9811	2.4299E-07	40.2390	-3.83%	
	Total (uW)	**984.6396**	**10.8277**	**56134100.0000**	**1051.6125**		

Report-Wire load Model FORQA (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	8.28				
2	2	18.49				
3	3	29.35				
4	4	40.92				
5	5	53.23				
6	6	66.36				
7	7	80.36				
8	8	95.27				
9	9	111.17				
10	10	128.09				
11	11	146.10				
12	12	165.26				
13	13	185.61				
14	14	207.22				
15	15	230.13				
16	16	254.41				
17	17	280.11				
18	18	307.28				
19	19	335.98				
20	20	366.27				
	Total Length	**3109.89**				

Report_clock_tree Global Skew Report

S.No		
1	**Clock Tree Name :**	"clk"
2	**Clock Period :**	6.000000
3	**Clock Tree root pin :**	"clk"
4	**Number of Levels :**	1
5	**Number of Sinks :**	1599
6	**Number of CT Buffers :**	0
7	**Number of CTS added gates :**	0
8	**Number of Preexisting Gates :**	0
9	**Number of Preexisting Buf/Inv :**	0
10	**Total Number of Clock Cells :**	0
11	**Total Area of CT Buffers :**	0.000000
12	**Total Area of CT cells :**	0.000000
13	**Max Global Skew :**	0.000072
14	**Number of MaxTran Violators :**	0
15	**Number of MaxCap Violators :**	1
16	**Number of MaxFanout Violators :**	0
1	**Operating Condition**	worst
2	**Clock global Skew**	0.001
3	**Longest path delay**	0.124
4	**Shortest path delay**	0.123

Report-Wire load Model -8000 (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	13.94				
2	2	31.80				
3	3	51.61				
4	4	73.61				
5	5	98.05				
6	6	125.17				
7	7	155.23				
8	8	188.46				
9	9	225.12				
10	10	265.45				
11	11	309.71				
12	12	358.13				
13	13	410.96				
14	14	468.46				
15	15	530.86				
16	16	598.42				
17	17	671.38				
18	18	749.98				
19	19	834.49				
20	20	925.13				
	Total Length	**7065.96**				

The longest path delay end pin: genblk1.pcpi_mul/active_reg[1]/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rs2_reg[31]/CLK

Clock_tree Longest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri
1	**clk**	0	1	0	0	0 r
2	**clk**	1001037.500	1599	0	0	0 r
3	**genblk1.pcpi_mul/rd_reg[03]/clocked_on**	1001037.500	0	0	0.124	0.124 r
	Clock Delay					0.124

Clock_tree Shortest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri
1	**clk**	0	1	0	0	0 r
2	**clk**	1001037.500	1599	0	0	0 r
3	**genblk1.pcpi_mul/rd_reg[03]/clocked_on**	1001037.500	0	0	0.123	0.123 r
	Clock Delay					0.123

Report-Wire load Model - 16000(Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8138.84**				

Report-qor (Compile)

S.No	Timing Path Group (none)	
1	Levels of Logic:	38.00
2	Critical Path Length:	5.82
3	Critical Path Slack:	-0.86
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	-9.26
6	No. of Violating Paths:	24.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	15
11	Hierarchical Port Count:	1510
12	Leaf Cell Count:	9464
13	Buf/Inv Cell Count:	1458
14	Buf Cell Count:	146
15	Inv Cell Count:	1312
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	7797
	Area	
18	Combinational Area:	21094.460267
19	Noncombinational Area:	10929.208921
20	Buf/Inv Area:	2076.356500
21	Total Buffer Area:	322.51
22	Total Inverter Area:	1753.85
	Macro/Black Box Area:	0.000000
	Net Area:	4328.556079
	Cell Area:	**32023.669188**
	Design Area:	**36352.225267**
	Design Rules	
	Max Trans Violations:	25
	Max Cap Violations:	0

Report_timing - 1 (Compile)

S.No		
1	**Startpoint:**	latched_stalu_reg (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	reg_next_pc_reg[31](rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	max

Report_timing-2 (Compile)

Des/Clust/Port	Wire Load Model	Library
picorv32a	ForQA	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_1	ForQA	saed32rvt_tt0p78vn40c

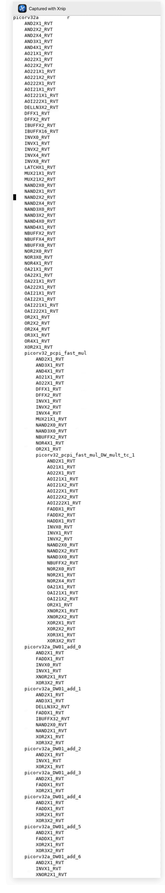
report_timing(Compile)

S.No	Point	Incr	Path
1	**clock clk (rise edge)**	0.00	0.00
2	**clock network delay (ideal)**	1.00	1.00
3	**latched_stalu_reg/CLK (DFFX2_RVT)**	0.00 #	1.00 r
4	**latched_stalu_reg/QN (DFFX2_RVT)**	0.28	1.28 f
5	**U46227/Y (NAND2X0_RVT)**	0.10	1.38 r
6	**U5842/Y (OAI222X1_RVT)**	0.18	1.56 f
7	**U45667/Y (MUX21X2_RVT)**	0.13	1.69 f
8	**U4629/Y (AND2X1_RVT)**	0.11	1.79 f
9	**add_1547/A[1] (picorv32a_DW01_add_1)**	0.00	1.79 f
10	**add_1547/U1/Y (AND2X1_RVT)**	0.10	1.89 f
11	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.15	2.04 f
12	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	2.20 f
13	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	2.36 f
14	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	2.51 f
15	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	2.67 f
16	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	2.83 f
17	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	2.99 f
18	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	3.15 f
19	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	3.30 f
20	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	3.46 f
21	**add_1547/A1/U1/CO (FADDX1_RVT)**	0.16	3.62 f
22	**add_1547/A1/U3/S (FADDX1_RVT)**	0.16	3.78 f
23	**add_1547/A1/U4/CO (FADDX1_RVT)**	0.16	3.94 f
24	**add_1547/A1/U5/CO (FADDX1_RVT)**	0.16	4.09 f
25	**add_1547/A1/U6/CO (FADDX1_RVT)**	0.16	4.25 f
26	**add_1547/A1/U7/CO (FADDX1_RVT)**	0.16	4.41 f
27	**add_1547/A1/U8/CO (FADDX1_RVT)**	0.16	4.57 f
28	**add_1547/A1/U9/CO (FADDX1_RVT)**	0.16	4.73 f
29	**add_1547/A1/U10/CO (FADDX1_RVT)**	0.16	4.88 f
30	**add_1547/A1/U11/CO (FADDX1_RVT)**	0.16	5.04 f
31	**add_1547/A1/U22/CO (FADDX1_RVT)**	0.16	5.20 f
32	**add_1547/A1/U23/CO (FADDX1_RVT)**	0.16	5.36 f
33	**add_1547/A1/U24/CO (FADDX1_RVT)**	0.16	5.52 f
34	**add_1547/A1/U25/CO (FADDX1_RVT)**	0.16	5.68 f
35	**add_1547/A1/U26/CO (FADDX1_RVT)**	0.16	5.83 f
36	**add_1547/A1/U27/CO (FADDX1_RVT)**	0.16	5.99 f
37	**add_1547/A1/U28/CO (FADDX1_RVT)**	0.16	6.15 f
38	**add_1547/A1/U29/CO (FADDX1_RVT)**	0.17	6.32 f
39	**add_1547/U7/Y (NAND2X0_RVT)**	0.09	6.41 r
40	**add_1547/U4/Y (AND2X1_RVT)**	0.12	6.52 r
41	**add_1547/U2/Y (XOR3X2_RVT)**	0.12	6.64 f
42	**add_1547/SUM[31] (picorv32a_DW01_add_1)**	0.00	6.64 f
43	**U5911/Y (NAND2X0_RVT)**	0.09	6.73 r
44	**U5917/Y (NAND3X0_RVT)**	0.08	6.81 f
45	**reg_next_pc_reg[31]/D (DFFX1_RVT)**	0.01	6.82 f
	data arrival time		6.82
	clock clk (rise edge)	6.00	6.00
	clock network delay (ideal)	1.00	7.00
	clock uncertainty	-1.00	6.00
	reg_next_pc_reg[31]/CLK (DFFX1_RVT)	0.00	6.00
	library setup time	-0.04	5.96
	data required time		5.96
	data required time		5.96
	data arrival time		-6.82
	slack (VIOLATED)		**-0.86**

Report- Threshold Voltage Group-compile

S.No	Vth Group Name->	saed32cell_svt
2	**All Cells**	9464 (100.00%)
3	**Blackbox Cells**	0 (0.00%)
4	**Non-Blackbox cells**	9464 (100.00%)
5	**All Cells Area**	32023.67 (100.00%)
6	**Blackbox Cells area**	0 (0.00%)
7	**Non-Blackbox cells area**	32023.67 (100.00%)
8	**All Cells leakage**	56.134uW (100.00%)
9	**Blackbox Cells leakage**	0 (0.00%)
10	**Non-Blackbox cells leakage**	0 056.134uW (100.00%)00%

Report_hierarchical



After Compile Ultra

Report-cell

S.No	Reference	Library	Area	Count	Total Area	Attributes
1	AND2X1_RVT	saed32rvt_ttf0p78vn40c	2.033152	416	845.791275	
2	AND2X2_RVT	saed32rvt_ttf0p78vn40c	2.287296	23	52.607809	
3	AND2X4_RVT	saed32rvt_ttf0p78vn40c	2.795584	1	2.795584	
4	AND3X1_RVT	saed32rvt_ttf0p78vn40c	2.287296	59	134.950467	
5	AND3X2_RVT	saed32rvt_ttf0p78vn40c	2.541440	3	7.624320	
6	AND4X1_RVT	saed32rvt_ttf0p78vn40c	2.541440	30	76.243200	
7	AO21X1_RVT	saed32rvt_ttf0p78vn40c	2.541440	107	271.934081	
8	AO22X1_RVT	saed32rvt_ttf0p78vn40c	2.541440	1469	3733.375375	
9	AO221X1_RVT	saed32rvt_ttf0p78vn40c	3.049728	19	57.944830	
10	AO222X1_RVT	saed32rvt_ttf0p78vn40c	3.303872	87	287.436873	
11	AOI21X1_RVT	saed32rvt_ttf0p78vn40c	3.049728	77	234.829050	
12	AOI22X1_RVT	saed32rvt_ttf0p78vn40c	3.049728	148	451.359732	
13	AOI222X2_RVT	saed32rvt_ttf0p78vn40c	4.066304	1	4.066304	
14	DFFSSRX1_RVT	saed32rvt_ttf0p78vn40c	7.116032	15	106.740482	n
15	DFFSSRX2_RVT	saed32rvt_ttf0p78vn40c	7.624320	1	7.624320	n
16	DFFX1_RVT	saed32rvt_ttf0p78vn40c	6.607744	1431	9455.681974	n
17	DFFX2_RVT	saed32rvt_ttf0p78vn40c	7.116032	2	14.232064	n
18	FADDX1_RVT	saed32rvt_ttf0p78vn40c	4.828736	49	236.608056	r
19	HADDX1_RVT	saed32rvt_ttf0p78vn40c	3.303872	49	161.889733	r
20	INVX0_RVT	saed32rvt_ttf0p78vn40c	1.270720	446	566.741122	
21	INVX2_RVT	saed32rvt_ttf0p78vn40c	1.524864	58	88.442110	
22	INVX4_RVT	saed32rvt_ttf0p78vn40c	2.033152	14	28.464129	
23	LATCHX1_RVT	saed32rvt_ttf0p78vn40c	5.082880	68	345.635841	n
24	MUX21X1_RVT	saed32rvt_ttf0p78vn40c	3.303872	11	36.342593	
25	NAND2X0_RVT	saed32rvt_ttf0p78vn40c	1.524864	516	786.829803	
26	NAND2X2_RVT	saed32rvt_ttf0p78vn40c	2.795584	1	2.795584	
27	NAND2X4_RVT	saed32rvt_ttf0p78vn40c	3.303872	2	6.607744	
28	NAND3X0_RVT	saed32rvt_ttf0p78vn40c	1.779008	158	281.083269	
29	NAND3X2_RVT	saed32rvt_ttf0p78vn40c	3.049728	3	9.149184	
30	NAND4X0_RVT	saed32rvt_ttf0p78vn40c	2.033152	65	132.154887	
31	NBUFFX2_RVT	saed32rvt_ttf0p78vn40c	2.033152	4	8.132608	
32	NBUFFX4_RVT	saed32rvt_ttf0p78vn40c	2.541440	1	2.541440	
33	NOR2X0_RVT	saed32rvt_ttf0p78vn40c	2.541440	307	780.222083	
34	NOR2X2_RVT	saed32rvt_ttf0p78vn40c	2.795584	4	11.182336	
35	NOR2X4_RVT	saed32rvt_ttf0p78vn40c	3.303872	1	3.303872	
36	NOR3X0_RVT	saed32rvt_ttf0p78vn40c	2.795584	19	53.116095	
37	NOR4X0_RVT	saed32rvt_ttf0p78vn40c	3.049728	106	323.271159	
38	OA21X1_RVT	saed32rvt_ttf0p78vn40c	2.541440	87	221.105281	
39	OA21X2_RVT	saed32rvt_ttf0p78vn40c	2.795584	1	2.795584	
40	OA22X1_RVT	saed32rvt_ttf0p78vn40c	2.541440	113	287.182721	
41	OA221X1_RVT	saed32rvt_ttf0p78vn40c	3.049728	10	30.497279	
42	OA221X2_RVT	saed32rvt_ttf0p78vn40c	3.303872	1	3.303872	
43	OA222X1_RVT	saed32rvt_ttf0p78vn40c	3.303872	6	19.823233	
44	OAI21X1_RVT	saed32rvt_ttf0p78vn40c	3.049728	147	448.310004	
45	OAI21X2_RVT	saed32rvt_ttf0p78vn40c	3.303872	1	3.303872	
46	OAI22X1_RVT	saed32rvt_ttf0p78vn40c	3.049728	109	332.420343	
47	OAI221X1_RVT	saed32rvt_ttf0p78vn40c	3.558016	3	10.674048	
48	OR2X1_RVT	saed32rvt_ttf0p78vn40c	2.033152	232	471.691288	
49	OR2X2_RVT	saed32rvt_ttf0p78vn40c	2.287296	2	4.574592	
50	OR3X1_RVT	saed32rvt_ttf0p78vn40c	2.541440	84	213.480961	
51	OR3X2_RVT	saed32rvt_ttf0p78vn40c	2.541440	27	68.618880	
52	OR4X1_RVT	saed32rvt_ttf0p78vn40c	3.558016	12	42.696193	
53	XNOR2X1_RVT	saed32rvt_ttf0p78vn40c	4.320448	88	380.199417	
54	XNOR3X1_RVT	saed32rvt_ttf0p78vn40c	6.099456	18	109.790205	
55	XOR2X1_RVT	saed32rvt_ttf0p78vn40c	4.320448	91	393.160761	
56	XOR3X1_RVT	saed32rvt_ttf0p78vn40c	7.116032	2	14.232064	
57	picorv32_pcpi_fast_mul	saed32rvt_ttf0p78vn40c	9466.355615	1	9466.355615	h, n
	TOTAL			**9651.118303**	**6806**	**32133.967601**

Report-area (Compile Ultra)

S.No		Area	Count
1	**Number of ports:**		543
2	**Number of nets:**		10793
3	**Number of cells:**		9651
4	**Number of combinational cells:**		7982
5	**Number of sequential cells:**		1650
6	**Number of macros/black boxes:**		0
7	**Number of buf/inv:**		845
8	**Number of references:**		57
9	**Combinational area:**	21324.206365	
10	**Buf/Inv area:**	1146.951876	
11	**Noncombinational area:**	10809.761239	
12	**Macro/Black Box area:**	0.000000	
13	**Net Interconnect area:**	12089.423766	
	Total cell area:	**32133.967604**	
	Total area:	**44223.391370**	

Report_power-1 (Compile Ultra)

S.No	Design	Wire Load Model	Library
1	**picorv32a**	35000	saed32rvt_ttf0p78vn40c
2	**picorv32_pcpi_fast_mul**	16000	saed32rvt_ttf0p78vn40c

Report-power-2 (compile ultra)

S.No	Power Group	Internal Power	Switching Power	Total Power	Leakage Power	Percentage	Attributes
1	**io_pad**	0.0000	0.0000	0.0000	0.0000	0.00%	
2	**memory**	0.0000	0.0000	0.0000	0.0000	0.00%	
3	**black_box**	0.0000	0.0000	0.0000	0.0000	0.00%	
4	**clock_network**	961.6392	0.0000	0.0000	961.6392	92.83%	i
5	**register**	3.9210	1.0050	2.99E+07	34.8283	3.36%	
6	**sequential**	0.5208	9.8819E-02	1.1326E+06	1.7523	0.17%	
7	**combinational**	6.4399	4.5740	2.6639E+07	37.6528	3.63%	
	Total (uW)	**972.5209**	**5.6778**	**5.7671e+07 pW**	**1.0359E+03**		
		Total Dynamic Power	**978.1987**				

```
Cell Internal Power  = 972.5272 uW   (99%)
Net Switching Power  =   5.6778 uW   (1%)
                       ---------
Total Dynamic Power  = 978.2050 uW  (100%)
Cell Leakage Power   =  57.6712 uW
```

Report_timing - 1 (Compile ultra)

S.No		
1	**Startpoint:**	genblk1.pcpi_mul/rs2_reg[10] rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	genblk1.pcpi_mul/rs2_reg[63] (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	max

Report_timing-2 (Compile ultra)

Des/Clust/Port	Wire Load Model	Library
picorv32a	**35000**	**saed32rvt_ttf0p78vn40c**
picorv32_pcpi_fast_mul	**16000**	**saed32rvt_ttf0p78vn40c**

Report_timing -3 (Compile ultra)

S.No	Point	Incr	Path
1	**clock clk (rise edge)**	0.00	0.00
2	**clock network delay (ideal)**	1.00	1.00
3	**genblk1.pcpi_mul/rs2_reg[10]/CLK (DFFX1_RVT)**	0.00 #	1.00 r
4	**genblk1.pcpi_mul/rs2_reg[10]/QN (DFFX1_RVT)**	0.29	1.29 f
5	**genblk1.pcpi_mul/U816/Y (INVX4_RVT)**	0.15	1.44 r
6	**genblk1.pcpi_mul/U817/Y (NOR2X0_RVT)**	0.19	1.63 f
7	**genblk1.pcpi_mul/U819/Y (NOR2X0_RVT)**	0.12	1.75 r
8	**genblk1.pcpi_mul/U833/Y (AOI21X1_RVT)**	0.12	1.88 f
9	**genblk1.pcpi_mul/U834/Y (INVX0_RVT)**	0.05	1.93 r
10	**genblk1.pcpi_mul/U841/Y (AOI21X1_RVT)**	0.10	2.03 r
11	**genblk1.pcpi_mul/U842/Y (AOI21X1_RVT)**	0.10	2.13 f
12	**genblk1.pcpi_mul/U47/Y (INVX2_RVT)**	0.09	2.22 r
13	**genblk1.pcpi_mul/U1156/Y (AO21X1_RVT)**	0.13	2.36 r
14	**genblk1.pcpi_mul/U753/Y (XOR2X1_RVT)**	0.23	2.59 f
15	**genblk1.pcpi_mul/U1878/Y (OAI21X1_RVT)**	0.20	2.79 r
16	**genblk1.pcpi_mul/U374/Y (XOR2X1_RVT)**	0.19	2.98 f
17	**genblk1.pcpi_mul/U1898/S (FADDX1_RVT)**	0.27	3.25 r
18	**genblk1.pcpi_mul/U1892/CO (FADDX1_RVT)**	0.15	3.40 r
19	**genblk1.pcpi_mul/U2302/CO (FADDX1_RVT)**	0.15	3.55 r
20	**genblk1.pcpi_mul/U2308/CO (FADDX1_RVT)**	0.17	3.72 r
21	**genblk1.pcpi_mul/U2325/Y (XOR3X1_RVT)**	0.29	4.01 f
22	**genblk1.pcpi_mul/U2309/Y (NOR2X0_RVT)**	0.14	4.14 r
23	**genblk1.pcpi_mul/U208/Y (OAI21X1_RVT)**	0.15	4.30 f
24	**genblk1.pcpi_mul/U2321/Y (AOI21X1_RVT)**	0.16	4.45 r
25	**genblk1.pcpi_mul/U757/Y (OAI21X1_RVT)**	0.15	4.60 f
26	**genblk1.pcpi_mul/U2350/Y (AO21X1_RVT)**	0.12	4.72 f
27	**genblk1.pcpi_mul/U2351/Y (AO21X1_RVT)**	0.08	4.80 f
28	**genblk1.pcpi_mul/U2353/Y (AO22X1_RVT)**	0.10	4.90 f
29	**genblk1.pcpi_mul/U2378/CO (FADDX1_RVT)**	0.16	5.06 f
30	**genblk1.pcpi_mul/U2354/CO (FADDX1_RVT)**	0.16	5.22 f
31	**genblk1.pcpi_mul/U2356/Y (AO22X1_RVT)**	0.11	5.33 f
32	**genblk1.pcpi_mul/U2364/CO (FADDX1_RVT)**	0.17	5.50 f
33	**genblk1.pcpi_mul/U2373/Y (AO22X1_RVT)**	0.10	5.60 f
34	**genblk1.pcpi_mul/U2377/CO (FADDX1_RVT)**	0.15	5.75 f
35	**genblk1.pcpi_mul/U446/Y (XOR2X2_RVT)**	0.15	5.90 r
36	**genblk1.pcpi_mul/rd_reg[63]/D (DFFX1_RVT)**	0.01	5.92 r
37	**data arrival time**		5.92
38	**clock clk (rise edge)**	0.00	0.00
39	**clock network delay (ideal)**	1.00	1.00
40	**genblk1.pcpi_mul/rs2_reg[10]/CLK (DFFX1_RVT)**	0.00 #	1.00 r
41	**genblk1.pcpi_mul/rs2_reg[10]/QN (DFFX1_RVT)**	0.29	1.29 f
42	**genblk1.pcpi_mul/U816/Y (INVX4_RVT)**	0.15	1.44 r
43	**genblk1.pcpi_mul/U817/Y (NOR2X0_RVT)**	0.19	1.63 f
44	**genblk1.pcpi_mul/U819/Y (NOR2X0_RVT)**	0.12	1.75 r
45	**genblk1.pcpi_mul/U833/Y (AOI21X1_RVT)**	0.12	1.88 f
	genblk1.pcpi_mul/U834/Y (INVX0_RVT)	0.05	1.93 r
	clock clk (rise edge)	6.00	6.00
	clock network delay (ideal)	1.00	7.00
	clock uncertainty	-1.00	6.00
	genblk1.pcpi_mul/rd_reg[63]/CLK (DFFX1_RVT)	0.00	6.00 R
	library setup time	-0.08	5.92
	data required time		5.92
	data required time		5.92
	data arrival time		-5.92
	slack (MET)		**0**

Report-Wire load Model (Compile ultra)-1

Wire load model:		**35000**
Location	:	**picorv32a (design)**
Resistance	:	**0.001157**
Capacitance	:	**0.000227**
Area	:	**0.01**
Slope	:	**140.36**

Report-Wire load Model -35000 (Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	16.92				
2	2	39.03				
3	3	64.09				
4	4	92.51				
5	5	124.73				
6	6	161.17				
7	7	202.25				
8	8	248.42				
9	9	300.09				
10	10	357.68				
11	11	421.63				
12	12	492.37				
13	13	570.31				
14	14	655.89				
15	15	749.54				
16	16	851.67				
17	17	962.72				
18	18	1083.11				
19	19	1213.28				
20	20	1353.64				
	Total Length	**9961.05**				

Report-Wire load Model (Compile ultra)-2

Wire load model:		**16000**
Location	:	**picorv32_pcpi_fast_mul (design)**
Resistance	:	**0.001262**
Capacitance	:	**0.000569**
Area	:	**0.01**
Slope	:	**108.438**

Report-Wire load Model - 16000(Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8138.84**				

Report- Threshold Voltage Group - (compile ultra)

S.No	Vth Group Name ->	saed32cell_svt
1	**All Cells**	9632 (100.00%)
2	**Blackbox Cells**	0 (0.00%)
3	**Non-Blackbox cells**	9632 (100.00%)
4	**All Cells Area**	32133.97 (100.00%)
5	**Blackbox Cells area**	0 (0.00%)
6	**Non-Blackbox cells area**	32133.97 (100.00%)
7	**All Cells leakage**	57.671uW (100.00%)
8	**Blackbox Cells leakage**	0 (0.00%)
9	**Non-Blackbox cells leakage**	57.671uW (100.00%)

Global Skew Report(Compile ultra)

S.No			
1	**Clock Tree Name**	:	"clk"
2	**Clock Period**	:	6.000000
3	**Clock Tree root pin**	:	"clk"
4	**Number of Levels**	:	1
5	**Number of Sinks**	:	1582
6	**Number of CT Buffers**	:	0
7	**Number of CTS added gates**	:	0
8	**Number of Preexisting Gates**	:	0
9	**Number of Preexisting Buf/Inv**	:	0
10	**Total Number of Clock Cells**	:	0
11	**Total Area of CT Buffers**	:	0.00000
12	**Total Area of CT cells**	:	0.00000
13	**Max Global Skew**	:	0.00075
14	**Number of MaxTran Violators**	:	0
15	**Number of MaxCap Violators**	:	1
16	**Number of MaxFanout Violators**	:	0
1	**Operating Condition**		worst
2	**Clock global Skew**		0.001
3	**Longest path delay**		0.124
4	**Shortest path delay**		0.123

The longest path delay end pin: is_lui_auipc_jal_jalr_addi_add_sub_reg/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rs2_reg[0]/CLK

Clock_tree Longest Path (Compile ultra)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri
1	**clk**	0	1	0	0	0 r
2	**clk**	1001037.500	1582	0	0	0 r
3	**is_lui_auipc_jal_jalr_addi_add_sub_reg/CLK**	1001037.500	0	0	0.124	0.124 r
	Clock Delay					0.124

Clock_tree Shortest Path (Compile ultra)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri
1	**clk**	0	1	0	0	0 r
2	**clk**	1001037.500	1582	0	0	0 r
3	**genblk1.pcpi_mul/rs2_reg[0]/CLK**	1001037.500	0	0	0.123	0.123 r
	Clock Delay					0.123

Report-qor (Compile ultra)

S.No		
	Timing Path Group (none)	
1	Levels of Logic:	31.00
2	Critical Path Length:	4.92
3	Critical Path Slack:	0.00
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	0.00
6	No. of Violating Paths:	0.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	1
11	Hierarchical Port Count:	134
12	Leaf Cell Count:	9632
13	Buf/Inv Cell Count:	845
14	Buf Cell Count:	8
15	Inv Cell Count:	837
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	7982
18	Sequential Cell Count:	1650
19	Macro Count:	0
	Area	
20	Combinational Area:	21324.206365
21	Noncombinational Area:	10809.761239
22	Buf/Inv Area:	1146.951876
23	Total Buffer Area:	18.55
24	Total Inverter Area:	1128.40
25	Macro/Black Box Area:	0.000000
26	Net Area:	12089.423766
	Cell Area:	**21324.206365**
	Design Area:	**10809.761239**
	Design Rules	
	Total Number of Nets:	10676
	Nets With Violations:	0
	Max Trans Violations:	0
	Max Cap Violations:	0

Report_cells

Report_Cells (Elobrate)

S.No	Cell Name/Refernece	Cell Count	Library	Area	Attributes
1	ADD_UNS_OP	10		0	S,u
2	ASH_UNS_UNS_OP	2		0	S,u
3	ASHR_TC_UNS_OP	1		0	S,u
4	EQ_UNS_OP	2		0	S,u
5	GTECH_AND2	387	Gtech	0	C,u
6	GTECH_AND3	4	Gtech	0	U
7	GTECH_AND4	12	Gtech	0	U
8	GTECH_AND5	4	Gtech	0	U
9	GTECH_BUF	124	Gtech	0	C,u
10	GTECH_NOT	373	Gtech	0	C,u
11	GTECH_OR2	919	Gtech	0	C,u
12	GTECH_XOR2	32	Gtech	0	C,u
13	LT_TC_OP	1		0	S,u
14	LT_TC_OP_32_32_1	1		0	S,u
15	LT_UNS_OP	1		0	S,u
16	LT_UNS_OP_32_32_1	1		0	S,u
17	MULT_UNS_OP_3_1_3	1		0	N,u
18	SELECT_OP_11	8		0	S,u
19	SELECT_OP_2	199		0	S,u
20	SELECT_OP_3	35		0	S,u
21	SELECT_OP_4	24		0	S,u
22	SELECT_OP_5	9		0	S,u
23	SELECT_OP_6	5		0	S,u
24	SELECT_OP_7	2		0	S,u
25	SELECT_OP_9	29		0	S,u
26	SEQGEN	1616		0	N,u
27	SUB_UNS_OP	6		0	S,u
28	picorv32_pcpi_fast_mul	1		0	H,n,u
	Total No.of Cells	3809		0	

Attributes:	
BO -	reference allows boundary optimization
b -	black box (unknown)
h -	hierarchical
n -	noncombinational
r -	removable
u -	contains unmapped logic

Report_cell (compile)

S.No	Reference	Cell Count	Library	Unit Area	Total Area	Attributes
1	AND2X1_RVT	234	saed32rvt_tt0p78vn40c	2.033152	475.757568	
2	AND2X2_RVT	5	saed32rvt_tt0p78vn40c	2.287296	11.43648	
3	AND2X4_RVT	6	saed32rvt_tt0p78vn40c	2.795584	16.773504	
4	AND3X1_RVT	37	saed32rvt_tt0p78vn40c	2.287296	84.629952	
5	AND4X1_RVT	27	saed32rvt_tt0p78vn40c	2.541440	68.61888	
6	AO21X1_RVT	105	saed32rvt_tt0p78vn40c	2.541440	266.8512	
7	AO221X1_RVT	221	saed32rvt_tt0p78vn40c	3.049728	673.989888	
8	AO221X2_RVT	8	saed32rvt_tt0p78vn40c	3.303872	26.430976	
9	AO222X1_RVT	200	saed32rvt_tt0p78vn40c	3.303872	660.7744	
10	AO22X1_RVT	1034	saed32rvt_tt0p78vn40c	2.541440	2627.84896	
11	AO22X2_RVT	82	saed32rvt_tt0p78vn40c	2.795584	229.237888	
12	AOI21X1_RVT	8	saed32rvt_tt0p78vn40c	3.049728	24.397824	
13	AOI221X1_RVT	27	saed32rvt_tt0p78vn40c	3.558016	96.066432	
14	AOI222X1_RVT	28	saed32rvt_tt0p78vn40c	3.812160	106.74048	
15	decoder_pseudo_trigger_reg	1		6.607744	6.607744	n
16	DELLN3X2_RVT	2	saed32rvt_tt0p78vn40c	9.657472	19.314944	
17	DFFX1_RVT	1432	saed32rvt_tt0p78vn40c	6.607744	9462.289408	n
18	DFFX2_RVT	34	saed32rvt_tt0p78vn40c	7.116032	241.945088	n
19	IBUFFX16_RVT	2	saed32rvt_tt0p78vn40c	6.607744	13.215488	
20	IBUFFX2_RVT	3	saed32rvt_tt0p78vn40c	2.541440	7.62432	
21	INVX0_RVT	40	saed32rvt_tt0p78vn40c	1.270720	50.8288	
22	INVX1_RVT	465	saed32rvt_tt0p78vn40c	1.270720	590.8848	
23	INVX2_RVT	65	saed32rvt_tt0p78vn40c	1.524864	99.11616	
24	INVX4_RVT	44	saed32rvt_tt0p78vn40c	2.033152	89.458688	
25	INVX8_RVT	1	saed32rvt_tt0p78vn40c	3.049728	3.049728	
26	is_beq_bne_blt_bge_bltu_bgeu_reg	1		6.607744	6.607744	n
27	is_jalr_addi_slti_sltiu_xori_ori_andi_reg	1		6.607744	6.607744	n
28	is_lui_auipc_jal_jalr_addi_add_sub_reg	1		6.607744	6.607744	n
29	LATCHX1_RVT	68	saed32rvt_tt0p78vn40c	5.082880	345.63584	
30	MUX21X1_RVT	297	saed32rvt_tt0p78vn40c	3.303872	981.249984	
31	MUX21X2_RVT	1	saed32rvt_tt0p78vn40c	3.558016	3.558016	
32	NAND2X0_RVT	189	saed32rvt_tt0p78vn40c	1.524864	288.199296	
33	NAND3X0_RVT	69	saed32rvt_tt0p78vn40c	1.779008	122.751552	
34	NAND3X2_RVT	3	saed32rvt_tt0p78vn40c	3.049728	9.149184	
35	NAND4X0_RVT	120	saed32rvt_tt0p78vn40c	2.033152	243.97824	
36	NBUFFX2_RVT	130	saed32rvt_tt0p78vn40c	2.033152	264.30976	
37	NBUFFX4_RVT	2	saed32rvt_tt0p78vn40c	2.541440	5.08288	
38	NBUFFX8_RVT	1	saed32rvt_tt0p78vn40c	3.812160	3.81216	
39	NOR2X0_RVT	4	saed32rvt_tt0p78vn40c	2.541440	10.16576	
40	NOR3X0_RVT	5	saed32rvt_tt0p78vn40c	2.795584	13.97792	
41	NOR4X1_RVT	13	saed32rvt_tt0p78vn40c	3.049728	39.646464	
42	OA21X1_RVT	11	saed32rvt_tt0p78vn40c	2.541440	27.95584	
43	OA221X1_RVT	170	saed32rvt_tt0p78vn40c	3.049728	518.45376	
44	OA222X1_RVT	145	saed32rvt_tt0p78vn40c	3.303872	479.06144	
45	OA22X1_RVT	54	saed32rvt_tt0p78vn40c	2.541440	137.23776	
46	OAI21X1_RVT	36	saed32rvt_tt0p78vn40c	3.049728	109.790208	
47	OAI221X1_RVT	2	saed32rvt_tt0p78vn40c	3.558016	7.116032	
48	OAI222X1_RVT	8	saed32rvt_tt0p78vn40c	3.812160	30.49728	
49	OAI22X1_RVT	15	saed32rvt_tt0p78vn40c	3.049728	45.74592	
50	OR2X1_RVT	23	saed32rvt_tt0p78vn40c	2.033152	46.762496	
51	OR2X2_RVT	1	saed32rvt_tt0p78vn40c	2.287296	2.287296	
52	OR2X4_RVT	1	saed32rvt_tt0p78vn40c	2.795584	2.795584	
53	OR3X1_RVT	6	saed32rvt_tt0p78vn40c	2.541440	15.24864	
54	OR4X1_RVT	21	saed32rvt_tt0p78vn40c	3.558016	74.718336	
55	pcpi_timeout_counter_reg[0]	1		6.607744	6.607744	n
56	pcpi_timeout_counter_reg[1]	1		6.607744	6.607744	n
57	pcpi_timeout_counter_reg[2]	1		6.607744	6.607744	n
58	pcpi_timeout_counter_reg[3]	1		6.607744	6.607744	n
59	picorv32_pcpi_fast_mul	1		9382.742271	9382.742271	h,n
60	picorv32a_DW_cmp_0	1		242.961665	242.961665	BO,h
61	picorv32a_DW01_add_5	1		158.585851	158.585851	BO,h
62	picorv32a_DW01_cmp6_0	1		198.994753	198.994753	BO,h
63	picorv32a_DW01_dec_0_DW01_dec_1	1		181.458819	181.458819	BO,h
64	picorv32a_DW01_sub_0	1		200.011323	200.011323	n
	Total Cells = 5505	5519			32023.669188	

Report-cell (Compile Ultra)

S.No	Reference	Library	Count	Unit Area	Total Area	Attributes
1	AND2X1_RVT	saed32rvt_tt0p78vn40c	416	2.033152	845.791275	
2	AND2X2_RVT	saed32rvt_tt0p78vn40c	23	2.287296	52.607809	
3	AND2X4_RVT	saed32rvt_tt0p78vn40c	1	2.795584	2.795584	
4	AND3X1_RVT	saed32rvt_tt0p78vn40c	59	2.287296	134.950467	
5	AND3X2_RVT	saed32rvt_tt0p78vn40c	3	2.541440	7.624320	
6	AND4X1_RVT	saed32rvt_tt0p78vn40c	30	2.541440	76.243200	
7	AO21X1_RVT	saed32rvt_tt0p78vn40c	107	2.541440	271.934081	
8	AO221X1_RVT	saed32rvt_tt0p78vn40c	19	3.049728	57.944830	
9	AO222X1_RVT	saed32rvt_tt0p78vn40c	87	3.303872	287.436873	
10	AO22X1_RVT	saed32rvt_tt0p78vn40c	1469	2.541440	3733.375375	
11	AOI21X1_RVT	saed32rvt_tt0p78vn40c	77	3.049728	234.829050	
12	AOI222X2_RVT	saed32rvt_tt0p78vn40c	1	4.066304	4.066304	
13	AOI22X1_RVT	saed32rvt_tt0p78vn40c	148	3.049728	451.359732	
14	DFFSSRX1_RVT	saed32rvt_tt0p78vn40c	15	7.116032	106.740482	n
15	DFFSSRX2_RVT	saed32rvt_tt0p78vn40c	1	7.624320	7.624320	n
16	DFFX1_RVT	saed32rvt_tt0p78vn40c	1431	6.607744	9455.681974	n
17	DFFX2_RVT	saed32rvt_tt0p78vn40c	2	7.116032	14.232064	n
18	FADDX1_RVT	saed32rvt_tt0p78vn40c	49	4.828736	236.608056	r
19	HADDX1_RVT	saed32rvt_tt0p78vn40c	49	3.303872	161.889733	r
20	INVX0_RVT	saed32rvt_tt0p78vn40c	446	1.270720	566.741122	
21	INVX2_RVT	saed32rvt_tt0p78vn40c	58	1.524864	88.442110	
22	INVX4_RVT	saed32rvt_tt0p78vn40c	14	2.033152	28.464129	
23	LATCHX1_RVT	saed32rvt_tt0p78vn40c	68	5.082880	345.635841	n
24	MUX21X1_RVT	saed32rvt_tt0p78vn40c	11	3.303872	36.342593	
25	NAND2X0_RVT	saed32rvt_tt0p78vn40c	516	1.524864	786.829803	
26	NAND2X2_RVT	saed32rvt_tt0p78vn40c	1	2.795584	2.795584	
27	NAND2X4_RVT	saed32rvt_tt0p78vn40c	2	3.303872	6.607744	
28	NAND3X0_RVT	saed32rvt_tt0p78vn40c	158	1.779008	281.083269	
29	NAND3X2_RVT	saed32rvt_tt0p78vn40c	3	3.049728	9.149184	
30	NAND4X0_RVT	saed32rvt_tt0p78vn40c	65	2.033152	132.154887	
31	NBUFFX2_RVT	saed32rvt_tt0p78vn40c	4	2.033152	8.132608	
32	NBUFFX4_RVT	saed32rvt_tt0p78vn40c	1	2.541440	2.541440	
33	NOR2X0_RVT	saed32rvt_tt0p78vn40c	307	2.541440	780.222083	
34	NOR2X2_RVT	saed32rvt_tt0p78vn40c	4	2.795584	11.182336	
35	NOR2X4_RVT	saed32rvt_tt0p78vn40c	1	3.303872	3.303872	
36	NOR3X0_RVT	saed32rvt_tt0p78vn40c	19	2.795584	53.116095	
37	NOR4X0_RVT	saed32rvt_tt0p78vn40c	106	3.049728	323.271159	
38	OA21X1_RVT	saed32rvt_tt0p78vn40c	87	2.541440	221.105281	
39	OA21X2_RVT	saed32rvt_tt0p78vn40c	1	2.795584	2.795584	
40	OA221X1_RVT	saed32rvt_tt0p78vn40c	10	3.049728	30.497279	
41	OA221X2_RVT	saed32rvt_tt0p78vn40c	1	3.303872	3.303872	
42	OA222X1_RVT	saed32rvt_tt0p78vn40c	6	3.303872	19.823233	
43	OA22X1_RVT	saed32rvt_tt0p78vn40c	113	2.541440	287.182721	
44	OAI21X1_RVT	saed32rvt_tt0p78vn40c	147	3.049728	448.310004	
45	OAI21X2_RVT	saed32rvt_tt0p78vn40c	1	3.303872	3.303872	
46	OAI221X1_RVT	saed32rvt_tt0p78vn40c	3	3.558016	10.674048	
47	OAI22X1_RVT	saed32rvt_tt0p78vn40c	109	3.049728	332.420343	
48	OR2X1_RVT	saed32rvt_tt0p78vn40c	232	2.033152	471.691288	
49	OR2X2_RVT	saed32rvt_tt0p78vn40c	2	2.287296	4.574592	
50	OR3X1_RVT	saed32rvt_tt0p78vn40c	84	2.541440	213.480961	
51	OR3X2_RVT	saed32rvt_tt0p78vn40c	27	2.541440	68.618880	
52	OR4X1_RVT	saed32rvt_tt0p78vn40c	12	3.558016	42.696193	
53	picorv32_pcpi_fast_mul	saed32rvt_tt0p78vn40c	1	9466.355615	9466.355615	h, n
54	XNOR2X1_RVT	saed32rvt_tt0p78vn40c	88	4.320448	380.199417	
55	XNOR3X1_RVT	saed32rvt_tt0p78vn40c	18	6.099456	109.790205	
56	XOR2X1_RVT	saed32rvt_tt0p78vn40c	91	4.320448	393.160761	
57	XOR3X1_RVT	saed32rvt_tt0p78vn40c	2	7.116032	14.232064	
	TOTAL		6806		32133.967601	

Report_area

Report_Area (Elobarte)			
S.No	**Number of**	**Count**	**AREA**
1	**Ports**	4129	0
2	**Nets**	15050	0
3	**Cells**	8326	0
4	**combinational cells**	6177	0
5	**sequential cells**	2076	0
6	**macros/black boxes**	0	0
7	**buf/inv**	870	0
8	**references:**	63	0
9	**Net Interconnect**		7809.67614
		TOTAL CELL AREA	**0**
		TOTAL AREA	**7809.67614**

Report_Area (Compile)			
S.No	**Number of**	**Count**	**Area**
1	**Number of ports:**	1919	
2	**Number of nets:**	12431	
3	**Number of cells:**	9537	
4	**Number of combinational cells:**	7797	
5	**Number of sequential cells:**	1667	
6	**Number of macros/black boxes:**	0	
7	**Number of buf/inv:**	1458	
8	**Number of references:**	69	
9	**Combinational area:**		21094.460267
10	**Buf/Inv area:**		2076.356500
11	**Noncombinational area:**		10929.208921
12	**Macro/Black Box area:**		0.000000
13	**Net Interconnect area:**		4328.556079
	Total Cell Area		**32023.669188**
	Total Area		**36352.225267**

Report-area (Compile Ultra)			
S.No		**Area**	**Count**
1	**Number of ports:**		543
2	**Number of nets:**		10793
3	**Number of cells:**		9651
4	**Number of combinational cells:**		7982
5	**Number of sequential cells:**		1650
6	**Number of macros/black boxes:**		0
7	**Number of buf/inv:**		845
8	**Number of references:**		57
9	**Combinational area:**	21324.206365	
10	**Buf/Inv area:**	1146.951876	
11	**Noncombinational area:**	10809.761239	
12	**Macro/Black Box area:**	0.000000	
13	**Net Interconnect area:**	12089.423766	
	Total cell area:	**32133.967604**	
	Total area:	**44223.391370**	

Report_power

Report_power -1 (Elobrate)

S.No	Design	Wire Load Model	Library
1	picorv32a	ForQA	saed32rvt_tt0p78vn40c
2	picorv32_pcpi_fast_mul	ForQA	saed32rvt_tt0p78vn40c
3	ASH_UNS_UNS_OP_4_2_4	ForQA	saed32rvt_tt0p78vn40c
4	DW_leftsh	ForQA	saed32rvt_tt0p78vn40c
5	*SUB_UNS_OP_32_32_32	ForQA	saed32rvt_tt0p78vn40c
6	DW01_sub_width32	ForQA	saed32rvt_tt0p78vn40c
7	ADD_UNS_OP_32_32_32	ForQA	saed32rvt_tt0p78vn40c
8	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
9	EQ_UNS_OP_32_32_1	ForQA	saed32rvt_tt0p78vn40c
10	DW01_cmp6_width32	ForQA	saed32rvt_tt0p78vn40c
11	LT_TC_OP_32_32_1	ForQA	saed32rvt_tt0p78vn40c
12	DW01_cmp2_width32	ForQA	saed32rvt_tt0p78vn40c
13	LT_UNS_OP_32_32_1	ForQA	saed32rvt_tt0p78vn40c
14	DW01_cmp2_width32	ForQA	saed32rvt_tt0p78vn40c
15	*ASH_UNS_UNS_OP_32_5_32	ForQA	saed32rvt_tt0p78vn40c
16	DW_leftsh	ForQA	saed32rvt_tt0p78vn40c
17	*ASHR_TC_UNS_OP_33_5_33	ForQA	saed32rvt_tt0p78vn40c
18	DW_rightsh	ForQA	saed32rvt_tt0p78vn40c
19	*ADD_UNS_OP_32_3_32	ForQA	saed32rvt_tt0p78vn40c
20	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
21	*SUB_UNS_OP_4_1_4	ForQA	saed32rvt_tt0p78vn40c
22	DW01_dec_width4	ForQA	saed32rvt_tt0p78vn40c
23	*ADD_UNS_OP_64_1_64	ForQA	saed32rvt_tt0p78vn40c
24	DW01_inc_width64	ForQA	saed32rvt_tt0p78vn40c
25	*SUB_UNS_OP_32_1_32	ForQA	saed32rvt_tt0p78vn40c
26	DW01_dec_width32	ForQA	saed32rvt_tt0p78vn40c
27	*EQ_UNS_OP_32_1_1	ForQA	saed32rvt_tt0p78vn40c
28	DW01_cmp6_width32	ForQA	saed32rvt_tt0p78vn40c
29	DW01_dec_width32	ForQA	saed32rvt_tt0p78vn40c
30	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
31	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
32	DW01_inc_width64	ForQA	saed32rvt_tt0p78vn40c
33	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
34	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
35	*SUB_UNS_OP_5_3_5	ForQA	saed32rvt_tt0p78vn40c
36	DW01_sub_width5	ForQA	saed32rvt_tt0p78vn40c
37	*SUB_UNS_OP_5_1_5	ForQA	saed32rvt_tt0p78vn40c
38	DW01_dec_width5	ForQA	saed32rvt_tt0p78vn40c
39	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
40	DW01_add_width32	ForQA	saed32rvt_tt0p78vn40c
41	*MULT_UNS_OP_3_1_3	ForQA	saed32rvt_tt0p78vn40c
42	DW02_mult	ForQA	saed32rvt_tt0p78vn40c
43	*MULT_TC_OP_33_33_64	ForQA	saed32rvt_tt0p78vn40c
44	DW02_mult	ForQA	saed32rvt_tt0p78vn40c
		ENCLOSED	**Operating Conditions:** tt0p78vn40c

Cell Internal Power = 0.0000 uW (0%)
Net Switching Power = 16.0247 uW (100%)

Total Dynamic Power = 16.0247 uW (100%)
Cell Leakage Power = 0.0000 pW

Report Power-2 (Elobrate)

Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
io_pad	0.0000	0.0000	0.0000	0.0000	0.00%	
memory	0.0000	0.0000	0.0000	0.0000	0.00%	
black_box	0.0000	0.0000	0.0000	0.0000	0.00%	
clock_network	0.0000	0.0000	0.0000	0.0000	0.00%	I
register	0.0000	0.0000	0.0000	0.0000	0.00%	
sequential	0.0000	1.5485	0.0000	1.5485	9.66%	
combinational	0.0000	14.4761	0.0000	14.4761	90.34%	
Total		**16.0246**	**0.0000**	**16.0246**	**100.00%**	

Report_power-1 (Compile)

S.No	Design	Wire Load Model	Library
1	picorv32a	ForQA	saed32rvt_tt0p78vn40c
2	picorv32_pcpi_fast_mul	ForQA	saed32rvt_tt0p78vn40c
3	picorv32a_DW01_add_0	ForQA	saed32rvt_tt0p78vn40c
4	picorv32a_DW01_add_1	ForQA	saed32rvt_tt0p78vn40c
5	picorv32a_DW01_add_2	ForQA	saed32rvt_tt0p78vn40c
6	picorv32a_DW01_add_3	ForQA	saed32rvt_tt0p78vn40c
7	picorv32a_DW_cmp_0	8000	saed32rvt_tt0p78vn40c
8	picorv32a_DW01_add_4	ForQA	saed32rvt_tt0p78vn40c
9	picorv32a_DW01_sub_0	ForQA	saed32rvt_tt0p78vn40c
10	picorv32a_DW01_add_5	ForQA	saed32rvt_tt0p78vn40c
11	picorv32a	ForQA	saed32rvt_tt0p78vn40c
12	picorv32a_DW01_dec_0_DW01_dec_1	ForQA	saed32rvt_tt0p78vn40c
13	picorv32a_DW01_cmp6_0	ForQA	saed32rvt_tt0p78vn40c
14	picorv32a_DW01_add_6	ForQA	saed32rvt_tt0p78vn40c
15	picorv32_pcpi_fast_mul_DW_mult_tc_1	16000	saed32rvt_tt0p78vn40c
16	picorv32a_DW01_inc_2	8000	saed32rvt_tt0p78vn40c
17	picorv32a_DW01_inc_3	8000	saed32rvt_tt0p78vn40c

Cell Internal Power = 984.6401 uW (99%)
Net Switching Power = 10.8277 uW (1%)

Total Dynamic Power = Internal + Switching Power
Total Dynamic Power = 995.4677 uW (100%)
Cell Leakage Power = 56.1337 uW

Total Power = Total Dynamic power + Leakage Power

Report-power-2 (compile)

S.No	Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
1	io_pad	0.0000	0.0000	0.0000	0.0000	0.00%	
2	memory	0.0000	0.0000	0.0000	0.0000	0.00%	
3	black_box	0.0000	0.0000	0.0000	0.0000	0.00%	
4	clock_network	972.4143	0.0000	0.0000	972.4143	-92.47%	i
5	register	4.6282	1.7049	3.0705E+07	37.0496	-3.52%	
6	sequential	0.6379	0.1417	1.1301E+06	1.9096	-0.18%	
7	combinational	6.9592	8.9811	2.4299E+07	40.2390	-3.83%	
	Total (uW)	**984.6396**	**10.8277**	**56.134(5.6134e+07 pW)**	**1051.6013**		
	Total Dynamic Power		**995.4673**				

Report_power-1 (Compile Ultra)

S.No	Design	Wire Load Model	Library
1	picorv32a	35000	saed32rvt_tt0p78vn40c
2	picorv32_pcpi_fast_mul	16000	saed32rvt_tt0p78vn40c

Cell Internal Power = 972.5272 uW (99%)
Net Switching Power = 5.6778 uW (1%)

Total Dynamic Power = 978.2050 uW (100%)
Cell Leakage Power = 57.6712 uW

Total Power = Total Dynamic power + Leakage Power

Report-power-2 (compile ultra)

S.No	Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
1	io_pad	0.0000	0.0000	0.0000	0.0000	0.00%)	
2	memory	0.0000	0.0000	0.0000	0.0000	0.00%)	
3	black_box	0.0000	0.0000	0.0000	0.0000	0.00%)	
4	clock_network	961.6392	0.0000	0.0000	961.6392	92.83%)	I
5	register	3.9210	1.0050	2.99E+07	34.8283	3.36%)	
6	sequential	0.5208	9.8819E-02	1.1326E+06	1.7523	0.17%)	
7	combinational	6.4399	4.5740	2.6639E+07	37.6528	3.63%)	
	Total (uW)	**972.5209**	**5.6778**	**57.671 (5.7671e+07 pW)**	**1035.9**		
	Total Dynamic Power(uW)		**978.1987**				

Report_timing

Report_timing - 1 (Elobrate &read sdc)

S.No		
1	**Startpoint:**	resetn (input port clocked by clk)
2	**Endpoint:**	mem_la_write (output port clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	max

Report_timing - 1 (Elobrate &read sdc)-1

S.No		
1	**Startpoint:**	mem_rdata_q_reg[0] (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	pcpi_insn_reg[0] (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	min

Report_timing - 1 (Compile)

S.No		
1	**Startpoint:**	latched_stalu_reg (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	reg_next_pc_reg[31](rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	max

Report_timing - 1 (Compile)-1

S.No		
1	**Startpoint:**	genblk1.pcpi_mul//active_reg[0] (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	genblk1.pcpi_mul//active_reg[1] (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	min

Report_timing - 1 (Compile ultra)

S.No		
1	**Startpoint:**	genblk1.pcpi_mul/rs2_reg[10] rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	genblk1.pcpi_mul//rd_reg[63] (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	max

Report_timing - 1 (Compile ultra)-1

S.No		
1	**Startpoint:**	instr_blt_reg (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:**	is_slti_blt_slt_reg (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:**	Clk
4	**Path Type:**	min

Report_timing-2 (Elobrate &read sdc)

Des/Clust/Port	Wire Load Model	Library
picorv32a	ForQA	saed32rvt_tt0p78vn40c

Report_timing-2 (Elobrate &read sdc)-1

Des/Clust/Port	Wire Load Model	Library
picorv32a	ForQA	saed32rvt_tt0p78vn40c

Report_timing-2 (Compile)

Des/Clust/Port	Wire Load Model	Library
picorv32a	ForQA	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_1	ForQA	saed32rvt_tt0p78vn40c

Report_timing-2 (Compile)-1

Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_1	16000	saed32rvt_tt0p78vn40c

Report_timing-2 (Compile ultra)

Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c
picorv32_pcpi_fast_mul	16000	saed32rvt_tt0p78vn40c

Report_timing-2 (Compile ultra)-1

Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c

Report_timing -3 (Elobrate &read sdc)

S.No	Point	Incr	Path	
1	**clock clk (rise edge)**	0.00	0.00	
2	**clock network delay (ideal)**	1.00	1.00	
3	**input external delay**	1.30	2.30	r
4	**resetn (in)**	0.00	2.30	r
5	**C12644/Z (GTECH_AND2)**	0.01	2.31	r
6	**C12643/Z (GTECH_AND2)**	0.00	2.32	r
7	**mem_la_write (out)**	0.01	2.33	r
8	**data arrival time**		2.33	
9	**clock clk (rise edge)**	6.00	6.00	
10	**clock network delay (ideal)**	1.00	7.00	
11	**clock uncertainty**	-1.00	6.00	
12	**output external delay**	-1.30	4.70	
13	**data required time**		4.70	
14	**clock clk (rise edge)**	0.00	0.00	
15	**clock network delay (ideal)**	1.00	1.00	
16	**clock uncertainty**	-1.00	6.00	
17	**output external delay**	-1.30	4.70	
18	**data required time**		4.70	
	data required time		4.70	
	data arrival time		-2.33	
	slack (MET)		**2.37**	

Report_timing -3 (Elobrate &read sdc)-1

S.No	Point	Incr	Path	
1	**clock clk (rise edge)**	0.00	0.00	
2	**clock network delay (ideal)**	0.00	0.00	
3	**mem_rdata_q_reg[0]/clocked_on (**SEQGEN**)**	0.00 #	0.00	r
4	**mem_rdata_q_reg[0]/Q (**SEQGEN**)**	0.00	0.00	r
5	**pcpi_insn_reg[0]/next_state (**SEQGEN**)**	0.01	0.01	r
6	**data arrival time**		0.01	
7	**clock clk (rise edge)**		0.00	
8	**clock network delay (ideal)**		0.00	
9	**pcpi_insn_reg[0]/clocked_on (**SEQGEN**)**		0.00	
10	**library hold time**		0.00	
11	**data required time**			
	data required time		0.00	
	data arrival time		-0.01	
	slack (MET)		**-0.01**	

Report_timing -3 (Compile)

S.No	Point	Incr	Path	
1	**clock clk (rise edge)**	0.00	0.00	
2	**clock network delay (ideal)**	1.00	1.00	
3	**latched_stalu_reg/CLK (DFFX2_RVT)**	0.00 #	1.00	r
4	**latched_stalu_reg/QN (DFFX2_RVT)**	0.28	1.28	f
5	**U4627/Y (NAND2X0_RVT)**	0.10	1.38	r
6	**U5842/Y (OAI222X1_RVT)**	0.18	1.56	f
7	**U4560/Y (MUX21X2_RVT)**	0.13	1.69	f
8	**U4629/Y (AND2X1_RVT)**	0.11	1.79	f
9	**add_1547/A[1] (picorv32a_DW01_add_1)**	0.00	1.79	f
10	**add_1547/U10/Y (AND2X1_RVT)**	0.10	1.89	f
11	**add_1547/L1[2]/U1/CO (FADDX1_RVT)**	0.15	2.04	f
12	**add_1547/L1[3]/U1/CO (FADDX1_RVT)**	0.16	2.20	f
13	**add_1547/L1[4]/U1/CO (FADDX1_RVT)**	0.16	2.36	f
14	**add_1547/L1[5]/U1/CO (FADDX1_RVT)**	0.16	2.51	f
15	**add_1547/L1[6]/U1/CO (FADDX1_RVT)**	0.16	2.67	f
16	**add_1547/L1[7]/U1/CO (FADDX1_RVT)**	0.16	2.83	f
17	**add_1547/L1[8]/U1/CO (FADDX1_RVT)**	0.16	2.99	f
18	**add_1547/L1[9]/U1/CO (FADDX1_RVT)**	0.16	3.15	f
19	**add_1547/L1[10]/U1/CO (FADDX1_RVT)**	0.16	3.30	f
20	**add_1547/L1[11]/U1/CO (FADDX1_RVT)**	0.16	3.46	f
21	**add_1547/L1[12]/U1/CO (FADDX1_RVT)**	0.16	3.62	f
22	**add_1547/L1[13]/U1/CO (FADDX1_RVT)**	0.16	3.78	f
23	**add_1547/L1[14]/U1/CO (FADDX1_RVT)**	0.16	3.94	f
24	**add_1547/L1[15]/U1/CO (FADDX1_RVT)**	0.16	4.09	f
25	**add_1547/L1[16]/U1/CO (FADDX1_RVT)**	0.16	4.25	f
26	**add_1547/L1[17]/U1/CO (FADDX1_RVT)**	0.16	4.41	f
27	**add_1547/L1[18]/U1/CO (FADDX1_RVT)**	0.16	4.57	f
28	**add_1547/L1[19]/U1/CO (FADDX1_RVT)**	0.16	4.73	f
29	**add_1547/L1[20]/U1/CO (FADDX1_RVT)**	0.16	4.88	f
30	**add_1547/L1[21]/U1/CO (FADDX1_RVT)**	0.16	5.04	f
31	**add_1547/L1[22]/U1/CO (FADDX1_RVT)**	0.16	5.20	f
32	**add_1547/L1[23]/U1/CO (FADDX1_RVT)**	0.16	5.36	f
33	**add_1547/L1[24]/U1/CO (FADDX1_RVT)**	0.16	5.52	f
34	**add_1547/L1[25]/U1/CO (FADDX1_RVT)**	0.16	5.68	f
35	**add_1547/L1[26]/U1/CO (FADDX1_RVT)**	0.16	5.83	f
36	**add_1547/L1[27]/U1/CO (FADDX1_RVT)**	0.16	5.99	f
37	**add_1547/L1[28]/U1/CO (FADDX1_RVT)**	0.16	6.15	f
38	**add_1547/L1[29]/U1/CO (FADDX1_RVT)**	0.17	6.32	f
39	**add_1547/U7/Y (NAND2X0_RVT)**	0.09	6.41	r
40	**add_1547/U4/Y (AND3X1_RVT)**	0.12	6.52	r
41	**add_1547/U2/Y (XOR3X2_RVT)**	0.12	6.64	f
42	**add_1547/SUM[31] (picorv32a_DW01_add_1)**	0.00	6.64	f
43	**U5911/Y (NAND2X0_RVT)**	0.09	6.73	r
44	**U5917/Y (NAND3X0_RVT)**	0.08	6.81	f
45	**reg_next_pc_reg[31]/D (DFFX1_RVT)**	0.01	6.82	f
	data arrival time		6.82	
	clock clk (rise edge)	6.00	6.00	
	clock network delay (ideal)	1.00	7.00	
	clock uncertainty	-1.00	6.00	
	reg_next_pc_reg[31]/CLK (DFFX1_RVT)	0.00	6.00	
	library setup time	-0.04	5.96	
	data required time		5.96	
	data required time		5.96	
	data arrival time		-6.82	
	slack (VIOLATED)		**-0.86**	

Report_timing -3 (Compile)-1

S.No	Point	Incr	Path	
1	**clock clk (rise edge)**	0.00	0.00	
2	**clock network delay (ideal)**	0.00	0.00	
3	**genblk1.pcpi_mul/active_reg[0]/CLK (DFFX1_RVT)**	0.00 #	0.00	r
4	**genblk1.pcpi_mul/active_reg[0]/Q (DFFX1_RVT)**	0.18	0.18	f
5	**genblk1.pcpi_mul/active_reg[1]/D (DFFSSRX1_RVT)**	0.01	0.18	f
6	**data arrival time**		0.18	
	clock clk (rise edge)	0.00	0.00	
	clock network delay (ideal)	0.00	0.00	
	genblk1.pcpi_mul/active_reg[1]/CLK (DFFSSRX1_RVT)	0.00	0.00	r
	library hold time	-0.05	-0.05	
	data required time		-0.05	
	data required time		-0.05	
	data arrival time		-0.18	
	slack (MET)		**-0.24**	

Report_timing -3 (Compile ultra)

S.No	Point	Incr	Path	
1	**clock clk (rise edge)**	0.00	0.00	
2	**clock network delay (ideal)**	1.00	1.00	
3	**genblk1.pcpi_mul/rs2_reg[10]/CLK (DFFX1_RVT)**	0.00 #	1.00	r
4	**genblk1.pcpi_mul/rs2_reg[10]/QN (DFFX1_RVT)**	0.29	1.29	f
5	**genblk1.pcpi_mul/U816/Y (INVX4_RVT)**	0.15	1.44	r
6	**genblk1.pcpi_mul/U817/Y (NOR2X0_RVT)**	0.19	1.63	f
7	**genblk1.pcpi_mul/U819/Y (NOR2X0_RVT)**	0.12	1.75	r
8	**genblk1.pcpi_mul/U833/Y (AOI21X1_RVT)**	0.12	1.88	f
9	**genblk1.pcpi_mul/U834/Y (INVX0_RVT)**	0.05	1.93	r
10	**genblk1.pcpi_mul/U841/Y (AOI21X1_RVT)**	0.10	2.03	r
11	**genblk1.pcpi_mul/U842/Y (AOI21X1_RVT)**	0.10	2.13	f
12	**genblk1.pcpi_mul/U47/Y (INVX2_RVT)**	0.09	2.22	r
13	**genblk1.pcpi_mul/U1156/Y (AO21X1_RVT)**	0.13	2.36	r
14	**genblk1.pcpi_mul/U73/Y (XOR2X1_RVT)**	0.23	2.59	f
15	**genblk1.pcpi_mul/U1878/Y (OAI21X1_RVT)**	0.20	2.79	r
16	**genblk1.pcpi_mul/U374/Y (XOR2X1_RVT)**	0.19	2.98	f
17	**genblk1.pcpi_mul/U1898/S (FADDX1_RVT)**	0.27	3.25	r
18	**genblk1.pcpi_mul/U1892/CO (FADDX1_RVT)**	0.15	3.40	r
19	**genblk1.pcpi_mul/U2302/CO (FADDX1_RVT)**	0.15	3.55	r
20	**genblk1.pcpi_mul/U2308/CO (FADDX1_RVT)**	0.17	3.72	r
21	**genblk1.pcpi_mul/U329/Y (XOR3X1_RVT)**	0.29	4.01	f
22	**genblk1.pcpi_mul/U2309/Y (NOR2X0_RVT)**	0.14	4.14	r
23	**genblk1.pcpi_mul/U208/Y (OAI21X1_RVT)**	0.15	4.30	f
24	**genblk1.pcpi_mul/U2321/Y (AOI21X1_RVT)**	0.16	4.45	r
25	**genblk1.pcpi_mul/U757/Y (OAI21X1_RVT)**	0.15	4.60	f
26	**genblk1.pcpi_mul/U2350/Y (AO21X1_RVT)**	0.12	4.72	f
27	**genblk1.pcpi_mul/U2351/Y (AO21X1_RVT)**	0.08	4.80	f
28	**genblk1.pcpi_mul/U2353/Y (AO22X1_RVT)**	0.10	4.90	f
29	**genblk1.pcpi_mul/U2378/CO (FADDX1_RVT)**	0.16	5.06	f
30	**genblk1.pcpi_mul/U2354/CO (FADDX1_RVT)**	0.16	5.22	f
31	**genblk1.pcpi_mul/U2356/Y (AO22X1_RVT)**	0.11	5.33	f
32	**genblk1.pcpi_mul/U2364/CO (FADDX1_RVT)**	0.17	5.50	f
33	**genblk1.pcpi_mul/U2373/Y (AO22X1_RVT)**	0.10	5.60	f
34	**genblk1.pcpi_mul/U2377/CO (FADDX1_RVT)**	0.15	5.75	f
35	**genblk1.pcpi_mul/U46/Y (XOR2X2_RVT)**	0.15	5.90	r
36	**genblk1.pcpi_mul/rd_reg[63]/D (DFFX1_RVT)**	0.01	5.92	r
37	**data arrival time**		5.92	
38	**clock clk (rise edge)**	0.00	0.00	
39	**clock network delay (ideal)**	1.00	1.00	
40	**genblk1.pcpi_mul/rs2_reg[10]/CLK (DFFX1_RVT)**	0.00 #	1.00	r
41	**genblk1.pcpi_mul/rs2_reg[10]/QN (DFFX1_RVT)**	0.29	1.29	f
42	**genblk1.pcpi_mul/U816/Y (INVX4_RVT)**	0.15	1.44	r
43	**genblk1.pcpi_mul/U817/Y (NOR2X0_RVT)**	0.19	1.63	f
44	**genblk1.pcpi_mul/U819/Y (NOR2X0_RVT)**	0.12	1.75	r
45	**genblk1.pcpi_mul/U833/Y (AOI21X1_RVT)**	0.12	1.88	f
	genblk1.pcpi_mul/U834/Y (INVX0_RVT)	0.05	1.93	r
	clock clk (rise edge)	6.00	6.00	
	clock network delay (ideal)	1.00	7.00	
	clock uncertainty	-1.00	6.00	
	genblk1.pcpi_mul/rd_reg[63]/CLK (DFFX1_RVT)	0.00	6.00	R
	library setup time	-0.08	5.92	
	data required time		5.92	
	data required time		5.92	
	data arrival time		-5.92	
	slack (MET)		**0**	

Report_timing -3 (Compile ultra)-1

S.No	Point	Incr	Path	
1	**clock clk (rise edge)**	0.00	0.00	
2	**clock network delay (ideal)**	0.00	0.00	
3	**instr_blt_reg/CLK (DFFX1_RVT)**	0.00 #	0.00	r
4	**instr_blt_reg/QN (DFFX1_RVT)**	0.13	0.13	f
5	**is_slti_blt_slt_reg/RSTB (DFFSSRX1_RVT)**	0.01	0.14	f
6	**data arrival time**		0.14	
	clock clk (rise edge)	0.00	0.00	
	clock network delay (ideal)	0.00	0.00	
	is_slti_blt_slt_reg/CLK (DFFSSRX1_RVT)	0.00	0.00	r
	library hold time	-0.06	-0.06	
	data required time		-0.06	
	data required time		-0.06	
	data arrival time		-0.14	
	slack (MET)		**0.21**	

report_wireload

Compile

Compile Ultra

Report-Wire load Model -1(Elobrate)

Wire load model	**ForQA**
Location	**picorv32a (design)**
Resistance	**0.002067**
Capacitance	**0.026724**
Area	**0.01**
Slope	**30.2854**

Report-Wire load Model -2 FORQA (Elobrate)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	8.28				
2	2	18.49				
3	3	29.35				
4	4	40.92				
5	5	53.23				
6	6	66.36				
7	7	80.36				
8	8	95.27				
9	9	111.17				
10	10	128.09				
11	11	146.10				
12	12	165.26				
13	13	185.61				
14	14	207.22				
15	15	230.13				
16	16	254.41				
17	17	280.11				
18	18	307.28				
19	19	335.98				
20	20	366.27				
	Total Length	**3109.89**				

Report-wireload model (Compile)

Wire load Model	**ForQA**
Location	**picorv32a (design)**
Resistance	**0.002067**
Capacitance	**0.026724**
Area	**0.01**
Slope	**30.2854**

Report-Wire load Model FORQA (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	8.28				
2	2	18.49				
3	3	29.35				
4	4	40.92				
5	5	53.23				
6	6	66.36				
7	7	80.36				
8	8	95.27				
9	9	111.17				
10	10	128.09				
11	11	146.10				
12	12	165.26				
13	13	185.61				
14	14	207.22				
15	15	230.13				
16	16	254.41				
17	17	280.11				
18	18	307.28				
19	19	335.98				
20	20	366.27				
	Total Length	**3109.89**				

Report-Wire load Model -2 (Compile)

Wire load model:	**8000**
Location :	**picorv32a_DW_cmp_0 (design)**
Resistance :	**0.0015727**
Capacitance :	**0.000312**
Area :	**0.01**
Slope :	**90.6464**

Report-Wire load Model -8000 (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	13.94				
2	2	31.80				
3	3	51.61				
4	4	73.61				
5	5	98.05				
6	6	125.17				
7	7	155.23				
8	8	188.46				
9	9	225.12				
10	10	265.45				
11	11	309.71				
12	12	358.13				
13	13	410.96				
14	14	468.46				
15	15	530.86				
16	16	598.42				
17	17	671.38				
18	18	749.98				
19	19	834.49				
20	20	925.13				
	Total Length	**7085.96**				

Report-Wire load Model -3 (Compile)

Wire load model:	**16000**
Location :	**picorv32_pcpi_fast_mul_DW_mult_tc_1 (design)**
Resistance :	**0.001282**
Capacitance :	**0.000569**
Area :	**0.01**
Slope :	**108.438**

Report-Wire load Model - 16000(Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8138.84**				

Report-Wire load Model (Compile ultra)-1

Wire load model:	**35000**
Location :	**picorv32a (design)**
Resistance :	**0.001187**
Capacitance :	**0.00027**
Area :	**0.01**
Slope :	**140.36**

Report-Wire load Model -35000 (Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	16.92				
2	2	39.03				
3	3	64.09				
4	4	92.51				
5	5	124.73				
6	6	161.17				
7	7	202.25				
8	8	248.42				
9	9	300.09				
10	10	357.68				
11	11	421.63				
12	12	492.37				
13	13	570.31				
14	14	655.89				
15	15	749.54				
16	16	851.67				
17	17	962.72				
18	18	1083.11				
19	19	1213.28				
20	20	1353.64				
	Total Length	**9961.05**				

Report-Wire load Model (Compile ultra)-2

Wire load model:	**16000**
Location :	**picorv32_pcpi_fast_mul (design)**
Resistance :	**0.001282**
Capacitance :	**0.000569**
Area :	**0.01**
Slope :	**108.438**

Report-Wire load Model - 16000(Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8138.84**				

report_voltage_grtoup

Report- Threshold Voltage Group - (Elobrate)

S.No	Vth Group Name->	undefined
1	**All Cells**	6504 (100.00%)
2	**Blackbox Cells**	0 (0.00%)
3	**Non-Blackbox cells**	6504 (100.00%)
4	**All Cells Area**	0 (0.00%)
5	**Blackbox Cells area**	0 (0.00%)
6	**Non-Blackbox cells area**	0 (0.00%)
7	**All Cells leakage**	0 (0.00%)
8	**Blackbox Cells leakage**	0 (0.00%)
9	**Non-Blackbox cells leakage**	0 (0.00%)

Report- Threshold Voltage Group - (compile)

S.No	Vth Group Name ->	saed32cell_svt
1	**All Cells**	9464 (100.00%)
2	**Blackbox Cells**	0 (0.00%)
3	**Non-Blackbox cells**	9464 (100.00%)
4	**All Cells Area**	32023.67 (100.00%)
5	**Blackbox Cells area**	0 (0.00%)
6	**Non-Blackbox cells area**	32023.67 (100.00%)
7	**All Cells leakage**	56.134uW (100.00%)
8	**Blackbox Cells leakage**	0 (0.00%)
9	**Non-Blackbox cells leakage**	0 (056.134uW (100.00%).00%)

Report- Threshold Voltage Group - (compile ultra)

S.No	Vth Group Name ->	saed32cell_svt
1	**All Cells**	9632 (100.00%)
2	**Blackbox Cells**	0 (0.00%)
3	**Non-Blackbox cells**	9632 (100.00%)
4	**All Cells Area**	32133.97 (100.00%)
5	**Blackbox Cells area**	0 (0.00%)
6	**Non-Blackbox cells area**	32133.97 (100.00%)
7	**All Cells leakage**	57.671uW (100.00%)
8	**Blackbox Cells leakage**	0 (0.00%)
9	**Non-Blackbox cells leakage**	57.671uW (100.00%)

report_clock_tree

Report_clock_tree Global Skew(Elobrate)

S.No		
1	Clock Tree Name	"clk"
2	Clock Period	6.00000
3	Clock Tree root pin	"clk"
4	Number of Levels	1
5	Number of Sinks	1681
6	Number of CT Buffers	0
7	Number of CTS added gates	0
8	Number of Preexisting Gates	0
9	Number of Preexisting Buf/Inv	0
10	Total Number of Clock Cells	0
11	Total Area of CT Buffers	0.00000
12	Total Area of CT cells	0.00000
13	Max Global Skew	0.00000
14	Number of MaxTran Violators	0
15	Number of MaxCap Violators	1
16	Number of MaxFanout Violators	0
1	Operating Condition	worst
2	Clock global Skew	0.000
3	Longest path delay	0.050
4	Shortest path delay	0.050

The longest path delay end pin: genblk1.pcpi_mul/rd_reg[63]/clocked_on
The shortest path delay end pin: genblk1.pcpi_mul/rd_reg[63]/clocked_on

Clock_tree Longest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001802.875	1681	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/clocked_on	1001802.875	0	0	0.050	0.050	r
	Clock Delay					0.05	

Clock_tree Shortest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001802.875	1681	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/clocked_on	1001802.875	0	0	0.050	0.050	r
	Clock Delay					0.05	

Global Skew Report(Compile)

S.No		
1	Clock Tree Name :	"clk"
2	Clock Period :	6.00000
3	Clock Tree root pin :	"clk"
4	Number of Levels :	1
5	Number of Sinks :	1599
6	Number of CT Buffers :	0
7	Number of CTS added gates :	0
8	Number of Preexisting Gates :	0
9	Number of Preexisting Buf/Inv :	0
10	Total Number of Clock Cells :	0
11	Total Area of CT Buffers :	0.00000
12	Total Area of CT cells :	0.00000
13	Max Global Skew :	0.00072
14	Number of MaxTran Violators :	0
15	Number of MaxCap Violators :	1
16	Number of MaxFanout Violators :	0
1	Operating Condition	worst
2	Clock global Skew	0.001
3	Longest path delay	0.124
4	Shortest path delay	0.123

The longest path delay end pin: genblk1.pcpi_mul/active_reg[1]/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rs2_reg[21]/CLK

Clock_tree Longest Path (Compile)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1599	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/clocked_on	1001037.500	0	0	0.124	0.124	r
	Clock Delay					0.124	

Clock_tree Shortest Path (Compile)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1599	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/clocked_on	1001037.500	0	0	0.123	0.123	r
	Clock Delay					0.123	

Global Skew Report(Compile ultra)

S.No		
1	Clock Tree Name :	"clk"
2	Clock Period :	6.00000
3	Clock Tree root pin :	"clk"
4	Number of Levels :	1
5	Number of Sinks :	1582
6	Number of CT Buffers :	0
7	Number of CTS added gates :	0
8	Number of Preexisting Gates :	0
9	Number of Preexisting Buf/Inv :	0
10	Total Number of Clock Cells :	0
11	Total Area of CT Buffers :	0.00000
12	Total Area of CT cells :	0.00000
13	Max Global Skew :	0.00075
14	Number of MaxTran Violators :	0
15	Number of MaxCap Violators :	1
16	Number of MaxFanout Violators :	0
1	Operating Condition	worst
2	Clock global Skew	0.001
3	Longest path delay	0.124
4	Shortest path delay	0.123

The longest path delay end pin: is_lui_auipc_jal_jalr_addi_add_sub_reg/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rs2_reg[0]/CLK

Clock_tree Longest Path (Compile ultra)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1582	0	0	0	r
3	is_lui_auipc_jal_jalr_addi_add_sub_reg/CLK	1001037.500	0	0	0.124	0.124	r
	Clock Delay					0.124	

Clock_tree Shortest Path (Compile ultra)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1582	0	0	0	r
3	genblk1.pcpi_mul/rs2_reg[0]/CLK	1001037.500	0	0	0.123	0.123	r
	Clock Delay					0.123	

report_qor

Report-qor (Elobrate)		
S.No		
	Timing Path Group (none)	
1	Levels of Logic:	0.00
2	Critical Path Length:	0.04
3	Critical Path Slack:	uninit
4	Critical Path Clk Period:	n/a
5	Total Negative Slack:	0.00
6	No. of Violating Paths:	0.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	51
11	Hierarchical Port Count:	3720
12	Leaf Cell Count:	8253
13	Buf/Inv Cell Count:	870
14	Buf Cell Count:	345
15	Inv Cell Count:	525
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	6504
18	Sequential Cell Count:	1749
19	Macro Count:	0
	Area	
20	Combinational Area:	0.000000
21	Noncombinational Area:	0.000000
22	Total Inverter Area:	0.000000
23	Macro/Black Box Area:	0.000000
24	Net Area	7809.676140
	Cell Area:	**0.000000**
	Design Area:	**7809.676140**
	Design Rules	
	Total Number of Nets:	11380
	Nets With Violations:	0
	Max Trans Violations:	0
	Max Cap Violations:	0

Report-qor (Compile)		
S.No		
	Timing Path Group (none)	
1	Levels of Logic:	38.00
2	Critical Path Length:	5.82
3	Critical Path Slack:	-0.86
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	-9.26
6	No. of Violating Paths:	24.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	15
11	Hierarchical Port Count:	1510
12	Leaf Cell Count:	9464
13	Buf/Inv Cell Count:	1458
14	Buf Cell Count:	146
15	Inv Cell Count:	1312
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	7797
18	Sequential Cell Count:	1667
19	Macro Count:	0
	Area	
20	Combinational Area:	21094.460267
21	Noncombinational Area:	10929.208921
22	Buf/Inv Area:	2076.356500
23	Total Buffer Area:	322.51
24	Total Inverter Area:	1753.85
25	Macro/Black Box Area:	0.000000
26	Net Area:	4328.556079
	Cell Area:	**32023.669188**
	Design Area:	**36352.225267**
	Design Rules	
	Total Number of Nets:	11058
	Nets With Violations:	25
	Max Trans Violations:	25
	Max Cap Violations:	0

Report-qor (Compile ultra)		
S.No		
	Timing Path Group (none)	
1	Levels of Logic:	31.00
2	Critical Path Length:	4.92
3	Critical Path Slack:	0.00
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	0.00
6	No. of Violating Paths:	0.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	1
11	Hierarchical Port Count:	134
12	Leaf Cell Count:	9632
13	Buf/Inv Cell Count:	845
14	Buf Cell Count:	8
15	Inv Cell Count:	837
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	7982
18	Sequential Cell Count:	1650
19	Macro Count:	0
	Area	
20	Combinational Area:	21324.206365
21	Noncombinational Area:	10809.761239
22	Buf/Inv Area:	1146.951876
23	Total Buffer Area:	18.55
24	Total Inverter Area:	1128.40
25	Macro/Black Box Area:	0.000000
26	Net Area:	12089.423766
	Cell Area:	**21324.206365**
	Design Area:	**10809.761239**
	Design Rules	
	Total Number of Nets:	10676
	Nets With Violations:	0
	Max Trans Violations:	0
	Max Cap Violations:	0

Comparison

Elobrate vs Compile

Comparison (Elobrate vs compile)

Report	Parameter	Before Compile Value	After Compile Value	Difference	Remarks
report_cell	Top Module cells	3808	5505	1697	Increased by ~1.5X
	Total Cells	4022	9411	5389	
	No of References	63	62	-1	
report_qor	Combinational count	6504	7797	1293	Increased by ~1.2X
	Sequntial Count	1749	1667	-82	Decreased by ~0.9X
	Buf/Inv	870	1458	588	Increased by ~1.6X
report_area	Total area (µm²)	7809.67614	36352.225267	28542.549127	Increased by ~4.6X
	Combinational	0	21094.460267	21094.460267	Same
	Sequential	0	10929.208921	10929.208921	Same
	Buf/Inv Area	0	2076.356500	2076.3565	Same
	Net Interconnect	7809.67614	4328.556079	-3481.120061	Decreased by ~0.5X
report_power	Switching power (uW)	0	10.8277	10.8277	Same
	Internal power (uW)	16.0246	984.6396	968.615	Increased by ~61X
	Leakage power (uW)	0	56134100.0	56134100	Increased by~35LX
	Total Dynamic Power(uW)	16.0247	995.4677	979.443	Increased by~62X
	Total power (uW)	16.0246	1.0516E+03	1035.5754	Increased by ~65X
report_timing	Data Required time	4.7	5.96	1.26	Increased by~1.26X
	Data Arrival time	-2.33	-6.82	-4.49	Increased by~3X
	Slack(max) - Setup	2.37	-0.86	-3.23	Decreased by ~0.5X (Violated)
	Slack(min) - Hold	-0.01	-0.24	-0.23	
report_threshold_voltage_group	All Cells	6504	9464	2960	Increased by~1.5X
	All Cells Area	0	32023.67	32023.67	Same
	All Cells Leakage(uW)	0	56.134	56.134	Same
report_clock_tree	No of sinks	1681	1599	-82	Decreased by ~1X
	Clock Global Skew	0.000	0.001	0.001	Decreased
	Longest path delay	0.050	0.124	0.074	Decreased
	Shortest path delay	0.050	0.123	0.073	Decreased

report_cells

S.No	Cells	Before Compile	After Compile	Difference
1	**ADD_UNS_OP**	10	0	-10
2	**AND2(X2)(X3)(X4)**	387	245	-142
3	**AND3**	4	37	33
4	**AND4**	12	27	15
5	**AND5**	4	0	-4
6	**AO21**		105	105
7	**AO22**	0	1116	1116
8	**AO221**	0	229	229
9	**AO222**	0	200	200
10	**AOI**	0	63	63
11	**ASH_UNS_UNS_OP**	2	0	-2
12	**ASHR_TC_UNS_OP**	1	0	-1
13	**BUF(X16)(X2)(X4)(X8)**	124	138	14
14	**decoder_pseudo_trigger_reg**	0	1	1
15	**DELLN3X2**		2	2
16	**DFF (X1) (X2)**	0	1466	1466
17	**EQ_UNS_OP**	2	0	-2
18	**is_beq_bne_blt_bge_bltu_bgeu_reg**	0	1	1
19	**is_jalr_addi_slti_sltiu_xori_ori_andi_reg**	0	1	1
20	**is_lui_auipc_jal_jalr_addi_add_sub_reg**	0	1	1
21	**LATCH**	0	68	68
22	**LT_TC_OP**	1	0	-1
23	**LT_TC_OP_32_32_1**	1	0	-1
24	**LT_UNS_OP**	1	0	-1
25	**LT_UNS_OP_32_32_1**	1	0	-1
26	**MULT_UNS_OP_3_1_3**	1	0	-1
27	**MUX21**	0	298	298
28	**NAND4**	0	120	120
29	**NAND2**	0	189	189
30	**NAND3X0 X2**	0	72	72
31	**NOR X2**	0	4	4
32	**NOR X3**	0	5	5
33	**NOR X4**	0	13	13
34	**NOT/INV(X0)(X1)(X2)(X4)(X8)**	373	615	242
35	**OA21**	0	11	11
36	**OA22**	0	54	54
37	**OA221**	0	170	170
38	**OA222**	0	145	145
39	**OAI**	0	61	61
40	**OR2(X1)(X2)(X4)**	919	25	-894
41	**OR3**	0	6	6
42	**OR4**	0	21	21
43	**pcpi_timeout_counter_reg[0]**	0	1	1
44	**pcpi_timeout_counter_reg[1]**	0	1	1
45	**pcpi_timeout_counter_reg[2]**	0	1	1
46	**pcpi_timeout_counter_reg[3]**	0	1	1
47	**picorv32_pcpi_fast_mul**	0	1	1
48	**picorv32a_DW_cmp_0**	0	1	1
49	**picorv32a_DW01_add_5**	0	1	1
50	**picorv32a_DW01_cmp6_0**	0	1	1
51	**picorv32a_DW01_dec_0_DW01_dec_1**	0	1	1
52	**picorv32a_DW01_sub_0**	0	1	1
53	**SELECT_OP_11**	8	0	-8
54	**SELECT_OP_2**	199	0	-199
55	**SELECT_OP_3**	35	0	-35
56	**SELECT_OP_4**	24	0	-24
57	**SELECT_OP_5**	9	0	-9
58	**SELECT_OP_6**	5	0	-5
59	**SELECT_OP_7**	2	0	-2
60	**SELECT_OP_9**	29	0	-29
61	**SEQGEN**	1616	0	-1616
62	**SUB_UNS_OP**	6	0	-6
63	**XOR2**	32	0	-32
	TOTAL CELLS	**3808**	**5519**	**1711**

Elobrate vs Compile

Compile vs Compile_ultra

Compile vs compile_ultra

Report	Parameter	compile Value	compile_ultra Value	Difference	Remarks
report_cell	Top Module cells	5505	6806	1301	Increased by ~ 1.5X
	Total Cells	9411	9398	-13	
	No of Refernces	62	57	-5	
report_qor	Combinational Count	7797	7982	185	Increased by ~ 1.1X
	Sequential Count	1667	1650	-17	Decreased by ~0.9X
	Buf/Inv Count	1458	845	-613	Decreased by ~0.5X
report_area	Total area (µm²)	36352.225267	44223.39137	7871.166103	Increased by ~1.3X
	Combinational Area	21094.460267	21324.206365	229.746098	Increased by ~ 1.1X
	Sequential Area	10929.208921	10809.761239	-119.447682	Decreased by ~0.9X
	Buf/Inv Area	2076.356500	1146.951876	-929.404624	Decreased by ~0.5X
	Net Interconnect Area	4328.556079	12089.423766	7760.867687	Increased by ~2.8X
report_power	Switching Power (µW)	10.8277	5.6778	-5.1499	Decreased by ~0.5X
	Internal Power (µW)	984.6396	972.5209	-12.1187	Decreased by ~0.9X
	Leakage Power (µW)	56134100.0	1.0359E+03	-56133064.1	Decreased by ~0.01X
	Total Dynamic Power (µW)	995.4677	978.1987	-17.269	Decreased by ~0.9X
	Total Power (µW)	1.0516E+03	5.7671E+07	5.76699484E+07	Increased by ~5.4X
report_timing	Data Required Time	5.96	5.92	-0.04	Decreased by ~0.9X
	Data Arrival Time	-6.82	-5.92	0.9	Improved by ~0.8X
	Slack(max) - Setup	-0.86	0		Improved by ~0.8X
	Slack(min) - Hold	-0.24			
report_threshold_voltage_group	Cell Count	9464	9632	168	Increased by ~1.1X
	Area	32023.67	32133.97	110.3	Increased by ~1.003X
	Leakage (µW)	56.134	57.671	1.537	Increased by ~1.02X
report_clock_tree	No of Sinks	1599	1582	-17	Decreased by ~0.9X
	Clock Global Skew	0.001	0.001	0	No Change
	Longest Path Delay	0.124	0.124	0	No Change
	Shortest Path Delay	0.123	0.123	0	No Change

report_cells Compile vs Compile ultra

S.No	Cells	Compile	Compile ultra	Difference
1	**AND2X1_RVT**	234	416	182
2	**AND2X2_RVT**	5	23	18
3	**AND2X4_RVT**	6	1	-5
4	**AND3X1_RVT**	37	59	22
5	**AND3X2_RVT**		3	3
6	**AND4X1_RVT**	27	30	3
7	**AO21X1_RVT**	105	107	2
8	**AO221X1_RVT**	221	19	-202
9	**AO221X2_RVT**	8	0	-8
10	**AO222X1_RVT**	200	87	-113
11	**AO22X1_RVT**	1034	1469	435
12	**AO22X2_RVT**	82	0	-82
13	**AOI21X1_RVT**	8	77	69
14	**AOI221X1_RVT**	27	0	-27
15	**AOI222X1_RVT**	28	0	-28
16	**AOI22X2_RVT**	0	1	1
17	**AOI22X1_RVT**	0	148	148
18	**decoder_pseudo_trigger_reg**	1	0	-1
19	**DELLN3X2_RVT**	2	0	-2
20	**DFFSSRX1_RVT**	0	15	15
21	**DFFSSRX2_RVT**	0	1	1
22	**DFFX1_RVT**	1432	1431	-1
23	**DFFX2_RVT**	34	2	-32
24	**FADDX1_RVT**	0	49	49
25	**HADDX1_RVT**	0	49	49
26	**IBUFFX16_RVT**	2	0	-2
27	**IBUFFX2_RVT**	3	0	-3
28	**INVX0_RVT**	40	446	406
29	**INVX1_RVT**	465	0	-465
30	**INVX2_RVT**	65	58	-7
31	**INVX4_RVT**	44	14	-30
32	**INVX8_RVT**	1	0	-1
33	**is_beq_bne_blt_bge_bltu_bgeu_reg**	1	0	-1
34	**is_jalr_addi_slti_sltiu_xori_ori_andi_reg**	1	0	-1
35	**is_lui_auipc_jal_jalr_addi_add_sub_reg**	1	0	-1
36	**LATCHX1_RVT**	68	68	0
37	**MUX21X1_RVT**	297	11	-286
38	**MUX21X2_RVT**	1	0	-1
39	**NAND2X0_RVT**	189	516	327
40	**NAND2X2_RVT**	0	1	1
41	**NAND2X4_RVT**	0	2	2
42	**NAND3X0_RVT**	69	158	89
43	**NAND3X2_RVT**	3	3	0
44	**NAND4X0_RVT**	120	65	-55
45	**NBUFFX2_RVT**	130	4	-126
46	**NBUFFX4_RVT**	2	1	-1
47	**NBUFFX8_RVT**	1	0	-1
48	**NOR2X0_RVT**	4	307	303
49	**NOR2X2_RVT**	0	4	4
50	**NOR2X4_RVT**	0	1	1
51	**NOR3X0_RVT**	5	19	14
52	**NOR4X0_RVT**	0	106	106
53	**NOR4X1_RVT**	13	0	-13
54	**OA21X1_RVT**	11	87	76
55	**OA21X2_RVT**	0	1	1
56	**OA221X1_RVT**	170	10	-160
57	**OA221X2_RVT**	0	1	1
58	**OA222X1_RVT**	145	6	-139
59	**OA22X1_RVT**	54	113	59
60	**OAI21X1_RVT**	36	147	111
61	**OAI21X2_RVT**	0	1	1
62	**OAI221X1_RVT**	2	3	1
63	**OAI222X1_RVT**	8	0	-8
64	**OAI22X1_RVT**	15	109	94
65	**OR2X1_RVT**	23	232	209
66	**OR2X2_RVT**	1	2	1
67	**OR2X4_RVT**	1	0	-1
68	**OR3X1_RVT**	6	84	78
69	**OR3X2_RVT**	0	27	27
70	**OR4X1_RVT**	21	12	-9
71	**pcpi_timeout_counter_reg[0]**	1	0	-1
72	**pcpi_timeout_counter_reg[1]**	1	0	-1
73	**pcpi_timeout_counter_reg[2]**	1	0	-1
74	**pcpi_timeout_counter_reg[3]**	1	0	-1
75	**picorv32_pcpi_fast_mul**	1	1	0
76	**picorv32a_DW_cmp_0**	1	0	-1
77	**picorv32a_DW01_add_5**	1	0	-1
78	**picorv32a_DW01_cmp6_0**	1	0	-1
79	**picorv32a_DW01_dec_0_DW01_dec_1**	1	0	-1
80	**picorv32a_DW01_sub_0**	1	0	-1
81	**XNOR2X1_RVT**	0	88	88
82	**XNOR3X1_RVT**	0	18	18
83	**XOR2X1_RVT**	0	91	91
84	**XOR3X1_RVT**	0	2	2
	TOTAL	**5519**	**6806**	**1287**

Compile vs Compile_ultra

Elobrate vs Compile vs compile_ultra

Report	Parameter	Elobrate	compile	compile_ultra
report_cell	Top Module cells	3808	5505	6806
report_qor	Combinational Count	6504	7797	7982
	Sequential Count	1749	1667	1650
	Buf/Inv Count	870	1458	845
report_area	Combinational Area	0	21094.460267	21324.206365
	Sequential Area	0	10929.208921	10809.761239
	Buf/Inv Area	0	2076.356500	1146.951876
	Net Interconnect Area	7809.67614	4328.556079	12089.423766
	Total area (µm²)	7809.67614	36352.225267	44223.39137
report_power	Internal Power (µW)	16.0246	984.6396	972.5209
	Switching Power (µW)	0	10.8277	5.6778
	Total Dynamic Power (µW)	16.0247	995.4677	978.1987
	Leakage Power (µW)	0	56.134	57.671
	Total Power (µW)	16.0246	1051.6013	1035.9
	SETUP			
report_timing	Data Required Time	4.7	5.96	5.92
	Data Arrival Time	-2.33	-6.82	-5.92
	Slack(max) - Setup	2.37	-0.86	0
	HOLD			
	Data Required Time	0.00	-0.05	-0.06
	Data Arrival Time	-0.01	-0.18	-0.14
	Slack(min) - Hold	-0.01	-0.24	0.21
report_threshold_voltage_group	Cell Count	6504	9464	9632
	Area	0	32023.67	32133.97
	Leakage (µW)	0	56.134	57.671
report_clock_tree	No of Sinks	1681	1599	1582
	Clock Global Skew	0.000	0.001	0.001
	Longest Path Delay	0.050	0.124	0.124
	Shortest Path Delay	0.050	0.123	0.123
get_cells -hierarchical	Total Cells	4022	9411	9398
report_reference	No of Refernces	63	62	57

Summary

Elobrate vs Compile vs compile_ultra				
Report	**Parameter**	**Elobrate**	**compile**	**compile_ultra**
report_cell	Top Module cells	3808	5505	6806
report_qor	Combinational Count	6504	7797	7982
	Sequential Count	1749	1667	1650
	Buf/Inv Count	870	1458	845
report_area	Combinational Area	0	21094.460267	21324.206365
	Sequential Area	0	10929.208921	10809.761239
	Buf/Inv Area	0	2076.356500	1146.951876
	Net Interconnect Area	7809.67614	4328.556079	12089.423766
	Total area (μm²)	7809.67614	36352.225267	44223.39137
report_power	Internal Power (μW)	16.0246	984.6396	972.5209
	Switching Power (μW)	0	10.8277	5.6778
	Total Dynamic Power (μW)	16.0247	995.4677	978.1987
	Leakage Power (μW)	0	56.134	57.671
	Total Power (μW)	16.0246	1051.6013	1035.9
	SETUP			
report_timing	Data Required Time	4.7	5.96	5.92
	Data Arrival Time	-2.33	-6.82	-5.92
	Slack(max) - Setup	2.37	-0.86	0
	HOLD			
	Data Required Time	0.00	-0.05	-0.06
	Data Arrival Time	-0.01	-0.18	-0.14
	Slack(min) - Hold	-0.01	-0.24	0.21
report_threshold_voltage_group	Cell Count	6504	9464	9632
	Area	0	32023.67	32133.97
	Leakage (μW)	0	56.134	57.671
report_clock_tree	No of Sinks	1681	1599	1582
	Clock Global Skew	0.000	0.001	0.001
	Longest Path Delay	0.050	0.124	0.124
	Shortest Path Delay	0.050	0.123	0.123
get_cells -hierarchical	Total Cells	4022	9411	9398
report_reference	No of Refernces	63	62	57

Report - Elobrate vs Compile vs Compile_ultra				
Report	**Parameter**	**Elobrate**	**compile**	**compile_ultra**
report_cell	Top Module cells	3808	5505	6806
report_reference	No of Refernces	63	62	57
report_area	Total area (μm²)	7809.67614	36352.225267	44223.39137
report_power	Total Power (μW)	16.0246	1051.6013	1035.9
report_timing	Slack(max) - Setup	2.37	-0.86	0
	Slack(min) - Hold	-0.01	-0.24	0.21
report_qor	Combinational Count	6504	7797	7982
	Sequential Count	1749	1667	1650
	Buf/Inv Count	870	1458	845
report_threshold_voltage_group	Cell Count	6504	9464	9632
	Area	0	32023.67	32133.97
	Leakage (μW)	0	56.134	57.671
report_clock_tree	No of Sinks	1681	1599	1582
	Clock Global Skew	0.000	0.001	0.001
	Longest Path Delay	0.050	0.124	0.124
	Shortest Path Delay	0.050	0.123	0.123
get_cells -hierarchical	Total Cells	4022	9411	9398

Cell Count = Combinational + Sequential Count