LVT AND RVT

COMPILE			
Report	**Parameter**	**NLDM**	**CCS**
report_cell	Top Module cells	**5343**	**5458**
get_cells -hierarchical	Total Cells	**8598**	**9327**
report_reference	No of Refernces	**71**	**63**
report_qor	Levels of Logic	**70.00**	**60.00**
	Critical Path Length	**6.36**	**4.93**
	Critical Path Slack	**-1.43**	**0.00**
	Total Negative Slack	**-13.62**	**0.00**
	No. of Violating Paths	**19.00**	**0.00**
report_area	Combinational Area	**18679.329838**	**20642.592267**
	Sequential Area	**1580.521542**	**2197.074930**
	Buf/Inv Area	**10927.684057**	**10911.418844**
	Net Interconnect Area	**8977.222396**	**8570.823434**
	Total area (µm²)	**38584.236291**	**40124.834545**
report_power	Internal Power (µW)	**1.7865E+03**	**1.3476E+03**
	Switching Power (µW)	**6.6952**	**5.8677**
	Total Dynamic Power (mW)	**3.1202**	**1.3535**
	Leakage Power (pW)	**3.1202E+09**	**8.3429E+08**
	Total Power (µW)	**4.9134E+03**	**2.1878E+03**
	SETUP		
report_timing	Data Required Time	**5.93**	**5.93**
	Data Arrival Time	**-7.36**	**-5.93**
	Slack(max) - Setup	**-1.43**	**0.00**
	HOLD		
	Data Required Time	**-0.02**	**-0.02**
	Data Arrival Time	**-0.11**	**-0.19**
	Slack(min) - Hold	**0.13**	**0.21**
report_threshold_voltage_group	**LVT**		
	Cell Count	**7619 (89.92%)**	**7768 (84.23%)**
	Area	**26258.41 (88.69%)**	**23872.76 (75.66%)**
	Leakage (µW)	**3.114 (99.80%)**	**660.927 (79.22%)**
	RVT		
	Cell Count	**854 (10.08%)**	**1454 (15.77%)**
	Area	**3348.60 (11.31%)**	**7681.25 (24.34%)**
	Leakage (µW)	**6.150 (0.20%)**	**173.367 (20.78%)**
report_clock_tree	No of Sinks	**1599**	**1599**
	Clock Global Skew	**0.002**	**0.004**
	Longest Path Delay	**0.125**	**0.113**
	Shortest Path Delay	**0.123**	**0.109**

In compile, ccs is better than nldm in terms of timing and power but a slightly higher in area
NLDM chose more LVT than CCS

LVT AND RVT

COMPILE_ULTRA			
Report	**Parameter**	**NLDM**	**CCS**
report_cell	Top Module cells	**7930**	**6387**
get_cells -hierarchical	Total Cells	**10841**	**9083**
report_reference	No of Refernces	**98**	**39**
report_qor	Levels of Logic	**36.00**	**43.00**
	Critical Path Length	**4.92**	**4.93**
	Critical Path Slack	**0.00**	**0.00**
	Total Negative Slack	**0.00**	**0.00**
	No. of Violating Paths	**0.00**	**0.00**
report_area	Combinational Area	**23998.309593**	**19846.359044**
	Sequential Area	**1639.482953**	**862.564742**
	Buf/Inv Area	**10804.932503**	**10799.595480**
	Net Interconnect Area	**11317.279926**	**12944.777122**
	Total area (µm²)	**46120.522022**	**43590.731646**
report_power	Internal Power (µW)	**1.1339E+03**	**1.8953E+03**
	Switching Power (µW)	**6.5549**	**5.6572**
	Total Dynamic Power (mW)	**1.1404**	**1.9009**
	Leakage Power (pW)	**4.7114E+08**	**8.1519E+08**
	Total Power (µW)	**1.6116E+03**	**2.7161E+03**
	SETUP		
report_timing	Data Required Time	**5.92**	**5.93**
	Data Arrival Time	**-5.92**	**-5.93**
	Slack(max) - Setup	**0.00**	**0.00**
	HOLD		
	Data Required Time	**-0.02**	**-0.02**
	Data Arrival Time	**-0.14**	**-0.16**
	Slack(min) - Hold	**0.16**	**0.18**
report_threshold_voltage_group	**LVT**		
	Cell Count	**499 (4.61%)**	**9056 (99.72%)**
	Area	**2375.99 (6.83%)**	**30607.83 (99.88%)**
	Leakage (µW)	**414.344 (87.94%)**	**813.229(99.76%)**
	RVT		
	Cell Count	**10336 (95.39%)**	**25 (0.28%)**
	Area	**32427.25 (93.17%)**	**38.12 (0.12%)**
	Leakage (µW)	**56.797 (12.06%)**	**1.965 (0.24%)**
report_clock_tree	No of Sinks	**1582**	**1582**
	Clock Global Skew	**0.002**	**0.000**
	Longest Path Delay	**0.125**	**0.113**
	Shortest Path Delay	**0.123**	**0.113**

With Compile_ultra, the ccs is better in terms of timing and area,
But power consumption is more.
CCS chose more LVT cells than in NLDM