COMPILE			
Report	**Parameter**	**NLDM**	**CCS**
report_cell	Top Module cells	**5453**	**5317**
get_cells -hierarchical	Total Cells	**9542**	**9659**
report_reference	No of Refernces	**79**	**77**
report_qor	Levels of Logic	**36.00**	**33.00**
	Critical Path Length	**5.72**	**5.33**
	Critical Path Slack	**-0.81**	**-0.36**
	Total Negative Slack	**18.85**	**-2.80**
	No. of Violating Paths	**53.00**	**11.00**
report_area	Combinational Area	20871.575957	**21446.449618**
	Sequential Area	**1827.803657**	**1835.427986**
	Buf/Inv Area	**10926.667481**	**11072.546111**
	Net Interconnect Area	**9290.181642**	**8698.929529**
	Total area (µm²)	**41088.425080**	**41217.925257**
report_power	Internal Power (µW)	**976.7583**	**1.0009E+03**
	Switching Power (µW)	**6.3517**	**5.5400**
	Total Dynamic Power (mW)	**983.1182**	**1.0065**
	Leakage Power (pW)	**4.1695E+07**	**8.5468E+08**
	Total Power (µW)	**1.0248E+03**	**1.8611E+03**
	SETUP		
report_timing	Data Required Time	**5.91**	**5.98**
	Data Arrival Time	**-6.72**	**-6.33**
	Slack(max) - Setup	**-0.81**	**-0.36**
	HOLD		
	Data Required Time	**-0.05**	**-0.02**
	Data Arrival Time	**-0.18**	**-0.26**
	Slack(min) - Hold	**0.24**	**0.28**
report_threshold_voltage_group	**HVT**		
	Cell Count	**1653 (17.46%)**	**1554 (16.52%)**
	Area	**7365.86 (23.16%)**	**7415.16 (22.80%)**
	Leakage (µW)	**3.955uW (9.49%)**	**171.332uW (20.05%)**
	RVT		
	Cell Count	**7815 (82.54%)**	**7852 (83.48%)**
	Area	**24432.39 (76.84%)**	**25103.84 (77.20%)**
	Leakage (µW)	**37.740uW (90.51%)**	**683.344uW (79.95%)**
report_clock_tree	No of Sinks	**1599**	**1599**
	Clock Global Skew	**0.022**	**0.009**
	Longest Path Delay	**0.124**	**0.109**
	Shortest Path Delay	**0.102**	**0.100**

In Compile, CCS is better in terms of timing slightly,
But more area and power consumption
CCS chose more HVT than NLDM

COMPILE_ULTRA			
Report	**Parameter**	**NLDM**	**CCS**
report_cell	Top Module cells	**8338**	**6833**
get_cells -hierarchical	Total Cells	**11150**	**9777**
report_reference	No of Refernces	**89**	**47**
report_qor	Levels of Logic	**15.00**	**41.00**
	Critical Path Length	**4.92**	**4.92**
	Critical Path Slack	**0.00**	**0.00**
	Total Negative Slack	**0.00**	**0.00**
	No. of Violating Paths	**0.00**	**0.00**
report_area	Combinational Area	**24732.023257**	**21768.450082**
	Sequential Area	**1560.190026**	**945.161542**
	Buf/Inv Area	**10841.020944**	**10803.661784**
	Net Interconnect Area	**11337.617419**	**12963.716499**
	Total area (μm²)	**46910.661620**	**45535.828365**
report_power	Internal Power (μW)	**991.1247**	**972.9865**
	Switching Power (μW)	**5.6776**	**5.4189**
	Total Dynamic Power (mW)	**996.8053**	**978.4088**
	Leakage Power (pW)	**5.0851E+07**	**8.6219E+08**
	Total Power (μW)	**1.0477E+03**	**1.8406E+03**
	SETUP		
report_timing	Data Required Time	**5.92**	**5.92**
	Data Arrival Time	**-5.92**	**-5.92**
	Slack(max) - Setup	**0.00**	**0.00**
	HOLD		
	Data Required Time	**0.06**	**-0.02**
	Data Arrival Time	**-0.28**	**-0.26**
	Slack(min) - Hold	**0.22**	**0.28**
report_threshold_voltage_group	**HVT**		
	Cell Count	**4872 (44.01%)**	**145 (1.48%)**
	Area	**11347.78 (31.90%)**	**383.00 (1.18%)**
	Leakage (μW)	**2.780uW (5.47%)**	**10.360uW (1.20%)**
	RVT		
	Cell Count	**6198 (55.99%)**	**9630 (98.52%)**
	Area	**24225.26 (68.10%)**	**32189.12 (98.82%)**
	Leakage (μW)	**48.071uW (94.53%)**	**851.826uW (98.80%)**
report_clock_tree	No of Sinks	**1582**	**1582**
	Clock Global Skew	**0.224**	**0.009**
	Longest Path Delay	**1.247**	**0.109**
	Shortest Path Delay	**1.023**	**0.100**

With Compile_ultra, CCS is good in terms of timing and area,
But more power consumption
NLDM chose more HVT than CCS