Report_cell (compile)

S.No	Reference	Cell Count	Library	Unit Area	Area	Attributes
1	AND2X1_RVT	244	saed32rvt_tt0p78vn40c	2.033152	496.089113	
2	AND3X1_RVT	32	saed32rvt_tt0p78vn40c	2.287296	73.193474	
3	AND4X1_RVT	21	saed32rvt_tt0p78vn40c	2.541440	53.370240	
4	AO21X1_RVT	102	saed32rvt_tt0p78vn40c	2.541440	259.226881	
5	AO221X1_RVT	236	saed32rvt_tt0p78vn40c	3.049728	719.735788	
6	AO222X1_RVT	207	saed32rvt_tt0p78vn40c	3.303872	683.901526	
7	AO22X1_RVT	1111	saed32rvt_tt0p78vn40c	2.541440	2823.539851	
8	AOI21X1_RVT	6	saed32rvt_tt0p78vn40c	3.049728	18.298368	
9	AOI221X1_RVT	23	saed32rvt_tt0p78vn40c	3.558016	81.834369	
10	AOI222X1_RVT	22	saed32rvt_tt0p78vn40c	3.812160	83.867520	
11	AOI22X1_RVT	1	saed32rvt_tt0p78vn40c	3.049728	3.049728	
12	DELLN3X2_RVT	2	saed32rvt_tt0p78vn40c	9.657472	19.314943	
13	DFFSSRX1_RVT	7	saed32rvt_tt0p78vn40c	7.116032	49.812225	n
14	DFFX1_RVT	1459	saed32rvt_tt0p78vn40c	6.607744	9640.698812	n
15	INVX0_RVT	88	saed32rvt_tt0p78vn40c	1.270720	111.823360	
16	INVX1_RVT	471	saed32rvt_tt0p78vn40c	1.270720	598.509122	
17	LATCHX1_RVT	68	saed32rvt_tt0p78vn40c	5.082880	345.635841	n
18	MUX21X1_RVT	298	saed32rvt_tt0p78vn40c	3.303872	984.553888	
19	NAND2X0_RVT	158	saed32rvt_tt0p78vn40c	1.524864	240.928505	
20	NAND3X0_RVT	75	saed32rvt_tt0p78vn40c	1.779008	133.425602	
21	NAND4X0_RVT	125	saed32rvt_tt0p78vn40c	2.033152	254.144013	
22	NBUFFX2_RVT	17	saed32rvt_tt0p78vn40c	2.033152	34.563586	
23	NOR2X0_RVT	7	saed32rvt_tt0p78vn40c	2.541440	17.790080	
24	NOR3X0_RVT	6	saed32rvt_tt0p78vn40c	2.795584	16.773504	
25	NOR4X1_RVT	15	saed32rvt_tt0p78vn40c	3.049728	45.745919	
26	OA21X1_RVT	14	saed32rvt_tt0p78vn40c	2.541440	35.580160	
27	OA221X1_RVT	173	saed32rvt_tt0p78vn40c	3.049728	527.602930	
28	OA222X1_RVT	138	saed32rvt_tt0p78vn40c	3.303872	455.934351	
29	OA22X1_RVT	65	saed32rvt_tt0p78vn40c	2.541440	165.193601	
30	OAI21X1_RVT	38	saed32rvt_tt0p78vn40c	3.049728	115.889661	
31	OAI221X1_RVT	3	saed32rvt_tt0p78vn40c	3.558016	10.674048	
32	OAI222X1_RVT	8	saed32rvt_tt0p78vn40c	3.812160	30.497280	
33	OAI22X1_RVT	15	saed32rvt_tt0p78vn40c	3.049728	45.745919	
34	OR2X1_RVT	17	saed32rvt_tt0p78vn40c	2.033152	34.563586	
35	OR3X1_RVT	6	saed32rvt_tt0p78vn40c	2.541440	15.248640	
36	OR4X1_RVT	8	saed32rvt_tt0p78vn40c	3.558016	28.464128	
37	picorv32_pcpi_fast_mul	1		9395.449458	9395.449458	h, n
38	picorv32a_DW_cmp_0	1		241.436800	241.436800	h
39	picorv32a_DW01_add_0	1		195.690874	195.690874	h
40	picorv32a_DW01_add_2	1		183.491969	183.491969	h
41	picorv32a_DW01_add_3	1		220.088705	220.088705	h
42	picorv32a_DW01_add_4	1		199.757178	199.757178	h
43	picorv32a_DW01_add_5	1		181.712954	181.712954	h
44	picorv32a_DW01_add_6	1		188.574849	188.574849	h
45	picorv32a_DW01_add_J5_0	1		298.365051	298.365051	h
46	picorv32a_DW01_cmp6_0	1		199.248897	199.248897	h
47	picorv32a_DW01_dec_0_DW01_dec_1	1		181.458819	181.458819	h
48	picorv32a_DW01_inc_J2_0	1		426.453630	426.453630	h
49	picorv32a_DW01_inc_J3_0	1		422.895614	422.895614	h
50	picorv32a_DW01_sub_0	1		202.044475	202.044475	h
51	XNOR2X1_RVT	2	saed32rvt_tt0p78vn40c	4.320448	8.640896	
	Total Cells = 9460	5302			31800.530731	

Total cells and refernece

Total cells	9460
Total reference	51

Report_Area

S.No	Number of	Count	Area
1	Number of ports:	1919	
2	Number of nets:	12367	
3	Number of cells:	9460	
4	Number of combinational cells:	7713	
5	Number of sequential cells:	1667	
6	Number of macros/black boxes:	0	
7	Number of buf/inv:	1351	
8	Number of references:	51	
9	Combinational area:		20885.553873
10	Buf/Inv area:		1764.267653
11	Noncombinational area:		10914.976860
12	Macro/Black Box area:		0.000000
13	Net Interconnect area:		9298.772721
	Total Cell Area		31800.530733
	Total Area		41099.303454

Report_power-1

S.No	Design	Wire Load Model	Library
1	picorv32a	35000	saed32rvt_tt0p78vn40c
2	picorv32_pcpi_fast_mul	16000	saed32rvt_tt0p78vn40c
3	picorv32a_DW01_add_0	ForQA	saed32rvt_tt0p78vn40c
4	picorv32a_DW01_add_2	ForQA	saed32rvt_tt0p78vn40c
5	picorv32a_DW01_add_3	8000	saed32rvt_tt0p78vn40c
6	picorv32a_DW_cmp_0	8000	saed32rvt_tt0p78vn40c
7	picorv32a_DW01_add_4	ForQA	saed32rvt_tt0p78vn40c
8	picorv32a_DW01_sub_0	ForQA	saed32rvt_tt0p78vn40c
9	picorv32a_DW01_add_5	ForQA	saed32rvt_tt0p78vn40c
10	picorv32a_DW01_dec_0_DW01_dec_1	ForQA	saed32rvt_tt0p78vn40c
11	icorv32a_DW01_cmp6_0	ForQA	saed32rvt_tt0p78vn40c
12	picorv32a_DW01_add_6	ForQA	saed32rvt_tt0p78vn40c
13	picorv32_pcpi_fast_mul_DW_mult_tc_1	16000	saed32rvt_tt0p78vn40c
14	picorv32a_DW01_inc_J2_0	8000	saed32rvt_tt0p78vn40c
15	picorv32a_DW01_inc_J3_0	8000	saed32rvt_tt0p78vn40c
16	picorv32a_DW01_add_J5_0	8000	saed32rvt_tt0p78vn40c

Cell Internal Power = 981.6295 uW (99%)
Net Switching Power = 5.5829 uW (1%)
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Total Dynamic Power = 987.2123 uW (100%)
Cell Leakage Power = 834.4452 uW

Report-power-2

S.No	Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
1	io_pad	0.0000	0.0000	0.0000	0.0000	0.00%	
2	memory	0.0000	0.0000	0.0000	0.0000	0.00%	
3	black_box	0.0000	0.0000	0.0000	0.0000	0.00%	
4	clock_network	972.2699	0.0000	0.0000	972.2699	53.37%	i
5	register	3.4109	0.9747	2.2543E+08	229.8086	12.62%	
6	sequential	0.4724	8.4505E-02	9.8156E+06	10.3725	0.57%	
7	combinational	5.4744	4.5237	5.992E+08	609.2015	33.44%	
	Total (uW)	981.6275 uW	5.5829 uW	8.3445e+08 pW	1.8217e+03 uW		

Report hierarchy (compile)

picorv32a	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
AND3X1_RVT	saed32rvt_tt0p78vn40c
AND4X1_RVT	saed32rvt_tt0p78vn40c
AO21X1_RVT	saed32rvt_tt0p78vn40c
AO22X1_RVT	saed32rvt_tt0p78vn40c
AO221X1_RVT	saed32rvt_tt0p78vn40c
AO222X1_RVT	saed32rvt_tt0p78vn40c
AOI21X1_RVT	saed32rvt_tt0p78vn40c
AOI22X1_RVT	saed32rvt_tt0p78vn40c
AOI221X1_RVT	saed32rvt_tt0p78vn40c
AOI222X1_RVT	saed32rvt_tt0p78vn40c
DELLN3X2_RVT	saed32rvt_tt0p78vn40c
DFFSSRX1_RVT	saed32rvt_tt0p78vn40c
DFFX1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
LATCHX1_RVT	saed32rvt_tt0p78vn40c
MUX21X1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND3X0_RVT	saed32rvt_tt0p78vn40c
NAND4X0_RVT	saed32rvt_tt0p78vn40c
NBUFFX2_RVT	saed32rvt_tt0p78vn40c
NOR2X0_RVT	saed32rvt_tt0p78vn40c
NOR3X0_RVT	saed32rvt_tt0p78vn40c
NOR4X1_RVT	saed32rvt_tt0p78vn40c
OA21X1_RVT	saed32rvt_tt0p78vn40c
OA22X1_RVT	saed32rvt_tt0p78vn40c
OA221X1_RVT	saed32rvt_tt0p78vn40c
OA222X1_RVT	saed32rvt_tt0p78vn40c
OAI21X1_RVT	saed32rvt_tt0p78vn40c
OAI22X1_RVT	saed32rvt_tt0p78vn40c
OAI221X1_RVT	saed32rvt_tt0p78vn40c
OAI222X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
OR3X1_RVT	saed32rvt_tt0p78vn40c
OR4X1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32_pcpi_fast_mul	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
AND3X1_RVT	saed32rvt_tt0p78vn40c
AND4X1_RVT	saed32rvt_tt0p78vn40c
AO21X1_RVT	saed32rvt_tt0p78vn40c
AO22X1_RVT	saed32rvt_tt0p78vn40c
DFFX1_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
MUX21X1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND3X0_RVT	saed32rvt_tt0p78vn40c
NAND4X0_RVT	saed32rvt_tt0p78vn40c
NOR4X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32_pcpi_fast_mul_DW_mult_tc_1	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
AO21X1_RVT	saed32rvt_tt0p78vn40c
AOI21X1_RVT	saed32rvt_tt0p78vn40c
AOI22X1_RVT	saed32rvt_tt0p78vn40c
AOI222X1_RVT	saed32rvt_tt0p78vn40c
FADDX1_RVT	saed32rvt_tt0p78vn40c
HADDX1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND3X0_RVT	saed32rvt_tt0p78vn40c
NOR2X0_RVT	saed32rvt_tt0p78vn40c
NOR2X1_RVT	saed32rvt_tt0p78vn40c
OA21X1_RVT	saed32rvt_tt0p78vn40c
OAI21X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_0	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
DELLN3X2_RVT	saed32rvt_tt0p78vn40c
FADDX1_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND3X0_RVT	saed32rvt_tt0p78vn40c
NAND3X2_RVT	saed32rvt_tt0p78vn40c
NBUFFX2_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR3X2_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_2	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_3	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
FADDX1_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_4	
AND2X1_RVT	saed32rvt_tt0p78vn40c
DELLN3X2_RVT	saed32rvt_tt0p78vn40c
FADDX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND3X0_RVT	saed32rvt_tt0p78vn40c
NBUFFX2_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR3X2_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_5	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
DELLN3X2_RVT	saed32rvt_tt0p78vn40c
FADDX1_RVT	saed32rvt_tt0p78vn40c
IBUFFX2_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR3X2_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_6	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_J5_0	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
AO21X1_RVT	saed32rvt_tt0p78vn40c
AOI21X1_RVT	saed32rvt_tt0p78vn40c
FADDX1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NOR2X0_RVT	saed32rvt_tt0p78vn40c
NOR2X1_RVT	saed32rvt_tt0p78vn40c
OA21X1_RVT	saed32rvt_tt0p78vn40c
OAI21X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_cmp6_0	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
AO221X1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND4X0_RVT	saed32rvt_tt0p78vn40c
NOR4X0_RVT	saed32rvt_tt0p78vn40c
OA22X1_RVT	saed32rvt_tt0p78vn40c
OA221X1_RVT	saed32rvt_tt0p78vn40c
OA222X1_RVT	saed32rvt_tt0p78vn40c
OAI22X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_dec_0_DW01_dec_1	r
AO21X1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_inc_J2_0	r
HADDX1_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NOR2X1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_inc_J3_0	r
HADDX1_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NOR2X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR2X1_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW01_sub_0	r
FADDX1_RVT	saed32rvt_tt0p78vn40c
IBUFFX2_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
OR2X2_RVT	saed32rvt_tt0p78vn40c
XNOR2X1_RVT	saed32rvt_tt0p78vn40c
XOR3X2_RVT	saed32rvt_tt0p78vn40c
picorv32a_DW_cmp_0	r
AND2X1_RVT	saed32rvt_tt0p78vn40c
AND4X1_RVT	saed32rvt_tt0p78vn40c
AO22X1_RVT	saed32rvt_tt0p78vn40c
AO221X1_RVT	saed32rvt_tt0p78vn40c
AOI22X1_RVT	saed32rvt_tt0p78vn40c
INVX0_RVT	saed32rvt_tt0p78vn40c
INVX1_RVT	saed32rvt_tt0p78vn40c
NAND2X0_RVT	saed32rvt_tt0p78vn40c
NAND3X0_RVT	saed32rvt_tt0p78vn40c
NAND4X0_RVT	saed32rvt_tt0p78vn40c
NOR3X0_RVT	saed32rvt_tt0p78vn40c
OA21X1_RVT	saed32rvt_tt0p78vn40c
OA22X1_RVT	saed32rvt_tt0p78vn40c
OA221X1_RVT	saed32rvt_tt0p78vn40c
OAI21X1_RVT	saed32rvt_tt0p78vn40c
OAI22X1_RVT	saed32rvt_tt0p78vn40c
OR2X1_RVT	saed32rvt_tt0p78vn40c

hierarchy (compile)

Attributes:	
r	- licensed design

Report-wireload model (Compile)

Wire load model	35000
Location	Picorv32a (design)
Resistance	0.00118
Capacitance	0.00027
Area	0.01
Slope	140.36

Report-Wire load Model 35000 (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	16.92				
2	2	39.03				
3	3	64.09				
4	4	92.51				
5	5	124.73				
6	6	161.17				
7	7	202.25				
8	8	248.42				
9	9	300.09				
10	10	357.68				
11	11	421.63				
12	12	492.37				
13	13	570.31				
14	14	655.89				
15	15	749.54				
16	16	851.67				
17	17	962.72				
18	18	1083.11				
19	19	1213.28				
20	20	1353.64				
	Total Length	9961.05				

Report-Wire load Model -2 (Compile)

Wire load model:	16000
Location :	picorv32_pcpi_fast_mul(design)
Resistance :	0.001282
Capacitance :	0.000569
Area :	0.01
Slope :	108.438

Report-Wire load Model -16000 (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	8138.84				

Report-Wire load Model -3 (Compile)

Wire load model:	ForQA
Location :	picorv32a_DW01_add_0 (design)
Resistance :	0.002067
Capacitance :	0.026724
Area :	0.01
Slope :	30.2854

Report-Wire load Model -FORQA(Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	8.28				
2	2	18.49				
3	3	29.35				
4	4	40.92				
5	5	53.23				
6	6	66.36				
7	7	80.36				
8	8	95.27				
9	9	111.17				
10	10	128.09				
11	11	146.10				
12	12	165.26				
13	13	185.61				
14	14	207.22				
15	15	230.13				
16	16	254.41				
17	17	280.11				
18	18	307.28				
19	19	335.98				
20	20	366.27				
	Total Length	3109.89				

Report-Wire load Model -4 (Compile)

Wire load model:	8000
Location :	picorv32a_DW01_add_3 (design)
Resistance :	0.0015727
Capacitance :	0.000312
Area :	0.01
Slope :	90.6464

Report-Wire load Model - 8000(Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	13.94				
2	2	31.80				
3	3	51.61				
4	4	73.61				
5	5	98.05				
6	6	125.17				
7	7	155.23				
8	8	188.46				
9	9	225.12				
10	10	265.45				
11	11	309.71				
12	12	358.13				
13	13	410.96				
14	14	468.46				
15	15	530.86				
16	16	598.42				
17	17	671.38				
18	18	749.98				
19	19	834.49				
20	20	925.13				
	Total Length	7085.96				

Report_clock_tree Global Skew Report

S.No		
1	Clock Tree Name :	"clk"
2	Clock Period :	6.00000
3	Clock Tree root pin :	"clk"
4	Number of Levels :	1
5	Number of Sinks :	1599
6	Number of CT Buffers :	0
7	Number of CTS added gates :	0
8	Number of Preexisting Gates :	0
9	Number of Preexisting Buf/Inv :	0
10	Total Number of Clock Cells :	0
11	Total Area of CT Buffers :	0.00000
12	Total Area of CT cells :	0.00000
13	Max Global Skew :	0.00031
14	Number of MaxTran Violators :	0
15	Number of MaxCap Violators :	1
16	Number of MaxFanout Violators :	0
1	Operating Condition	worst
2	Clock global Skew	0.000
3	Longest path delay	0.109
4	Shortest path delay	0.109

The longest path delay end pin: count_cycle_reg[57]/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rs1_reg[5]/CLK

Clock_tree Longest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0.000	1	0.000	0.000	0.000	r
2	clk	1001037.500	1599	0.000	0.000	0.000	r
3	count_cycle_reg[57]/CLK	1001037.500	0	0.000	0.109	0.109	r
	Clock Delay					0.109	

Clock_tree Shortest Path

S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1599	0	0	0	r
3	genblk1.pcpi_mul/rs1_reg[5]/CLK	1001037.500	0	0	0.109	0.109	r
	Clock Delay					0.109	

Report- Threshold Voltage Group-compile

S.No	Vth Group Name->	saed32cell_svt
2	All Cells	9380 (100.00%)
3	Blackbox Cells	0 (0.00%)
4	Non-Blackbox cells	9380 (100.00%)
5	All Cells Area	31800.53 (100.00%)
6	Blackbox Cells area	0 (0.00%)
7	Non-Blackbox cells area	31800.53 (100.00%)
8	All Cells leakage	834.445uW (100.00%)
9	Blackbox Cells leakage	0.000pW (0.00%)
10	Non-Blackbox cells leakage	834.445uW (100.00%)

Report-qor (Compile)-1

S.No	Timing Path Group (clk)	
1	Levels of Logic:	36.00
2	Critical Path Length:	5.29
3	Critical Path Slack:	-0.36
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	-2.43
6	No. of Violating Paths:	10.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	15
11	Hierarchical Port Count:	1510
12	Leaf Cell Count:	9380
13	Buf/Inv Cell Count:	1315
14	Buf Cell Count:	29
15	Inv Cell Count:	1286
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	7713
18	Sequential Cell Count:	1667
	Area	
19	Combinational Area:	20885.553873
20	Noncombinational Area:	10914.976860
21	Buf/Inv Area:	1764.267653
22	Total Buffer Area:	127.58
23	Total Inverter Area:	1636.69
24	Macro/Black Box Area:	0.000000
25	Net Area:	9298.772721
26	Cell Area:	31800.530733
27	Design Area:	41099.303454
	Design Rules	
28	Total Number of Nets:	10994
29	Nets With Violations:	0
30	Max Trans Violations:	0
31	Max Cap Violations:	0

Report_timing - 1 (Compile)

S.No		
1	Startpoint:	decoded_imm_reg[0] (rising edge-triggered flip-flop clocked by clk)
2	Endpoint:	reg_out_reg[31] (rising edge-triggered flip-flop clocked by clk)
3	Path Group:	Clk
4	Path Type:	max

Report_timing-2 (Compile)

Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_0	ForQA	saed32rvt_tt0p78vn40c

report_timing(Compile)

S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	1.00	1.00	
3	decoded_imm_reg[0]/CLK (DFFX1_RVT)	0.00 #	1.00	r
4	decoded_imm_reg[0]/Q (DFFX1_RVT)	0.30	1.30	f
5	add_1784/B[0] (picorv32a_DW01_add_0)	0.00	1.30	f
6	add_1784/U8/Y (AND2X1_RVT)	0.08	1.39	f
7	add_1784/U11/Y (NAND2X0_RVT)	0.06	1.45	r
8	add_1784/U12/Y (NAND3X0_RVT)	0.09	1.54	f
9	add_1784/L1(2)/U1/CO (FADDX1_RVT)	0.17	1.70	f
10	add_1784/L1(3)/U1/CO (FADDX1_RVT)	0.15	1.86	f
11	add_1784/L1(4)/U1/CO (FADDX1_RVT)	0.15	2.01	f
12	add_1784/L1(5)/U1/CO (FADDX1_RVT)	0.15	2.16	f
13	add_1784/L1(6)/U1/CO (FADDX1_RVT)	0.15	2.31	f
14	add_1784/L1(7)/U1/CO (FADDX1_RVT)	0.15	2.47	f
15	add_1784/L1(8)/U1/CO (FADDX1_RVT)	0.15	2.62	f
16	add_1784/L1(9)/U1/CO (FADDX1_RVT)	0.15	2.77	f
17	add_1784/L1(10)/U1/CO (FADDX1_RVT)	0.15	2.92	f
18	add_1784/L1(11)/U1/CO (FADDX1_RVT)	0.15	3.07	f
19	add_1784/L1(12)/U1/CO (FADDX1_RVT)	0.15	3.23	f
20	add_1784/L1(13)/U1/CO (FADDX1_RVT)	0.15	3.38	f
21	add_1784/L1(14)/U1/CO (FADDX1_RVT)	0.15	3.53	f
22	add_1784/L1(15)/U1/CO (FADDX1_RVT)	0.15	3.68	f
23	add_1784/L1(16)/U1/CO (FADDX1_RVT)	0.15	3.83	f
24	add_1784/L1(17)/U1/CO (FADDX1_RVT)	0.15	3.99	f
25	add_1784/L1(18)/U1/CO (FADDX1_RVT)	0.15	4.14	f
26	add_1784/L1(19)/U1/CO (FADDX1_RVT)	0.15	4.29	f
27	add_1784/L1(20)/U1/CO (FADDX1_RVT)	0.15	4.44	f
28	add_1784/L1(21)/U1/CO (FADDX1_RVT)	0.15	4.60	f
29	add_1784/L1(22)/U1/CO (FADDX1_RVT)	0.15	4.75	f
30	add_1784/L1(23)/U1/CO (FADDX1_RVT)	0.15	4.90	f
31	add_1784/L1(24)/U1/CO (FADDX1_RVT)	0.15	5.05	f
32	add_1784/L1(25)/U1/CO (FADDX1_RVT)	0.15	5.20	f
33	add_1784/L1(26)/U1/CO (FADDX1_RVT)	0.15	5.36	f
34	add_1784/L1(27)/U1/CO (FADDX1_RVT)	0.15	5.51	f
35	add_1784/L1(28)/U1/CO (FADDX1_RVT)	0.15	5.66	f
36	add_1784/L1(29)/U1/CO (FADDX1_RVT)	0.15	5.81	f
37	add_1784/L1(30)/U1/CO (FADDX1_RVT)	0.15	5.96	f
38	add_1784/L1(31)/U1/Y (XOR3X2_RVT)	0.12	6.08	r
39	add_1784/SUM[31] (picorv32a_DW01_add_0)	0.00	6.08	r
40	U4213/Y (NAND2X0_RVT)	0.05	6.13	f
41	U4214/Y (NAND3X0_RVT)	0.06	6.20	r
42	U4215/Y (OR2X1_RVT)	0.08	6.28	r
43	reg_out_reg[31]/D (DFFX1_RVT)	0.01	6.29	r
44	data arrival time		6.29	
	clock clk (rise edge)	6.00	6.00	
	clock network delay (ideal)	1.00	7.00	
	clock uncertainty	-1.00	6.00	
	reg_out_reg[31]/CLK (DFFX1_RVT)	0.00	6.00	r
	library setup time	-0.08	5.92	
	data required time		5.92	
	data required time		5.92	
	data arrival time		-6.29	
	slack (VIOLATED)		-0.36	

Report_timing - 1 (Compile)-1

S.No		
1	Startpoint:	instr_blt_reg (rising edge-triggered flip-flop clocked by clk)
2	Endpoint:	is_slti_blt_slt_reg (rising edge-triggered flip-flop clocked by clk)
3	Path Group:	Clk
4	Path Type:	min

Report_timing-2 (Compile)-1

Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c

report_timing(Compile)-1

S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	0.00	0.00	
3	instr_blt_reg/CLK (DFFX1_RVT)	0.00 #	0.00	r
4	instr_blt_reg/QN (DFFX1_RVT)	0.13	0.13	f
5	U3050/Y (NAND3X0_RVT)	0.07	0.20	r
6	is_slti_blt_slt_reg/D (DFFX1_RVT)	0.01	0.21	r
7	data arrival time		0.21	
	clock clk (rise edge)	0.00	0.00	
	clock network delay (ideal)	0.00	0.00	
	is_slti_blt_slt_reg/CLK (DFFX1_RVT)	0.00	0.00	r
	library hold time	-0.04	-0.04	
	data required time		-0.04	
	data required time		-0.04	
	data arrival time		-0.21	
	Slack (MET)		0.25	

Report-cell

S.No	Reference	Count	Library	Unit Area	Total Area	Attributes
1	AND2X1_RVT	917	saed32rvt_tt0p78vm40c	2.033152	1251.139637	
2	AND3X1_RVT	65	saed32rvt_tt0p78vm40c	2.287296	148.674244	
3	AND4X1_RVT	22	saed32rvt_tt0p78vm40c	2.541440	55.911680	
4	AO21X1_RVT	130	saed32rvt_tt0p78vm40c	2.541440	330.387201	
5	AO22X1_RVT	1458	saed32rvt_tt0p78vm40c	2.541440	3705.419535	
6	AO221X1_RVT	18	saed32rvt_tt0p78vm40c	3.049728	54.895103	
7	AO222X1_RVT	70	saed32rvt_tt0p78vm40c	3.303872	231.271048	
8	AOI21X1_RVT	89	saed32rvt_tt0p78vm40c	3.049728	271.425785	
9	AOI22X1_RVT	157	saed32rvt_tt0p78vm40c	3.049728	478.807283	
10	AOI222X1_RVT	12	saed32rvt_tt0p78vm40c	3.812160	45.745920	
11	DFFSSRX1_RVT	7	saed32rvt_tt0p78vm40c	7.116032	49.812225	n
12	DFFX1_RVT	1442	saed32rvt_tt0p78vm40c	6.607744	9528.367161	n
13	FADD1_RVT	58	saed32rvt_tt0p78vm40c	4.828736	280.066678	r
14	HADD1_RVT	48	saed32rvt_tt0p78vm40c	3.303872	158.585861	r
15	INV0Z_RVT	263	saed32rvt_tt0p78vm40c	1.270720	334.198361	
16	INVX1_RVT	177	saed32rvt_tt0p78vm40c	1.270720	224.917441	
17	LATCHX1_RVT	68	saed32rvt_tt0p78vm40c	5.083880	345.635841	n
18	MUX21X1_RVT	11	saed32rvt_tt0p78vm40c	3.303872	36.342593	
19	NAND2X0_RVT	588	saed32rvt_tt0p78vm40c	1.524864	896.620008	
20	NAND3X0_RVT	168	saed32rvt_tt0p78vm40c	1.779008	298.873349	
21	NAND4X0_RVT	63	saed32rvt_tt0p78vm40c	2.033152	128.086983	
22	NBUFFX2_RVT	30	saed32rvt_tt0p78vm40c	2.033152	60.994563	
23	NOR2X0_RVT	260	saed32rvt_tt0p78vm40c	2.541440	660.774403	
24	NOR3X0_RVT	14	saed32rvt_tt0p78vm40c	2.795584	39.138175	
25	NOR4X1_RVT	101	saed32rvt_tt0p78vm40c	3.049728	308.022520	
26	OA21X1_RVT	78	saed32rvt_tt0p78vm40c	2.541440	198.232321	
27	OA22X1_RVT	80	saed32rvt_tt0p78vm40c	2.541440	203.315201	
28	OA221X1_RVT	11	saed32rvt_tt0p78vm40c	3.049728	33.547007	
29	OA222X1_RVT	6	saed32rvt_tt0p78vm40c	3.303872	19.823233	
30	OAI21X1_RVT	148	saed32rvt_tt0p78vm40c	3.049728	451.359732	
31	OAI22X1_RVT	114	saed32rvt_tt0p78vm40c	3.049728	347.668983	
32	OAI221X1_RVT	3	saed32rvt_tt0p78vm40c	3.558016	10.674048	
33	OAI222X1_RVT	1	saed32rvt_tt0p78vm40c	3.812160	3.812160	
34	ORDX1_RVT	262	saed32rvt_tt0p78vm40c	2.033152	532.685851	
35	ORX1_RVT	50	saed32rvt_tt0p78vm40c	2.541440	127.072001	
36	ORX2_RVT	28	saed32rvt_tt0p78vm40c	2.541440	71.160320	
37	ORAI1_RVT	19	saed32rvt_tt0p78vm40c	3.558016	67.602305	
38	XNOR2X1_RVT	92	saed32rvt_tt0p78vm40c	4.320448	397.481209	
39	XNOR3X1_RVT	6	saed32rvt_tt0p78vm40c	6.099456	36.596735	
40	XOR2X1_RVT	89	saed32rvt_tt0p78vm40c	4.320448	384.519865	
41	XOR3X1_RVT	3	saed32rvt_tt0p78vm40c	7.116032	21.348096	
42	picorv32_pcpi_fast_mul	1	saed32rvt_tt0p78vm40c	9690.510610	9690.510610	h, n
	TOTAL	**6827**			**9924.698642**	**32321.525870**

Total cells and refernece

Total cells	9780
Total reference	42

Report-area (Compile Ultra)

S.No		Area	Count
1	**Number of ports:**		543
2	**Number of nets:**		10906
3	**Number of cells:**		9780
4	**Number of combinational cells:**		8121
5	**Number of sequential cells:**		1650
6	**Number of macros/black boxes:**		0
7	**Number of buf/inv:**		751
8	**Number of references:**		42
9	**Combinational area:**	21518.880665	
10	**Buf/Inv area:**	977.183687	
11	**Noncombinational area:**	10802.643208	
12	**Macro/Black Box area:**	0.000000	
13	**Net Interconnect area:**	12629.902996	
	Total cell area:	**32321.525872**	
	Total area:	**44951.428869**	

Report-power-1 (Compile Ultra)

S.No	Design	Wire Load Model	Library
1	**picorv32a**	35000	saed32rvt_tt0p78vm40c
2	**picorv32_pcpi_fast_mul**	16000	saed32rvt_tt0p78vm40c

Report-power-2 (compile ultra)

S.No	Power Group	Internal Power	Switching Power	Total Power	Leakage Power	Percentage	Attributes
1	**io_pad**	0.0000	0.0000	0.0000	0.0000	0.00%	
2	**memory**	0.0000	0.0000	0.0000	0.0000	0.00%	
3	**black_box**	0.0000	0.0000	0.0000	0.0000	0.00%	
4	**clock_network**	961.9947	0.0000	0.0000	961.9947	82.83%	i
5	**register**	3.4721	0.9064	2.2303E+08	227.4086	3.36%	
6	**sequential**	0.4688	8.3301E-02	9.8156E+06	10.3677	0.17%	
7	**combinational**	5.4148	4.2287	6.3192E+08	642.5816	3.63%	
	Total (uW)	**972.3504**	**5.2184**	**8.6477e+08 pW**	**1.0423E+03**		
			Total Dynamic Power	**977.5688**			

Report hierarchy (compile_ultra)

picorv32a	r
AND2X1_RVT	saed32rvt_tt0p78vm40c
AND3X1_RVT	saed32rvt_tt0p78vm40c
AND4X1_RVT	saed32rvt_tt0p78vm40c
AO21X1_RVT	saed32rvt_tt0p78vm40c
AO22X1_RVT	saed32rvt_tt0p78vm40c
AO221X1_RVT	saed32rvt_tt0p78vm40c
AO222X1_RVT	saed32rvt_tt0p78vm40c
AOI21X1_RVT	saed32rvt_tt0p78vm40c
AOI22X1_RVT	saed32rvt_tt0p78vm40c
AOI222X1_RVT	saed32rvt_tt0p78vm40c
DFFSSRX1_RVT	saed32rvt_tt0p78vm40c
DFFX1_RVT	saed32rvt_tt0p78vm40c
FADD1_RVT	saed32rvt_tt0p78vm40c
HADD1_RVT	saed32rvt_tt0p78vm40c
INV0Z_RVT	saed32rvt_tt0p78vm40c
INVX1_RVT	saed32rvt_tt0p78vm40c
LATCHX1_RVT	saed32rvt_tt0p78vm40c
MUX21X1_RVT	saed32rvt_tt0p78vm40c
NAND2X0_RVT	saed32rvt_tt0p78vm40c
NAND3X0_RVT	saed32rvt_tt0p78vm40c
NAND4X0_RVT	saed32rvt_tt0p78vm40c
NBUFFX2_RVT	saed32rvt_tt0p78vm40c
NOR2X0_RVT	saed32rvt_tt0p78vm40c
NOR3X0_RVT	saed32rvt_tt0p78vm40c
NOR4X1_RVT	saed32rvt_tt0p78vm40c
OA21X1_RVT	saed32rvt_tt0p78vm40c
OA22X1_RVT	saed32rvt_tt0p78vm40c
OA221X1_RVT	saed32rvt_tt0p78vm40c
OA222X1_RVT	saed32rvt_tt0p78vm40c
OAI21X1_RVT	saed32rvt_tt0p78vm40c
OAI22X1_RVT	saed32rvt_tt0p78vm40c
OAI221X1_RVT	saed32rvt_tt0p78vm40c
OAI222X1_RVT	saed32rvt_tt0p78vm40c
ORDX1_RVT	saed32rvt_tt0p78vm40c
ORX1_RVT	saed32rvt_tt0p78vm40c
ORX2_RVT	saed32rvt_tt0p78vm40c
ORAI1_RVT	saed32rvt_tt0p78vm40c
XNOR2X1_RVT	saed32rvt_tt0p78vm40c
XNOR3X1_RVT	saed32rvt_tt0p78vm40c
XOR2X1_RVT	saed32rvt_tt0p78vm40c
XOR3X1_RVT	saed32rvt_tt0p78vm40c
picorv32_pcpi_fast_mul	saed32rvt_tt0p78vm40c
AND2X1_RVT	saed32rvt_tt0p78vm40c
AND3X1_RVT	saed32rvt_tt0p78vm40c
AO21X1_RVT	saed32rvt_tt0p78vm40c
AO22X1_RVT	saed32rvt_tt0p78vm40c
AO222X1_RVT	saed32rvt_tt0p78vm40c
DFFX1_RVT	saed32rvt_tt0p78vm40c
FADD1_RVT	saed32rvt_tt0p78vm40c
HADD1_RVT	saed32rvt_tt0p78vm40c
INVX0_RVT	saed32rvt_tt0p78vm40c
INVX1_RVT	saed32rvt_tt0p78vm40c
NAND2X0_RVT	saed32rvt_tt0p78vm40c
NAND3X0_RVT	saed32rvt_tt0p78vm40c
NAND4X0_RVT	saed32rvt_tt0p78vm40c
NOR2X0_RVT	saed32rvt_tt0p78vm40c
NOR4X1_RVT	saed32rvt_tt0p78vm40c
OA21X1_RVT	saed32rvt_tt0p78vm40c
OA21X1_RVT	saed32rvt_tt0p78vm40c
ORX1_RVT	saed32rvt_tt0p78vm40c
XNORX1_RVT	saed32rvt_tt0p78vm40c
XORX1_RVT	saed32rvt_tt0p78vm40c

hierarchy (compile_ultra)

Attributes:
r - licensed design

Cell Internal Power = 972.3518 uW (99%)
Net Switching Power = 5.2183 uW (1%)

Total Dynamic Power = 977.5701 uW (100%)

Cell Leakage Power = 864.7657 uW

Report_timing - 1 (Compile ultra)

S.No	
1	**Startpoint:** latched_branch_reg (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:** reg_next_pc_reg[31] (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:** Clk
4	**Path Type:** max

Report_timing-2 (Compile ultra)

Des/Clust/Port	Wire Load Model	Library
picorv32a	**35000**	**saed32rvt_tt0p78vm40c**

Report_timing -3 (Compile ultra)

S.No	Point	Incr	Path
1	**clock clk (rise edge)**	0.00	0.00
2	**clock network delay (ideal)**	1.00	1.00
3	**latched_branch_reg/CLK (DFFX1_RVT)**	0.00 #	1.00 r
4	**latched_branch_reg/Q (DFFX1_RVT)**	0.39	1.39 f
5	**U464/Y (OR2X1_RVT)**	0.23	1.63 f
6	**U5290/Y (OR2X1_RVT)**	0.17	1.79 f
7	**U5291/Y (INVX1_RVT)**	0.19	1.99 r
8	**U5292/Y (OR2X1_RVT)**	0.15	2.13 r
9	**U5313/Y (INVX1_RVT)**	0.08	2.21 f
10	**U5343/Y (AND2X1_RVT)**	0.11	2.33 f
11	**U5345/Y (OR2X1_RVT)**	0.10	2.43 f
12	**U5376/Y (NOR2X0_RVT)**	0.13	2.55 r
13	**U5384/Y (OA21X1_RVT)**	0.15	2.71 f
14	**U5399/Y (AO21X1_RVT)**	0.15	2.86 r
15	**U5406/Y (AO21X1_RVT)**	0.15	3.01 f
16	**U4140/Y (AO22X1_RVT)**	0.12	3.13 f
17	**U7478/CO (FADD1_RVT)**	0.14	3.27 f
18	**U7377/CO (FADD1_RVT)**	0.15	3.42 f
19	**U7373/CO (FADD1_RVT)**	0.15	3.57 f
20	**U7371/CO (FADD1_RVT)**	0.15	3.72 f
21	**U7369/CO (FADD1_RVT)**	0.15	3.87 f
22	**U7367/CO (FADD1_RVT)**	0.15	4.02 f
23	**U7365/CO (FADD1_RVT)**	0.15	4.17 f
24	**U7363/CO (FADD1_RVT)**	0.15	4.32 f
25	**U7361/CO (FADD1_RVT)**	0.15	4.48 f
26	**U7359/CO (FADD1_RVT)**	0.15	4.63 f
27	**U7357/CO (FADD1_RVT)**	0.15	4.78 f
28	**U7345/CO (FADD1_RVT)**	0.15	4.94 f
29	**U7343/CO (FADD1_RVT)**	0.15	5.09 f
30	**U7355/CO (FADD1_RVT)**	0.15	5.25 f
31	**U7353/CO (FADD1_RVT)**	0.15	5.40 f
32	**U7351/CO (FADD1_RVT)**	0.15	5.55 f
33	**U7341/Y (XOR2X1_RVT)**	0.16	5.71 r
34	**U7342/Y (AO222X1_RVT)**	0.12	5.83 r
35	**reg_next_pc_reg[31]/D (DFFX1_RVT)**	0.01	5.84 r
36	**data arrival time**		5.84
37	**clock clk (rise edge)**	6.00	6.00
38	**clock network delay (ideal)**	1.00	7.00
39	**clock uncertainty**	-1.00	6.00
40	**reg_next_pc_reg[31]/CLK (DFFX1_RVT)**	0.00	6.00 r
41	**library setup time**	-0.10	5.90
42	**data required time**		5.90
	data required time		5.90
	data arrival time		-5.84
	slack (MET)		**0.07**

Report_timing - 1 (Compile ultra)-1

S.No	
1	**Startpoint:** instr_blt_reg (rising edge-triggered flip-flop clocked by clk)
2	**Endpoint:** is_slti_blt_slt_reg (rising edge-triggered flip-flop clocked by clk)
3	**Path Group:** Clk
4	**Path Type:** Min

Report_timing-2 (Compile ultra)-1

Des/Clust/Port	Wire Load Model	Library
picorv32a	**35000**	**saed32rvt_tt0p78vm40c**

Report_timing -3 (Compile ultra)-1

S.No	Point	Incr	Path
1	**clock clk (rise edge)**	0.00	0.00
2	**clock network delay (ideal)**	0.00	0.00
3	**instr_blt_reg/CLK (DFFX1_RVT)**	0.00 #	0.00 r
4	**instr_blt_reg/QN (DFFX1_RVT)**	0.13	0.13 f
5	**is_slti_blt_slt_reg/RSTB (DFFSSRX1_RVT)**	0.01	0.14 f
6	**data arrival time**		0.14
7	**clock clk (rise edge)**	0.00	0.00
8	**clock network delay (ideal)**	0.00	0.00
9	**is_slti_blt_slt_reg/CLK (DFFSSRX1_RVT)**	0.00	0.00 r
10	**library hold time**	-0.06	-0.06
11	**data required time**		-0.06
	data required time		-0.06
	data arrival time		-0.14
	slack (MET)		**0.21**

Report-Wire load Model (Compile ultra)-1

Wire load model:		**35000**
Location	:	**Picorv32a (design)**
Resistance	:	**0.001187**
Capacitance	:	**0.00027**
Area	:	**0.01**
Slope	:	**140.36**

Report-Wire load Model (Compile ultra)-2

Wire load model:		
Location	:	**picorv32_pcpi_fast_mul (design)**
Resistance	:	
Capacitance	:	
Area	:	
Slope	:	

Report-Wire load Model -35000 (Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	16.92				
2	2	39.03				
3	3	64.09				
4	4	92.51				
5	5	124.73				
6	6	161.17				
7	7	202.25				
8	8	248.42				
9	9	300.09				
10	10	357.68				
11	11	421.63				
12	12	492.37				
13	13	570.31				
14	14	655.89				
15	15	749.54				
16	16	851.67				
17	17	962.72				
18	18	1083.11				
19	19	1213.28				
20	20	1353.84				
	Total Length	**9961.05**				

Report-Wire load Model - 16000(Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.00				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8130.84**				

Report- Threshold Voltage Group - (compile ultra)

S.No	Vth Group Name ->	saed32rvt_ss1
1	**All Cells**	9771 (100.00%)
2	**Blackbox Cells**	0 (0.00%)
3	**Blackbox cells**	9771 (100.00%)
4	**Blackbox Area**	32321.53 (100.00%)
5	**Blackbox Cells area**	0 (0.00%)
6	**Non-Blackbox cells area**	32321.53 (100.00%)
7	**All Cells leakage**	864.766JW (100.00%)
8	**Blackbox Cells leakage**	0 (0.00%)
9	**Non-Blackbox cells leakage**	864.766JW (100.00%)

Global Skew Report(Compile ultra)

S.No		
1	**Clock Tree Name** :	"clk"
2	**Clock Period** :	6.00000
3	**Clock Tree root pin** :	"clk"
4	**Number of Levels** :	1
5	**Number of Sinks** :	1582
6	**Number of CT Buffers** :	0
7	**Number of CTS added gates** :	0
8	**Number of Preexisting Gates** :	0
9	**Number of Preexisting Buf/Inv** :	0
10	**Total Number of Clock Cells** :	0
11	**Total Area of CT Buffers** :	0.00000
12	**Total Area of CT cells** :	0.00000
13	**Max Global Skew** :	0.00031
14	**Number of MaxTran Violators** :	0
15	**Number of MaxCap Violators** :	1
16	**Number of MaxFanout Violators** :	0
1	**Operating Condition**	worst
2	**Clock global Skew**	0.000
3	**Longest path delay**	0.109
4	**Shortest path delay**	0.109

The longest path delay end pin: is_slti_blt_slt_reg/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rd_reg[63]/CLK

Clock_tree Longest Path (Compile ultra)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri
1	**clk**	0	1	0	0	0 r
2	**clk**	1001037.500	1582	0	0	0 r
3	**is_slti_blt_slt_reg/CLK**	1001037.500	0	0	0.109	0.109 r
	Clock Delay					0.109

Clock_tree Shortest Path (Compile ultra)

S.No	Pin	Cap	Fanout	Trans	Incr	Arri
1	**clk**	0	1	0	0	0 r
2	**clk**	1001037.500	1582	0	0	0 r
3	**genblk1.pcpi_mul/rd_reg[63]/CLK**	1001037.500	0	0	0.109	0.109 r
	Clock Delay					0.109

Report-qor (Compile ultra)

S.No		
	Timing Path Group (none)	
1	Levels of Logic:	30.00
2	Critical Path Length:	4.84
3	Critical Path Slack:	0.07
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	0.00
6	No. of Violating Paths:	0.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	1
11	Hierarchical Port Count:	134
12	Leaf Cell Count:	9771
13	Buf/Inv Cell Count:	751
14	Buf Cell Count:	30
15	Inv Cell Count:	721
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	8121
18	Sequential Cell Count:	1650
19	Macro Count:	0
	Area	
20	Combinational Area:	21518.880665
21	Noncombinational Area:	10802.643208
22	Buf/Inv Area:	977.183687
23	Total Buffer Area:	60.99
24	Total Inverter Area:	916.19
25	Macro/Black Box Area:	0.000000
26	Net Area:	12629.902996
	Cell Area:	**32321.525872**
	Design Area:	**44951.428869**
	Design Rules	
	Total Number of Nets:	10789
	Nets With Violations:	0
	Max Trans Violations:	0
	Max Cap Violations:	0

Report_cell (compile)

S.No	Reference	Cell Count	Library	Unit Area	Area	Attributes
1	AND2X1_RVT	244	saed32rvt_tt0p78vn40c	2.033152	496.089113	
2	AND3X1_RVT	32	saed32rvt_tt0p78vn40c	2.287296	73.193474	
3	AND4X1_RVT	21	saed32rvt_tt0p78vn40c	2.541440	53.370240	
4	AO21X1_RVT	102	saed32rvt_tt0p78vn40c	2.541440	259.226881	
5	AO221X1_RVT	236	saed32rvt_tt0p78vn40c	3.049728	719.735788	
6	AO222X1_RVT	207	saed32rvt_tt0p78vn40c	3.303872	683.901526	
7	AO22X1_RVT	1111	saed32rvt_tt0p78vn40c	2.541440	2823.539851	
8	AOI21X1_RVT	6	saed32rvt_tt0p78vn40c	3.049728	18.298368	
9	AOI221X1_RVT	23	saed32rvt_tt0p78vn40c	3.558016	81.834369	
10	AOI222X1_RVT	22	saed32rvt_tt0p78vn40c	3.812160	83.867520	
11	AOI22X1_RVT	1	saed32rvt_tt0p78vn40c	3.049728	3.049728	
12	DELLN3X2_RVT	2	saed32rvt_tt0p78vn40c	9.657472	19.314943	
13	DFFSSRX1_RVT	7	saed32rvt_tt0p78vn40c	7.116032	49.812225	n
14	DFFX1_RVT	1459	saed32rvt_tt0p78vn40c	6.607744	9640.698812	n
15	INVX0_RVT	88	saed32rvt_tt0p78vn40c	1.270720	111.823360	
16	INVX1_RVT	471	saed32rvt_tt0p78vn40c	1.270720	598.509122	
17	LATCHX1_RVT	68	saed32rvt_tt0p78vn40c	5.082880	345.635841	n
18	MUX21X1_RVT	298	saed32rvt_tt0p78vn40c	3.303872	984.553888	
19	NAND2X0_RVT	158	saed32rvt_tt0p78vn40c	1.524864	240.928505	
20	NAND3X0_RVT	75	saed32rvt_tt0p78vn40c	1.779008	133.425602	
21	NAND4X0_RVT	125	saed32rvt_tt0p78vn40c	2.033152	254.144013	
22	NBUFFX2_RVT	17	saed32rvt_tt0p78vn40c	2.033152	34.563586	
23	NOR2X0_RVT	7	saed32rvt_tt0p78vn40c	2.541440	17.790080	
24	NOR3X0_RVT	6	saed32rvt_tt0p78vn40c	2.795584	16.773504	
25	NOR4X1_RVT	15	saed32rvt_tt0p78vn40c	3.049728	45.745919	
26	OA21X1_RVT	14	saed32rvt_tt0p78vn40c	2.541440	35.580160	
27	OA221X1_RVT	173	saed32rvt_tt0p78vn40c	3.049728	527.602930	
28	OA222X1_RVT	138	saed32rvt_tt0p78vn40c	3.303872	455.934351	
29	OA22X1_RVT	65	saed32rvt_tt0p78vn40c	2.541440	165.193601	
30	OAI21X1_RVT	38	saed32rvt_tt0p78vn40c	3.049728	115.889661	
31	OAI221X1_RVT	3	saed32rvt_tt0p78vn40c	3.558016	10.674048	
32	OAI222X1_RVT	8	saed32rvt_tt0p78vn40c	3.812160	30.497280	
33	OAI22X1_RVT	15	saed32rvt_tt0p78vn40c	3.049728	45.745919	
34	OR2X1_RVT	17	saed32rvt_tt0p78vn40c	2.033152	34.563586	
35	OR3X1_RVT	6	saed32rvt_tt0p78vn40c	2.541440	15.248640	
36	OR4X1_RVT	8	saed32rvt_tt0p78vn40c	3.558016	28.464128	
37	picorv32_pcpi_fast_mul	1		9395.449458	9395.449458	h, n
38	picorv32a_DW_cmp_0	1		241.436800	241.436800	h
39	picorv32a_DW01_add_0	1		195.690874	195.690874	h
40	picorv32a_DW01_add_2	1		183.491969	183.491969	h
41	picorv32a_DW01_add_3	1		220.088705	220.088705	h
42	picorv32a_DW01_add_4	1		199.757178	199.757178	h
43	picorv32a_DW01_add_5	1		181.712954	181.712954	h
44	picorv32a_DW01_add_6	1		188.574849	188.574849	h
45	picorv32a_DW01_add_J5_0	1		298.365051	298.365051	h
46	picorv32a_DW01_cmp6_0	1		199.248897	199.248897	h
47	picorv32a_DW01_dec_0_DW01_dec_1	1		181.458819	181.458819	h
48	picorv32a_DW01_inc_J2_0	1		426.453630	426.453630	h
49	picorv32a_DW01_inc_J3_0	1		422.895614	422.895614	h
50	picorv32a_DW01_sub_0	1		202.044475	202.044475	h
51	XNOR2X1_RVT	2	saed32rvt_tt0p78vn40c	4.320448	8.640896	
	Total Cells = 9460	5302			31800.530731	

Report-cell (compile_ultra)

S.No	Reference	Cell Count	Library	Unit Area	Total Area	Attributes
1	AND2X1_RVT	517	saed32rvt_tt0p78vn40c	2.033152	1051.139637	
2	AND3X1_RVT	65	saed32rvt_tt0p78vn40c	2.287296	148.674244	
3	AND4X1_RVT	22	saed32rvt_tt0p78vn40c	2.541440	55.911680	
4	AO21X1_RVT	130	saed32rvt_tt0p78vn40c	2.541440	330.387201	
5	AO22X1_RVT	1458	saed32rvt_tt0p78vn40c	2.541440	3705.419535	
6	AO221X1_RVT	18	saed32rvt_tt0p78vn40c	3.049728	54.895103	
7	AO222X1_RVT	70	saed32rvt_tt0p78vn40c	3.303872	231.271048	
8	AOI21X1_RVT	89	saed32rvt_tt0p78vn40c	3.049728	271.425785	
9	AOI22X1_RVT	157	saed32rvt_tt0p78vn40c	3.049728	478.807283	
10	AOI222X1_RVT	12	saed32rvt_tt0p78vn40c	3.812160	45.745920	
11	DFFSSRX1_RVT	7	saed32rvt_tt0p78vn40c	7.116032	49.812225	n
12	DFFX1_RVT	1442	saed32rvt_tt0p78vn40c	6.607744	9528.367161	n
13	FADDX1_RVT	58	saed32rvt_tt0p78vn40c	4.828736	280.066678	r
14	HADDX1_RVT	48	saed32rvt_tt0p78vn40c	3.303872	158.585861	r
15	INVX0_RVT	263	saed32rvt_tt0p78vn40c	1.270720	334.199361	
16	INVX1_RVT	177	saed32rvt_tt0p78vn40c	1.270720	224.917441	
17	LATCHX1_RVT	68	saed32rvt_tt0p78vn40c	5.082880	345.635841	n
18	MUX21X1_RVT	11	saed32rvt_tt0p78vn40c	3.303872	36.342593	
19	NAND2X0_RVT	588	saed32rvt_tt0p78vn40c	1.524864	896.620008	
20	NAND3X0_RVT	168	saed32rvt_tt0p78vn40c	1.779008	298.873349	
21	NAND4X0_RVT	63	saed32rvt_tt0p78vn40c	2.033152	128.088583	
22	NBUFFX2_RVT	30	saed32rvt_tt0p78vn40c	2.033152	60.994563	
23	NOR2X0_RVT	260	saed32rvt_tt0p78vn40c	2.541440	660.774403	
24	NOR3X0_RVT	14	saed32rvt_tt0p78vn40c	2.795584	39.138175	
25	NOR4X1_RVT	101	saed32rvt_tt0p78vn40c	3.049728	308.022520	
26	OA21X1_RVT	78	saed32rvt_tt0p78vn40c	2.541440	198.232321	
27	OA22X1_RVT	80	saed32rvt_tt0p78vn40c	2.541440	203.315201	
28	OA221X1_RVT	11	saed32rvt_tt0p78vn40c	3.049728	33.547007	
29	OA222X1_RVT	6	saed32rvt_tt0p78vn40c	3.303872	19.823233	
30	OAI21X1_RVT	148	saed32rvt_tt0p78vn40c	3.049728	451.359732	
31	OAI22X1_RVT	114	saed32rvt_tt0p78vn40c	3.049728	347.668983	
32	OAI221X1_RVT	3	saed32rvt_tt0p78vn40c	3.558016	10.674048	
33	OAI222X1_RVT	1	saed32rvt_tt0p78vn40c	3.812160	3.812160	
34	OR2X1_RVT	262	saed32rvt_tt0p78vn40c	2.033152	532.685851	
35	OR3X1_RVT	50	saed32rvt_tt0p78vn40c	2.541440	127.072001	
36	OR3X2_RVT	28	saed32rvt_tt0p78vn40c	2.541440	71.160320	
37	OR4X1_RVT	19	saed32rvt_tt0p78vn40c	3.558016	67.602305	
38	XNOR2X1_RVT	92	saed32rvt_tt0p78vn40c	4.320448	397.481209	
39	XNOR3X1_RVT	6	saed32rvt_tt0p78vn40c	6.099456	36.596735	
40	XOR2X1_RVT	89	saed32rvt_tt0p78vn40c	4.320448	384.519865	
41	XOR3X1_RVT	3	saed32rvt_tt0p78vn40c	7.116032	21.348096	
42	picorv32_pcpi_fast_mul	1	saed32rvt_tt0p78vn40c	9690.510610	9690.510610	h, n
	TOTAL = 9780	6827		9824.698642	32321.525875	

Report_Area (compile)

S.No	Number of	Count	Area
1	Number of ports:	1919	
2	Number of nets:	12367	
3	Number of cells:	9460	
4	Number of combinational cells:	7713	
5	Number of sequential cells:	1667	
6	Number of macros/black boxes:	0	
7	Number of buf/inv:	1351	
8	Number of references:	51	
9	Combinational area:		20885.553873
10	Buf/Inv area:		1764.267653
11	Noncombinational area:		10914.976860
12	Macro/Black Box area:		0.000000
13	Net Interconnect area:		9298.772721
	Total Cell Area		31800.530733
	Total Area		41099.303454

Report-area (Compile Ultra)

S.No		Area	Count
1	Number of ports:		543
2	Number of nets:		10906
3	Number of cells:		9780
4	Number of combinational cells:		8121
5	Number of sequential cells:		1650
6	Number of macros/black boxes:		0
7	Number of buf/inv:		751
8	Number of references:		42
9	Combinational area:	21518.880665	
10	Buf/Inv area:	977.183687	
11	Noncombinational area:	10802.645208	
12	Macro/Black Box area:	0.000000	
13	Net Interconnect area:	12629.902996	
	Total cell area:	32321.525872	
	Total area:	44951.428869	

Report_timing - 1 (Compile)		
S.No		
1	Startpoint:	decoded_imm_reg[0] (rising edge-triggered flip-flop clocked by clk)
2	Endpoint:	reg_out_reg[31] (rising edge-triggered flip-flop clocked by clk)
3	Path Group:	Clk
4	Path Type:	max

Report_timing-2 (Compile)		
Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c
picorv32a_DW01_add_0	ForQA	saed32rvt_tt0p78vn40c

report_timing(Compile)				
S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	1.00	1.00	
3	decoded_imm_reg[0]/CLK (DFFX1_RVT)	0.00 #	1.00	r
4	decoded_imm_reg[0]/Q (DFFX1_RVT)	0.30	1.30	f
5	add_1784/B[0] (picorv32a_DW01_add_0)	0.00	1.30	f
6	add_1784/U8/Y (AND2X1_RVT)	0.08	1.39	f
7	add_1784/U11/Y (NAND2X0_RVT)	0.06	1.45	r
8	add_1784/U12/Y (NAND3X0_RVT)	0.09	1.54	f
9	add_1784/L1(2)/U1/CO (FADDX1_RVT)	0.17	1.70	f
10	add_1784/L1(3)/U1/CO (FADDX1_RVT)	0.15	1.86	f
11	add_1784/L1(4)/U1/CO (FADDX1_RVT)	0.15	2.01	f
12	add_1784/L1(5)/U1/CO (FADDX1_RVT)	0.15	2.16	f
13	add_1784/L1(6)/U1/CO (FADDX1_RVT)	0.15	2.31	f
14	add_1784/L1(7)/U1/CO (FADDX1_RVT)	0.15	2.47	f
15	add_1784/L1(8)/U1/CO (FADDX1_RVT)	0.15	2.62	f
16	add_1784/L1(9)/U1/CO (FADDX1_RVT)	0.15	2.77	f
17	add_1784/L1(10)/U1/CO (FADDX1_RVT)	0.15	2.92	f
18	add_1784/L1(11)/U1/CO (FADDX1_RVT)	0.15	3.07	f
19	add_1784/L1(12)/U1/CO (FADDX1_RVT)	0.15	3.23	f
20	add_1784/L1(13)/U1/CO (FADDX1_RVT)	0.15	3.38	f
21	add_1784/L1(14)/U1/CO (FADDX1_RVT)	0.15	3.53	f
22	add_1784/L1(15)/U1/CO (FADDX1_RVT)	0.15	3.68	f
23	add_1784/L1(16)/U1/CO (FADDX1_RVT)	0.15	3.83	f
24	add_1784/L1(17)/U1/CO (FADDX1_RVT)	0.15	3.99	f
25	add_1784/L1(18)/U1/CO (FADDX1_RVT)	0.15	4.14	f
26	add_1784/L1(19)/U1/CO (FADDX1_RVT)	0.15	4.29	f
27	add_1784/L1(20)/U1/CO (FADDX1_RVT)	0.15	4.44	f
28	add_1784/L1(21)/U1/CO (FADDX1_RVT)	0.15	4.60	f
29	add_1784/L1(22)/U1/CO (FADDX1_RVT)	0.15	4.75	f
30	add_1784/L1(23)/U1/CO (FADDX1_RVT)	0.15	4.90	f
31	add_1784/L1(24)/U1/CO (FADDX1_RVT)	0.15	5.05	f
32	add_1784/L1(25)/U1/CO (FADDX1_RVT)	0.15	5.20	f
33	add_1784/L1(26)/U1/CO (FADDX1_RVT)	0.15	5.36	f
34	add_1784/L1(27)/U1/CO (FADDX1_RVT)	0.15	5.51	f
35	add_1784/L1(28)/U1/CO (FADDX1_RVT)	0.15	5.66	f
36	add_1784/L1(29)/U1/CO (FADDX1_RVT)	0.15	5.81	f
37	add_1784/L1(30)/U1/CO (FADDX1_RVT)	0.15	5.96	f
38	add_1784/L1(31)/U1/Y (XOR3X2_RVT)	0.12	6.08	r
39	add_1784/SUM[31] (picorv32a_DW01_add_0)	0.00	6.08	r
40	U4213/Y (NAND2X0_RVT)	0.05	6.13	f
41	U4214/Y (NAND3X0_RVT)	0.06	6.20	r
42	U4215/Y (OR2X1_RVT)	0.08	6.28	r
43	reg_out_reg[31]/D (DFFX1_RVT)	0.01	6.29	r
44	data arrival time		6.29	
	clock clk (rise edge)	6.00	6.00	
	clock network delay (ideal)	1.00	7.00	
	clock uncertainty	-1.00	6.00	
	reg_out_reg[31]/CLK (DFFX1_RVT)	0.00	6.00	r
	library setup time	-0.08	5.92	
	data required time		5.92	
	data required time		5.92	
	data arrival time		-6.29	
	slack (VIOLATED)		-0.36	

Report_timing - 1 (Compile)-1		
S.No		
1	Startpoint:	instr_blt_reg (rising edge-triggered flip-flop clocked by clk)
2	Endpoint:	is_slti_blt_slt_reg (rising edge-triggered flip-flop clocked by clk)
3	Path Group:	Clk
4	Path Type:	min

Report_timing-2 (Compile)-1		
Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c

report_timing(Compile)-1			
S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	0.00	0.00	
3	instr_blt_reg/CLK (DFFX1_RVT)	0.00 #	0.00	r
4	instr_blt_reg/QN (DFFX1_RVT)	0.13	0.13	f
5	U3050/Y (NAND3X0_RVT)	0.07	0.20	r
6	is_slti_blt_slt_reg/D (DFFX1_RVT)	0.01	0.21	r
7	data arrival time		0.21	
	clock clk (rise edge)	0.00	0.00	
	clock network delay (ideal)	0.00	0.00	
	is_slti_blt_slt_reg/CLK (DFFX1_RVT)	0.00	0.00	r
	library hold time	-0.04	-0.04	
	data required time		-0.04	
	data required time		-0.04	
	data arrival time		-0.21	
	Slack (MET)		0.25	

Report_timing - 1 (Compile ultra)		
S.No		
1	Startpoint:	latched_branch_reg (rising edge-triggered flip-flop clocked by clk)
2	Endpoint:	reg_next_pc_reg[31] (rising edge-triggered flip-flop clocked by clk)
3	Path Group:	Clk
4	Path Type:	max

Report_timing-2 (Compile ultra)		
Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c

Report_timing -3 (Compile ultra)				
S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	1.00	1.00	
3	latched_branch_reg/CLK (DFFX1_RVT)	0.00 #	1.00	r
4	latched_branch_reg/Q (DFFX1_RVT)	0.39	1.39	f
5	U4647/Y (OR2X1_RVT)	0.23	1.63	f
6	U5290/Y (OR2X1_RVT)	0.17	1.79	f
7	U5291/Y (INVX1_RVT)	0.19	1.99	r
8	U5292/Y (OR2X1_RVT)	0.15	2.13	r
9	U5313/Y (INVX1_RVT)	0.08	2.21	f
10	U5343/Y (AND2X1_RVT)	0.11	2.33	f
11	U5345/Y (OR2X1_RVT)	0.10	2.43	f
12	U5378/Y (NOR2X0_RVT)	0.13	2.55	r
13	U5384/Y (OAI21X1_RVT)	0.15	2.71	f
14	U5399/Y (AOI21X1_RVT)	0.15	2.86	r
15	U5406/Y (OAI21X1_RVT)	0.15	3.01	f
16	U4140/Y (AO21X1_RVT)	0.12	3.13	f
17	U7478/CO (FADDX1_RVT)	0.14	3.27	f
18	U7377/CO (FADDX1_RVT)	0.15	3.42	f
19	U7373/CO (FADDX1_RVT)	0.15	3.57	f
20	U7371/CO (FADDX1_RVT)	0.15	3.72	f
21	U7369/CO (FADDX1_RVT)	0.15	3.87	f
22	U7367/CO (FADDX1_RVT)	0.15	4.02	f
23	U7365/CO (FADDX1_RVT)	0.15	4.17	f
24	U7363/CO (FADDX1_RVT)	0.15	4.32	f
25	U7361/CO (FADDX1_RVT)	0.15	4.48	f
26	U7359/CO (FADDX1_RVT)	0.15	4.63	f
27	U7357/CO (FADDX1_RVT)	0.15	4.78	f
28	U7345/CO (FADDX1_RVT)	0.15	4.94	f
29	U7343/CO (FADDX1_RVT)	0.15	5.09	f
30	U7355/CO (FADDX1_RVT)	0.15	5.25	f
31	U7353/CO (FADDX1_RVT)	0.15	5.40	f
32	U7351/CO (FADDX1_RVT)	0.15	5.55	f
33	U7341/Y (XOR2X1_RVT)	0.16	5.71	r
34	U7342/Y (AO222X1_RVT)	0.12	5.83	r
35	reg_next_pc_reg[31]/D (DFFX1_RVT)	0.01	5.84	r
36	data arrival time		5.84	
37	clock clk (rise edge)	6.00	6.00	
38	clock network delay (ideal)	1.00	7.00	
39	clock uncertainty	-1.00	6.00	
40	reg_next_pc_reg[31]/CLK (DFFX1_RVT)	0.00	6.00	r
41	library setup time	-0.10	5.90	
42	data required time		5.90	
	data required time		5.90	
	data arrival time		-5.84	
	slack (MET)		0.07	

Report_timing - 1 (Compile ultra)-1		
S.No		
1	Startpoint:	instr_blt_reg (rising edge-triggered flip-flop clocked by clk)
2	Endpoint:	is_slti_blt_slt_reg (rising edge-triggered flip-flop clocked by clk)
3	Path Group:	Clk
4	Path Type:	min

Report_timing-2 (Compile ultra)-1		
Des/Clust/Port	Wire Load Model	Library
picorv32a	35000	saed32rvt_tt0p78vn40c

Report_timing -3 (Compile ultra)-1				
S.No	Point	Incr	Path	
1	clock clk (rise edge)	0.00	0.00	
2	clock network delay (ideal)	0.00	0.00	
3	instr_blt_reg/CLK (DFFX1_RVT)	0.00 #	0.00	r
4	instr_blt_reg/QN (DFFX1_RVT)	0.13	0.13	f
5	is_slti_blt_slt_reg/RSTB (DFFSSRX1_RVT)	0.01	0.14	f
6	data arrival time		0.14	
7	clock clk (rise edge)	0.00	0.00	
8	clock network delay (ideal)	0.00	0.00	
9	is_slti_blt_slt_reg/CLK (DFFSSRX1_RVT)	0.00	0.00	r
10	library hold time	-0.06	-0.06	
11	data required time		-0.06	
	data required time		-0.06	
	data arrival time		-0.14	
	slack (MET)		0.21	

Report_power-1 (compile)

S.No	Design	Wire Load Model	Library
1	**picorv32a**	35000	saed32rvt_tt0p78vn40c
2	**picorv32_pcpi_fast_mul**	16000	saed32rvt_tt0p78vn40c
3	**picorv32a_DW01_add_0**	ForQA	saed32rvt_tt0p78vn40c
4	**picorv32a_DW01_add_2**	ForQA	saed32rvt_tt0p78vn40c
5	**picorv32a_DW01_add_3**	8000	saed32rvt_tt0p78vn40c
6	**picorv32a_DW_cmp_0**	8000	saed32rvt_tt0p78vn40c
7	**picorv32a_DW01_add_4**	ForQA	saed32rvt_tt0p78vn40c
8	**picorv32a_DW01_sub_0**	ForQA	saed32rvt_tt0p78vn40c
9	**picorv32a_DW01_add_5**	ForQA	saed32rvt_tt0p78vn40c
10	**picorv32a_DW01_dec_0_DW01_dec_1**	ForQA	saed32rvt_tt0p78vn40c
11	**icorv32a_DW01_cmp6_0**	ForQA	saed32rvt_tt0p78vn40c
12	**picorv32a_DW01_add_6**	ForQA	saed32rvt_tt0p78vn40c
13	**picorv32_pcpi_fast_mul_DW_mult_tc_1**	16000	saed32rvt_tt0p78vn40c
14	**picorv32a_DW01_inc_J2_0**	8000	saed32rvt_tt0p78vn40c
15	**picorv32a_DW01_inc_J3_0**	8000	saed32rvt_tt0p78vn40c
16	**picorv32a_DW01_add_J5_0**	8000	saed32rvt_tt0p78vn40c

Cell Internal Power = 981.6295 uW (99%)
Net Switching Power = 5.5829 uW (1%)

Total Dynamic Power = 987.2123 uW (100%)
Cell Leakage Power = 834.4452 uW

Report-power-2 (compile)

S.No	Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
1	**io_pad**	0.0000	0.0000	0.0000	0.0000	0.00%	
2	**memory**	0.0000	0.0000	0.0000	0.0000	0.00%	
3	**black_box**	0.0000	0.0000	0.0000	0.0000	0.00%	
4	**clock_network**	972.2699	0.0000	0.0000	972.2699	53.37%	i
5	**register**	3.4109	0.9747	2.2543E+08	229.8086	12.62%	
6	**sequential**	0.4724	8.4505E-02	9.8156E+06	10.3725	0.57%	
7	**combinational**	5.4744	4.5237	5.992E+08	609.2015	33.44%	
	Total (uW)	**981.6275**	**5.5829**	**8.3445e+08 pW**	**1.8217e+03 uW**		
		Total Dynamic Power	**987.2104**				

Report_power-1 (Compile Ultra)

S.No	Design	Wire Load Model	Library
1	**picorv32a**	35000	saed32rvt_tt0p78vn40c
2	**picorv32_pcpi_fast_mul**	16000	saed32rvt_tt0p78vn40c

Cell Internal Power = 972.3518 uW (99%)
Net Switching Power = 5.2183 uW (1%)

Total Dynamic Power = 977.5701 uW (100%)
Cell Leakage Power = 864.7657 uW

Report-power-2 (compile ultra)

S.No	Power Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage	Attributes
1	**io_pad**	0.0000	0.0000	0.0000	0.0000	0.00%)	
2	**memory**	0.0000	0.0000	0.0000	0.0000	0.00%)	
3	**black_box**	0.0000	0.0000	0.0000	0.0000	0.00%)	
4	**clock_network**	961.9947	0.0000	0.0000	961.9947	92.83%)	I
5	**register**	3.4721	0.9064	2.2303E+08	227.4086	3.36%)	
6	**sequential**	0.4688	8.3301E-02	9.8156E+06	10.3677	0.17%)	
7	**combinational**	6.4148	4.2287	6.3192E+08	642.5616	3.63%)	
	Total (uW)	**972.3504**	**5.2184**	**8.6477e+08 pW**	**1.8423E+03**		
		Total Dynamic Power	**977.5688**				

Report-wireload model (Compile)	
Wire load model	**35000**
Location	**Picorv32a (design)**
Resistance	**0.00118**
Capacitance	**0.00027**
Area	**0.01**
Slope	**140.36**

Report-Wire load Model -2 (Compile)	
Wire load model:	**16000**
Location :	**picorv32_pcpi_fast_mul(design)**
Resistance :	**0.001282**
Capacitance :	**0.000569**
Area :	**0.01**
Slope :	**108.438**

Report-Wire load Model -3 (Compile)	
Wire load model:	**ForQA**
Location :	**picorv32a_DW01_add_0 (design)**
Resistance :	**0.002067**
Capacitance :	**0.026724**
Area :	**0.01**
Slope :	**30.2854**

Report-Wire load Model -4 (Compile)	
Wire load model:	**8000**
Location :	**picorv32a_DW01_add_3 (design)**
Resistance :	**0.0015727**
Capacitance :	**0.000312**
Area :	**0.01**
Slope :	**90.6464**

Report-Wire load Model (Compile ultra)-1	
Wire load model:	**35000**
Location :	**Picorv32a (design)**
Resistance :	**0.001187**
Capacitance :	**0.00027**
Area :	**0.01**
Slope :	**140.36**

Report-Wire load Model (Compile ultra)-2	
Wire load model:	**16000**
Location :	**picorv32_pcpi_fast_mul (design)**
Resistance :	**0.001282**
Capacitance :	**0.000569**
Area :	**0.01**
Slope :	**108.438**

Report-Wire load Model 35000 (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	16.92				
2	2	39.03				
3	3	64.09				
4	4	92.51				
5	5	124.73				
6	6	161.17				
7	7	202.25				
8	8	248.42				
9	9	300.09				
10	10	357.68				
11	11	421.63				
12	12	492.37				
13	13	570.31				
14	14	655.89				
15	15	749.54				
16	16	851.67				
17	17	962.72				
18	18	1083.11				
19	19	1213.28				
20	20	1353.64				
	Total Length	**9961.05**				

Report-Wire load Model -16000 (Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8138.84**				

Report-Wire load Model -FORQA(Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	8.28				
2	2	18.49				
3	3	29.35				
4	4	40.92				
5	5	53.23				
6	6	66.36				
7	7	80.36				
8	8	95.27				
9	9	111.17				
10	10	128.09				
11	11	146.10				
12	12	165.26				
13	13	185.61				
14	14	207.22				
15	15	230.13				
16	16	254.41				
17	17	280.11				
18	18	307.28				
19	19	335.98				
20	20	366.27				
	Total Length	**3109.89**				

Report-Wire load Model - 8000(Compile)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	13.94				
2	2	31.80				
3	3	51.61				
4	4	73.61				
5	5	98.05				
6	6	125.17				
7	7	155.23				
8	8	188.46				
9	9	225.12				
10	10	265.45				
11	11	309.71				
12	12	358.13				
13	13	410.96				
14	14	468.46				
15	15	530.86				
16	16	598.42				
17	17	671.38				
18	18	749.98				
19	19	834.49				
20	20	925.13				
	Total Length	**7085.96**				

Report-Wire load Model -35000 (Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	16.92				
2	2	39.03				
3	3	64.09				
4	4	92.51				
5	5	124.73				
6	6	161.17				
7	7	202.25				
8	8	248.42				
9	9	300.09				
10	10	357.68				
11	11	421.63				
12	12	492.37				
13	13	570.31				
14	14	655.89				
15	15	749.54				
16	16	851.67				
17	17	962.72				
18	18	1083.11				
19	19	1213.28				
20	20	1353.64				
	Total Length	**9961.05**				

Report-Wire load Model - 16000(Compile ultra)

S.No	Fanout	Lengths	Points	Average cap	Standard Deviation	%SD
1	1	15.10				
2	2	34.61				
3	3	56.42				
4	4	80.84				
5	5	108.20				
6	6	138.79				
7	7	172.92				
8	8	210.91				
9	9	253.07				
10	10	299.71				
11	11	351.13				
12	12	407.64				
13	13	469.57				
14	14	537.20				
15	15	610.87				
16	16	690.86				
17	17	777.51				
18	18	871.11				
19	19	971.97				
20	20	1080.41				
	Total Length	**8138.84**				

Report-qor (Compile)		
S.No	**Timing Path Group (clk)**	
1	Levels of Logic:	36.00
2	Critical Path Length:	5.29
3	Critical Path Slack:	-0.36
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	-2.43
6	No. of Violating Paths:	10.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	15
11	Hierarchical Port Count:	1510
12	Leaf Cell Count:	9380
13	Buf/Inv Cell Count:	1315
14	Buf Cell Count:	29
15	Inv Cell Count:	1286
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	7713
18	Sequential Cell Count:	1667
	Area	
19	Combinational Area:	20885.553873
20	Noncombinational Area:	10914.976860
21	Buf/Inv Area:	1764.267653
22	Total Buffer Area:	127.58
23	Total Inverter Area:	1636.69
24	Macro/Black Box Area:	0.000000
25	Net Area:	9298.772721
26	**Cell Area:**	**31800.530733**
27	**Design Area:**	**41099.303454**
	Design Rules	
28	Total Number of Nets:	10994
29	Nets With Violations:	0
30	Max Trans Violations:	0
31	Max Cap Violations:	0

Report-qor (Compile ultra)		
S.No	**Timing Path Group (none)**	
1	Levels of Logic:	30.00
2	Critical Path Length:	4.84
3	Critical Path Slack:	0.07
4	Critical Path Clk Period:	6.00
5	Total Negative Slack:	0.00
6	No. of Violating Paths:	0.00
7	Worst Hold Violation:	0.00
8	Total Hold Violation:	0.00
9	No. of Hold Violations:	0.00
	Cell Count	
10	Hierarchical Cell Count:	1
11	Hierarchical Port Count:	134
12	Leaf Cell Count:	9771
13	Buf/Inv Cell Count:	751
14	Buf Cell Count:	30
15	Inv Cell Count:	721
16	CT Buf/Inv Cell Count:	0
17	Combinational Cell Count:	8121
18	Sequential Cell Count:	1650
19	Macro Count:	0
	Area	
20	Combinational Area:	21518.880665
21	Noncombinational Area:	10802.645208
22	Buf/Inv Area:	977.183687
23	Total Buffer Area:	60.99
24	Total Inverter Area:	916.19
25	Macro/Black Box Area:	0.000000
26	Net Area:	12629.902996
	Cell Area:	**32321.525872**
	Design Area:	**44951.428869**
	Design Rules	
	Total Number of Nets:	10789
	Nets With Violations:	0
	Max Trans Violations:	0
	Max Cap Violations:	0

Report_clock_tree Global Skew Report		
S.No		
1	Clock Tree Name :	"clk"
2	Clock Period :	6.00000
3	Clock Tree root pin :	"clk"
4	Number of Levels :	1
5	Number of Sinks :	1599
6	Number of CT Buffers :	0
7	Number of CTS added gates :	0
8	Number of Preexisting Gates :	0
9	Number of Preexisting Buf/Inv :	0
10	Total Number of Clock Cells :	0
11	Total Area of CT Buffers :	0.00000
12	Total Area of CT cells :	0.00000
13	Max Global Skew :	0.00031
14	Number of MaxTran Violators :	0
15	Number of MaxCap Violators :	1
16	Number of MaxFanout Violators :	0
1	Operating Condition	worst
2	Clock global Skew	0.000
3	Longest path delay	0.109
4	Shortest path delay	0.109

The longest path delay end pin: count_cycle_reg[57]/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rs1_reg[5]/CLK

Clock_tree Longest Path							
S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0.000	1	0.000	0.000	0.000	r
2	clk	1001037.500	1599	0.000	0.000	0.000	r
3	count_cycle_reg[57]/CLK	1001037.500	0	0.000	0.109	0.109	r
	Clock Delay					0.109	

Clock_tree Shortest Path							
S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1599	0	0	0	r
3	genblk1.pcpi_mul/rs1_reg[5]/CLK	1001037.500	0	0	0.109	0.109	r
	Clock Delay					0.109	

Global Skew Report(Compile ultra)		
S.No		
1	Clock Tree Name :	"clk"
2	Clock Period :	6.00000
3	Clock Tree root pin :	"clk"
4	Number of Levels :	1
5	Number of Sinks :	1582
6	Number of CT Buffers :	0
7	Number of CTS added gates :	0
8	Number of Preexisting Gates :	0
9	Number of Preexisting Buf/Inv :	0
10	Total Number of Clock Cells :	0
11	Total Area of CT Buffers :	0.00000
12	Total Area of CT cells :	0.00000
13	Max Global Skew :	0.00031
14	Number of MaxTran Violators :	0
15	Number of MaxCap Violators :	1
16	Number of MaxFanout Violators :	0
1	Operating Condition	worst
2	Clock global Skew	0.000
3	Longest path delay	0.109
4	Shortest path delay	0.109

The longest path delay end pin: is_slti_blt_slt_reg/CLK
The shortest path delay end pin: genblk1.pcpi_mul/rd_reg[63]/CLK

Clock_tree Longest Path (Compile ultra)							
S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1582	0	0	0	r
3	is_slti_blt_slt_reg/CLK	1001037.500	0	0	0.109	0.109	r
	Clock Delay					0.109	

Clock_tree Shortest Path (Compile ultra)							
S.No	Pin	Cap	Fanout	Trans	Incr	Arri	
1	clk	0	1	0	0	0	r
2	clk	1001037.500	1582	0	0	0	r
3	genblk1.pcpi_mul/rd_reg[63]/CLK	1001037.500	0	0	0.109	0.109	r
	Clock Delay					0.109	

Report- Threshold Voltage Group-compile

S.No	Vth Group Name->	saed32cell_svt
2	**All Cells**	9380 (100.00%)
3	**Blackbox Cells**	0 (0.00%)
4	**Non-Blackbox cells**	9380 (100.00%)
5	**All Cells Area**	31800.53 (100.00%)
6	**Blackbox Cells area**	0 (0.00%)
7	**Non-Blackbox cells area**	31800.53 (100.00%)
8	**All Cells leakage**	834.445uW (100.00%)
9	**Blackbox Cells leakage**	0.000pW (0.00%)
10	**Non-Blackbox cells leakage**	834.445uW (100.00%)

Report- Threshold Voltage Group - (compile ultra)

S.No	Vth Group Name ->	saed32cell_svt
1	**All Cells**	9771 (100.00%)
2	**Blackbox Cells**	0 (0.00%)
3	**Non-Blackbox cells**	9771 (100.00%)
4	**All Cells Area**	32321.53 (100.00%)
5	**Blackbox Cells area**	0 (0.00%)
6	**Non-Blackbox cells area**	32321.53 (100.00%)
7	**All Cells leakage**	864.766uW (100.00%)
8	**Blackbox Cells leakage**	0 (0.00%)
9	**Non-Blackbox cells leakage**	864.766uW (100.00%)

Compile vs compile_ultra

Report	Parameter	compile	compile_ultra
report_cell	Top Module cells	5302	6827
get_cells -hierarchical	Total Cells	9460	9780
report_reference	No of Refernces	51	42
report_qor	Combinational Cell Count	7713	8121
	Sequential Cell Count	1667	1650
	Buf/Inv Cell Count	1315	751
	No. of Violating Paths:	10	0
report_area	Combinational Area	20885.553873	21518.880665
	Sequential Area	10914.976860	10802.645208
	Buf/Inv Area	1764.267653	977.183687
	Net Interconnect Area	9298.772721	12629.902996
	Total area (µm²)	41099.303454	44951.428869
report_power	Internal Power (µW)	981.6275	972.3504
	Switching Power (µW)	5.5829	5.2184
	Total Dynamic Power (µW)	987.2123	977.5701
	Leakage Power (pW)	8.3445E+08	8.6477E+08
	Total Power (µW)	972.3504	1.8423E+03
	SETUP		
report_timing	Data Required Time	5.92	5.90
	Data Arrival Time	-6.29	-5.84
	Slack(max) - Setup	-0.36	0.07
	HOLD		
	Data Required Time	-0.04	-0.06
	Data Arrival Time	-0.21	-0.14
	Slack(min) - Hold	-0.25	0.21
report_threshold_voltage_group	Cell Count	9380	9771
	Area	31800.53	32321.53
	Leakage (µW)	834.445	867.766
report_clock_tree	No of Sinks	1599	1582
	Clock Global Skew	0.000	0.000
	Longest Path Delay	0.109	0.109
	Shortest Path Delay	0.109	0.109

Report - Compile vs Compile_ultra

Report	Parameter	compile	compile_ultra
report_cell	Top Module cells	5302	6827
get_cells -hierarchical	Total Cells	9460	9780
report_reference	No of Refernces	51	42
report_qor	Combinational Count	7713	8121
	Sequential Count	1667	1650
	Buf/Inv Count	1315	751
report_area	Total area (µm²)	41099.303454	44951.428869
report_power	Total Power (µW)	972.3504	1.8423E+03
report_timing	Slack(max) - Setup	-0.36	0.07
	Slack(min) - Hold	-0.25	0.21
report_threshold_voltage_group	Cell Count	9380	9771
	Area	31800.53	32321.53
	Leakage (µW)	834.445	867.766
report_clock_tree	No of Sinks	1599	1582
	Clock Global Skew	0.000	0.000
	Longest Path Delay	0.109	0.109
	Shortest Path Delay	0.109	0.109

Cell Count = Combinational + Sequential Count

Compile			
Report	**Parameter**	**NLDM**	**CCS**
report_cell	Top Module cells	5505	5302
get_cells -hierarchical	Total Cells	9411	9460
report_reference	No of Refernces	62	51
report_qor	Combinational Cell Count	7797	7713
	Sequential Cell Count	1667	1667
	Buf/Inv Cell Count	1458	1315
report_area	Combinational Area	21094.460267	20885.553873
	Sequential Area	10929.208921	10914.976860
	Buf/Inv Area	2076.356500	1764.267653
	Net Interconnect Area	4328.556079	9298.772721
	Total area (μm^2)	36352.225267	41099.303454
report_power	Internal Power (µW)	984.6396	981.6275
	Switching Power (µW)	10.8277	5.5829
	Total Dynamic Power (µW)	995.4677	987.2123
	Leakage Power (pW)	56.134	8.3445E+08
	Total Power (µW)	1051.6013	972.3504
	SETUP		
report_timing	Data Required Time	5.96	5.92
	Data Arrival Time	-6.82	-6.29
	Slack(max) - Setup	-0.86	-0.36
	HOLD		
	Data Required Time	-0.05	-0.04
	Data Arrival Time	-0.18	-0.21
	Slack(min) - Hold	-0.24	-0.25
report_threshold_voltage_group	Cell Count	9464	9380
	Area	32023.67	31800.53
	Leakage (µW)	56.134	834.445
report_clock_tree	No of Sinks	1599	1599
	Clock Global Skew	0.001	0.000
	Longest Path Delay	0.124	0.109
	Shortest Path Delay	0.123	0.109

Compile_ultra			
Report	**Parameter**	**NLDM**	**CCS**
report_cell	Top Module cells	6806	6827
get_cells -hierarchical	Total Cells	9398	9780
report_reference	No of Refernces	57	42
report_qor	Combinational Cell Count	7982	8121
	Sequential Cell Count	1650	1650
	Buf/Inv Cell Count	845	751
report_area	Combinational Area	21324.206365	21518.880665
	Sequential Area	10809.761239	10802.645208
	Buf/Inv Area	1146.951876	977.183687
	Net Interconnect Area	12089.423766	12629.902996
	Total area (μm^2)	44223.39137	44951.428869
report_power	Internal Power (µW)	972.5209	972.3504
	Switching Power (µW)	5.6778	5.2184
	Total Dynamic Power (µW)	978.1987	977.5701
	Leakage Power (pW)	57.671	8.6477E+08
	Total Power (µW)	1035.9	1.8423E+03
	SETUP		
report_timing	Data Required Time	5.92	5.90
	Data Arrival Time	-5.92	-5.84
	Slack(max) - Setup	0	0.07
	HOLD		
	Data Required Time	-0.06	-0.06
	Data Arrival Time	-0.14	-0.14
	Slack(min) - Hold	0.21	0.21
report_threshold_voltage_group	Cell Count	9632	9771
	Area	32133.97	32321.53
	Leakage (µW)	57.671	867.766
report_clock_tree	No of Sinks	1582	1582
	Clock Global Skew	0.001	0.000
	Longest Path Delay	0.124	0.109
	Shortest Path Delay	0.123	0.109