

COMPILE			
Report	Parameter	NLDM	CCS
report_cell	Top Module cells	5400	5343
get_cells -hierarchical	Total Cells	9138	9338
report_reference	No of Refernces	72	64
	Levels of Logic	52.00	59.00
	Critical Path Length	4.94	4.93
report_qor	Critical Path Slack	0.00	0.02
	Total Negative Slack	0.00	0.00
	No. of Violating Paths	0.00	0.00
	Combinational Area	19946.491795	20557.453992
report_area	Sequential Area	1553.836422	1693.361483
	Buf/Inv Area	10929.971353	10911.418844
	Net Interconnect Area	8993.566112	9337.433828
	Total area (μm^2)	39870.029260	40806.306664
	Internal Power (μW)	1.4561E+03	1.4308E+03
report_power	Switching Power (μW)	6.3124	5.7802
	Total Dynamic Power (mW)	1.4624	1.4365
	Leakage Power (pW)	2.5382E+09	8.2961E+08
	Total Power (μW)	4.0006E+03	2.2662E+03
	SETUP		
report_timing	Data Required Time	5.94	5.96
	Data Arrival Time	-5.94	-5.93
	Slack(max) - Setup	0.00	0.02
	HOLD		
	Data Required Time	0.05	-0.02
	Data Arrival Time	-0.11	-0.19
	Slack(min) - Hold	0.07	0.21
	HVT		
report_threshold_voltage_group	Cell Count	1595 (17.60%)	1399 (15.10%)
	Area	7455.57 (24.15%)	6965.83 (22.14%)
	Leakage (μW)	3.531uW (0.14%)	159.016uW (19.17%)
	LVT		
	Cell Count	7470 (82.40%)	7866 (84.90%)
	Area	23420.89 (75.85%)	24503.04 (77.86%)
	Leakage (μW)	2.535mW (99.86%)	670.599uW (80.83%)
report_clock_tree	No of Sinks	1599	1599
	Clock Global Skew	0.023	0.013
	Longest Path Delay	0.125	0.113
	Shortest Path Delay	0.102	0.100

In Compile, CCS is better in terms of area and power,
But slightly bad in timing
CCS chose more HVT and NLDM chose more LVT cells

COMPILE_ULTRA			
Report	Parameter	NLDM	CCS
report_cell	Top Module cells	8152	6265
get_cells -hierarchical	Total Cells	11032	9053
report_reference	No of References	94	43
report_qor	Levels of Logic	9.00	48.00
	Critical Path Length	4.92	4.95
	Critical Path Slack	0.01	0.00
	Total Negative Slack	0.00	0.00
	No. of Violating Paths	0.00	0.00
report_area	Combinational Area	24852.487507	19522.325387
	Sequential Area	1487.758986	768.277317
	Buf/Inv Area	10824.755731	10800.357912
	Net Interconnect Area	11331.263691	12707.414537
	Total area (μm^2)	47008.506930	43030.097836
report_power	Internal Power (μW)	1.1886E+03	1.8790E+03
	Switching Power (μW)	5.9689	5.5791
	Total Dynamic Power (mW)	1.1946	1.8846
	Leakage Power (pW)	1.6764E+09	8.2406E+08
	Total Power (μW)	2.8710E+03	2.7086E+03
report_timing	SETUP		
	Data Required Time	5.92	5.95
	Data Arrival Time	-5.92	-5.95
	Slack(max) - Setup	0.01	0.00
	HOLD		
report_threshold_voltage_group	Data Required Time	0.06	-0.02
	Data Arrival Time	-0.27	-0.16
	Slack(min) - Hold	0.21	0.18
	HVT		
	Cell Count	7027 (63.99%)	92 (1.02%)
report_clock_tree	Area	21579.62 (60.49%)	330.90 (1.09%)
	Leakage (μW)	6.534uW (0.39%)	8.701uW (1.06%)
	LVT		
	Cell Count	3955 (36.01%)	8958 (98.98%)
	Area	14097.62 (39.51%)	29991.79 (98.91%)
report_clock_tree	Leakage (μW)	1.670mW (99.61%)	815.356uW (98.94%)
	No of Sinks	1582	1582
	Clock Global Skew	0.242	0.014
	Longest Path Delay	1.265	0.114
report_clock_tree	Shortest Path Delay	1.023	0.100

In compile_ultra, CCS better in terms of area and power,
But slightly bad timing
NLDM chose more HVT and CCS chose more LVT cells