

RVT ,LVT AND HVT

COMPILE			
Report	Parameter	NLDM	CCS
report_cell	Top Module cells	5416	5457
get_cells -hierarchical	Total Cells		
report_reference	No of References	75	86
	Levels of Logic	62.00	31.00
report_qor	Critical Path Length	5.05	4.68
	Critical Path Slack	-0.12	0.24
	Total Negative Slack	-0.31	0.00
	No. of Violating Paths	5.00	0.00
report_area	Combinational Area	20242.823721	21092.173082
	Sequential Area	1733.007942	2124.389745
	Buf/Inv Area	10929.208921	10914.468572
	Net Interconnect Area	9253.215096	8388.093693
	Total area (μm^2)	40425.247738	40394.735347
report_power	Internal Power (μW)	1.4089E+03	1.9071E+03
	Switching Power (μW)	6.317	5.2447
	Total Dynamic Power (mW)	1.4152	1.9124
	Leakage Power (pW)	2.3706E+09	8.5100E+08
	Total Power (μW)	3.7858E+03	2.7634E+03
report_timing	SETUP		
	Data Required Time	5.93	5.92
	Data Arrival Time	-6.05	-5.68
	Slack(max) - Setup	-0.12	0.24
	HOLD		
report_threshold_voltage_group	Data Required Time	0.06	-0.03
	Data Arrival Time	-0.16	-0.17
	Slack(min) - Hold	0.09	0.21
	HVT		
	Cell Count	1839 (20.16%)	2972 (31.91%)
	Area	8413.95 (26.99%)	8123.71 (25.38%)
	Leakage (μW)	4.358uW (0.18%)	218.944uW (25.73%)
	LVT		
	Cell Count	6950 (76.18%)	6261 (67.23%)
	Area	21606.56 (69.31%)	23640.73 (73.86%)
	Leakage (μW)	2.365mW (99.75%)	625.485uW (73.50%)
	RVT		
	Cell Count	334 (3.66%)	80 (0.86%)
	Area	1151.53 (3.69%)	242.20 (0.76%)
	Leakage (μW)	1.574uW (0.07%)	6.569uW (0.77%)
report_clock_tree	No of Sinks	1599	1599
	Clock Global Skew	0.023	0.013
	Longest Path Delay	0.125	0.113
	Shortest Path Delay	0.102	0.100

In Compile, NLDM is better in terms of timing
 But CCS is better terms of area and power consumption
 NLDM chose more LVT cells than CCS

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COMPILE_ULTRA			
Report	Parameter	NLDM	CCS
report_cell	Top Module cells	8131	6367
get_cells -hierarchical	Total Cells		
report_reference	No of Refernces	119	46
report_qor	Levels of Logic	9.00	35.00
	Critical Path Length	3.39	4.91
	Critical Path Slack	0.00	0.01
	Total Negative Slack	0.00	0.00
	No. of Violating Paths	0.00	0.00
report_area	Combinational Area	24865.448858	20151.840089
	Sequential Area	1434.134602	835.879621
	Buf/Inv Area	10826.788883	10799.087193
	Net Interconnect Area	11361.423671	12839.718345
	Total area (μm^2)	47053.661412	43790.645626
report_power	Internal Power (μW)	1.1538E+03	1.8406E+03
	Switching Power (μW)	5.8843	5.6608
	Total Dynamic Power (mW)	1.1597	1.8463
	Leakage Power (pW)	5.2612E+08	8.2351E+08
	Total Power (μW)	1.6858E+03	2.6698E+03
report_timing	SETUP		
	Data Required Time	5.70	5.93
	Data Arrival Time	-5.69	-5.91
	Slack(max) - Setup	0.00	0.01
	HOLD		
	Data Required Time	-0.02	-0.02
	Data Arrival Time	-0.19	-0.16
	Slack(min) - Hold	0.21	0.18
	HVT		
report_threshold_voltage_group	Cell Count	5937 (54.17%)	123 (1.33%)
	Area	18205.61 (51.01%)	682.12 (2.20%)
	Leakage (μW)	5.778uW (1.10%)	15.238uW (1.85%)
	LVT		
	Cell Count	700 (6.39%)	8958 (97.19%)
report_clock_tree	Area	3009.32 (8.43%)	30061.42 (97.13%)
	Leakage (μW)	498.394uW (94.73%)	797.583uW (96.85%)
	RVT		
	Cell Count	4323 (39.44%)	136 (1.48%)
	Area	14477.31 (40.56%)	207.38 (0.67%)
	Leakage (μW)	21.943uW (4.17%)	10.688uW (1.30%)
report_clock_tree	No of Sinks	1582	1582
	Clock Global Skew	0.235	0.013
	Longest Path Delay	1.258	0.113
	Shortest Path Delay	1.023	0.100

With compile_ultra, CCS is better in terms of all PPA
CCS chose more LVT cells than the NLDM