



## RS232 UART for Intel® DE-Series Boards

For Quartus® Prime 18.0

## 1 Core Overview

The RS232 UART Core implements a method for communication of serial data. The core provides a simple register-mapped Avalon® interface. Master peripherals (such as a Nios® II processor) communicate with the core by reading and writing control and data registers.

## 2 Instantiating the Core

The RS232 UART core can be instantiated in a system using Platform Designer or as a standalone component from the IP Catalog within the Quartus® Prime software. Designers use the core's configuration wizard to specify the desired features. The following section describes the available options in the configuration wizard.

### 2.1 Configuration Settings

This section describes the configuration settings.

#### 2.1.1 Interface Settings

The RS232 UART Core can either have a Avalon Memory-Mapped port or two Avalon Streaming ports. It is recommended to select Memory Mapped when connecting to a processor, otherwise set it to Streaming.

#### 2.1.2 Baud Rate Options

The RS232 UART Core can implement any of the standard baud rates for RS-232 connections. The baud rate is fixed at system generation time and cannot be changed via the Avalon slave port.

 The baud rate is calculated based on the clock frequency provided by the Avalon interface. Changing the system clock frequency in hardware without regenerating the RS232 UART Core hardware will result in incorrect signaling.

#### 2.1.3 Baud Rate (bps) Setting

The Baud Rate<sup>1</sup> setting determines the default baud rate after reset. The Baud Rate option offers standard preset values (e.g. 9600, 57600, 115200 bps<sup>2</sup> ).

<sup>1</sup>Baud rate: symbol rate, number of symbols transmitted per second.

<sup>2</sup>UART uses one bit per symbol, so the unit of baud rate is equivalent to Bits Per Second.

The baud rate value is used to calculate an appropriate clock divisor value to implement the target baud rate. The baud rate and divisor values are related as follows:

$$\text{divisor} = \text{int}(\text{clock frequency})/(\text{baud rate}) + 0.5$$

$$\text{baud rate} = (\text{clock frequency})/(\text{divisor} + 1)$$

#### 2.1.4 Data Width, Stop Bits, and Parity

The RS232 UART core's parity, data bits and stop bits are configurable. These settings are fixed at system generation time; they cannot be altered via the core's registers. The available settings are shown in Table 1.

<b>Table 1. Bit settings</b>		
<b>Settings</b>	<b>Allowed values</b>	<b>Description</b>
Data Width	7, 8, or 9 bits	This setting determines the widths of the txdata, rxdata, and endofpacket registers.
Stop Bits	1, 2	This setting determines whether the core transmits 1 or 2 stop bits with every character. The core always terminates a receive transaction at the first stop bit, and ignores all subsequent stop bits, regardless of the Stop Bits setting.
Parity	None, Even, Odd	This setting determines whether the UART transmits characters with parity checking, and whether it expects received characters to have parity checking. See below for further details.

**Parity Setting** When Parity is set to None, the transmitting logic sends data without including a parity bit, and the receiving logic presumes that the incoming data does not include a parity bit. When parity is None, the data register's PE (parity error) bit is not implemented; it always reads 0.

When Parity is set to Odd or Even, the transmit logic computes and inserts the required parity bit into the outgoing TXD bitstream, and the receive logic checks the parity bit in the incoming RXD bitstream. When parity is Even, the parity bit is 1 if the data has an even number of 1 bits; otherwise the parity bit is 0. Similarly, when parity is Odd, the parity bit is 1 if the data has an odd number of 1 bits.

## 3 Software Programming Model

### 3.1 Register Map

Table 2 shows the register map for the RS232 UART Core when Memory-Mapped Avalon Type is selected for the core. Device drivers control and communicate with the core through the two 32-bit memory-mapped registers.

<b>Table 2. RS232 UART Core register map</b>												
<b>Offset in bytes</b>	<b>Register Name</b>	<b>R/W</b>	<b>Bit description</b>									
			31...24	23...16	15	14...11	10	9	8	7	6...2	1
0	data	RW	(1)	RAVAIL	RVALID	(1)		PE	(2)	(2)	DATA	
4	control	RW	(1)	WSPACE		(1)		WI	RI	(1)	WE	RE

*Notes on Table 2:*

- (1) Reserved. Read values are undefined. Write zero.
- (2) These bits may or may not exist, depending on the specified **Data Width**. If they do not exist, they read zero and writing has no effect.

#### 3.1.1 Data Register

The read and write FIFOs are accessed via the data register. Table 3 gives the format of this register.

<b>Table 3. Data register bits</b>			
<b>Bit number</b>	<b>Bit/Field name</b>	<b>Read/Write</b>	<b>Description</b>
8...0	DATA	R/W	The value to transfer to/from the RS232 UART Core. When writing, the DATA field is a character to be written to the write FIFO. When reading, the DATA field is a character read from the read FIFO.
9	PE	R	Indicates whether the DATA field had a parity error.
15	RVALID	R	Indicates whether the DATA and PE fields contain valid data.
23...16	RAVAIL	R	The number of characters remaining in the read FIFO (including this read).

A read from the data register returns the first character from the FIFO (if one is available) in the DATA field. Reading also returns information about the number of characters remaining in the FIFO in the RAVAIL field. A write to the data register stores the value of the DATA field in the write FIFO. If the write FIFO is full, then the character is lost.

#### 3.1.2 Control Register

RS232 UART Core's interrupt generation and read-status information are controlled by the Control register. Table 4 describes the function of each bit.

**Table 4. Control register bits**

Bit number	Bit/Field name	Read/Write	Description
0	RE	R/W	Interrupt-enable bit for read interrupts
1	WE	R/W	Interrupt-enable bit for write interrupts
8	RI	R	Indicates that the read interrupt is pending
9	WI	R	Indicates that the write interrupt is pending
23...16	WSPACE	R	The number of spaces available in the write FIFO.

A read from the control register returns the status of the read and write FIFOs. Writing to the register is used to enable and disable interrupts.

The RE and WE bits enable interrupts for the Read and Write FIFOs, respectively. The WI and RI bits indicate the status of the interrupt sources, qualified by the setting of the interrupt enable bits (WE and RE). Bits RI and WI can be examined to determine what condition generates the interrupt request.

### 3.2 Device Driver for the Nios® II Processor

The RS232 UART core is packaged with C-language functions accessible through the [hardware abstraction layer \(HAL\)](#). These functions implement basic operations that users need for the RS232 UART Core.

To use the functions, the C code must include the statement:

```
#include "altera_up_avalon_rs232.h"
```

#### 3.2.1 alt\_up\_rs232\_enable\_read\_interrupt

**Prototype:** void alt\_up\_rs232\_enable\_read\_interrupt(alt\_up\_rs232\_dev \*rs232)  
**Include:** <altera\_up\_avalon\_rs232.h>  
**Parameters:** rs232 – the RS232 device structure  
**Description:** Enable the read interrupts for the RS232 UART core.

#### 3.2.2 alt\_up\_rs232\_disable\_read\_interrupt

**Prototype:** void alt\_up\_rs232\_disable\_read\_interrupt(alt\_up\_rs232\_dev \*rs232)  
**Include:** <altera\_up\_avalon\_rs232.h>  
**Parameters:** rs232 – the RS232 device structure  
**Description:** Disable the read interrupts for the RS232 UART core.

### 3.2.3 alt\_up\_rs232\_check\_parity

**Prototype:** int alt\_up\_rs232\_check\_parity(alt\_u32 data\_reg)  
**Include:** <altera\_up\_avalon\_rs232.h>  
**Parameters:** data\_reg – the date register  
**Returns:** 0 for no errors, -1 for parity error.  
**Description:** Check whether the DATA field has a parity error.

### 3.2.4 alt\_up\_rs232\_get\_used\_space\_in\_read\_FIFO

**Prototype:** unsigned alt\_up\_rs232\_get\_used\_space\_in\_read\_FIFO(alt\_up\_rs232\_dev \*rs232)  
**Include:** <altera\_up\_avalon\_rs232.h>  
**Parameters:** rs232 – the RS232 device structure  
**Returns:** The number of data words remaining.  
**Description:** Gets the number of data words remaining in the read FIFO.

### 3.2.5 alt\_up\_rs232\_get\_available\_space\_in\_write\_FIFO

**Prototype:** unsigned alt\_up\_rs232\_get\_available\_space\_in\_write\_FIFO(alt\_up\_rs232\_dev \*rs232)  
**Include:** <altera\_up\_avalon\_rs232.h>  
**Parameters:** rs232 – the RS232 device structure  
**Returns:** The amount of available space remaining.  
**Description:** Gets the amount of available space remaining in the write FIFO.

### 3.2.6 alt\_up\_rs232\_write\_data

**Prototype:** int alt\_up\_rs232\_write\_data(alt\_up\_rs232\_dev \*rs232, alt\_u8 data)  
**Include:** <altera\_up\_avalon\_rs232.h>  
**Parameters:** rs232 – the RS232 device structure  
                data – the character to be transferred to the RS232 UART Core.  
**Returns:** 0 for success or -1 on error.  
**Description:** Write data to the RS232 UART core.  
**Notes:** User should ensure the write FIFO is not full before writing, otherwise the character is lost.

### 3.2.7 alt\_up\_rs232\_read\_data

**Prototype:** int alt\_up\_rs232\_read\_data(alt\_up\_rs232\_dev \*rs232, alt\_u8 \*data, alt\_u8 \*parity\_error)

**Include:** <altera\_up\_avalon\_rs232.h>

**Parameters:** rs232 – the RS232 device structure  
data – pointer to the memory where the character read from the RS232 UART core should be stored.  
parity\_error – pointer to the memory where the parity error should be stored.

**Returns:** 0 for success or -1 on error.

**Description:** Read data from the RS232 UART core.

**Notes:** This function will clear the DATA field of the data register after reading and it uses the alt\_up\_rs232\_check\_parity function to check the parity for the DATA field.

### 3.2.8 alt\_up\_rs232\_read\_fd

**Prototype:** int alt\_up\_rs232\_read\_fd(alt\_fd \*fd, char \*ptr, int len)

**Include:** <altera\_up\_avalon\_rs232.h>

**Parameters:** –

**Description:**

### 3.2.9 alt\_up\_rs232\_write\_fd

**Prototype:** int alt\_up\_rs232\_write\_fd(alt\_fd \*fd, const char \*ptr, int len)

**Include:** <altera\_up\_avalon\_rs232.h>

**Parameters:** –

**Description:**

### 3.2.10 alt\_up\_rs232\_open\_dev

**Prototype:** alt\_up\_rs232\_dev\* alt\_up\_rs232\_open\_dev(const char \*name)

**Include:** <altera\_up\_avalon\_rs232.h>

**Parameters:** name – the device name in Platform Designer

**Returns:** the device structure

**Description:** Open the RS232 device according to device name.

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