**B.E. Mid Semester Examination, September 2014**

**COE-301-Computer Graphics**

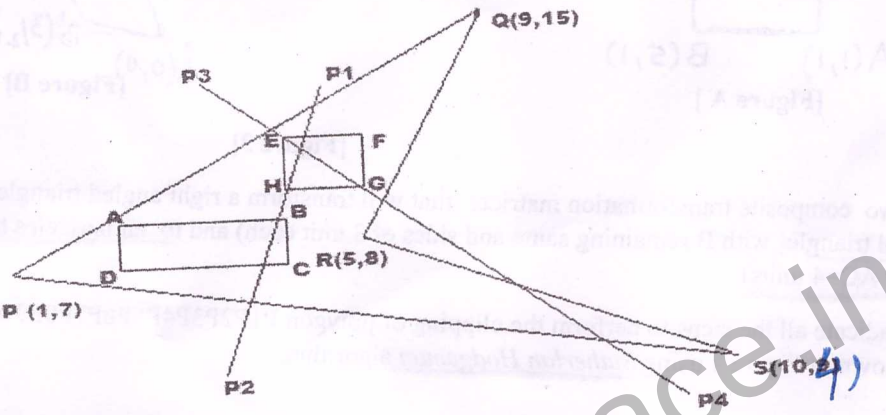
Page(s): 2

**Max Marks:20**

**Time:1:30 hrs.**

**Note: Attempt all FOUR questions.**

Q1: Using *Cyrus-Beck* and *Cohen –Sutherland* Line Clipping algorithms ,clearly show all the steps to clip lines **P1P2** a **P3P4** against a *concave* clipping window PQRS. The clipping window has a *rectangular* hole **ABCD** and a *square* h **EFGH**.



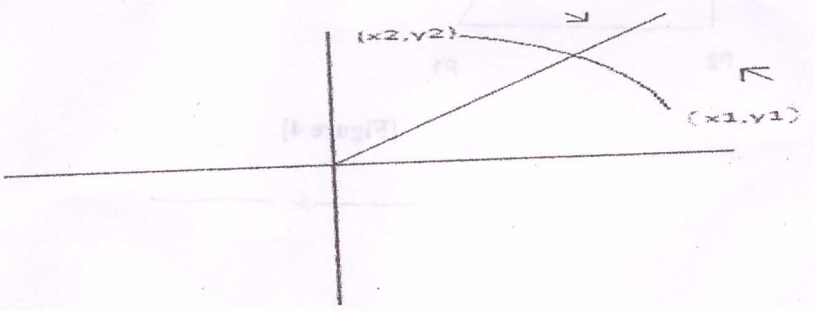

**[Figure 1]**

Coordinates :

*P1*: **(5,13)** ; *P2*: **(3,4)** ; *P3*: **(3,11)** ; *P4*: **(12,1)** ;*A* : **(2,8)** ; *B* : **(4,8)** ; *C* : **(4,7)** ; *D*: (2,7) ;*E* : **(4,10)** ; *F* : **(5,10)** ; *G* : **(5,9** **(4,9)**;

Q2. **(3.5**

a. Using Bresenham's approach propose a technique to scan convert the arcs in Figure 2. simultaneously



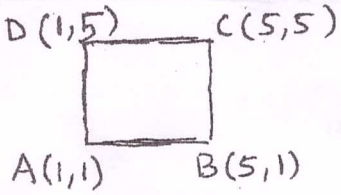

**[Figure 2]**

— PTO —

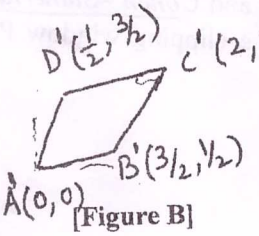
b. Digitize a line by scan converting a line AB (A(-1,-1), B(-15,-7) in quadrant IV using midpoint approach

Q3.

a. In Figure 3. below derive a composite transformation matrix that will transform figure A to Figure B. Give the final coordinates of the transformed figure




[Figure A ]

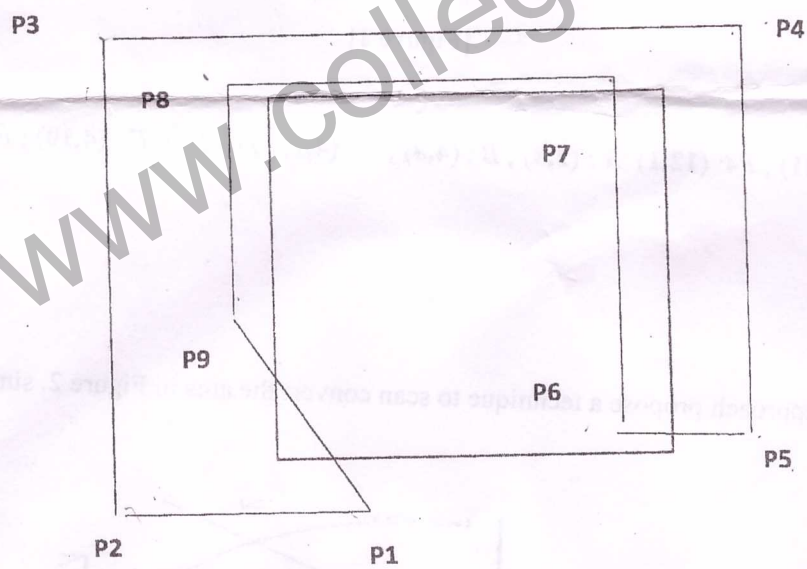



[Figure B]

[Figure 3]

b. Derive two composite transformation matrices that will transform a right angled triangle[A(1,1), B(4,1), C(1,3) ]to an equilateral triangle( with B remaining same and sides of 3 unit each) and to an isosceles triangle(with A remaining same and AB = AC=4 units)

Q4. Clearly indicate all the steps to perform the clipping of polygon P1P2P3P4P5P6P7P8P9 against an upright rectangular window as shown in Figure 4 using *Sutherlan Hodgeman* algorithm.




[Figure 4]

Total No. of Pages:1 Roll No

# B.E.(COE) B.E. V SEM MID EXAMINATION Sept, 2014

## COE-302, Discrete Maths and Design of Algorithms

Time: 1:30 Hours Max. Marks: 20

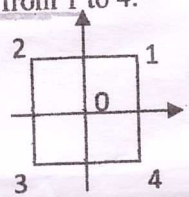
Note:

- *Attempt all questions, each carries equal mark.*
- *Assume suitable missing data, if any*

Q.1 A relation R is defined as $b=a^r$, a, b are in Z, set of integers, wher is a positive integer. Show that R is partial order on Z.

Q.2 Let S be the square in plane $R^2$ (refer Figure), with its centre at ori and its vertices are numbered counter clockwise from 1 to 4.

(a) Define group G of symmetries of S.
(b) List the elements of G.
(c) Find a minimum set of generators of G.




Q.3 Let R be a relation on A. A={2,3,4,8,12,36,48}, R={(a,b) | a divisor of b}.

(a) Draw Hasse Diagram.
(b) Find its maximum and minimal elements?
(c) Is poset a lattice?

Q.4 Let Fx be the set of all one-to-one onto mapping from X onto where X={1,2,3}. Find all elements of Fx and find the inverse of element.

Q.5 Write short note on the following:

(a) Distributive Lattice
(b) Complemented Lattice
(c) Commutative Ring
(d) Reflexive and symmetric closure

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Total No. of Page(s):2 Roll. No.....

# B.E. MID SEMESTER EXAMINATION September, 2014

## COE-303: COMPUTER SYSTEM ORGANIZATION

**Time: 1:30 Hrs.** **Max. Marks: 20**

**Note:** All Questions are Compulsory.
Question 1 to 5 carry 2 marks each.
Question 6 and 7 carry 5 marks each.
Assume any missing information, if any.

Q1 In a bus system of registers, the number of registers are 32. What are the
a) Number of multiplexers
b) Size of multiplexer
c) Number of bits in each register?

Q2 Write a subroutine for the following instruction using 3 address, 2 address, 1 address and 0 address instruction formats

A*B+A*(B*D+C*E)

Q3 What are interrupts. Explain the interrupt cycle with flow chart?

Q4
a) What must be the address field of index addressing mode to make it equal to register indirect addressing mode?

b) What is the number of memory references in?
(i) Indirect addressing mode
(ii) Branch instruction.

Q5 Explain the difference between the following:
a) Hard-wired control and micro-programmed control
b) RISC and CISC

Q6 Early processors used accumulator to store intermediate results whereas modern processors uses either a register file or a stack.
a) Why use a stack or register file rather than accumulator? 2 marks
b) What are the advantage and disadvantage of using register file over stack? 3 marks

Q7 Design a CPU that meets the following specifications.

- It can access 256 words of memory, each word being 8 bits wide. The CPU does this by outputting an 8 bit address on its output pins A[7..0] and reading in 8 bit value from memory on its input D[7..0]
- The CPU contains an 8 bit address register, program counter and accumulator, data register and 3 bit instruction register.
- The CPU must realize the following instruction set. Note that α is a 8 bit value stored in location immediately following the instruction

| Instruction | Instruction Code | Operation |
|---|---|---|
| LDI | 000XXXXXα | AC ← α |
| STO | 001XXXXXα | M[α] ← AC |
| ADD | 010XXXXXα | AC ← AC+M[α] |
| OR | 011XXXXXα | AC ← ACVM[α] |
| JUMP | 100XXXXXα | PC ← α |
| JREL | 101XXXXXα | PC ← PC+ 000AAAAA |
| SKIP | 110XXXXXα | PC ← PC+1 |
| RST | 111XXXXXα | PC ← 0 AC ← 0 |

Total No. of pages: 2 Roll No.

BE (ECE/COE/ICE) V SEMESTER
MID-SEMESTER EXAMINATION September 2014

***ECE/COE/ICE-304: Linear Integrated Circuits***

Time: 1 hour and 30 minutes Max. Marks: 20

**Note: Attempt any five questions; all carry equal marks.**

1. Explain how does one realize: (a) a non-inverting integrator using a single op-amp (ii) an all pass filter using op-amp(s)?

2. What are the advantages of *inductance simulation circuits using IC op-amps* over the *passive wire-wound inductors*? Determine an expression for the input impedance of the circuit of **Fig. 1** and determine its equivalent circuit looking into terminal 1 (with respect to ground):

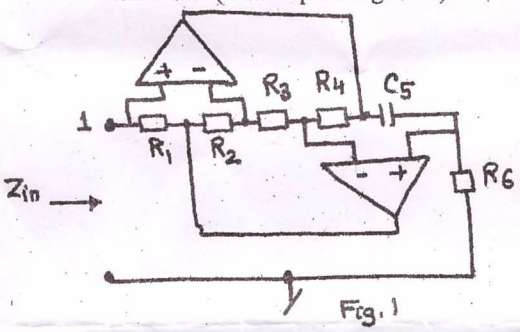

Fig. 1

3. What are the advantages of op-amp-RC filters over passive RLC filters? For the circuit shown in **Fig. 2** derive an expression for the transfer function $V_0/V_{in}$ and hence, identify the type of filter realized. Find the expressions for the filter parameters $H_o$, $Q_o$ (or bandwidth; whichever applicable) and $\omega_o$ from the resulting transfer function.

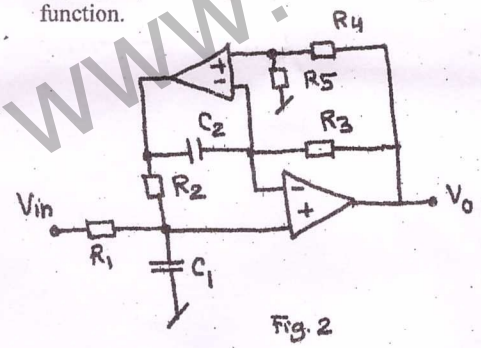

Fig. 2

4. Determine the condition of oscillation and frequency of oscillation for the sinusoidal oscillator circuit of **Fig. 3.**

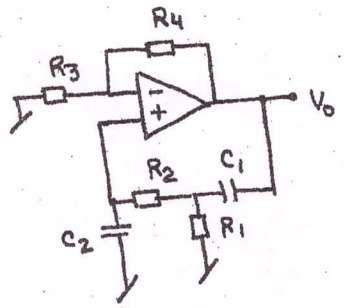

Fig. 3

5. Can the OTA-circuit shown in **Fig. 4** function as a sinusoidal oscillator? If not, what changes are needed to make it function as a sinusoidal oscillator? Find the condition and frequency of oscillation of the corrected circuit.

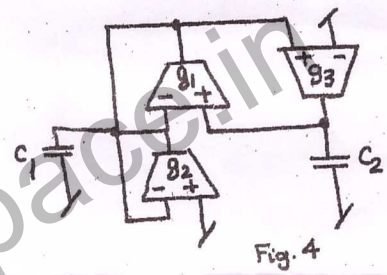

Fig. 4

6. Devise an OTA-based circuit which realizes the same transfer function as that of the op-amp circuit of **Fig. 5(a).**

**OR**

What are the applications of log/antilog circuits? Analyze the circuit of **Fig. 5(b)** and determine an expression for the output voltage in terms of the two inputs and hence, determine the function performed by the circuit.

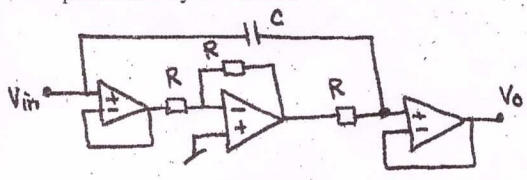

Fig. 5(a)

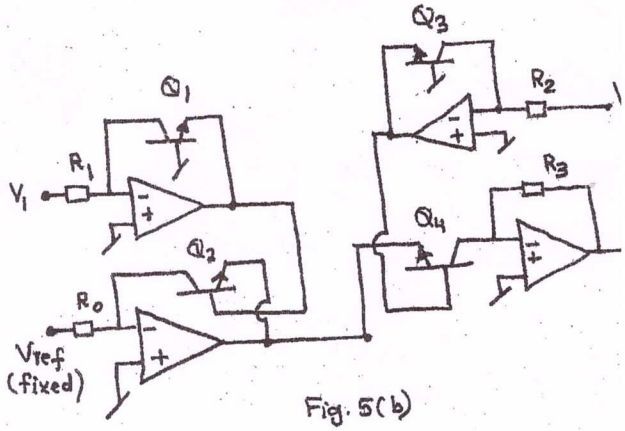

Fig. 5(b)

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# Mid Semester examination, September-2014
# ECE/COE/ICE 305
# Industrial Organization and Managerial Economics

**Time 1 ½ hours** **Max. Marks 20**

**Note: Attempt any FIVE Questions.**
**All questions carry equal marks.**

Q.1. What is management'? Explain briefly important functions of management.

Q.2. What were the important contributions of Frederick Taylor to scientific management approach?

Q.3. Describe various types of organizational structure with appropriate examples.

Q.4.What is plant location? Explain the principle factors influencing the choice of plant location.

Q.5. Differentiate between Bureaucratic model and administrative theory of management.

Q.6. What do you understand by Break-Even analysis? Explain its significance in manufacturing industry with an example.

Q.7. Briefly describe the Hawthorne experiments and how they influenced the human relations/behavioural approach to management.