Total Number of Pages: 01

Roll No.:- 515/IC/10

FIFTH SEMESTER

B.E. (ECE/COE/ICE)

B.E. Mid-Semester Examination, September, 2012

EC-304/COE-304/IC-304: Linear Integrated Circuits

Time: 1½ Hours

Max. Marks: 20

Note: Attempt any **FIVE** questions. Missing data/information, if any, may be suitably assumed and mentioned in the answer.

[1] Determine the relation between R_1, R_2 and R_3 for which the circuit shown in Fig. 1 realizes a band-reject filter. Assume op-amps to be ideal.

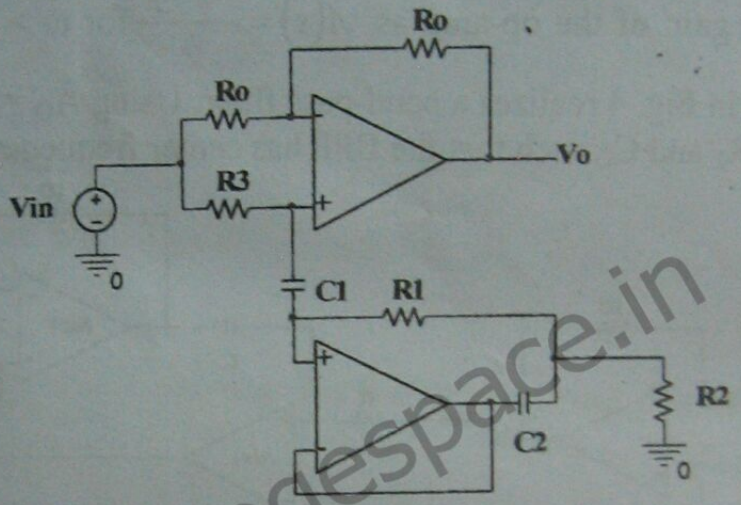


Figure-1

[2] For the circuit shown in Fig. 2.1, derive the required condition and frequency of oscillation.

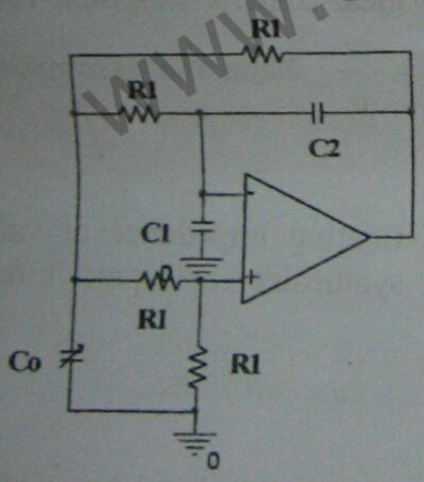


Figure-2.1

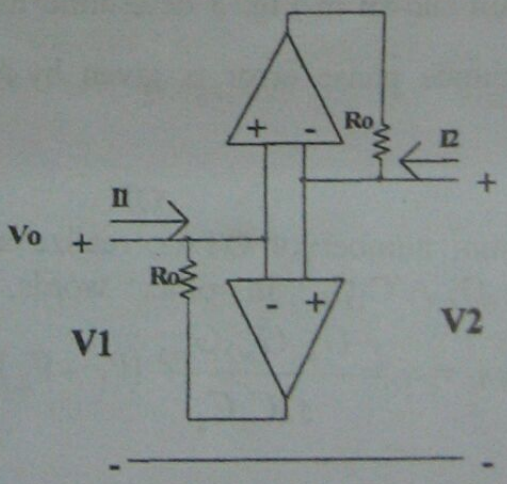


Figure-2.2

OR

[2] For the circuit shown in Fig. 2.2, derive the [Y] matrix and hence, draw the equivalent impedance, assuming that the op-amps are non-ideal with identical gains given by $A \approx \omega_t/s$ where ω_t is the gain band width product of the op-amps.

[3] Find the expression for the input impedance of the circuit shown in Fig. 3 and hence, find the function performed by the circuit.

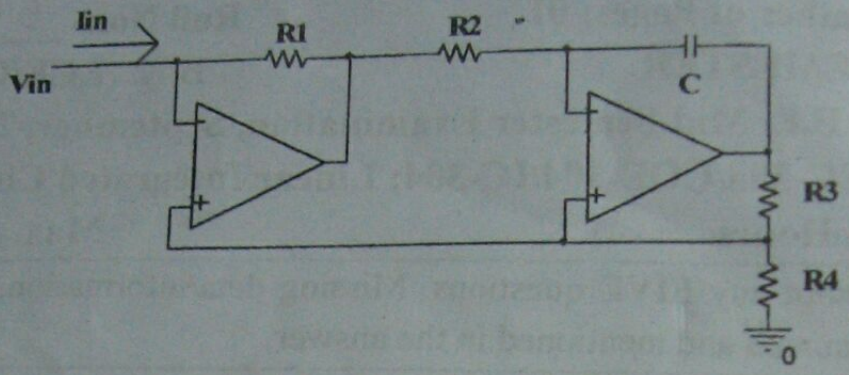


Figure-3

[4] Using the gain of the op-amp as $A(s)=\frac{A_o\omega_p}{s}$ for $\omega > \omega_p$, verify that the circuit shown in Fig. 4 realizes a band-pass filter. Using $A_O = 2 \times 10^5$, $f_p = 5$ Hz, calculate R_1, R_2 and C_O such that the BPF has center frequency of 100 KHz.

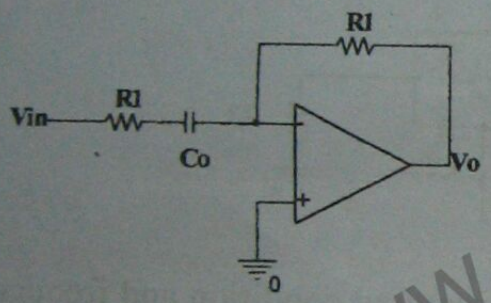


Figure-4

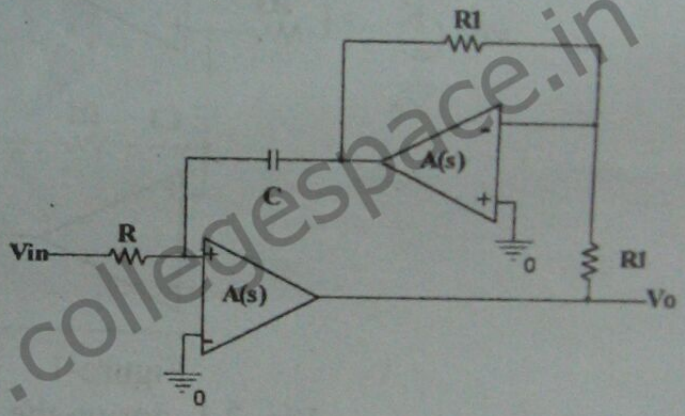


Figure-5

[5] For the circuit shown in Fig. 5 determine its ideal transfer function. Prove that the approximate phase error is given by $\phi \cong \frac{\omega}{\omega_t}$. State the assumptions made.

OR

Using a minimum number of OTAs, realize a floating impedance of value $Z(s)=G_{m1}\ G_{m2}\ G_{m3}/s^2C_1C_2$. In other words, synthesize a 2-port circuit characterized by $i_1 = -i_2 = \frac{G_{m1}G_{m2}G_{m3}}{s^2C_1C_2}(V_1 - V_2)$.

[6] Define the following terms for an op-amp: input bias current, input-offset voltage, slew-rate and CMRR.

OR

Elaborate, with appropriate justifications, two major advantages and two major disadvantages of the operational transconductance amplifier (OTA)-based analog circuits.

Total No. of Page(s): 2

Roll No. 515/IC/10

FIFTH SEMESTER **BE (EC/CO/IC)**

B.E MID SEMESTER EXAMINATION, SEPT 2012

EC/CO/IC -305: INDUSTRIAL ORGANISATION AND MANAGERIAL ECONOMICS

Time: 1:30 Hrs. *Max. Marks: 20*

Note: Attempt any four questions.
All questions carry equal marks.
Assume suitable missing data, if any.

1 What were the contributions of Fredrick Taylor, Elton Mayo, Gilbreth and Gantt? [5]

2 Differentiate among the following structures of the organization:
a) Line and staff organization
b) Functional organization
c) Informal organization
d) Matrix organization [5]

3 Describe the concept and appraisal of modern organization theory. Differentiate between empirical school and human behaviour school of management. [5]

4 What are the principles and functions of management? [5]

5 With the help of activities given below draw a network. Determine its critical path, earliest start time, earliest finish time, latest start time, latest finish time and total project duration. [5]

Activity	*Duration (in weeks)*
1-2	4
1-4	36
2-3	2
3-5	15
3-8	10
4-8	2
5-6	4
5-8	9
6-7	9
7-8	9
7-9	8
8-9	20
9-10	20

6 Discuss the various factors that influence the plant location decision. Outlining the types of plant layout, explain the salient features of single point or fixed position layout. [5]

PTO

OR

A project has the following characteristics.

Activity	*Most optimistic time*	*Most pessimistic time*	*Most likely time*
1-2	1	5	1.5
2-3	1	3	2
2-4	1	5	3
3-5	3	5	4
4-5	2	4	3
4-6	3	7	5
5-7	4	6	5
6-7	6	8	7
7-8	2	6	4
7-9	5	8	6
8-10	1	3	2
9-10	3	7	5

Construct a PERT network. Find critical path, EST, LST, EFT, LFT and project duration.

Fifth Semester

Roll No. 337/0110

B.E. (COE)

B.E. MID SEM EXAMINATION, September 2012

COE-301: PRINCIPLES OF COMPUTER GRAPHICS

Time: 1:30 Hrs

Max. Marks:20

Note: Attempt All questions. Assume any missing data suitable.

1.

a) A rectangular clipping window ABCD is defined as shown in Fig.1. The window is having a triangular hole EFG inside it. A line PQ cuts the window ABCD and EFG . Perform Cohen Sutherland clipping algorithm on ABCD and Cyrus Beck on triangle EFG to display the final clipped line P'P'' and Q'Q''. 4

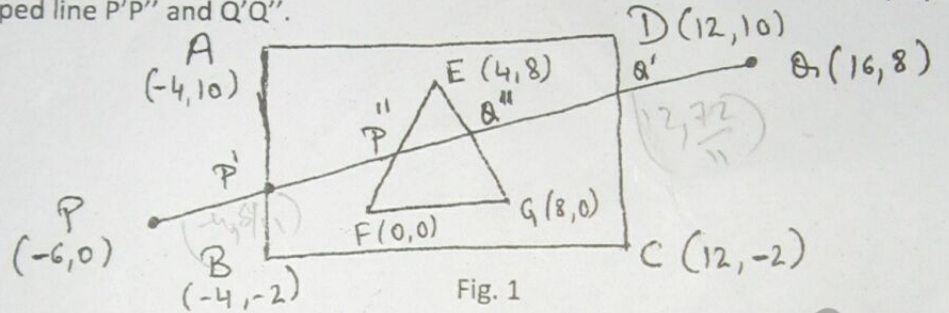


Fig. 1

b) Given the parametric equation of a line vector as x=3+2t, y=- 6+t, z=4, find the end points P1 and P2 of a collinear line segment.?

2.

a) When eight way symmetry is used to obtain a full circle from pixel coordinates generated from the 0° to 45° or the 90° to 45° octant, certain pixels are set or plotted twice. This phenomenon is referred to as overstrike. Identify where overstrike occurs 1

b) Design an algorithm for plotting an arc of an Ellipse in 1st quadrant ,from (x1,y1) to (x2,y2) in clockwise direction using Midpoint Algorithm. Plotting should proceed from both the endpoints of arc simultaneously. The condition is that there should not be any overstrike. 4

3. a) There are two vectors namely V and N. V is defined as i+j and N as i-j. Write the transformation steps so as to align V on N. 1.5

b) Derive the homogeneous transformation matrix about the line y=2x-6. 1.5

c) Prove that two successive 2D Rotations are additive; $R(\alpha)\,R(\beta) = R(\alpha+\beta)$. 2

4.

a) Using Scan Line Filling Algorithm fill the following Polygon in Fig. 2 showing all the necessary steps: 3

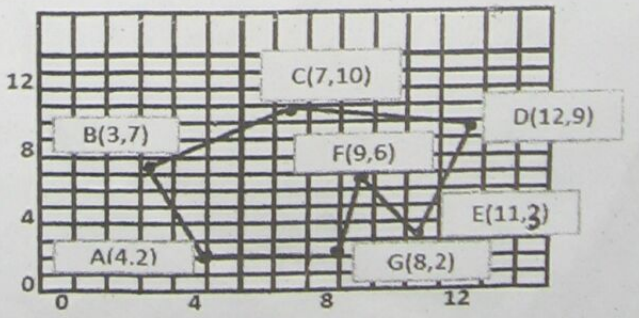


Fig. 2

b) Apply the stack based seed fill algorithm to fill the polygon defined by the vertices (1,1),(1,4),(3,6),(8,6) and (8,1). The seed pixel is at (4,3) and polygon is boundary filled. 2

Total no. of Pages: 2 Roll no: .....

FIFTH SEMESTER BE (COE) - V th Sem.

MID SEMESTER EXAMINATION
SEPT, 2012

COE-302 : DMDA (Discrete Maths and design of Algorithm)

Time: 1:30 Hrs. Max Marks: 20

NOTE: Attempt all questions.
All questions carry equal marks.

Q.1. Thirty cars are assembled in a factory. The options available were radio, air-conditioner and white wall tyres. 15 cars have radios, 8 have air-conditioner and 6 of them have white wall tyres. 3 of them have all the three options. Find out at least how many cars do not have any option. [4]

Q.2. Prove that partially ordered set is said to be a lattice if every two elements in the set have a unique least upper bound and a unique greatest lower bound. [4]

Q.3. Find CNF and DNF of the following [4]

$$(\neg P \rightarrow R) \wedge (Q \rightleftharpoons P)$$

Q.4. Define sum and product of two partitions. Find sum and product of π_1 & π_2.

$\pi_1 = \{\overline{lmn}, \overline{opqr}, \overline{st}, \overline{uv}\}$

$\pi_2 = \{\overline{lm}, \overline{nuv}, \overline{ot}, \overline{prs}, \overline{q}\}$

where $A = \{l, m, n, o, p, q, r, s, t, u, v\}$ [4]

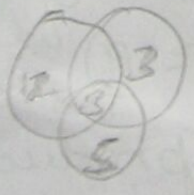
cont.

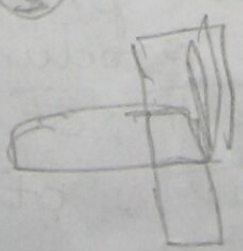
Q.5. Let $X = \{1, 2, 3, 4\}$

A function is defined as $f: X \to X$ such that $f \neq I_x$ and is one-to-one.

Find $fof = f^2$ and f^{-1}.

How a function is different from relation [4]





Date: Roll No. 337/60/10

B.E. COMPUTER ENGINEERING
MID SEMESTER EXAMINATION, Sept 2012
V SEMESTER, COMPUTER SYSTEM ORGANISATION COE 303

Instructions:-
Time Duration: 1.5 hrs
Maximum marks: 20
Attempt all questions

Q1) An aircraft is fitted with four processors, all of the same type, to perform the functions F1 to F4 given below. The memory requirement for the code for each function is also given.

F1) Monitor the environmental conditions inside and outside the aircraft by collecting data from 30 transducers continuously and analyzing the data using matrix manipulations – 8 KB code.
F2) Control the wing engines and the tail engine by repeatedly invoking small functions that control the speed and direction of 16 stepper motors – 2 KB code.
F3) Accept "request for attention" from 300 passengers through an port – 1KB code.
F4) A main controller that collects status information from the above processors and displays them on the dashboard inside the cockpit. In addition, it monitors emergency conditions such as bad weather and displays the scenes – 16 KB.

You have to architect the ISA of a processor type that can fulfill the above functions. Answer the following questions in given sequence.

A) What addressing modes are required? Give justification for each addressing mode you think will be needed.
B) What is the maximum memory space required? Why?
C) Is a stack required? Justify.
D) Suggest a suitable data bus width. Justify.
E) Briefly discuss what **kinds** of instructions are needed? Why?
F) What registers and flags are needed in the data path?
G) Using the above guidelines, design the instruction format.
H) Write the instructions set.
I) Write the RTL statements for (i) a *Load* instruction (ii) an *Unconditional branch* instruction, (iii) any *call* type of instruction for the ISA you have designed.

Q2) It is obvious that each of the 4 processors in Q1 is connected to a number of input output devices. For each processor:

1) Suggest the IO address space mapping for each processor. Justify.
2) Suggest the data transfer mechanism(s) (programmed /Interrupt /DMA) for each processor. Justify.
3) Write an ISR for preparing a 1-D matrix of size 100 prepared by the data collected from any single transducer for the processor implementing function F1.