

Sixth SEMESTER

B.E. (ECE/COE/ICE)
END SEMESTER EXAMINATION, May-2014

EC/COE/IC-311: Microprocessors

Time: 3:00 Hours

Max. Marks: 70

Note: Attempt EIGHT questions in all. Question 1 is compulsory and worth 21 marks. Rest all are worth 7 marks each.

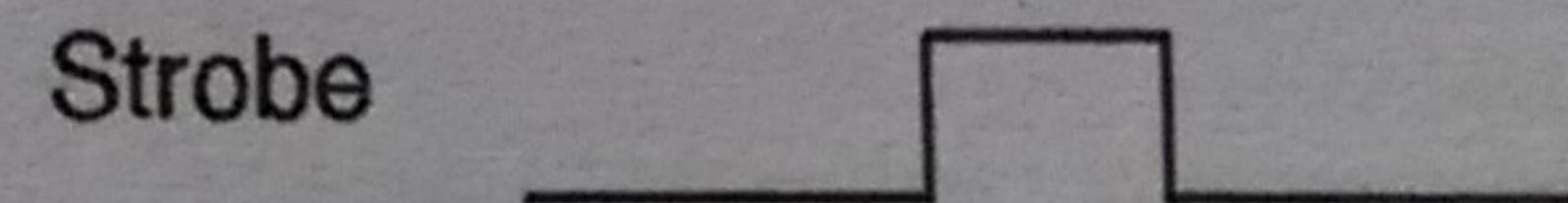
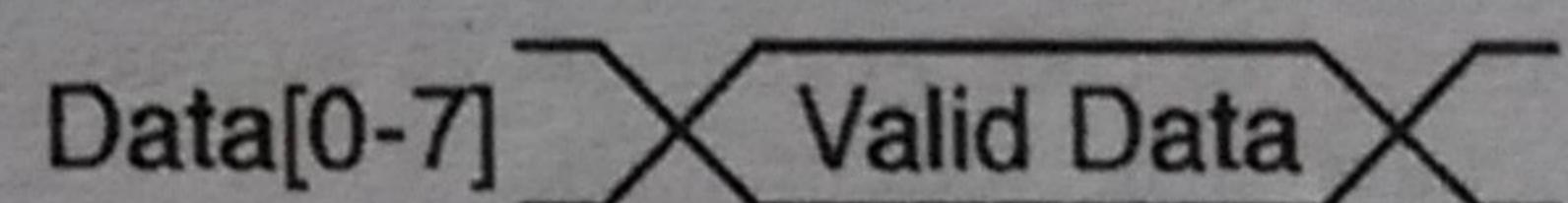
Assume suitable missing data, if any.

Abki baar... tension Na lo yaar!

1. [a] Compare and contrast memory mapped I/O and normal I/O.
- [b] Write a sequence of instructions to reset all the flags in 8085 without performing any arithmetic or logical operation.
- [c] Which flags are affected by the INR H, INX H and MVI A, 00h instructions?
- [d] If an 8085 system operates with a 2 MHz crystal and is designed to insert 2 wait states in **every memory access**, how much time would it take to execute an OUT instruction. Draw the timing diagram.
- [e] Right after a reset, if the first instruction that is executed is PUSH PSW, which memory locations will the registers be saved and what will be the contents of these memory locations right after the PUSH instruction is executed?
- [f] List all the machine cycles that 8085 uses. How many clock cycles do these machine cycles take? List an instruction that uses smallest variety of machine cycles. List another instruction that uses largest variety of machine cycles.
- [g] What is the difference between (i) RST6 and RST6.5; (ii) SUB B and CMP B; (iii) ADD A and DAD

2. Design a memory interface for an 8085 system using the following components: IC1, IC2: each is a 16Kbytes EPROM; IC3, IC4: each is a 16Kbytes SRAM. IC1 and IC2 are mapped in the lower memory map (addresses 0000H to 7FFFH) and IC3 and IC4 are mapped in the upper half (8000H to FFFFH). Show suitable glue logic to connect the four memory chips to the 8085 such that IC1 and IC3 occupy **only even addresses** and IC2 and IC4 occupy **only odd addresses**.

3. An 8085 system has 32Kbytes of SRAM from address 8000H onwards. It has an output port at I/O address 00H. **Write an assembler program** to transfer 16Kbytes of data from the upper half of the SRAM to the output port using a strobe signal generated on the SOD pin. For each data byte, strobe signal should be generated as seen in the figure below. Also, estimate the time required to transfer the required data if the 8085 system runs on a 10 MHz crystal.



4. An 8251 USART is interfaced to an 8085.
 - (a) How can it be ensured that 8251 is reset every time 8085 itself gets reset?
 - (b) How can 8085 reset 8251 under software control?
 - (c) Show hardware connections and suitable code snippet so that the 8251 can transmit and receive data at 38400 bits per second, 7 data bits, no parity and 1 stop bit.
5. Write an 8085 assembler program to control an 8253 timer which is mapped as an I/O port at base address 20H to generate a continuous

Roll No.....

No. of pages: 02

Date

SIXTH SEMESTER

B.E. (COE)

END SEMESTER EXAMINATION, May-2014
COE 312- INFORMATION SYSTEMS AND DATA MANAGEMENT

Time: 3:00 Hrs.

Max. Marks: 70

Note: Attempt ANY FIVE questions.

All questions carry equal marks.

Assume suitable missing data, if any

1. [a] Define atomicity and durability of transactions (2)

[b] Consider the following two transactions:

T1: read(A);
read(B);
if A = 0 then B := B + 1;
write(B).

T2: read(B);
read(A);
if B = 0 then A := A + 1;
write(A).

Let the consistency requirement be $A = 0 \vee B = 0$, with $A = B = 0$ the initial values.

- Show that every serial execution involving these two transactions preserves the consistency of the database.
- Add **lock** and **unlock** instructions to transactions T1 and T2, so that they observe two-phase locking protocol. Can the execution of these transactions result in deadlock.

(4+8)

2. [a] Discuss validation based concurrency control protocol in detail. Whether there will be deadlocks in this protocol or not? Justify your answer. (8)

[b] What benefits does rigorous two-phase locking provide? How does it differ from other forms of two-phase locking? (6)

3. Differentiate between the following with the help of suitable example

- [a] Serial and Serializable schedules
- [b] Mutual exclusive participation and overlapping constraints
- [c] Composite and derived attribute
- [d] Clustering Index and Secondary index

(14)

4. [a] What is log based recovery mechanism? Explain the checkpoint mechanism.

[b] How will you recover the database system in case of concurrent transactions? (10+4)

5. Consider the following relational Schema

StaffContract(Emp_id, ContractNo, hours, EmployeeName, CompanyID, CompanyLocation).

The set of functional dependencies is given as:

Emp_id, ContractNo \rightarrow hours

Emp_id \rightarrow Employee Name

ContractNo \rightarrow CompanyId, CompanyLocation

- [a] Find a candidate key for the relational schema.

[b] Find if R is in 3NF or BCNF? If yes, justify else decompose the relation R to 3NF.

[c] Verify whether the resulting decomposition achieved in part [b] is lossless?

(2+6+6)

6. [a] Consider following relational schema

Customer(cust_id, name, date_of_birth, city, state)

Products(pid, pname, unit price, stock)

Purchase(custid, pid, date)

Write the following queries in SQL and relational algebra.

- i. Find the names of the customers who live in the same state and city.
- ii. Find the products which have been purchased by most of the customers.
- iii. Find the customers who have bought all the products.

(2+4+2)

[b] What are triggers? Why are they used? (2)

[c] Discuss two type of integrity constraints which may be imposed on database. (4)

7. Write short note on any four of the following

[a] Hashing

[b] RAID

[c] Collision Resolution Techniques

[d] Deadlock handling

[e] Mapping of ER model

[f] Functional dependency and Multivalued dependency (14)

Roll No..... No. of pages : 2

Date :

b0/c
B.E.(COE)

SIXTH SEMESTER

END SEMESTER EXAMINATION, MAY-2014

COE – 313: OPERATING SYSTEMS

Time: 3:00 Hrs.

Max Marks: 70

Note : Attempt any five questions. Assume suitable missing data, if any.

Q.1 (a) What are the various scheduling criteria's on the basis of which we find that which algorithm is the best? Draw the gantt charts and find out the average turn around time and average waiting time in the case of five processes with arrival time and burst time as given using FCFS, SJF, RR with quantum = 4 algorithms.

Process	Arrival time	Burst time
P1	0	24
P2	2	30
P3	4	5
P4	6	17
P5	8	10

[10]

[4]

Q.1 (b) Explain the various methods of hardware protection ?

Q.2 (a) What is deadlock? Explain with example the deadlock algorithms when we have

(i) Single instance of each resource type.

[10]

(ii) Several instances of each resource type.

Q.2 (b) Explain the difference between multiprogramming and time sharing systems? [4]

Q.3 (a) What are the various page replacement algorithms? Let the address sequence is given as follows

0104, 0100, 0432, 0101, 0612, 0102, 0103, 0104, 0611, 0102, 0103, 0104, 0610, 0502, 0303,

0609, 0105, 0402, 0503, 0607, 0416, 0705, 0204, 0308, 0509, 0206, 0409, 0307, 0206

(i) Find the reference string?

(ii) Find the number of page faults if we have 3 frames using at least any four algorithms?

[10]

Q. 3 (b) What are system calls? Classify the various types of system calls. [4]

Q.4 (a) Explain semaphores? What are the various types of semaphores? Explain reader's-writer's problem. Also write the algorithm for the processes using semaphores for solving reader's-writer's problem. [10]

Q.4 (b) What is inter-process communication? Give the various system calls used in IPC. [4]

Q.5 (a) Explain how disk management is done? Suppose that the disk drive have 2,000 cylinders, numbered 0 to 1999. The drive is currently serving a request at cylinder 168 and the previous request was at cylinder 125. The queue of pending requests in FIFO order is

86, 1470, 813, 1674, 948, 456, 1286, 1509, 1022, 1750, 130, 45, 219, 518.

Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for each of the following disk scheduling algorithms : SSTF, SCAN, LOOK, C-SCAN, C-LOOK. [10]

Q.5 (b) Explain the synchronization hardware for critical-section problem in brief. [4]

Q.6 (a) Explain paging and segmentation with the help of suitable diagrams. How is paging different from demand paging ? [10]

Q.6 (b) Explain the solaris threads? [4]

Q.7 Write short notes (any four) on the following. Write suitable examples?

(i) Context Switching

(ii) Goals and methods of protection

(iii) Schedulers

(iv) Cryptography

(v) Directory structures

(vi) Critical regions/sections

[14]

Roll No.

No of pages: 3

Date.....

END SEMESTER EXAMINATION, MAY 14

VI Sem B.E COE

COE-314 Control Engineering

Time: 3.00Hrs

MM-70

Note: 1. All questions carry equal marks.

2. Assume suitable missing data.

3. Attempt any five questions.

1. a) Discuss the advantages of feedback in control systems.

7

- b) A unity feedback system is characterized by the open loop transfer function

$$G(s) = \frac{1}{s(0.5s + 1)(0.2s + 1)}$$

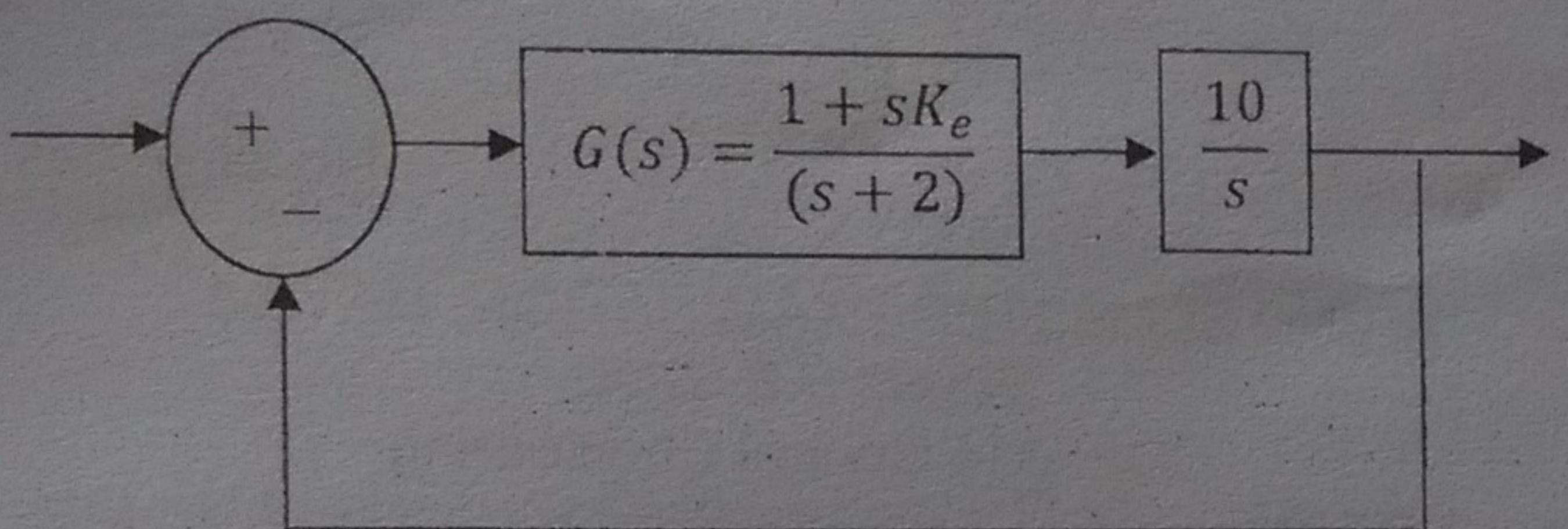
Determine the steady state errors for unit step, unit ramp and unit acceleration inputs. Also determine the damping ratio and natural frequency of the dominant roots.

7

2. a) Derive the expression for peak time and peak overshoot.

7

- b) Figure shows a system employing proportional plus error rate control. Determine the value of the error-rate factor K_e so that the damping ratio is 0.5. Determine the values of settling time, maximum overshoot and steady state error (for ramp input) with and without error rate control. Comment upon the effect of error rate control on system dynamics.



3. a) What is stability of a system? Define the terms asymptotic stability, conditional stability and relative stability. 7

- b) Determine the range of values of K ($K > 0$) such that the characteristic equation

$$s^3 + 3(k+1)s^2 + (7k+5)s + (4K+7) = 0$$

has roots more negative than $s=-1$. 7

4. Sketch the bode plot for the transfer function

$$G(s) = \frac{75(1 + 0.2s)}{s(s^2 + 16s + 100)}$$

Determine the gain crossover frequency, phase cross over frequency, gain margin and phase margin. 14

5. a) Discuss the frequency response specifications. 7

- b) By use of the Nyquist criterion, determine whether the closed loop system having the open-loop transfer function is stable or not. If not how many closed loop poles lie in the right half s-plane?

$$G(s) = \frac{1+4s}{s^2(1+s)(1-2s)}$$

6. a) Derive the transfer function of armature controlled dc motor. 7

- b) Explain gain margin and phase margin. 7

7. b) For the unity feedback system with

$$G(s) = \frac{K(s+2)(s+3)}{(s^2+2s+2)(s+4)(s+5)(s+6)}$$

Sketch the root locus plot. Also find the angles of departure from the complex poles. 14

8. Write short notes on any two:

- a) Signal flow graph
b) AC servomotor
c) Static error constants

7+7

**SIXTH SEMESTER - B.E. COMPUTER ENGINEERING
END SEMESTER EXAMINATION, MAY, 2014
COE- 315: ADVANCED COMPUTER ARCHITECTURE**

Time: 3 hours

Maximum marks: 70

1. Attempt any five questions.
2. All questions carry equal marks. The subparts of all questions carry 7 marks each.

Q1) (a) Attempt any one of the following Q. (a-1)or (a-2):

(a-1) Write a CREW program to implement merge sort on an array of the items: 21, 9, 19, 13, 1, 4, 2, 12, 38, 11, 14, 5, 16, 10, 7, 6. Show the output at each step. Calculate its complexity.

OR

(a-2) Draw the sorting network based on Bitonic Sort algorithm. Show the step-wise output for sorting the following list of unordered numbers on 4-cube network: 21, 9, 19, 13, 1, 4, 2, 12, 38, 11, 14, 5, 16, 10, 7, 6.

(b) Compare the S-access, C-access and combined access schemes for interleaved memory access. How can the memory space of a uni-processor be increased in a parallel architecture?

Q2) (a) Among RISC, VLIW, CISC and vector processing architectures, which of the following architectures will you choose to make a new processor, given the following requirements. Justify your choice by explaining the architectural features that support it.

- i. Tight budget constraint, low power dissipation required and a high degree of parallel operation needed.
- ii. A high performance DSP processor for high quality voice and image processing.

(b) Compare the static prediction, dynamic prediction, insertion of delay slots and speculative branch handling techniques in terms of (i) performance (ii) hardware requirements (iii) power dissipation.

Q3) (a) For the following reservation table of a pipeline processor, give the list of the forbidden latencies, the collision vector, the state diagram, the minimum average latency and all greedy cycles. Explain the procedure to optimize the MAL. Have you obtained the optimal MAL? If not, achieve it.

	1	2	3	4	5	6	7
S1	X			X			
S2		X					X
S3			X				
S4					X		
S5						X	

(b) Write a program using a shared memory IPC model to perform the following computation: There is a NXN matrix containing zeros and ones. The problem is to count the total number of ones in the four quadrants of the matrix separately. This will be done with the help of several processes that divide the work equally amongst themselves.

Q4) (a) Among MNS, tree, mesh, linear network, which of them would you choose for communication between processors and memory modules in the following applications? Evaluate your choice in terms of (i) performance (ii) communication overhead (iii) scalability (iv) cost.

- i. All processors need to send messages to each other in a fault tolerant manner such that even if a link breaks, an alternative route can be found.
- ii. All processors need to handle a routing table that stores the connectivity between 10^6 nodes and find the most suitable path between two nodes.
- (b) Compare the Write-through, Write-back and Write-Once (WEO) snoopy cache coherence protocols in terms of (i) Memory Traffic (ii) Traffic in the snoop bus (iii) Suitability for an application in which (i) all processors write equally but rarely and (ii) all of them read heavily.

- Q5) (a) Write the uni-processor performance equation. How do the following affect various terms of the processor performance equation: Instruction Set Architecture, Better Fabrication Technology, Compiler Optimization, and Instruction Pipelining.
- (b) Why do following optimization techniques increase available parallelism? List the limitation of each technique: (i) Software Pipelining (ii) Loop Unrolling (iii) Tiling.

Q6) (a) Attempt any two of the following three:

- I. List all the dependencies in the following code fragments. Indicate whether these are loop carried or not. Is the loop parallelizable?

```
for( i = 1; i < 100; i++ ){
    a[i] = b[i] + c[i];           /* S1 */
    b[i] = a[i] + d[i];           /* S2 */
    a[i+1] = a[i] + e[i];           /* S3 */
}
```

- II. Improve the following code:

```
for(i=1, i<=n, i++){
    a[i] = a[i] + C*i;
    b[i] = b[i] - C*x + sqrt(x);
}
```

- III. You have a vector processor that supports a stride of 128. How would you vectorize the following loop?

```
for(i=1, i<=n, i++){
    a[i] = a[i] + b[i];
}
```

- (b) Draw the structure of a 8×8 Baseline network. Show blocking characteristic of this network. Compare this network with a crossbar network in terms of switching and link complexity.

- Q7) (a) Write short notes on any two of the following topics. Give sub-topics for different parts.
- (i) The sequential, TSO and relaxed memory consistency models
 - (ii) Implementation of matrix multiplication on n^3 and n^2 processors
 - (iii) Special Instructions, pipeline, and applications of chaining in vector processors
 - (iv) Data forwarding, reservation stations and use of various buffers for dynamic performance optimization in processors.