End Semester Examination, May 2009

B.E. 6th Semester. EC/CoE/IC-311; Microprocessors

Maximum Marks: 70. Time: Three Hours. Assume any missing data. Question number 1 is compulsory. Attempt any four other questions.

Q1. (7 x 2 marks)

(a) Differentiate between (i) the instructions "RST0" and "JMP 0000" and (ii) the action of executing the "HLT" instruction and asserting the "HOLD" signal.

(b) Explain the function of READY signal with the help of a timing diagram.

(c) Right after an 8085 system is reset, the first instruction that is executed at address 0000 (hex) is "Push B". What are the contents of the Stack and the Stack Pointer after this instruction is executed? Justify your answer.

(d) If the Interrupt Response time of a system is defined as the elapsed time between the occurrence of an interrupt signal and execution of the corresponding interrupt subroutine, then what is the **worst case** interrupt response time for an 8085 system operating with a **2 MHz crystal**? Assume that all interrupts are enabled and that none of the interrupts is masked.

(e) Write a program segment with exactly 2 instructions that would call a subroutine at address ABCD(hex) only if the contents of Accumulator are less than or equal to 50(hex).

(f) List all the machine cycles that 8085 uses. Which is the longest machine cycle? Assume that the system operates without any wait states.

(g) List all the instructions of 8085 that can be used to read and write data to memory mapped I/O ports.

Q2. (2 x 7 marks)

(a) Design the memory interface logic to interface 32KByte EPROM and 32KByte SRAM to an 8085. IC1 is 27128 which is a 16KByte EPROM chip; IC2 is also 27128, while IC3 is 62256, which is a 32KByte SRAM chip. The EPROM chips are mapped to cover the lower half of the 64Kbyte address space while the SRAM is mapped to the upper half. Also, IC1 maps all even addresses and IC2 maps all odd addresses, i.e. addresses 0000, 0002, 0004, 0006 etc map to IC1 and addresses 0001, 0003, 0005 etc map to IC2.

6(b) Write initialization routine for the 8259 PIC configured as an I/O port with base address F0(hex), to set it up for operation with the following specifications: 8085 system, normal EOI mode, non-buffered environment and Fully Nested Mode. Call address interval to be 4 bytes. All IR pins except IR2 are masked. Assume that the call address for IR0 is 0F40(hex).

(b) For the question in part (a), design the memory interface such that the EPROM is accessed with no wait states while the SRAM access includes one wait state.

Q3. (2 x 7 marks)

(a) Draw a flowchart and write 8085 assembly code for a subroutine to generate a Pulse Width Modulated (PWM) signal on the SOD pin. The input parameter to the subroutine is the value of the desired duty cycle 'D'. The value of 'D' lies between 0 to 100% and corresponds to an 8 bit value between (and including) 0 to 255, is communicated to the subroutine by the calling program through the Accumulator. The 8085 system runs at 1 MHz clock signal and desired PWM frequency is 100 Hz.

(b) An I/O device generates 10 uS positive pulses that is used to interrupt an 8085 using RST7.5 interrupt input pin. Draw a flowchart and write an Interrupt Subroutine (ISR) which toggles the value of an output port on each interrupt. The port address is 40(hex). The reset value at the output of the port is 00(hex).

Q4. (2 x 7 marks)

(a) A set of 'n' bytes is stored in memory starting at address 2000(hex). The value of 'n' is stored at address 1FFF(hex). Draw a flowchart and write 8085 assembly subroutine labeled 'CHKSUM' to calculate the checksum of these 'n' bytes and store the result at memory address 1FFE(hex). The checksum is the two's complement of mod-256 sum of the 'n' bytes.

(b) Estimate the delay incurred by the 'CHKSUM' subroutine mentioned in part (a), as a function of the value of 'n'. The 8085 system operates at 2 MHz clock.

Q5. (2 x 7 marks)

(a) Explain the mode 1 operation of 8255 with the timing diagrams for the handshake signals as well as the control signals used by both the input port mode and output port mode.

(b) Explain the transmitter section of the 8251 USART chip, including the modem control signals, with a neat block diagram. Explain the purpose of the mode and command instruction bytes in asynchronous format.

Q6. (2 x 7 marks)

(a) Explain the function and purpose of OCW1, OCW2 and OCW3 for the 8259 PIC chip.

Q7. (2 x 7 marks)

Write short notes on any two topics:

(a) 8257 DMA controller configured as a memory mapped I/O port in slave mode.
(b) 8253 modes of operation.
(c) 8279 Keyboard and Display controller.
(d) 8255 operation in mode 2.