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Roll No. 499

SIXTH SEMESTER B.E. (ECE/COE/ICE)

B.E. END SEM. EXAMINATION, May 2012

EC/COE/IC-311: Microprocessors

Time: 3:00 Hrs. Max. Marks: 70

Note: Question 1 is compulsory. Attempt any five from the rest.

Q1. (5 x 4 marks each)

[a] How many types of machine cycles does 8085 have? Give an example each of an 8085 instruction that has

(i) Maximum number of machine cycles.
(ii) Maximum variety of machine cycles.

[b] If the HOLD signal and RST7.5 interrupt signal are asserted exactly at the same time, how does the 8085 system react? What happens to an 8085 system if a square wave signal of 1 KHz frequency is applied to the HOLD signal of the 8085?

[c] Assuming a 2 MHz crystal for an 8085 system, calculate the time delay generated by the following code snippet:

```
      MVI A, 0
      MVI B, 0
      MVI C, 0
LP1:  DCR A
      JNZ LP1
      DCR B
      JNZ LP1
      DCR C
      JNZ LP1
```

[d] Describe the impact of the following code on an 8085 system:

```
MVI A, C1(Hex)
SIM
```

[e] Write a program to shift a 16-bit number in register pair BC, 1 bit to the left.

Q2. (2 x 5 marks)

[a] Draw a schematic diagram of an output port using 74LS373 at a memory mapped address of 8000(hex) for an 8085 system.

[b] Write an 8085 assembler program to transmit serial data using 9600, 8, N, 1 format on the SOD line of the 8085. The 8085 system operates at 2 MHz crystal.

Q3. (2 x 5 marks)

[a] Explain the operation of the Ready signal of 8085. Draw a circuit to add 2 wait states in every machine cycle of the 8085.

[b] A '1' pulse of 1 mS duration is to be applied to the RST6.5 interrupt pin. The associated ISR lasts 200 uS only. How to ensure that the ISR is executed only once per pulse? Describe a suitable hardware scheme.

Q4. (2 x 5 marks)

[a] An 8251 USART is operated in an asynchronous mode. It offers two types of control words: Mode instruction and command. Describe the bit configurations for the mode instruction and command byte.

[b] How many DMA channels does 8257 DMAC offer? What is the maximum number of bytes that can be transferred using 8257 through a single DMA request by the 8257 to 8085? Explain the function of the AEN signal of 8257.

Q5. (2 x 5 marks)

[a] Write command words to initialize an 8279 which is located at a base address of 20(hex), with the following requirements:

- 16, 8-bit display with left entry
- Encoded scan keyboard with 2-key lockout
- 100 KHz scan clock for 1Mhz input clock signal

[b] An 8254 PIT is to be used in an 8085 system with a 1 MHz system clock. Write 8085 program to initialize the 8254 in an appropriate mode such that the 8254 can interrupt the 8085 using RTS7.5 interrupt exactly after 10 seconds after the 8254 is programmed.

Q6. (2 x 5 marks)

[a] Using 8255 PPI with a base address of B0(hex), interface a single 7-segment display to the PortC of the PPI chip and write a program to count 0 to 9 on the display with a delay of 1 second between each number change.

[b] With the help of suitable timing diagram, explain the operation of PortA as input in mode 1.

Q7. (2 x 5 marks)

Write short notes on any two of the following:

[a] ICWs and OCWs of 8259 PIC

[b] Interrupt structure of 8085

[c] Multiplexed 7-segment display using 8279.

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