(96)

16/5/2016 (AN)

VI Sem

No. of Pages: 2 Roll No: .....

SIXTH SEMESTER **B.E. (ECE/COE/ICE)**

B.E. END SEM. EXAMINATION, May-2016

ECE/COE/ICE-311: Microprocessors

Time: 3:00 Hrs. Max. Marks: 70

Note: Attempt **FIVE** questions in all. Assume any missing data. Question 1 is compulsory.

1.

(a) How and when does 8085 decide how many bytes to be fetched from memory to execute an instruction?

(b) Reset all the 8085 flags using only data transfer instructions.

(c) Differentiate between RST6 and RST6.5.

(d) What are the advantages of the register-addressing mode over the register-indirect addressing mode?

(e) Write a small 8085 assembly program to illustrate indirect jump capability of 8085.

(f) Differentiate between XCHG and XTHL instructions.

(g) List all the 8085 instructions that have 6 T-states for the opcode fetch machine cycle.

[7*2]

2. (a) Write a program to decompose a list of fifty numbers stored in the memory starting at the location 2001H into a list of odd numbers and a list of even numbers. The list of odd numbers is to be stored in the memory starting at the location 2101H and the list of even numbers is to be stored in the memory starting at the location 2151H. The number of odd numbers and the number of even numbers should be stored in the memory locations 2100H and 2150H, respectively.

(b) Write a program to sort the numbers stored in the memory locations 2001H to 2050H using a suitable sort algorithm. [7+7]

3. (a) A sorted list of fifty numbers is stored in the memory starting at the location 2001H. Write a program to search for the number stored in the memory location 2000H in the list using the binary search algorithm. If the number is found, then store the index in the memory location 2100H. Otherwise, clear the memory location 2100H.

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Sixth Semester

BE(COE)

END SEMESTER EXAMINATION, May-2016
COE 312: Information Systems and Database Management

Note: Question no. 1 is compulsory
Attempt any four questions from the remaining questions.
Assume missing data, suitably, if any.

Q1. Define the following terms
a) Relational model and hierarchical
b) Entity and entity set
c) Integrity constraints
d) DBA
e) Generalisation
f) Views

(7X2=14)

Q2. Consider the following schema
Salesperson(salesman_no, sname, commission)
Sales(date, customer-no., salesman_no, product_id, qty)
Product(product_id, description)
Customer(customer_no., cname, address)

a) Write the following queries using SQL and Relational algebra

(i) Find the names of all the salesmen who sold 50 products in Jan. 2016.
(ii) Find the names of those customers who bought table lamps in addition to other products.
(iii) Find the names of sales persons who sold all the products
(iv) Find the salesmen who have sold maximum number of different products.
(v) Arrange the salespersons in increasing order of their commission (10)

b) Define triggers. Write a trigger for above mentioned schema. (4)

Q3a. Consider a relational schema R(A,B,C,D,E) and following set of functional dependencies
F = { A→BC, CD→E, B→D, E→A, B→E)
i) Find candidate key for R
ii Decompose R into 3NF
iii Verify if the decomposition is lossless join and dependency preserving decomposition? Justify your answer. (2+4+4)

b) What are different database security measures which can be taken? (4)

Q4a. Differentiate between cascade-less and recoverable schedules. (4)
b) What are various states of transaction? (3)
c) What are locks? Explain three concurrency control protocols which use locks, in detail. (7)

(1)

(104)

Q5a. What is an index? (2)

b. Differentiate between following kind of indexes?
   i) Dense and sparse index
   ii) Ordered and Hash index (6)

c. Discuss B+ trees in detail. (6)

Q6a. What are the symbols used for ER model? Draw an extended ER model for a Book Shop. (7)

b. Explain different recovery mechanism which can be used for recovery from failure? Give suitable examples. (7)

Q7. Write short notes on any four
   a) ACID properties
   b) Serializability
   c) Hashing
   d) Multivalued dependency with example
   e) Fixed and variable length records with example

(3.5X4=14)

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SIXTH SEMESTER **B.E. (COE)**

B.E. END SEM. EXAMINATION, May-2016

COE-313: Operating Systems

Time: 3:00 Hrs. Max. Marks: 70

Note: Attempt **ANY FIVE** questions. Assume any missing data.

1. (a) Why is the concept of process so important to an operating system? Describe the lifecycle of a process.

(b) A system has six processes as follows.

Process	Arrival time (ms)	CPU burst time (ms)
P1	0	90
P2	4	8
P3	8	50
P4	28	70
P5	30	60
P6	32	20

Calculate the average waiting time for the processes if round robin scheduling is used with a time quantum of (*i*) 80 ms, (*ii*) 20 ms and (*iii*) 10 ms. **[7+7]**

2. (a) What are the required properties of a solution of the critical section problem? Show that the Peterson's solution satisfies these conditions.

(b) Solve the dining philosophers problem using (*i*) semaphores or (*ii*) a monitor. **[7+7]**

3. (a) What is a **deadlock?** What are the necessary conditions for a deadlock to occur? Describe the different deadlock handling techniques.

(b) Use a suitable **deadlock detection** algorithm to check if there is a deadlock in a system where Available = [2 1 2 3 1], Allocation = $\begin{bmatrix} 2&3&1&3&3 \\ 1&2&2&1&1 \\ 2&3&2&2&2 \\ 1&2&1&2&2 \\ 1&2&3&1&1 \end{bmatrix}$ and Request = $\begin{bmatrix} 1&0&1&0&0 \\ 1&1&0&0&0 \\ 0&0&0&0&1 \\ 1&1&0&1&0 \\ 1&1&1&1&0 \end{bmatrix}$.

[7+7]

4. (a) A system has 64KB RAM and uses contiguous memory allocation. The sizes of the operating system and the user processes are as follows.

Process	Size (KB)
Operating system	32
P1	7
P2	7
P3	7
P4	6
P5	7
P6	5

The following sequence of events occurs in the system: the operating system is loaded, P1 arrives, P2 arrives, P3 arrives, P2 terminates, P4 arrives, P5 arrives and P6 arrives. Determine if all the processes can be allocated space in the memory following (*i*) first-fit, (*ii*) best-fit and (*iii*) worst-fit strategies.

(b) What is paging? Why page size is always a power of 2. Explain with a suitable example. describe the different ways of implementing page tables? **[7+7]**

5. (a) What is a page fault? How does an operating system handle a page fault? How can a system end up in a situation where it spends more time servicing page faults than doing computation?

(b) Calculate the number of page faults that will occur for a process for the reference string 0, 1, 2, 0, 1, 3, 4, 1, 4, 1, 5, 2, 3, 2, 5, 6, if the least frequently used page replacement algorithm is used and the process is allocated (*i*) 3 frames, (*ii*) 4 frames and (*iii*) 5 frames. If two pages have been referenced the same number of times, then the one which was loaded in the memory first should be selected for replacement. **[7+7]**

6. (a) Write notes on (*i*) different levels of a file system, (*ii*) kernel i/o subsystem and (*iii*) access control matrix and its implementations.

(b) A hard disk has 1000 cylinders. The read/write head is now at cylinder 615 and moving outwards. The disk queue has requests to access cylinders 14, 918, 680, 183, 788 and 144. Calculate the number of cylinders that the read/write head will have to traverse to

serve these requests if (*i*) FCFS, (*ii*) SSTF, (*iii*) SCAN and (*iv*) LOOK scheduling algorithms are used. **[7+7]**

7. Differentiate between **(any four)** –

(a) Kernel and microkernel

(b) Single-threaded process and multi-threaded process

(c) Safety algorithm and resource-request algorithm

(d) Logical address space and physical address space

(e) Logical file system and basic file system

(f) Seek time and rotational latency

(g) Virus and Trojan horse **[4x3.5]**

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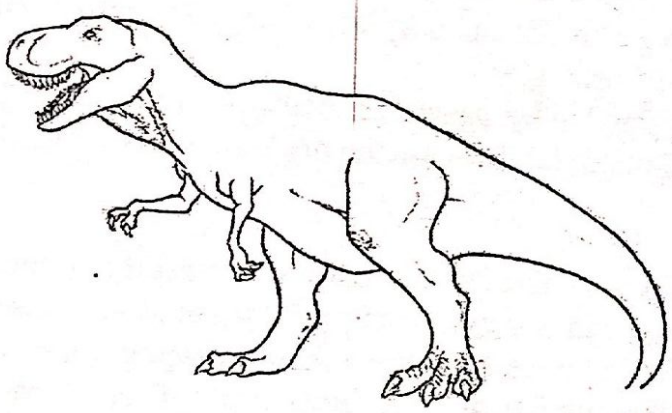

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SIXTH SEMESTER **B.E. (COE)**

B.E. END SEM. EXAMINATION, MAY-2016

COE – 314: Control Engineering

Time: 3:00 Hrs. Max. Marks: 70

Note: Answer any *FIVE* questions.
Assume any suitable missing data, if any.

1. [a] Define transfer function of a system. What are the features and advantages of the transfer function? What are the disadvantages of transfer function? [2]

[b] Derive mathematical model of armature controlled d.c. servomotor. Drive the transfer function and draw the block diagram of it. [6]

[c] Derive mathematical model of field controlled d.c. servomotor. Drive the transfer function and draw the block diagram of it. [6]

2. [a] The equations that describes the automatic control system are [7]

$$x_2 = x_1 t_{12} - x_2 t_{22} - x_4 t_{42} - x_5 t_{52}$$
$$x_3 = x_2 t_{23} - x_3 t_{33} - x_4 t_{43}$$
$$x_4 = x_2 t_{24} + x_3 t_{34} - x_4 t_{44}$$
$$x_5 = x_4 t_{45}$$

a. Plot the Signal Flow graph of the system.

b. Compute the transfer function $G(s) = X_5(s)/X_1(s)$ of the system by applying Mason's gain formula.

[b] A closed-loop system is used to track the sun to obtain maximum power from a photovoltaic array. The tracking system have $H(s) = 1$ and $G(s) = \dfrac{100}{(\tau s + 1)}$ where $\tau = 4$ seconds nominally, (a) Calculate the sensitivity of this system for a small change in τ. (b) Calculate the time constant of the closed-loop system response. [7]

3. [a] In a case of simple industrial control system, $G(s) = \dfrac{K}{(s+a)}$. [7]

i. If step input is applied and the output reaches 50% of its final value in 1 sec, find "a".

ii. If K=10 and "a" is same as obtained in part (i), find impulse response.

[b] Input to unity feedback control system is $r(t) = (3 + 5t + t^2)$. Here $G(s) = \dfrac{1}{s(s+4)}$. Determine various generalized error coefficients and steady-state error. [7]

4. [a] Determine the maximum value of magnitude M_r (resonant peak), resonant frequency (ω_r) and bandwidth for a second order system whose transfer function is given by

$$G(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

Also, drive the relationship between damping ratio and phase margin for the above 2nd order system. [10]

[b] The open loop transfer function of a unity feedback control system is given by $G(s) = \dfrac{K}{s(1+st)}$. By what factor the amplifier gain K should be multiplied so that the damping ratio is increased from 0.2 to 0.8? [4]

5. [a] Draw the Nyquist plot and assess the stability of the closed loop system whose transfer function is [10]

$$G(s)H(s) = \frac{(6s+1)}{s^2(s+1)(3s+1)}$$

[b] Calculate the offset to a step set-point change due to P-only control, for the following process $G_p(s) = \dfrac{1}{s(2s+1)}$. Explain the result. [4]

6. Sketch the root locus for the system whose transfer function [14]

$$G(s)H(s) = \frac{K}{s(s+2)(s+4)}.$$

Also, (i) determine gain K when M_p=16.3%. (ii) determine the settling time t_s and peak time t_p using gain value obtain in (i).

7. Consider the system shown in the Fig. 1. Design a suitable compensator such that the closed loop system will have a phase margin of 50°, a gain margin not less than 10dB and a gain crossover frequency of 1 rad/sec. [14]

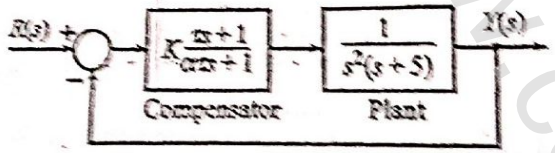

Fig. 1. Feedback system

8. Write short note on any two. [7+7]

i. magnetic amplifiers
ii. Gyroscope
iii. Regenerative feedback loop
iv. Constant M and N loci

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B.E. (COE) 6th Semester END SEMESTER EXAMINATION, May 2016

COE- 315 Advanced Computer Architecture

Time: 3 Hrs. Max. Marks: 70

Note: Attempt any 5 questions. Attempt all parts of each question together. Assume suitable missing data, if any and specify it clearly.

Question 1: [4 + 4 + 6 = 14]

(a) Suppose we have a simple 100 MHz processor that executes one instruction at a time (no pipelining). Memory access instructions (loads and stores) take 3 cycles to complete, while all other instructions take 1 cycle to complete (assume no stall). If our processor executes 10^8 instructions in a program in 1.5 seconds, what fraction of the instructions accessed memory?

(b) Write the Bitonic Sort algorithm for 4-cube Hypercube interconnection network. Show the step-wise output for sorting the following list of unordered numbers on 4-cube network: 21, 9, 19, 13, 1, 4, 2, 12, 38, 11, 14, 5, 16, 10, 7, 6.

(c) Write the assembly language code (using **load, add, addi, store, bne** instructions) for following C program fragment for which variable i is assigned to reg0 and is already initialized to 0 (zero), constant 10 is in reg1, base address of array A is in reg2, base address of array B is in reg3 and reg4 is initialized to point to last array element index. Arrays A and B contains 4-byte integer type elements. reg5 to reg9 are available for temporary result storage. Indicate the true data dependencies in the code.

```
do {
    A[i] = B[i] + 10 ;
    i = i + 1 ;
} while ( i < 100)
```

Question 2: [2 + 3 + 3 + 6 = 14]

(a) Scalar pipelines can't have WAW/WAR hazards. Justify or refute.

(b) A program performs 90% of its work (measured as processor-seconds) in the parallel portion and 10% of its work in this serial portion. The parallel portion is perfectly parallelizable. What is the maximum speedup of the program if the multicore processor had an infinite number of cores? How many processors would be required to attain a speedup of 4?

(c) Optimize the following code by reducing the number of memory accesses to A[] and C[] arrays. Assume A[], B[], and C[] are integer arrays.

```
for (i=0;i<N;i++)
    for (j=0;j<M;j++)
        A[i] += B[j][j] * C[i];
```

(d) A pipelined processor has a clock rate of 1.25 GHz. It is used to run a program in which branches constitute 20% of the dynamic instruction count and 80% of all the branches are taken. The customer who runs the program requires that the processor must deliver a throughput of 1 million instructions per millisecond. The processor uses a 2-bit branch predictor with a branch target buffer (BTB) accessed in the IF stage of the pipeline. Branches which are incorrectly predicted, there is a penalty of 2 cycles. Calculate the minimum branch prediction accuracy required to satisfy the throughput demand.

Question 3: [2 + 2 + 2 + 8 = 14]

(a) Give 2 reasons why don't processor designers design processors with massive register files (e.g. thousands of registers).

(136)

(b) Which optimization can be done by a compiler in the following code segment so that none of the three instructions get blocked in ISSUE stage, when these are executed under Scoreboard control?

I1: LOAD t2, 0(t3); I2: ADD t2, t0, t2; I3: MUL t8, t2, t0

(c) Write a branch outcome sequence which will be always mispredicted by a 2-bit Bimodal Branch Predictor initialized to Strongly NotTaken state.

(d) Write the various steps of Batcher's Odd-Even Merge algorithm. Show the stage-wise structure of a 4 x 4 Odd-Even Merge Network. Draw the complete structure of a Sorting Network based upon Batcher's Odd-Even Merge algorithm that sorts the following random sequence in increasing order: 23, 2, 14, 24, 9, 5, 10, 1.

Question 4: **[2 + 4 + 4 + 4 = 14]**

(a) Name a hardware technique and a software approach to reduce the stalls due to RAW dependency.

(b) Write the Processor time equation used to compute time needed to execute a program? How do the following techniques affect its various parameters: CISC/RISC ISA, Pipelining, Compiler Optimizations, Multi-level Memory, incorporating a Branch Predictor in a processor, and making a scalar processor superscalar?

(c) Explain the Subscript Partitioning Algorithm to partition the subscripts into separable and minimal coupled groups.

(d) Three processors P1, P2, P3 with their individual caches are connected via a bus with a shared memory. In the initial state memory location x has the value 3 and the caches are empty. Given is the following sequence of operations:

1. P1 reads location x.
2. P2 writes 8 into location x.
3. P3 reads location x.
4. P1 reads location x.
5. P2 writes 9 into location x.

Fill the following table entries after each of the above mentioned steps if basic write-back write invalidate cache coherence protocol is used.

Step No.	State of P1 cache	Content of x in P1 cache	State of P2 cache	Content of x in P2 cache	State of P3 cache	Content of x in P3 cache	Content of memory location x

Question 5: **[2 + 2 + 2 + 4 + 4 = 14]**

(a) To design a multiprocessor system, 1024 processors are required to be connected, and we are considering three different network topologies: Bus, Point-to-Point, and Mesh. Describe one disadvantage of each. Which one would you choose? Why?

(b) Which of the following versions will require more cycles per iteration? Give justification.

Version - 1

```
for (i = 0; i < n; i++)
    x = y * a[i];
```

Version - 2

```
for (i = 0; i < n; i++)
    x = x * a[i];
```

(c) Is the following loop vectorizable? If yes, justify. If not, can you perform some modification to make it vectorizable?

```
for (i = 0; i < 256; i++) {
        a[i] = b[i] + c[i];
        b[i+1] = e[i] - g[i];
        }
```

(137)

(d) Design a processor time optimal algorithm to find the maximum of N numbers on an EREW-PRAM model. Assume that initially each location holds one input value.

(e) If n is very large, name one optimization which can be applied to above code segment to improve the cache hit rate. Show the code after applying the optimization.

```
for( i=1; i<n-1; i++ )
    for( j=1; j<n-1; j++ )
        temp[i][j] = A[i-1][j] + A[i+1][j] + A[i][j-1] + A[i][j-1];
```

[4 + 4 + 6 = 14]

Question 6:

(a) A three-stage Omega Network connects eight processors numbered P0, P1, ... P7 to eight independent memory modules numbered M0, M1, ... M7. Draw the network. Highlight the following connections through the network: P0 → M2, P4 → M4, P6 → M3. Can these accesses be performed concurrently or do they conflict?

(b) Explain the Goodman's Write Once cache coherence protocol.

(c) Draw the fine gain program graph for computing sum of all elements of resultant matrix C obtained by matrix multiplication of two 2x2 matrices A and B. Draw a sequential schedule and 8-processor parallel schedule for the above program flow graph if a multiplication node has a grain size of 101 CPU cycles, addition node has a grain size of 8 CPU cycles and inter-node communication delay is 8 CPU cycles.

[3.5 x 4 = 14

Question 7:

Write short note on all of the following by taking suitable example:

(a) Loop Skewing
(b) Loop Peeling
(c) Loop Splitting
(d) Node Splitting Vectorization Technique

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... target buffer (BT
...ly predicted, there is a penalty
accuracy required to satisfy the through

[2 + 2 + 2 + 8 =

...easons why don't processor designers design processors with massive register files thousands of registers).

Anil Sahi
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