Total No. of pages:

Roll No. 515/IC/10

MID SEMESTER THEORY EXAMINATION (March 2013)

SIXTH SEMESTER

BE (ECE / ICE / COE)

EC [redacted] / ICE -311: MICROPROCESSORS

Time: 90 minutes

Max. Marks; 20

Note: Attempt all questions.

1 a) Explain the function of Program counter and Stack pointer in 8085. What is the reset value of these counters? [2]

b) How many memory mapped I/O ports can 8085 address? [2]

c) Give the number of bytes, number of machine cycles, T-states of the instruction XTHL. [2]

d) Draw a simple circuit to decode three controls signals RD, WR, IO/$\overline{M}$ and to produce separate read/write control signal for memory and I/O device. [1]

e) Draw the timing diagram of DAD instruction. [2]

f) Write 8085 assembly program to copy data from an array of 512 bytes starting from memory location 2000H to another array starting at memory location 3000H and estimate the time taken to transfer the data. [3]

2. Connect a switch to the SID pin and an LED to the SOD pin. Using a 555 based astable multivibrator generating a rectangular waveform of 1KHz to interrupt the 8085 using RST7.5 interrupt and a suitable ISR, reproduce the state of the switch onto the LED; if the switch is pressed, the LED should be turned on and if the switch is not pressed, the LED is turned off. Assume that the all the general purpose registers would be used in the main program and their values should not be disturbed. [4]

3. The memory space of an 8085A microprocessor system consists of one 8K by 8-bit EPROM starting from the memory location 0000H and two 2K by 4-bit RAM chips from the memory location 4000H and a memory mapped output port at address F000H, design the decoding circuit to generate chip selects for the above chips. [4]

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Total No. of pages: 1
SIXTH SEMESTER

Roll No. _____
BE (COE)

MIDSEMESTER EXAMINATION, March 2013
COE 312 –Information Systems and Data Management

Time: 1Hr 30 min
Note: Attempt all questions
Assume missing data suitably, if any.

Max Marks: 20

Q1. Consider following relational schema

BOOK_ROYALTY (ISBN, BOOK_TITLE, EDITION, PUBLISHER, AUTHOR_ID, AUTHOR_LASTNAME, ROYALTY)

Primary Key (ISBN, AUTHOR_ID)

Other Functional Dependencies are given as
(ISBN→ BOOK_TITLE, PUBLISHER, EDITION),
(AUTHOR_ID → AUTHOR_LASTNAME),
(BOOK_TITLE→ PUBLISHER)

Is the above relational schema in 3NF? If yes, justify your answer? If no, illustrate the reduction of the schema to 3 NF. (4)

Q2. Consider following relational schema for Public Library data base systems

BOOK (ISBN, BOOK_TITLE, BOOK_YEAR)
LIBRARY_DETAIL (BOOK_NUM, ISBN, DATE_ENTRY)
MEMBERSHIP (MEM_NUM, MEM_NAME, MEM_HOUSE#, MEM_CITY, MEM_PHONE, MEM_BALANCE)
RENTAL (RENT_NUM, MEM_NUM, RENT_DATE)
DETAILRENTAL (RENT_NUM, BOOK_NUM, DATE_DUE, DATE_RETURN, FINE)
**A book may be rented for 15 days. i.e. DUE_DATE =RENT_DATE+15.
If the books are not returned on or before DUE_DATE, late fee of Rs. 50/day will be charged.

a) Write the following queries in SQL and Relational Algebra:
   i) Find the total number of copies of each book.
   ii) Find the members who have rented more than ten books after May 2010.

b) Illustrate the concept of LEFT OUTER JOIN using above relational schema. (4+2)

Q3. Differentiate between the following using suitable examples:

a) Mutual Exclusion and Overlapping constraints
b) Primary Key and Superkey, and candidate key (6)

Q4. Discuss various levels of database abstraction. Define materialized views? (4)

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Roll No. 308/co/10

MID SEMESTER THEORY EXAMINATION (March 2013)

VI Sem.

B.E.(COE)

COE-313: OPERATING SYSTEMS

Time: 1:30 Hrs.

Max. Marks: 20

Note: *Attempt all questions. Assume missing data suitably, if any.*

Q1. In a multiprogramming system, an I/O-bound activity is given higher priority than non-I/O-bound activities. However, in real time applications an I/O-bound activity will be given a lower priority. Why is this so? Explain. 4

Q2. OUR-OS has a unique feature: it has distinct resource allocation phase. OUR-OS enters in this phase, whenever OUR-OS creates a new process, deletes a process or receives a request for a new resource. During this phase it also collects any resources, which the processes are ready to release. For each process OUR-OS maintains a list with the processes maximum demand for each resource. This list is maintained in the time order in which the processes need their resources. If a process cannot run for lack of some resource, its resource denial count (rdc), is raised by 1. During each allocation phase, processes with higher rdc get preference for allocation. When a process reaches a rdc of some value, say 20, then all processes with minimum rdc in contention are required to relinquish resources held by them and their rdc is given at current minimum value prevailing. Write a critique on this resource management policy. Can this policy result in deadlock? Can there be starvation? Explain. 6

Q3. In a real computer system, neither the resources available nor the demand of processes for resources are consistent over long period (months). Resources break or are replaced, new processes come and go, new resources bought and added to the system. If deadlock is controlled by the Banker's algorithm, which of the following changes can be made safely without introducing the possibility of deadlock and under what circumstances? (italicized variables have usual meaning) 5

a. Increase *Available*
b. Decrease *Available*
c. Increase *Max* for one process
d. decrease *Max* for one process
e. Increase number of processes

5

Q4. Discuss historical developments of Operating Systems.

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M. Marks - 20

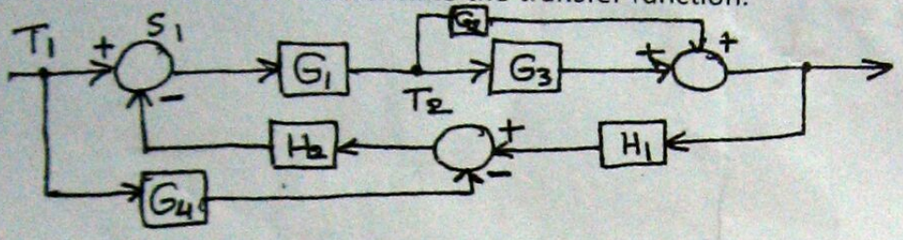
MID SEM . EXAMINATION (MARCH-20130)

Sixth Sem. COE

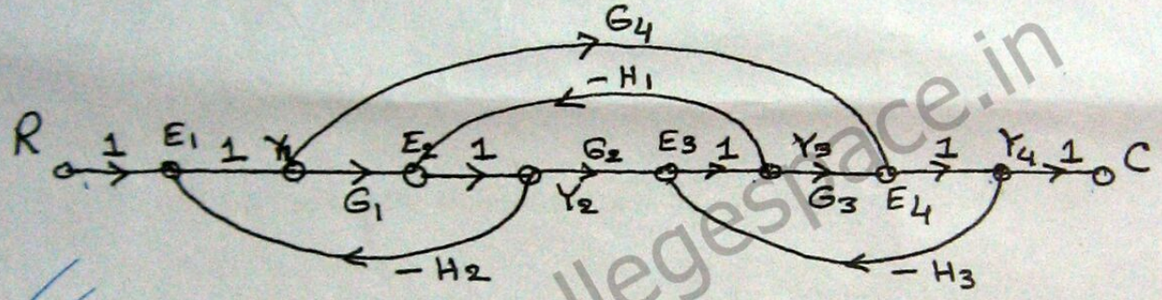
COE -314 (Control Engg.)

Note:- Attempt all the Questions. Assume Suitable missing data, if any

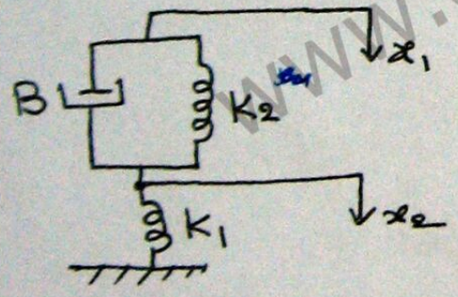
Q1. Reduce the block and determine the transfer function. (5)



Q2. Use Mason's gain formula to find the transfer function of the control system shown in Fig. below.(5)



Q3. A) Draw the electrical analogous circuit (use F-V) analogy and derive the transfer function. (2)



b) Discus armature controlled d.c. servo motor in details (3)

Q-4 a) Define and derive peak time, rise time and settling time in the step response of a second order control system. (2)

b) A second order system has a transfer function given by $G(s)= \frac{25}{s^2+8s+25}$

if system initially at rest is subjected to a unit step input at t=0, the second peak in the response will occur at (a) π Sec. (b) $\pi/3$ sec. (c) $2\pi/3$ sec (d) $\pi/2$ sec (2)

c) How the feedback affects the dynamics of a control system (1)

Total No. of Pages: 1 Roll No:.....

B.E. (COE) 6th Semester MID SEMESTER EXAMINATION, March 2013

COE- 315 (Section –II) Advanced Computer Architecture

Time: 1½ Hrs. **Max. Marks: 20**

NOTE: Attempt the questions IN ORDER only. Assume suitable missing data (if any) and specify it clearly.

ONLY FOR SECTION – II STUDENTS

A load/store ISA based processor's data-path can be divided into 5 stages. Latencies for the individual stages are: Stage 1 - 200 ps, Stage 2 - 150 ps, Stage 3 - 150 ps, Stage 4 - 400 ps, Stage 5 - 100 ps (ps represents picoseconds). Operations performed in various stages are:

Stage 1 - Instruction Fetch

Stage 2 - Instruction Decode, Processor Register read, Computes Target Address for unconditional jump instruction

Stage 3 – ALU operation in ALU type instruction, Computes Target Address for conditional branch instruction and outcome of these conditional branches get resolved, Computes Data Memory Address for load/store instructions

Stage 4 – Access (read/write) Data Memory **Stage 5** - Writes into Processor Register (wherever required)

Assume that clock cycles for each stage will be consumed irrespective of type of instruction (i.e. if some stage is not needed in some type of instruction, its allotted clock cycle will still be used to by-pass this stage)

Q. 1) What is the clock cycle time in a non-pipelined and pipelined implementation version of this processor? Compute the speed up obtained (if any) because of pipelining. If we can split one stage of the pipelined data-path into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the pipelined processor? [3]

Q. 2) For the above processor, write the assembly language code (using **load, add, addi, store, bne** instructions) for following C program fragment for which variable i is assigned to reg0 and is already initialized to 0 (zero), constant 10 is in reg1, base address of array A is in reg2, base address of array B is in reg3 and reg4 is initialized to point to last array element index. Arrays A and B contains 4-byte integer type elements. reg5 to reg9 are available for temporary result storage. Indicate the true data dependencies in the code. [3]

```
do {
    A[i] = B[i] + 10 ;
    i = i – 1 ;
} while ( i < 100)
```

Q. 3) Say data forwarding is implemented to remove/reduce stalls wherever possible (information if available inside processor can be used at the place where it is needed in next cycle). Show the set of instructions of Q.3 where pipeline stall will occur and how many. Re-order the instruction sequence of Q. 3 to remove (if possible) any pipeline stalls that occur. How much reduction is possible in clock cycles required between your re-ordered instruction sequence and the original sequence? [3]

Q. 4) For the processor under consideration, compute the stall cycles for conditional and unconditional branch instruction. (*Note that, here, we do not have any separate CC set instruction. So, class discussion will not be straight forward applicable. Please read the processor specification carefully.)* [3]

Q. 5) Compute the average number of stall cycles because of conditional branch instructions for the case when we always statically "**predict target**". Say, 80% of the conditional branches always go to target. [3]

Q. 6) [1+1+1+2 = 5]

A) Give 2 reasons why don't we build processors with massive register files (e.g. thousands of registers).

B) What is the effect of making a scalar processor superscalar on CPI and Clock Cycle time? Explain Briefly.

C) Scalar pipelines can't have WAW/WAR hazards. Justify or refute.

D) Write a loop in C language which contains a branch that will be completely mis-predicted by a one-bit branch prediction scheme.

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Roll No. 251010

MID SEMESTER THEORY EXAMINATION, MARCH 2013

V1 SEMESTER, B.E. COE, SECTION I

COE 315 ADVANCED COMPUTER ARCHITECTURE

Time 1.5 Hrs

Max Marks: 20

Instructions:
Assume missing data

Question) A set of space probes capture multiple images of the universe in 360^0 with the objective of identifying remote galaxies and **one unique galaxy** that is collapsing into a black hole. Each image can be represented as a matrix of size 1K X 1K **blocks,** (where M $= 2^{20}$) where a block is a fragment of an image that can store one object.
There are 1024 such images that are captured and must be analyzed in real time.
There are two objects of interest to scientists:
(1) Total number of remote galaxies. These objects can be recognized by a known remote-galaxy recognition algorithm A1. The total number of these remote galaxies must be recorded.
(2) The location of the unique galaxy. There is another object recognition program A2 to recognize this unique object which is being searched for.

Suggest a parallel architecture to solve the above two problems in real time. Write your answer in the following steps:

a) Decide how you will decompose the huge amount of data taking into account that each image is large and there are many such images.
b) Describe the parallel architecture which is suitable to solve the problems with the granularity obtained by the data decomposition in step 1a. State the number of processors, their static and/or dynamic networked interconnections (you may use more than one type of network). Justify your choices on the basis of the way you have decomposed the data.
c) Compare the performance of this proposed architecture with a bus based UMA MIMD architecture to perform the same task.
d) Using your proposed architecture, devise a set of parallel algorithms to implement **any one** the above two tasks. In each algorithm, highlight the data dependencies, the modes of operation and communication model (shared memory/message passing).
e) Assess the performance of the parallel computer system w.r.t to single processor.

4x5 =20