Total No. of Pages: 3

69/C

Roll No.:

FIFTH SEMESTER - B.E. COMPUTER ENGINEERING
END SEMESTER EXAMINIATION, DEC, 2013
COE- 303: COMPUTER SYSTEM ORGANIZATION

Time: 3 hours
Maximum marks: 70

Instructions:

1. All questions carry equal marks = 14.
2. There are five questions. ANSWER ALL FIVE QUESTIONS.
3. Each question two choices. You can choose any one of them. Answer all parts of your choice (DON'T MIX subparts of different choices).
4. Number the answers correctly to match their corresponding question number.
5. Assume missing data.

Good Luck!

Q1) An 8-bit processor fetches 40 Kilobytes of data from memory and transmits it over an **asynchronous** transmission line through a modem in the form of a frame using **Bit Oriented** protocol.

- The memory access time is 50 ns.
- The transmission speed is 640 kbps.
- The frame is composed in the following manner:- First there is a Flag 01111110. This is followed by a 32-bit address. Next the data is inserted. This is followed by a 16-bit CRC. Finally the Flag 01111110 is appended.
- One start bit and 1 stop bit is inserted automatically by the modem for every byte that is transmitted. Bit stuffing is employed.
- There are 30 instances when the data contains five consecutive ones.
- The three instructions in the main loop to access data are (ignore loop overhead instructions)

  Load (I) X : A three-byte instruction that Loads indirect X to accumulator.

  OUT PortM: A 2-byte instruction that outputs contents of accumulator to the I/O port address of the modem.

  INC X: A three-byte instruction that reads location X, increments its contents and then stores it back.

Calculate the following, giving step wise analysis:

a) The number of memory accesses for fetching and executing each instruction in the main loop.
b) The total memory access time given for executing the loop repetitively for transferring 40 KB of data.
c) How many bits are transmitted in total after the modem inserts start-stop bits?
d) What is the total time for the frame's transmission?
e) What is the total time for transferring the data from memory to remote destination if the propagation delay of the transmission line is 0.5 millisec.

OR

Q1Alt) Trace the execution of the program given below. In each step, give the contents of the accumulator, PC, C,Z, DR (aka MBR), and Memory content, for each instruction.

-Write in a tabular form with the following columns:

Instruction, Accu, PC, C, Z, Loc 400, Loc 500, Loc 600, Comments

-For any loop, you should trace the first instance and the last instance only – stating in your table: FIRST INSTANCE TRACE and LAST INSTANCE TRACE.

- Explain the function of the program.

70/C

```
PROGRAM (overleaf)
ORG     100
100:    LDA 200
        CIR
        STA 200
        SZE
        BSA 300
        ISZ 600
        BUN 100
        LDA 400
        CIR
        SZE
        HLT
        CLA
        INA
        STA 500
        HLT
200 :   Hex ABCD
301 :   LDA 400
        INC
        STA 400
        BUN I 300
400:    Hex 0
500:    Hex 0
600:    Dec -16
        END
```

Q2) a)Describe, in a tabular format, the working of a Booth multiplier. The two signed 6-bit operands are: 111000 and 011100.

Qb) Write the sequence of micro-instructions and the usual macro-instructions that are executed when an interrupt occurs.

OR

Q2a Alt) Describe in a tabular format, the working of a shift and subtract divider in which the 6 bit dividend is 110111 and the 3 bit divisor is 101.

Q2b Alt) Write the sequence of micro-instructions and the usual macro-instructions that are executed when an interrupt occurs.

Q3)

3a) Describe the working of a DMA controlled data transfer system.

3b) Describe an addressing mode which allows segmentation?

3c) A processor with memory mapped IO has 10 address lines and 200 IO devices, each having a data port and a status port. The maximum memory space available is?

OR

Q3Alt)

3aAlt) Describe the organization of an associative cache memory sub-system.

3a Alt)What is the maximum floating point number that can be represented with 20 bits mantissa one of them for sign bit and 8 bits 2-Compliment exponent. The base is 10.

3c Alt) Describe an addressing mode that allows jumps to an address near the PC?

Q4)

VII Sem

7I/C

4a) Compare daisy chained interrupt with priority encoded interrupt system in terms of hardware requirements and average time to service any interrupt.

4b)For each of the automated applications given below, suggest the most suitable interrupt mechanism among (i) Vectored interrupt with daisy chaining (ii) Vectored interrupt with priority encoder (iii) Vectored interrupt with software polling (iv) Non vectored Multiple interrupts. **Give clear reasons for your choice.**

1. Monitoring faults at different points in a gas pipeline
2. Accepting user inputs from a GUI
3. Data acquisition system in which data is collected and stored from multiple sensors whenever an event occurs on any one of them.
4. Monitoring the path of different probes in Laparoscopic heart surgery.

OR

Q4Alt)

4a Alt) Compare hardwired control unit with microprogrammed control unit in terms of performance and flexibility.

4b Alt) For each of the applications given below, suggest the most suitable type of control unit (i) hardwired (ii) Vertical microprogrammed (iii) Horizontal microprogrammed (iv) direct microprogrammed.

Justify your answer clearly.

1. A toy robot that moves around hurdles.
2. A fast hardware emulator that "copies the ISA of another processor in hardware".
3. A processor for home automation that must be improved with changing internet technology but the new processor versions must also be able to run old applications.
4. A number crunching processor that does a lot of operations in parallel.

Q5) For each of the following applications, suggest one instructions (other than the basic types) that you would like to be added to the instruction set of a processor dedicated for the given application. Suggest the additional hardware requirements such as registers and ALU operations for executing that instruction.

5a) A digital signal processor

5b) A database manager that performs database operations

5c) A processor that renders anti-aliased images on the screen very fast.

OR

Q5Alt)Processors are now multicore, thus enabling parallel processing. What would be the architecture of future processors? Write an essay giving your opinions on possible **architectural trends** in future. You can take the human system as a reference model and discuss possible directions in:

5a Alt) Input output architecture

5b Alt) System bus architecture

5c Alt) Processing unit architecture

Total No. of Page(s): ...2... Roll No.....

FIFTH SEMESTER B.E. (EC/COE/IC)

89/C

B.E. END SEM. EXAMINATION, Dec. 2013

EC/COE/IC -305: INDUSTRIAL ORGANISATION AND MANAGERIAL ECONOMICS

Time: 3 Hrs. Max. Marks: 70

Note: *Attempt all questions.*
Assume missing data, if any.

1. Discuss(Attempt any thirteen): [3*13]
   (a)Classical Organisation Theory
   (b)Neo Classical Organisation Theory
   (c)Management Process School
   (d)Humam Behaviour School
   (e)Contribution of F. W Taylor
   (f)Contributions of Henry Fayol
   (g)Product Layout
   (h)Process Layout
   (i)Fixed Position Layout
   (j)Sales Forecasting Techniques
   (k)Process Charts Symbols
   (l)Theory X and Theory Y
   (j) ABC Analysis
   (k) Economic Order Quantity
   (l) Breakeven Analysis
2. With the help of activities given below draw a network. Determine its critical path, earliest start time, earliest finish time, latest start time, latest finish time, total project duration, total float, free float and independent float. [6]

Activity	*Duration (in weeks)*
1-2	2
1-4	2
1-7	1
2-3	4
3-6	1

4-5	5
4-8	8
5-6	4
6-9	3
7-8	3
8-9	5

3. A project has the following characteristics. [6]

Activity	*Most Optimistic Time*	*Most Pessimistic Time*	*Most Likely Time*
1-2	5	10	8
1-3	18	22	20
1-4	26	40	33
2-5	16	20	18
2-6	15	25	20
3-6	6	12	9
4-7	7	12	10
5-7	7	9	8
6-7	3	5	4

Construct a PERT network. Find total float, critical path, variances and total project duration

4. A comparison of monthly sales of an expensive item, against the total number of visits made by salesman during the previous month, yields the following data. Is the correlation of the two variables good enough to enable the number of sales visits, to be adopted as an efficient indicator of future sales? [6]

Sales (x)	1	3	5	7	11
Visits made (y)	2	4	8	9	10

5. The fixed costs for the year 1975-1976 are Rs. 800000. Variable cost per unit is Rs. 40. The estimated sales for the period are valued at Rs. 2000000. Each unit sells at Rs. 200. [6]

(a)Find the breakeven point

(b)If Rs. 1600000 will be the likely sales turnover for

the next budget period, calculate the estimated contribution and profit.

(c) If a profit target of Rs. 600000 has been budgeted, compute the turnover required.

3.5

6. (a)Given that

(i) Annual usage, U=60 units

(ii) Procurement cost, P=Rs. 15 per order

(iii) Cost per piece, C=Rs. 100

(iv) Cost of carrying inventory I, a percentage including expenditure on obsolescence, taxes, insurance, deterioration etc.=10%, Calculate E.O.Q

(b)Find Q and M from the following data: 3.5

U=10000 units, P=Rs. 100 per order, C= Rs. 10 per unit B=Rs. 15 per each backorder incurred, I=20%

-----x-----

31/12/13 (A-N)

Total No. of Pages: 04 Roll No.....

FIFTH SEMESTER BE (ECE/COE/ICE)

B.E. END SEM. EXAMINATION, December, 2013

EC-304/ICE-304/COE-304 Linear Integrated Circuits

Time: 3 hours Max. Marks: 70

Note: Attempt any 10 questions; all questions carry equal marks. ***Answer as precisely and briefly as required.*** Missing data/information, if any, may be suitably assumed and mentioned in the answer.

1. In the context of an op-amp explain the significance of (i) input bias current (ii) level shifter. Determine an expression for the current I_L in the circuit of Fig.1 and determine the condition, in terms of the resistors, for which the circuit can realize a current-controlled-current-source.

2. Explain how the closed-loop characteristic equation of a sinusoidal oscillator is determined. Determine the condition of oscillation and frequency of oscillation for the oscillator circuit of Fig.2.

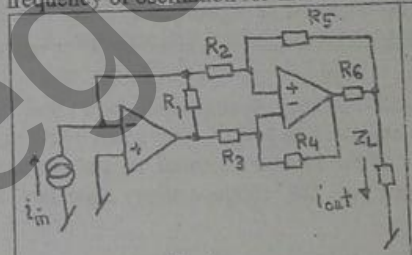

Fig.1

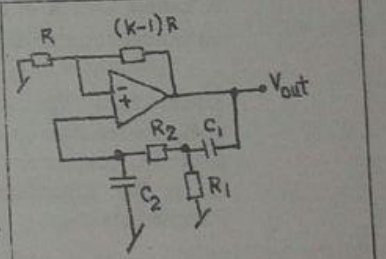

Fig.2

3. Outline the significant advantages of op-amp RC filters over passive RLC filters? Design and draw a first order low pass op-amp RC filters having infinite input impedance, zero output impedance, maximum gain = 10 and cut-off frequency of 10kHz. Use as many op-amps as necessary.

10. Using a simplified block diagram, explain the various operating modes of IC 555 timer. Explain its use as astable multi-vibrator sketching relevant waveforms and also determine an expression for the frequency of the generated square wave.

11. Explain what is meant by the *stability* of a circuit. For the circuit of Fig. 11, determine the condition for ensuring *stable* operation.

12. Analyze the circuit given in Fig. 12 and determine the condition under which the circuit can realize a grounded resistance controllable by the external control signal V_c.

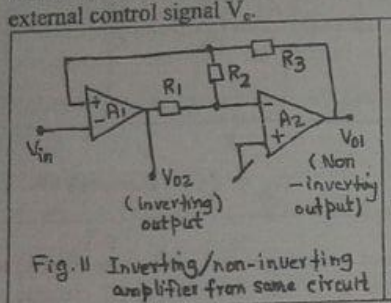

Fig. 11 Inverting/non-inverting amplifier from same circuit

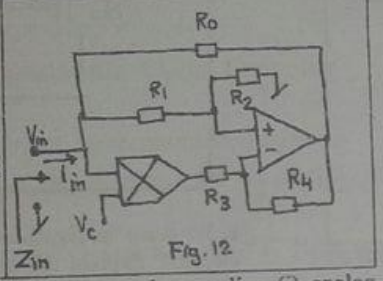

Fig. 12

13. Explain how an analog-multiplier can be used to realize (i) analog divider (ii) square rooter (iii) voltage-controlled integrator and (iv) frequency doubler.

14. Write short notes on *any two* of the following:
(i) Voltage regulators
(ii) IC Function generators
(iii) Phase locked loop
(iv) Precision rectifiers
(v) Log/antilog Circuits

4. What for *active compensation* is used in op-amp circuits? Determine approximate expression for the normalized magnitude error and phase error for the compensated amplifier shown in Fig. 4.

5. What is the basic principle and the advantages of active-R filters over active-RC filters? For the active-R filter circuit of Fig.5, determine V_{o1}/V_{in} and V_{o2}/V_{in} and comment on the filters realized by these transfer functions. Assume $A_1 \approx \omega_{t1}/s$ and $A_2 \approx \omega_{t2}/s$ where symbols have their usual meaning.

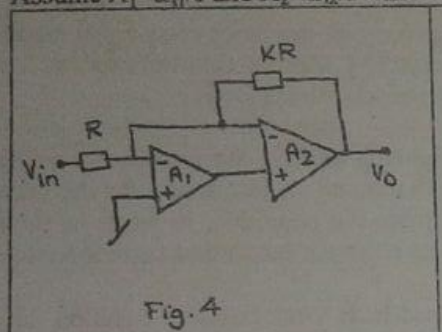

Fig. 4

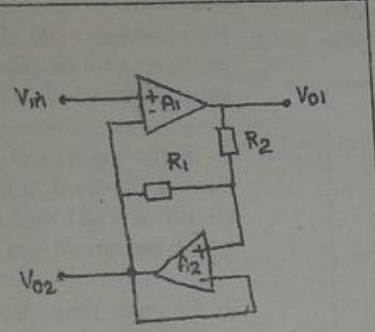

Fig. 5

6. Define CMRR of op-amp and its significance. Prove that the CMRR of an emitter coupled differential amplifier is given by $\rho \approx -g_m R_e$.

OR

Define *Slew Rate (SR)* of an op-amp and show that for internally compensated type op-amp such as uA741, it is given by $SR = I_B/C_c$ where I_B is the DC bias current of the input differential trans-conductance stage and C_c is the capacitance of the *compensating capacitor* bridging the intermediate stage.

7. For the current repeater circuit of Fig. 7, having N output terminals as shown, assume that all the transistors are identical having same β. Determine expressions for the output currents in terms of the reference current I_{ref} and β.

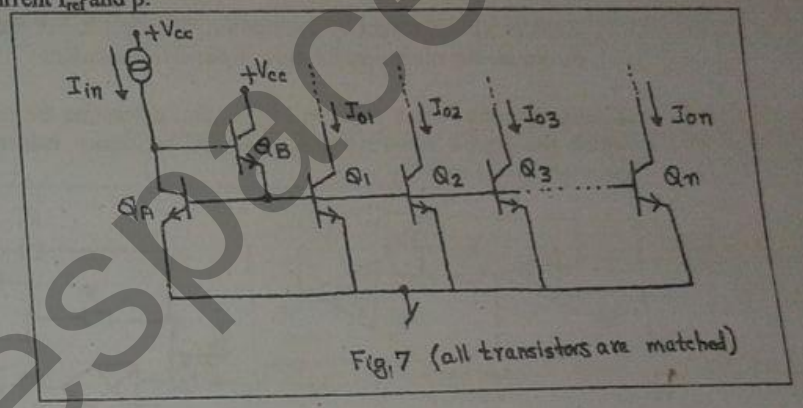

Fig. 7 (all transistors are matched)

8. What are the significant advantages and limitations (if any) of the OTA-C circuits? Explain the use of OTAs in realizing (i) electronically variable grounded resistor (ii) simulated lossless inductor.

9. Draw an OTA equivalent of Tow-Thomas biquad filter or any other op-amp filter of your choice, capable of realizing low pass and band pass filter simultaneously, determine its various transfer functions and comment on the filter functions realized by the OTA version.