Roll No. 124

Dated:

FIFTH SEMESTSER **BE(COE)**

END SEMESTER EXAMINATION –November 2006

COE-301: Principles of Computer Graphics

Time: 3 hrs Max. Marks: 70

Note: Attempt five questions in all. Q.1. is compulsory. All Questions carry equal marks. Assume suitable missing data, if any.

Q.1. (a) Define blending functions for Bezier curves. (2x7=14)

(b) Differentiate between the natural splines and B-splines used for drawing curves in computer graphics.

(c) What is a wireframe model? Give one example.

(d) Suppose we have a video monitor with a display area that measures 12 inches across and 9.6 inches high. If the resolution of the monitor is 1280 by 1024 and the aspect ratio is 1, what is the diameter of each screen point?

(e) Find out the normalization transformation that maps a window where lower left corner is at (1,1) and upper right corner is at (3,5) onto a viewport that has lower left corner at (0,0) and upper right corner at (0.5,0.5).

(f) What are the advantages of using homogeneous/affine co-ordinate system of representation?

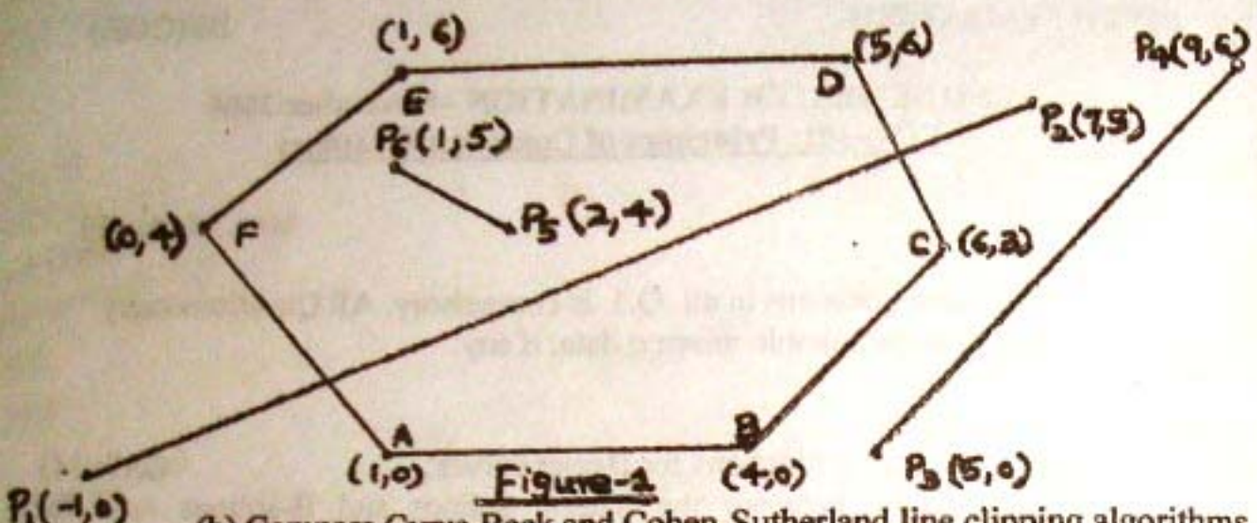
(g) How long would it take to load a 640 by 480 refresh buffer with 12 bits per pixel, if 10^5 bits can be transferred per second?

Q.2. (a) Compute the transformation matrix to reflect an object about an arbitrary line y=mx+c. (4)

(b) Reflect an object defined by the co-ordinates A(2,6), B(3,8) and C(5,2) about the line y= -3x+5. (3)

(c) Rotate the rectangle with diagonal co-ordinates at (2,2) and (8,6) by 45° in anti-clockwise direction with respect to point (1,1). (7)

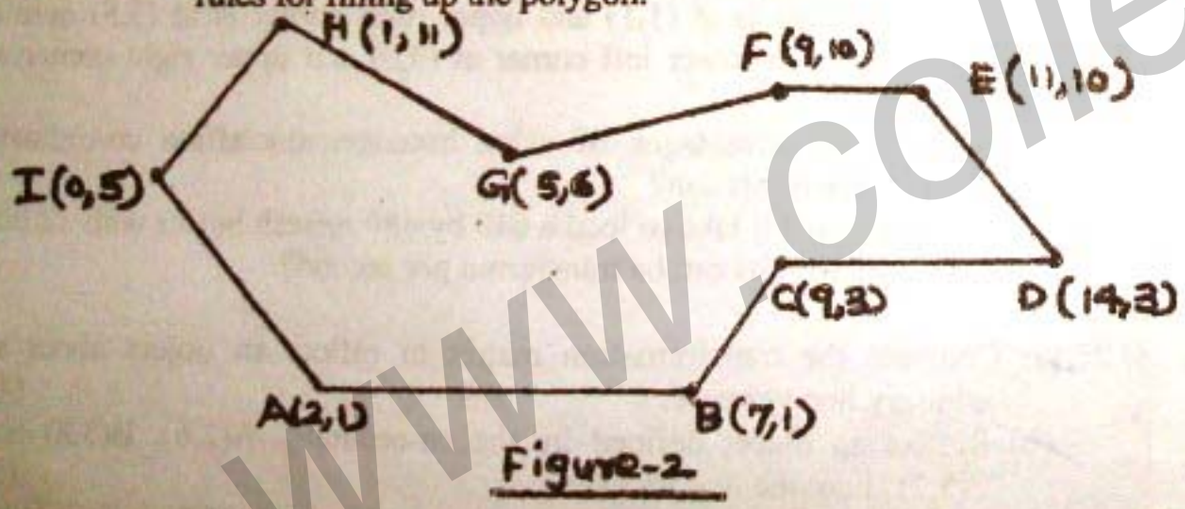
Q.3. (a) Use the Cyrus-Beck line clipping algorithm to clip the lines against the window shown in Figure-1. (7)



(b) Compare Cyrus-Beck and Cohen-Sutherland line clipping algorithms. Write their advantages and disadvantages. (3)

(c) Explain Sutherland-Hodgeman algorithm of polygon clipping with the help of an example. (4)

Q.4. (a) Use scan line fill algorithm to fill up the polygon given in Figure-2. Draw sorted edge table and also the AET for each scan line. Write the rules for filling up the polygon. (8)



(b) Suppose the equations relating the Hermite geometry to the Bezier geometry were of the form $R_1=b(P_2-P_1)$, $R_4=b(P_4-P_3)$. Consider the four equally spaced Bezier control points $P_1=(0,0)$, $P_2=(1,0)$, $P_3=(2,0)$ and $P_4=(3,0)$. Show that for the parametric curve Q(t) to have constant velocity from P_1 to P_4, the coefficient b must be equal to 3. (6)

Q.5. Construct an isometric projection onto the yz-plane and show the projection of unit cube. (14)

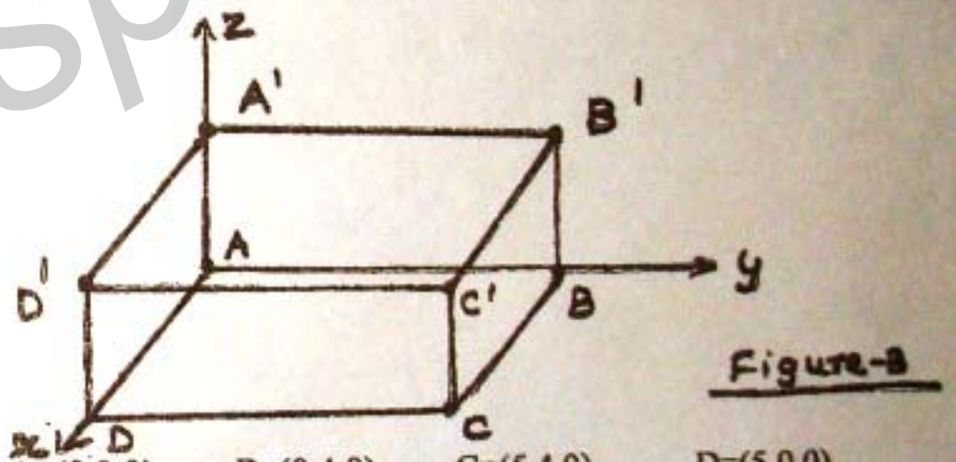
OR

(a) What is hidden surface removal? Discuss its need. Explain z-buffer and scan line methods for hidden surface removal. (8)

(b) Explain 3-D Cohen Sutherland Clipping algorithm. (6)

Q.6. (a) Draw the chart of classification of perspective and parallel projections. (4)

(b) Draw the perspective transformation of the cuboid depicted in Figure-3 onto xy-plane where the center of projection is
(i) (0,0,1) and
(ii) (0,0,-5). (10)



A=(0,0,0) B=(0,4,0) C=(5,4,0) D=(5,0,0)
A'=(0,0,1) B'=(0,4,1) C'=(5,4,1) D'=(5,0,1)

(3.5x4)

Q.7. Write short notes on any four:
(a) Continuity in curves
(b) B-Spline curves
(c) Anti-aliasing algorithm
(d) Input devices
(e) Bresenham algorithm for scan conversion of line
(f) Derive transformation matrix for oblique projection

END SEMESTER EXAMINATION, Nov.-2006

V Sem. B.E. (COE)

COE-302 : DISCRETE MATHEMATICS AND DESIGN OF ALGORITHMS (DMDA)

Time: 3:00 Hrs. **Max. Marks: 70**

Note: Attempt any FIVE questions.
Also give suitable examples where ever required

Q.1(a). Verify if ((P V Q) $\wedge$ ~P) -> ~P is an implication ? [3]

(b). Use an indirect argument to test the validity of the following arguments, expressing it in symbolic form [4]

"My teacher likes me only if I work hard. Either I do well in sports or I cannot work hard. If I am not confident, I cannot do well in sports . Hence if my teacher likes me, then I am confident."

(c). Express each of the following statements in the form of predicate formulas
(i). One must be true to himself.
(ii). Some people who have courage, reach great heights. [4]

(d). Obtain the principle CNF of the formula
(~P -> R) $\wedge$ (Q <-> P) [3]

Q.2(a). Solve the recurrence relation
$$a_r - 5a_{r-1} + 6a_{r-2} = 2^r + r$$ [5]

(b). State the generalized pigeon hole principle.
Suppose the members of a class of 27 pupils each go swimming on some of the days from Monday to Friday in a certain week . If each pupil goes at least twice show that there must be two pupil who go swimming on exactly the same day. [5]

(c). Suppose R = { (x, x+1) | x $\in$ N } .Show that for any natural number k > 0 ,
$$R^k = \{ (x, x+k) \mid x \in N \} .$$
Hence find the transitive closure of R
where N = { 0,1,2,3..... } [4]

Q.3(a). Let S = N X N and let R be a binary relation on S defined by
(x , y) R (z , w) iff x + y = z + w
Show that R is an equivalence relation on S and describe the resulting equivalence classes. [5]

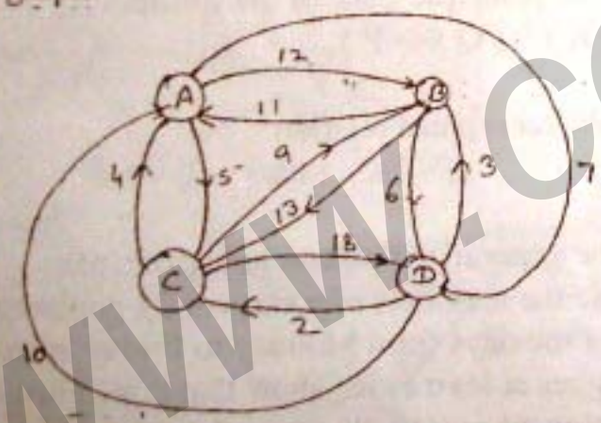
(b). Show that (n log n) $\in \Theta$ (log n!) [4]

(c). Assuming tree representation of sets , describe the Disjoint set, Union and Find algorithms. How can you improve the performance of your Union and Find algorithms using the weighing and collapsing rules ? [5]

Q.4(a). Define 0/1 knapsack problem. Design the dynamic algorithm for finding its solution and discuss its time complexity . Give suitable example. [8]

(b). Let n = 7,
$(p_1, p_2, p_3, p_4, p_5, p_6, p_7) = (3, 5, 20, 18, 1, 6, 30)$
and
$(d_1, d_2, d_3, d_4, d_5, d_6, d_7) = (1, 3, 4, 3, 2, 1, 2)$.
Find the optimal solution using the JS job sequencing function. [6]

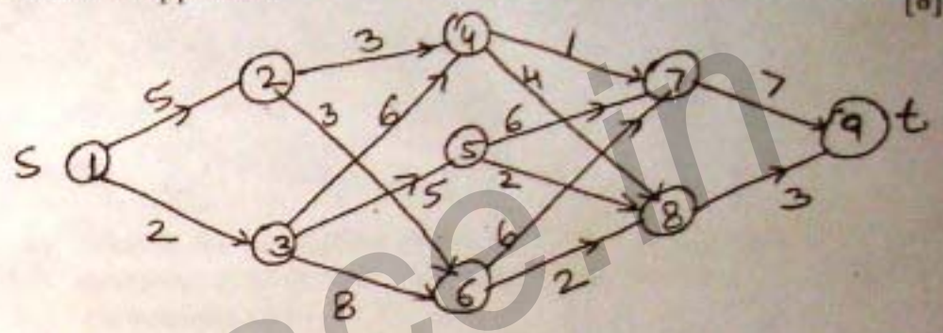
Q.5(a). Consider the graph



Find an optimal tour of the graph that starts at A and goes through The other nodes and terminates at A using dynamic programming Approach. [8]

(b). Find an optimal placement for 13 programs on three tapes T_0, T_1, T_2, where the programs are of lengths 12, 5, 8, 32, 7, 5, 18, 26, 4, 3, 11, 10 and 6. [6]

Q.6(a). Find the minimum cost path from s to t in a multistage graph of the Figure given. Do this first using the forward approach and then the Backward approach. [8]



(b). Write an algorithm that multiplies two n x n matrices using O (n^3) operations. Determine the precise number of multiplications, additions, subtractions and array element accesses using other than conventional method. [6]

Q.7(a). Suppose a student wants to make up a schedule for a seven day period during which she will study one subject each day. She is taking four subjects maths, physics, chemistry, and economics. Find the number of schedules that devote at least one day to each subject. [4]

(b). Explain any two in detail with the help of suitable examples
(i) DFT and IDFT
(ii) P, NP and Co – NP problems
(iii) Partitions
(iv) POSET and Lattices
(v) Combinations in lexicographic order algorithm
[5x2 = 10]

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Roll No. 124

FIFTH EMESTER **B.E (COE/EC)**

END SEMESTER EXAMINATION,, Nov/Dec-2006

COE/EC-303 Computer System Organization

Time: 3:00 Hours **Max. Marks: 70**

Note: Answer any **Five** Questions.
Assume suitable missing data, if any.

Q1)

a) Explain the basic concept of von Neumann architecture. How does it differ from the Harvard architecture? (4)

b) The memory unit of a computer has 256 K word of 32 bits each. The computer has an instruction format with four fields: an Opcode field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers and a memory addresses. Specify the instruction format and he number of bits in each field if the instruction is in one memory word. (4)

c) Show the hardware to implement the following RTL code:

I) δ:X← X+Y
II) σ:X← X + Y'+1
III) ϵ:X← X .EXOR. Y

(6)

Q2) Consider the following CPU specifications

- It can access 64 words of memory, each word being 8 bit wide. The CPU does this by outputting a 6 bit address on its output pins A[5..0] and reading in the 8-bit value from memory on its input D[7..0].
- The CPU contains a 6 bit address register (AR) and program counter (PC); an 8-bit accumulator (AC) and data register (DR) and a 2-bit instruction register (IR).
- The CPU must realize the following instruction set

Instruction	Instruction Code	Operation
COM	00XXXXXX	AC← AC'
IREL	01AAAAAA	PC←PC+ 00AAAAAA
OR	10AAAAAA	AC← AC .OR M[00AAAAAA]
SUB	11AAAAAA	AC←AC – M[00AAAAAA]-1

Design the micro-program control unit for the above CPU using

(i) Horizontal micro-coding
(ii) Vertical micro-coding

(14)

Q3) Design a CPU that meets the following specifications:

- It can access 256 words of memory, each word being 8-bits wide. The CPU does this by outputting an 8-bit address on its output pins A[7..0] and reading in the 8-bit value from memory on its inputs D[7..0].
- The CPU contains an 8-bit address register AR, program counter PC, accumulator AC, data register DR and a 3-bit instruction register IR.
- The CPU must realize the following instruction set, where ϵ is an 8-bit value stored in the location immediately following instructions.

Instruction	Instruction code	Operation
LDI	000XXXXX €	AC← €
STO	001XXXXX €	M[€]← AC
ADD	010 XXXXX €	AC←AC + M[€]
OR	011 XXXXX €	AC←AC .OR. M[€]
JUMP	100 XXXXX €	PC← €
RST	101 XXXXX	PC←0, AC←0

(14)

Q4)

a) The parameters of a computer memory system are specified as follows:
–Memory size= 64K words
–cache memory size = 2K words
–Block size = 16 words
Determine the address format of main memory under the following mapping techniques:

i) Fully associative
ii) Direct mapping
iii) Set associative with 2 blocks per set.

Also explain how a main memory block I is mapped to one of the cache blocks using above said mapping techniques. (6)

b) Compare the memory consistency and performance of write back and write through caches. (3)

c) Consider the following information about a memory system that employs cache: Cache access time = 50 ns, main memory access time = 500 ns. It is estimated that the 80% of the main memory requests are for READ and remaining are for WRITE. The hit ratio for read access only is 0.9 and a write through policy is used.

(i) Calculate the average access time considering only READ cycles
(ii) Calculate average access time if the write requests are also taken into consideration. (5)

Q5)

a) Explain the various modes of data transfer techniques.
How many characters per second can be transmitted over 1200 baud line in each of the following modes - Synchronous serial communication, -Asynchronous serial communication with 2 stop bits (6)

c) Differentiate between vectored and non-vectored interrupts. Explain the concept of daisy chaining priority interrupt system with a practical application. (8)

Q6)

a) Consider two 5-bit signed numbers -12 and +14. Trace the steps of the Booth multiplication algorithm to multiply the two numbers. Illustrate with a block diagram the data path and control path for the SHIFT-and-ADD multiplication algorithm. (7)

b) Explain the following terms for floating point numbers:

(i) Exponent overflow and underflow
(ii) Mantissa overflow and underflow.

Give the flow chart of a floating point division, illustrating all the relevant exception conditions. (7)

Q7)

Comment upon any **three** of the following technologies:

(i) Various types of ROM technologies
(ii) USB serial port
(iii) Bus hierarchy for desktop and servers
(iv) Combinational array multiplier (14)

Roll No 124 No. of pages: 4 Date _____

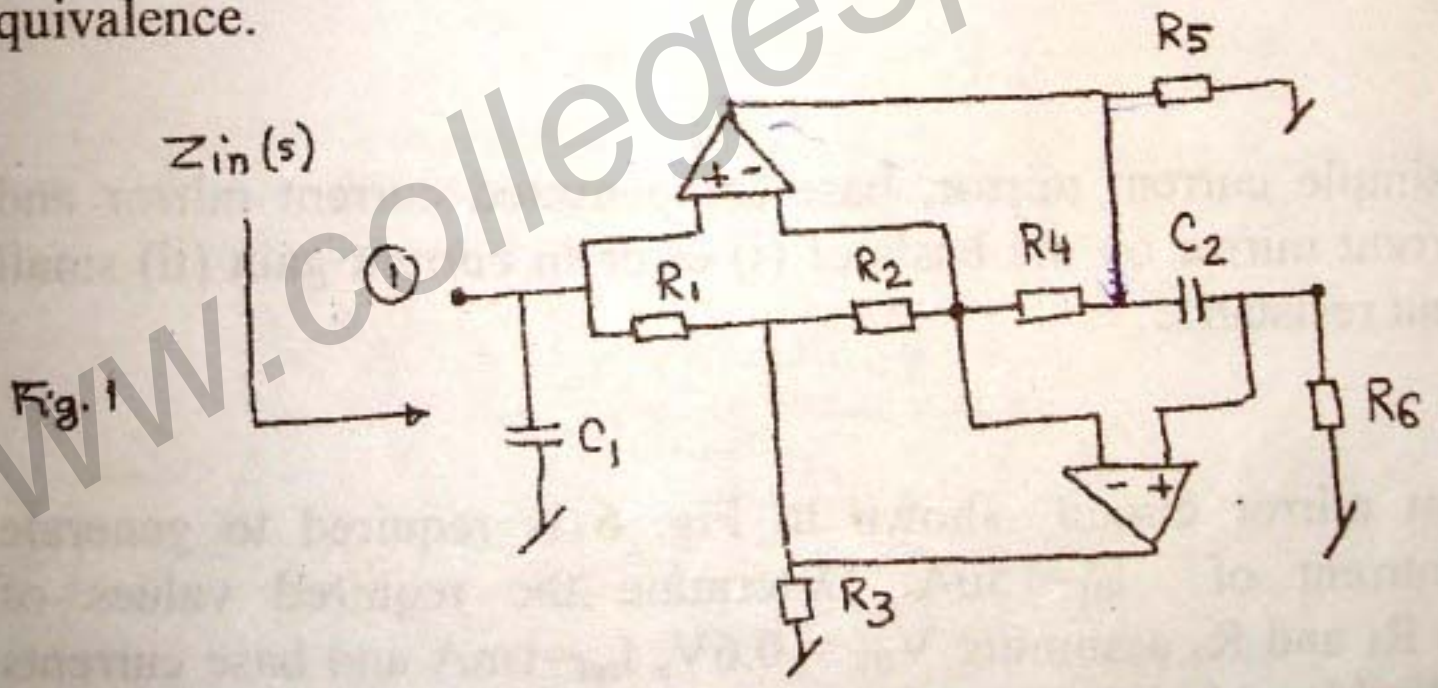
END SEMESTER EXAMINATION, NOV.-2006

Vth Semester. BE (ECE/COE/ICE-304)
Linear Integrated Circuits

Note: Attempt any 10 questions: all carry equal marks. Be concise and use the space available in the answer book judiciously. Wastage of paper and using too many supplementary answer books will be taken negatively. Missing data/information, if any, may be suitably assumed and mentioned in the answer.

Time: 03.00 Hrs. Max. Marks: 70

1. Using ideal op-amps, determine the expression for the input impedance of the circuit shown in Fig. 1 and show its passive equivalence.



2. Find out the condition of oscillation and frequency of oscillation for the oscillator circuit shown in Fig. 2.

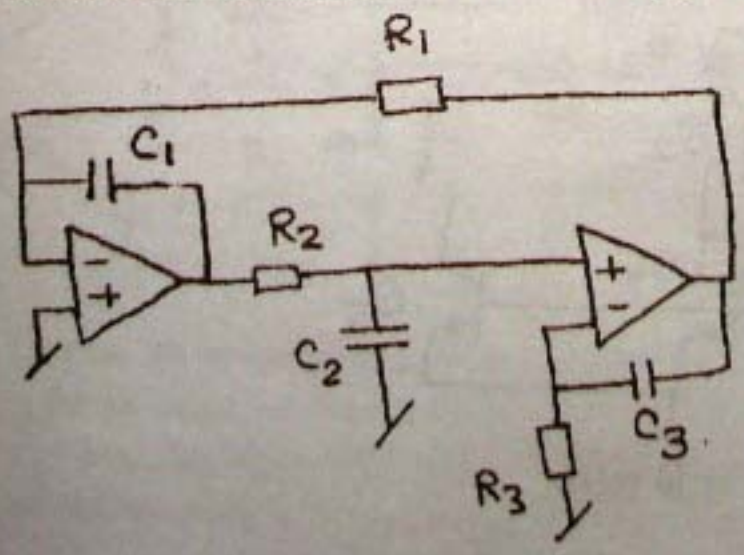


Fig. 2

3. What are the advantages of OTA-C circuits as compared to op-amp-RC circuits? Devise on OTA-C circuit which should produce an output voltage V_o given by

$V_0(s) = V_1(s) + \frac{1}{s}\left(V_2(s) - V_3(s)\right)$ (where V_1, V_2 and V_3 are input signals). Use a minimum possible number of active devices and passive elements.

4. Devise an OTA-based circuit which realizes the same transfer function as that of the op-amp circuit of Fig. 4.

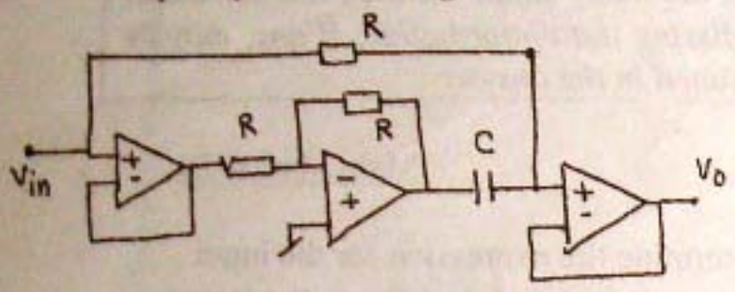


Fig. 4

5. Compare simple current mirror, base-compensated current mirror and Wilson current mirror on the basis of (i) error in current gain (ii) small signal output resistance.

6. The current mirror circuit shown in Fig. 6 is required to generate constant current of I_{01}=15uA. Determine the required values of resistances R_1 and R_2 assuming V_{BE} = 0.6V, I_{ref}=1mA and base currents being negligible. Modify the circuit to give two additional out put currents I_{02} = 1mA and I_{03} = -1mA.

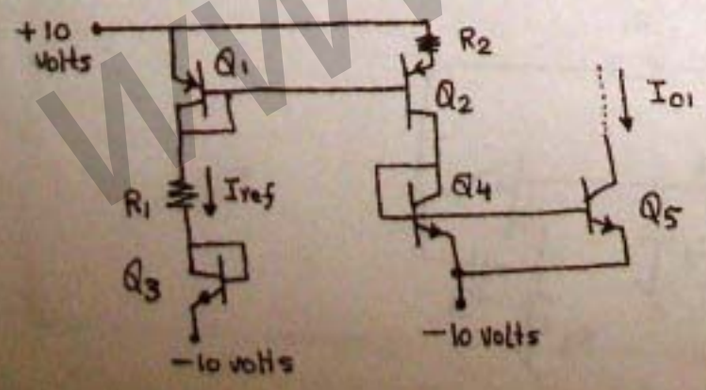


Fig. 6

7. Under what condition, the circuit of Fig. 7 can function as a log amplifier?

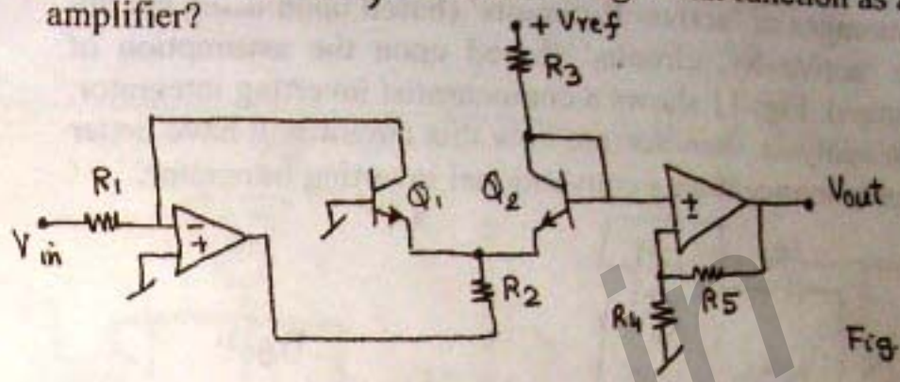


Fig. 7

8. Explain the Gilbert multiplier circuit using bipolar transistors with the help of relevant analysis. Two square wave signals of frequency 100Hz, with magnitude alternating between ±10V and having a phase difference of ϕ are applied to a Gilbert multiplier biased from ± 15V DC and a DC current source of 1mA. Sketch the out put wave form and comment on the function performed by the circuit.

9. What is the difference between 2-quadrant and 4-quadrant multiplier? Analyze the circuit of Fig. 9 and determine the condition under which the input resistance (R_{in}) is inversely proportional to the control voltage (V_c).

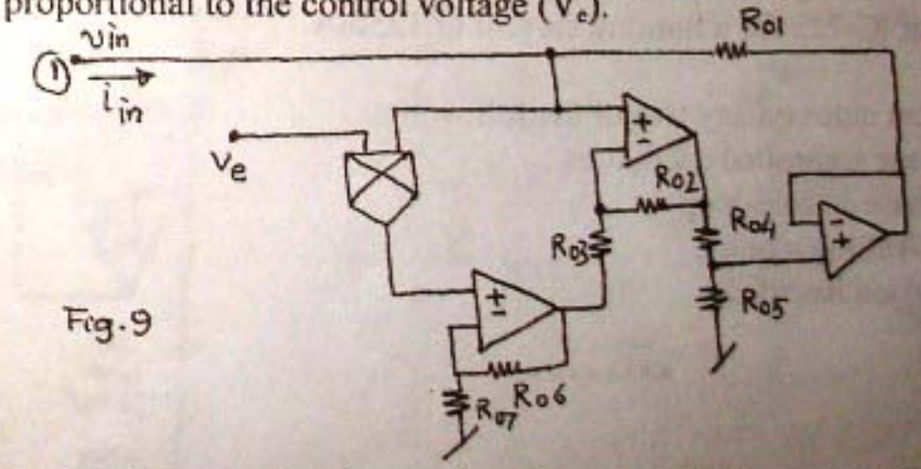


Fig. 9

10. Explain the circuit and operation of a mono-stable multi-vibrator using an op-amp comparator or an IC timer 555.

...are the advantages of `active- R circuits' (based upon using the op-amp poles) over `active–RC circuits' (based upon the assumption of infinite gain op-amps). Fig. 11 shows a compensated inverting integrator. By an appropriate analysis, demonstrate how this circuit will have better high frequency performance than a conventional inverting integrator.

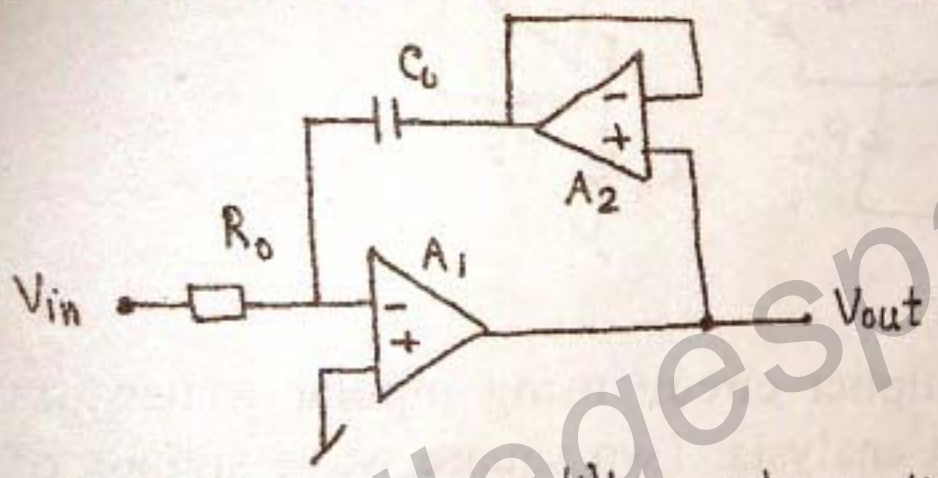


Fig. 11

Assume, $A_1 \cong \frac{\omega_{t_1}}{s}$, $A_2 \cong \frac{\omega_{t_2}}{s}$ where ω_{t_1} and ω_{t_2} are gain-bandwidth products of the two op-amps.

12. Show by analysis how an analog multiplier, in conjunction with op-amps and resistors (use as many as you need) can be used to perform the following functions:
    (a) Frequency doubler
    (b) Square rooter

13. Explain the circuit and operation of an op-amp regulator. How current limit is achieved in IC-723 regulator? Explain and design the current limit circuit of IC-723 for a limiting current of 125mA.

14. Write technical notes on any two of the following:
    (a) Voltage controlled oscillators
    (b) IC phase-locked-loop
    (c) Log/Antilog module
    (d) Precision Rectifier

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