*Total No. of Pages:* *Roll No.....*

**SIXTH SEMESTER** **B.E. (ECE /COE/ICE)**

**MID SEMESTER EXAMINATION, MARCH 2014**

**EC/CO/IC– 311: MICROPROCESSORS**

*Time: 1-½ hrs* *Max. Marks: 20*

NOTE: Assume and mention any missing data.

Q1. a) Draw the timing diagram for RET instruction [2]

b) What is the format of STA instruction? Give the number of bytes, machine cycles and T-states for this instruction. [1]

c) What will happen if the READY signal is held low for 10 mS? Explain with a timing diagram. [2]

Q2. a) Design an 8085 system with 16KB EPROM and 16KB RAM, one 8255 (Programmable Peripheral Interface) and two additional output ports using 74373 latches. The latches are connected to two common anode seven segment displays. Draw the interface diagram. Allocate addresses to all the devices. The peripheral ICs must be IO-mapped. [5]

b) Write 8085 Assembly language program for the above system, to display a BCD up counter on two seven segment displays. It should count numbers from 00 to 99 and reset to 00 after reaching 99 and increment every 1s. Assume that the crystal frequency of the 8085 is 2 MHz. Write the 1-second delay routine also. [5]

Q3. a) If SP=0000H, which registers in which memory locations will be stored if PUSH B instruction is executed? [2]

b) Explain with suitable diagram, the hardware interrupts of 8085. Classify them as maskable or non-maskable, vectored or non-vectored. [3]

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Sixth Semester
BE(COE)

MID SEMESTER EXAMINATION, Mar'2014
COE 312: Information System and Data Management

Time: 1:30Hrs

Max. Marks:20

Note: Attempt all questions.
Assume missing data suitably, if any.

Q1. Differentiate between candidate key, primary key, foreign key and super key with suitable example. (6)

Q2. Explain **On Delete Cascade** with the help of an example. (2)

Q3a. What is canonical cover? Consider following set F of functional dependencies on schema R(A,B,C) and compute canonical cover for F:
F = { A → BC, B → C, A → B, AB → C } (2)

b. Consider a relation R with five attributes A, B, C, D, E having following dependencies: A → B, BC → E and ED → A
Find any candidate key for R. Justify your answer. (2)

Q4. Consider following relational schema

Person (ss#, name, address, license no)
Car (registration_no, year, model)
Accident (date, driver, damage-amount)
Owns (ss#, registration_no))
Log (registration_no, date, driver)

**Answer** the following queries in SQL and relational algebra
**(i)** Find the total number of people whose cars were involved in accidents in 2013.
**(ii)** Find the numbers of accidents in which the cars belonging to "XYZ" were involved. (4)

Q5a. Differentiate between 3NF and BCNF (2)

b. How will you verify the property of dependency preservation during the process of normalization? (2)

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BE (COE) Sixth Semester

# B.E. MID SEMESTER EXAMINATION, MARCH 2014
## COE - 313 : OPERATING SYSTEMS

Time : 1:30 Hrs.

Max Marks: 20

Note : Attempt all questions. Assume suitable missing data, if any.

Q.1. Explain the following terms with example in brief.
(i) I/O interrupt handling methods
(ii) Hardware protection methods
(iii) Various Operating system structures
(iv) Solaris Threads [2 x 4 = 8]

Q. 2. What is PCB? How it is used in CPU switching from process to process? [3]

Q. 3. Explain the various types of schedulers with example. [3]

Q. 4. What are semaphores? Explain dining-philosophers problem using semaphores. Write C/C++ code with system calls. [3]

Q. 5. What is resource allocation graph? Explain the algorithm which will be used if resource allocation graph algorithm can not be used for deadlock avoidance. Take suitable example. [3]

MID SEMESTER EXAMINATION, March-2014

VI Semester, ICE/COE

IC-314: Control System/ COE-314: Control Engineering

Time: 1:30 Hrs M.M.-20

**Note: Attempt all questions. Each question is of equal marks.**
**Assume suitable data, if missing.**

Q1. Explain the sensitivity analysis of open loop and close loop control systems.

Q2. Using block diagram reduction technique, find the overall transfer function C(s)/R(s) of Fig 1.

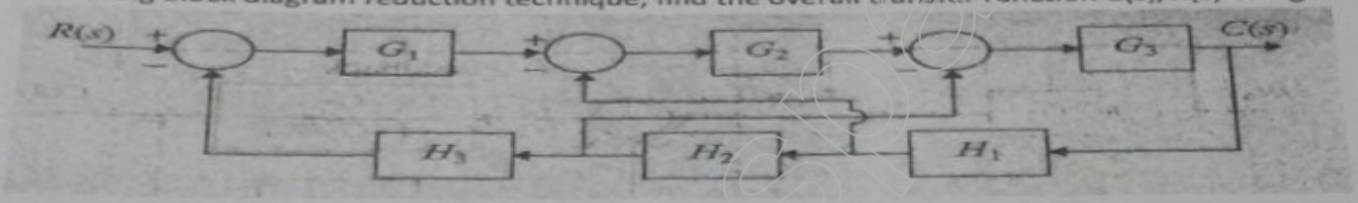


Fig.1

Q3. Derive the transfer function of field controlled DC servomotor.

Q4. Draw the force-voltage analogy of the mechanical system of Fig 2.

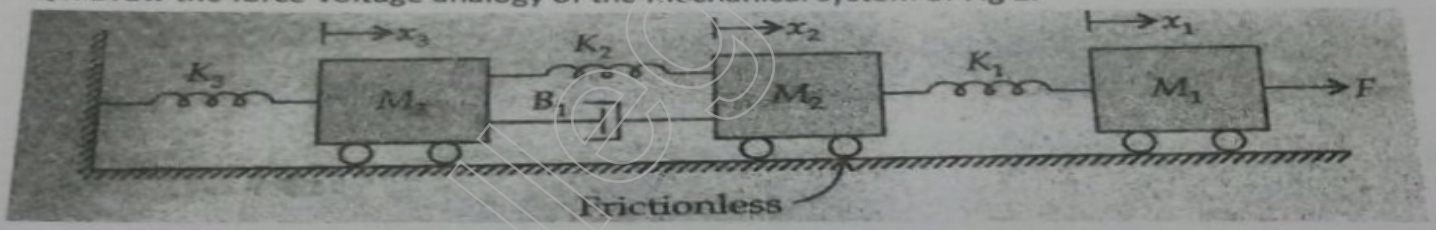


Fig.2

Q5. Calculate delay time, rise time, peak overshoot, peak time, natural frequency, damping factor and settling time for the unit step input of following transfer function.

$$G(s) = \frac{1}{s^2 + 3s + 1}$$

OR

Q5. What do you mean by stability? Determine the value of $K$ such that the system is stable.

$$q(s) = s^6 + 2s^5 + 4s^4 + 9s^3 + 8s^2 + 6s + K$$

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B.E. (COE) 6th Semester MID SEMESTER EXAMINATION, March 2014

COE- 315 (Section –I, II) Advanced Computer Architecture

Time: 1½ Hrs. Max. Marks: 20

**NOTE: Attempt all the questions IN ORDER only. Assume missing data (if any) and specify it clearly.**

# ONLY FOR SECTION – I & II STUDENTS

**Question 1** [8]

a) To which category of parallel architectures does a SIMD processor and a VLIW processor belong to?
b) Do all instructions write their result to "Register File" in Tomasulo's scheduling technique? Justify.
c) Which optimization can be done by a compiler in the following code segment so that none of the three instructions get blocked in ISSUE stage, when these are executed under Scoreboard control?
I1: LOAD t2, 0(t3) ; I2: ADD t2, t0, t2 ; I3: MUL t8, t2, t0
d) Explain how Tomasulo's algorithm handles a name dependency in the following code.
I1: LOAD F6, 34(R2) ; I2: DIV F10, F6, F0; I3: ADD F6, F8, F2
e) Loop Unrolling and Software Pipelining accomplish the same goal: reducing stalls and increasing parallelism. So, if we use one technique, other is unnecessary as it won't yield a significant payoff. Justify or refute.
f) Write a branch outcome sequence which will be always mispredicted by a 2-bit Bimodal Branch Predictor initialized to Strongly NotTaken state.
g) Instruction Scheduling, whether static or dynamic, removes dependencies between instructions, increasing possible instruction level parallelism. Justify or refute.
h) Name a hardware techniques and a software approach to reduce the stalls due to RAW dependency.

**Question 2** [2]

Are the following two loops parallelizable? If not, Why? Can you perform some modification to make them parallelizable? If yes, show.

a)
```
for (i=1; i<=100; i= i+1){
  a[i] = a[i] + b[i];      //s1
  b[i+1] = c[i] + d[i];    //s2
}
```

b)
```
for (i=1; i<=100; i= i+1){
  a[i+1] = a[i] + c[i];    //S1
  b[i+1] = b[i] + a[i+1];  //S2
}
```

**Question 3** [2]

A BTB is implemented in a deeply pipelined processor for the conditional branches only. Assume that the misprediction penalty is always 5 cycles and the buffer miss penalty is always 3 cycles. Assume 80% hit rate and 90% accuracy, and 20% branch frequency. How much faster is the processor with the BTB versus a processor that has a fixed 2-cycle branch penalty?

**Question 4** [4]

A program with the following instruction mix is executed on a load/store processor:

| Operation | Frequency | No. of Clock cycles | Operation | Frequency | No. of Clock cycles |
|---|---|---|---|---|---|
| ALU ops | 35% | 1 | Stores | 15% | 2 |
| Loads | 25% | 2 | Branches | 25% | 3 |

a) We observe that 35% of the ALU ops are immediately followed with a load instruction, and it is proposed to replace these ALU ops and their loads with a new instruction. The new instruction takes 1 clock cycle. Compute the CPI for the new version.
b) If the clock of the old version is 20% faster than the new version, which version has faster CPU Execution time and by how much percent?

**Question 5** [4]

a) Write a command to link a "prog.o" file with POSIX thread library file.
b) Write the header files that are needed to use POSIX thread and POSIX semaphore function in a C program.
c) Write the header files required for using fork system call, and wait system call.
d) Write the Linux command that reports System V inter-process communication facility status and that removes the corresponding identifiers.

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