

Total no. of Pages: 1

Roll No.

MID SEMESTER EXAMINATION MARCH 2015
VI SEMESTER B.E. (COE)

COE-311 : Microprocessors

Time: 1.30 Hrs.

Max. Marks: 20

Note: Attempt all Questions. Assume missing data suitably, if any.

- 1a. What are tri-state devices and why are they essential in a bus oriented system? 2
- b. what is difference between: (i) Program counter and memory address register, (ii) Accumulator and instruction register 2
- 2a. In Opcode Fetch cycle, what are the control and status signals asserted by 8085 to enable memory buffer? 2
- b. If the 8085 uP loads 87H and 79H, specify the contents of the accumulator and the status of S, Z, and CY flag. 2
- 3a. Write down 8085 timing diagram for IN instruction execution. 3
- b. Assume that an uP has only two registers R₁ and R₂ and that only the instruction: $XOR\ R_i, R_j \quad //R_i \leftarrow R_i \oplus R_j, \quad i, j=1,2.$
Using this XOR, find an instruction sequence to exchange the contents of the registers R₁ and R₂. 3
- 4a. Following 8085 program is supposed to clear a block of 100 memory bytes starting address 2000H:

```
ORG 2000H
BSIZE EQU 100
LXI B, BSIZE
LXI H, START
MVI A, 0
LOOP: MOV A, M
      INX H
      INX B
      JNZ LOOP
      HLT
START DS 2000H      //DS define storage
      END
```

Comment on its working. 3

- b. Write an instruction sequence using the LXI and PCHL instructions in order to jump unconditionally to 2010H. 3

62

Total No. of pages: 1
Fifth Semester

Roll no. _____
BE(COE)

MID SEMESTER EXAMINATION, March 2015
COE 312: INFORMATION SYSTEM AND DATA MANAGEMENT

Time: 1:30Hrs

Max. Marks: 20

Note: Attempt all questions.
Assume missing data, if any, suitably.

- Q1. Consider a relation schema $R(X, Y, Z, U, V)$ and set of functional dependencies F as : $F = \{X \rightarrow YZ, ZU \rightarrow V, Y \rightarrow U, V \rightarrow X, Y \rightarrow V\}$

Answer the following questions:

- [a] Find the candidate keys of R
 - [b] Is R in 3NF? If not, then decompose R in 3NF.
 - [c] Is the resulting decomposition in part [b] lossless join decomposition? Justify your answer? (6)
- Q2. Describe the following terms, briefly
- [a] Data abstraction
 - [b] Role of database administrator
 - [c] Referential integrity
 - [d] Superkey (4)
- Q3. Define the term specialization/generalization. Explain with the help of suitable example. (2)

- Q4. Consider the following schema
- salesperson(id, name, commission)
 - Product(id, description)
 - Sales(id, pid, date, customer_id, qty)
 - customer(id, customer_id, cname, address)

Answer the following queries using relational algebra and SQL statements.

- [a] Find the names of the salesmen who sold product X and Y on 8/2/2015.
 - [b] Find the names of those customers who bought "COMPUTER" through salesperson named "JOHN"
 - [c] Find the total quantity of products sold by each salesman. (6)
- Q5. Define triggers. How is it different from function/procedure? (2)

— X —

Time: 1.30 Hours

Max. Marks: 20

Note: Assume suitable missing data, if any.

- Q1. (a) What is an operating system?
 (b) Why an operating system is said to be a resource allocator and a control program?
 (c) What is a kernel?
 (d) How a microkernel differs from a kernel?
 (e) What is a shell?
 (f) What is a system call?
 (g) What is a real time operating system?
 (h) What are the advantages of an operating system that runs on different computer architectures?
 (i) Draw the block diagram of MS DOS.
 (j) Draw the block diagram of Unix.

[10x0.5]

Q2. A system uses the round robin algorithm for CPU scheduling and has six processes as follows.

Process	Arrival time (ms)	CPU burst time (ms)
P1	0	4
P2	6	10
P3	7	2
P4	9	8
P5	11	2
P6	15	10

Calculate the mean and the standard deviation of the waiting times of the processes if (a) time quantum = 8 ms and (b) time quantum = 2 ms. Discuss the real world implications of the results.

$$\bar{x} = \frac{1}{n} \sum_{i=1}^n x_i$$

N.B.: mean, \bar{x} and standard deviation, $\sigma = \sqrt{\frac{1}{n} \sum_{i=1}^n (x_i - \bar{x})^2}$

[2+2+1]

Q3. A clinic consists of a doctor's chamber and a waiting room. There are n chairs in the waiting room. A patient enters the waiting room, sits on a chair, and waits for the doctor to become free. If there is no vacant chair then the patient should wait for one to become vacant. There is only one doctor in the clinic. He calls a patient sitting in the waiting room to his chamber, examines him/her, and then dismisses him/her. This sequence of events is repeated for a long time. Write the pseudocode for patients' and doctor's processes using semaphores.

[5]

Q4. Write short notes on any two of the following topics with a suitable example :

- Threads
- Monitor
- Bus effect
- PCB

[2.5, 2.5]

— x —

74

Total No. of Page(s): 01

Roll No.

SIX SEMESTER

B.E. (ICE)

B.E. MID SEM. THEORY EXAM. (MARCH-2015)

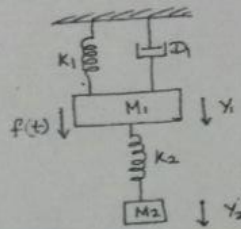
COE/IC-314 : CONTROL SYSTEMS - I

Time: 1:30 Hrs.

Max. Marks: 20

Note: Attempt ALL questions. All questions carry equal marks.
Assume missing data if any.

- Q1.** A dynamic vibration observer is shown below. Find the transfer function $\frac{Y_1(s)}{F(s)}$.



- Q2.** The open loop transfer function of a unity feedback system is $G(s) = \frac{K}{s(sT+1)}$ where K and T are positive constants. By what factor should, the amplifier gain K be reduced so that the peak overshoot of unit step response of the system is reduced from 75% to 25%.
- Q3.** For a unity feedback system $G(s) = \frac{100}{s(s+8)}$ and $r(t)=2t$, determine steady state error. If it is desired to reduce this existing error by 5%, find new value of gain of the system.
- Q4.** A two-phase AC servomotor has open loop transfer function $G(s) = \frac{2.58}{0.25s^2 + s}$. Its feedback path gain is unity. Find ω_n and ρ . If ρ is to be made critical using derivative control, determine the time constant of derivative control action.
- Q5.** Let $G(s) = \frac{K}{s(s^2 + \alpha s + \beta)}$ where $K = 20, \alpha = 4, \beta = 1$
Find
i) $S_K^G \rightarrow$ Sensitivity of open loop transfer function to parameter variation in K.
ii) $S_K^T \rightarrow$ Sensitivity of closed loop transfer function to parameter variation in K.

-----X-----

(80)

Total No. of Pages: 1

B.E. (COE) 6th SEMESTER

Roll Number:

MID SEMESTER EXAMINATION, MARCH

COE - 315:- ADVANCED COMPUTER ARCHITECTURE

TIME: 1.5 HOURS

MAX. MARK

NOTE: Attempt all questions. Assume suitable missing data, if any, and specify it clearly.

(For Section – III Students only)

Q. 1

[1 x]

- [a] Explain briefly the convergence division method.
- [b] Describe briefly Amdahl's law for a fixed workload.
- [c] What is the basic difference between broadcast and multicast in a network?
- [d] Explain a crossbar switch network with an example.

Q. 2

Explain the various techniques that help to smooth the pipeline flow, remove bottlenecks and connect memory access operations in the instruction pipeline design.

Q. 3

Explain different dependencies present amongst instructions in a program and how do we resolve them?

Q. 4

How do we perform fixed-point multiplication of 8-bit integers using a pipeline?

Q. 5

Give a description of the various shared-memory multiprocessor models.

(For Section – I & II Students only)

Q. 1

Ideally, a processor with an N-stage pipeline would execute with clock frequency N times faster than pipelined processor. Give two reasons why the clock frequency of a real pipelined processor would be less than N.

Q. 2

Explain the effect of following modifications on the performance of the processor perform equation: (a) incorporating a Branch Predictor in a processor (b) making a scalar processor superscalar.

Q. 3

Instruction Scheduling, whether static or dynamic, resolves dependencies between instructions, increase possible instruction level parallelism. Justify.

Q. 4

Briefly explain the reasons that caused multiprocessors to become common on the desktop / laptop.

Q. 5

For the following code segment, which predictor will perform better for B1 branch: Static Predictor or Dynamic Predictor?

```
for (i=0; i<10; i++)  
{ if (i%2) printf("%d\n",i); } //If Branch B1 is "Taken", printf is executed
```

Q. 6

In a 3-stage pipelined processor, S1 stage is used in clock cycle 1, 6, 8; S2 stage is used in clock cycles 3, 5, 7. Prove the lower bound and upper bound on the MAL for this processor.

Q. 7

Consider the following two designs for alleviating the effect of branches: (a) **First design** defines a branch with two delay slots and does not use branch prediction. Compile-time code scheduling is used to fill delay slots with useful instructions where possible. Suppose for 30% of the branch instructions, the compiler can fill both branch delay slots and for 60% of the instructions, only one delay slot can be filled. (b) **Second design** employs branch prediction and does not use delay slots. The mis-prediction penalty is 3 cycles. What prediction accuracy is required in the second design to achieve the same performance as the first design?

Q. 8

A pipelined processor has a clock rate of 1.25 GHz. It is used to run a program in which branches constitute 20% of the dynamic instruction count and 80% of all the branches are taken. The customer who runs the program requires that the processor must deliver a throughput of 1 million instructions per millisecond. The processor uses a 2-bit branch predictor with a branch target buffer (BTB) accessed in the IF stage of the pipeline. Branches which are incorrectly predicted, there is a penalty of 2 cycles. Calculate the minimum branch prediction accuracy required to satisfy the throughput demand.

-----X-----X-----

85