Time: 3:00 Hrs. Max. Marks: 70

Note: Q.-1 is compulsory. Attempt any four from the rest.
Assuming any missing data.
Attempt all parts of a question at the same place and start each question form a new page.

1. [a] Draw the flag register of 8085 and give the function of the various flags.

[b] At what stage in the machine cycle is the READY signal sampled by the processor?

[c] What is the function of $\overline{\text{RESETIN}}$ signal in 8085?

[d] Explain the instruction PCHL. Give the number of bytes, T-states, machine cycles and addressing modes of PCHL. Also mention the names of the machine cycles involved.

[e] What is the function of ADSTB in DMA controller?

[f] How is the RS232C serial bus interfaced to the TTL logic device?

[g] A TTL compatible clock signal of frequency 3MHz and 30% duty cycle is connected to X1 input pin of 8085. What is the system clock frequency and duty cycle of CLKOUT signal pin of 8085? [14]

2. [a] A system requires 16 KB EPROM, 16 KB RAM, two 8255, one 8251 and one 8253. Draw the interface diagram. Allocate addresses to all the devices. The peripheral ICs should be I/O mapped and foldback addressing is permissible. [10]

[b] Write a program to find the number of negative, zero and positive numbers from an array of 10 signal byte numbers. Store the selected negative, positive and zero numbers in three different arrays. [4]

3. [a] Explain the format of the SIM and RIM instruction. [4]

[b] Assume the 8085 returns to the main program after servicing RST6.5. It should be clear that while one interrupt is being serviced all other interrupts are disabled. Write a subroutine check whether RST5.5 interrupt is pending. If it is pending, then the program should enable RST5.5 without affecting any other

interrupts. Otherwise the program should enable all the interrupts and return to the main program. [4]

[c] Fig.-1 shows the handshaking of ADC 0801 with 8085 for conversion of analog data into digital data. It is given that the start of conversion of ADC is given on $\overline{WR}$ pin (pin no.3). Write a main program and subroutine to read the converted data and store in a mem location INDATA. [6]

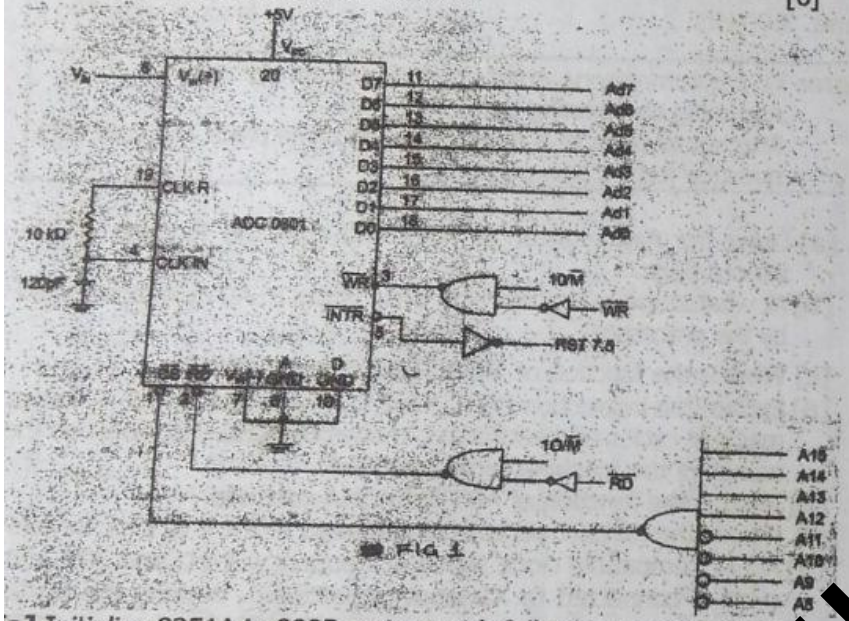


Fig. 1

a] Initialize 8251A in 8085 system with following specifications:
Asynchronous mode X16
7 bit character length
odd parity
2 stop bits

ASCII data is being received on an asynchronous serial link using 8251A. Write a program to do the following

i) Do nothing till four characters received match the password that is stored in locations 2100-2103. Following the password, a message of four bytes of data is received which ends at either a "." or a "$".

ii) If message ends at "." then do the following:
(a) Store the message in RAM at the mem location starting with BOSS.
(b) Transmit "SIR" on the serial link.

iii) If message ends at "$", then do the following
(a) Store the message in RAM at mem locations 2100-2103.
(b) Transmit "ALT" on the link.
The hex codes for the ASCII on the link

"."	2EH	"S" 53H	"R" 52H	"L" 4CH
"$"	24H	"I" 49H	"A" 41H	"T" 54H

[10]

[b] Draw and explain how an external latch is used to demultiplex the address and data bus in 8085. [4]

5. [a] Interface an 8254 to 8085. The address of the Control Register should be 5FH. Specify whether the 8254 is interfaced as I/O mapped or Memory mapped I/O device. Using a clock of 2MHz, write the set of instructions to generate an interrupt once after 1 sec. Also draw the interface diagram. [8]

[b] Explain the initialization command words of 8259A. Discuss the sequence of events that occur when one or more interrupt request lines ($1R_0$ to $1R_7$) in an 8259A go high. [3+3]

6. [a] Draw a complete schematic diagram showing the decode logic required to interface 8 push button keys and a common anode 7-segment LED to the 8085 using 8255. Write a subroutine programs to read the valid key press and store the corresponding key code in a mem location, and also to display the same on the seven segment LED. [8]

[b] Write a subroutine with three loops nested one inside the other. How much time delay does it produce if the clock frequency of 8085 is 2.5 MHz? [4]

[c] Reset all flags without performing any arithmetic or logic operation. [2]

7. [a] Draw the complete timing diagram of RSTn instruction. [4]

[b] Explain the mode-2 operation of 8255. [4]

[c] Explain the auto load option of DMAC 8257. [2]

[d] Write initialization instructions for DMA controller to initialize CH3 to transfer 4K bytes of data from floppy disk to system memory. Specify which control signals will be generated and the mode operation of DMA. [4]

-----X-----

Roll No._____
BE(COE)

End SEMESTER EXAMNATION May, 2013
COE -312: Information System and Data Management

Time: 3.00 Hrs

Max. Marks: 70

Note: Attempt any five questions.
All questions carry equal marks.
Assume missing data suitably, if any.

Q1a. Consider the following set of functional dependencies:

$F = \{A \rightarrow C, B \rightarrow AG, CD \rightarrow BE, E \rightarrow F, F \rightarrow D\}$

Prove that the functional dependency $BF \rightarrow ADG$ exists in the closure of F. (4)

b. Consider a relational schema R = (ABCDEFGH) and a set of functional dependencies F as given below:

$F = \{ AF \rightarrow B, AF \rightarrow E, AH \rightarrow GC, AHF \rightarrow C, B \rightarrow DE, H \rightarrow G\}$

Compute a minimal cover of F. (6)

c. Differentiate between 3NF and BCNF. (4)

Q2a. Differentiate between the following with the help of examples

i. Aggregation and Ternary relationship
ii. Primary Key and Super Key
iii. Composite and multivalued attributes

(12)

b. What do you mean by insertion anomaly? Give example. (2)

Q3a. Explain the views. Illustrate with the help of example. Discuss briefly materialized views. (5)

b. Discuss various states of a transaction. Differentiate between strict, rigorous and conservative 2PL protocol. (9)

Q4a. Discuss in detail Time stamp based concurrency control protocol. (8)

b. Critically examine the Time Stamp based protocol in view of deadlocks, serializability and starvation. (6)

Q5a. Consider the following relational schema:

Sales (OrderID, OrderDate, OrderPrice, OrderQuantity, CustomerName)
Products(Product_id,OrderId, Manufacture_Date, Raw_Material, Vendor_id)
vendor_info(Vendor_id, Vendor_name)
Vendor(Raw_Material, Vendor_id)

Answer the following queries in SQL and relational algebra:

i) Display total no. of orders placed in each year.

ii) Display all those customers who are ordering products of milk by smith.

iii) Display total no. of food items made from Bread, ordered every year.

iv) Display name of those vendors whose products sale per year is more than Rs. 200,000.

v) Delete those vendors from the database, who have not sold any product in last two years.

b. Define triggers? Give an example of Row level trigger for the above database. (10)

(4)

Q6a. Define various kinds of failure?

b. What do you mean by Log? Discuss Log based recovery techniques to recover form concurrently executing transactions. (3)

c. What do you mean by blocking factor? How does it affect the storage capacity in sequential storage devices? (7)

(4)

Q7. Write short notes on any two of the following:

a. Fourth and Fifth normal forms

b. Dependency preserving and lossless join decomposition.

c. Indexed sequential file organization.

(7X2)

COE-313
Time: 3.0 Hrs.

Operating Systems
Max. Marks: 70

Note:

- *Attempt any five Questions. All questions carry equal marks.*
- *Assume missing data suitably, if any.*

1a. What is safety algorithm? Discuss. Find if the following system is in safe state or not.

	Allocation	Max	Available
	A B C D	A B C D	A B C D
P0	0 0 1 2	0 0 1 2	1 5 2
P1	1 0 0 0	1 7 5 0	
P2	1 3 5 4	2 3 5 6	
P3	0 6 3 2	0 6 5 2	
P4	0 0 1 4	0 6 5 6	

9

b. What are various system threats? Discuss. 5

2a. Explain various methods of hardware protections. 6

b. Discuss process control block and explain CPU switching between processes. 8

3a. Differentiate between user level and kernel level threads. 6

b. Fragmentation on a storage device could be eliminated by recompaction of the information. Typical disk devices do not have relocation or base registers (such as are used in when memory is to be compacted), so how can we relocate files? Give three reasons why recompacting and relocation of files are often avoided. 8

4a. Describe different types of indexed allocation of memory in a file system. 4

b. Assume that the disk can perform a seek to an adjacent cylinder in 1 millisecond, and a full-stroke seek over all 5000 cylinders (numbered as 0 to 4999) in 18 millisecond. Assume that the drive is currently serving a request at cylinder 143, and previous request was at cylinder 125. The queue of pending requests, in FIFO order, is 86, 1470, 913, 1774, 948, 1509, 1022, 1750, 130. Answer the following:

i. Calculate the total seek time for C-LOOK and SSTF methods.

ii. The percentage speedup is the time saved divided by the original time. What is the percentage speed up of the C-SCAN over FCFS? 10

5a. Discuss the critical section problem in detail. Write the algorithm for the Dining Philosophers problem.

b. When a file is opened concurrently by several processes, should each process construct a separate file control block of its own to connect to the shared file, or should the involved processes share a single file control block? Discuss the relative merits of each approach, and propose a strategy that seems fit for managing the sharing of files. 6

6a. What does file structuring mean? Some operating systems design a file system as a tree structured but limit the depth of the tree to some small number of levels. What effect does this limit have on users? What are the advantages of this type of structuring? How does this simplify file system design, if it does at all? 8

b. What are differences between capability lists and access lists used for system protection? 6

7a. A password may become known to other users in a variety of ways. Is there a simple method for detecting that such an event has occurred? Explain your answer. 5

b. Discuss resource allocation graph. 4

c. Discuss memory management using segmentation hardware. 5

*****

Roll No.....

SIXTH SEMESTER **B.E. (COE)**

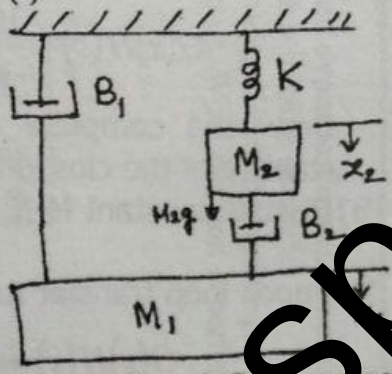
B.E. END SEM. THEORY EXAM. (May-June 2013)

COE-314 : CONTROL ENGINEERING

Time: 3:00 Hrs. Max. Marks: 70

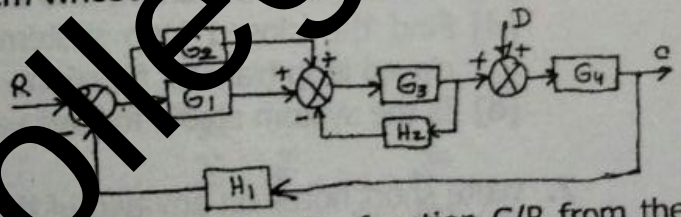
Note: Answer any five questions. Any missing data can be assumed. All questions carry equal marks.

1. [a] Mechanical system is shown in figure below. Obtain transfer function connecting the displacement of mass M_2 and the applied force $f(t)$.

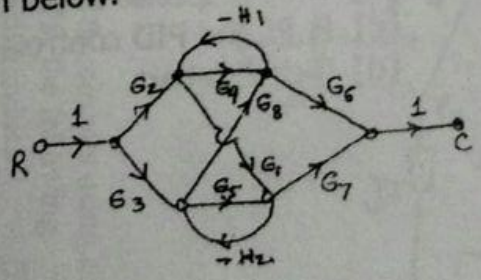


[b] Discuss the working of an A.C. servomotor. Also find out its mathematical modeling.

2. [a] Determine the ratio of C/R, C/D and the total output for the system whose block diagram is shown below.



[b] Obtain the overall transfer function C/R from the signal flow graph shown below.



equation of a system is

$$2s^5 + 2s^4 + 5s^3 + 5s^2 + 3s + 5 = 0$$

Use Routh criterion to determine stability.

[b] How feedback affects the sensitivity and dynamics of a control system? Explain.

4. Sketch Bode plot and find the acceleration error constant and the gain crossover frequency. The transfer function of the system is given as

$$G(s) = \frac{4(s+5)(s+10)}{s^2(s+20)}$$

5. [a] The transfer function of a system is given below

$$G(s)H(s) = \frac{10(s+3)}{s(s-1)}$$

Draw the complete Nyquist plot and then determine the stability of the closed loop system.

[b] Discuss constant M-N circles.

6. The open loop transfer function of a system is

$$G(s)H(s) = \frac{K}{(s+4)(s^2+4s+20)}$$

Draw the root locus for $0 \leq K \leq \infty$. Identify the following:

[a] Breakaway points and the value of K at these points.

[b] Critical value of K and the oscillation frequency.

[c] The angle of departure and the angle of arrival if any.

[d] Find the closed loop system poles for K=3000 and also closed loop transfer function.

[e] Is the system stable for this value of K?

Write short notes on any two of the following:

[a] Transportation lag

[b] Time response specifications of a second order system

[c] P, PI and PID controls

[d] Nichol's chart.

-----X-----

Roll No.....

B.E. (COE) 6th Semester END SEMESTER EXAMINATION, May 2013

COE- 315 Advanced Computer Architecture

Time: 3 Hrs. Max. Marks: 70

Note: Question 1 is compulsory. Attempt any 5 from the remaining. Attempt all parts of each question together. Assume suitable missing data, if any and specify it clearly.

Question 1 [2 x 10 = 20]

(i) Explain the relationship between grain size and communication latency.

(ii) What are different kinds of data dependencies? For each of them, illustrate one compiler / hardware driven technique to remove it.

(iii) Compare a hypercube static network with a Binary tree in terms of various network parameters.

(iv) Write down the major advantages and disadvantages of VLIW processors.

(v) Illustrate with an **application,** the speedup of Guftanson's scalability law.

(vi) Write down two concrete iteration vectors that cause a true dependence in statement S1 in LoopNest.

LoopNest (For Q 1.vi)

```
for (i=1; i<=N; i++) {
    for (j=1; j<=M; j++) {
        for (k=1; k<=L; k++) {
            A[i+3, j-1, k] = A[i, j+1, k+1] + 7;  // S1
        }
    }
}
```

(vii) Comment on the statement: Superscalar processors require more transistors whereas superpipelined processors require faster transistors.

(viii) How does "Delayed Branch" reduce the branch penalty? Is it a purely hardware solution? Justify your answer.

(ix) Why does loop unrolling may increase the processor performance? What is the possible disadvantage of this technique?

(x) Explain how the memory order of load operations may not follow the program order in a TSO weak consistency model? [3 + 4 + 3 = 10]

Question 2

(a) Derive the maximum throughput latency sequence for a 3-stage pipeline in which 1, 3 and 6 are the permissible latencies.

(b) Design an algorithm to find the maximum of n numbers in O(log n) time using O(n) processors on an EREW-PRAM model. Assume that initially each location holds one input value.

(c) Differentiate between predictive and speculative execution. [4 + 6 = 10]

Question 3

(a) A three-stage Omega Network connects eight processors numbered P0, P1, … P7 to eight independent memory modules numbered M0, M1, . . . M7. Draw the network. Highlight the following connections through the network: P0 → M2, P4 → M4, P6 → M3. Can these accesses be performed concurrently or do they conflict?

(b) Explain whether the following loops vectorizable / parallelizable? If the code fragment is vectorizable / parallelizable, show how.

(i)
```
for (i = 0; i < 64; i++)
{
    a[i] = b[i] + c[i];
    d[i] = a[i] - e[i];
}
```

(ii)
```
for (i = 0; i < 64; i++)
{
    a[i] = b[i] + c[i];
    c[i+1] = e[i] - g[i];
}
```

(i)
```
for (i=1; i<n; i++)
{ for (j=0; j<n; j++)
    A[i][j] = A[i-1][j];
}
```


(12)

Question 4 [4 + 6 = 10]

(a) A symmetric shared memory multiprocessor has four processors (P0 through P3), each with a direct-mapped write-back data cache supporting Snoopy Cache Coherence Protocol. Each cache has 8 blocks and each block is 8 bytes long. All cache blocks in all caches have state *Invalid* before the following instructions are executed:

Inst a executed by P2:	*SD R2, 0x10*	*; Mem[0x10] ← R2*
Inst b executed by P1:	*LD R2, 0x88*	*; R2 ← Mem[0x88]*
Inst c executed by P3:	*SD R3, 0x12*	*; Mem[0x12] ← R3*
Inst d executed by P3:	*SD R8, 0x0A*	*; Mem[0x0A] ← R8*
Inst e executed by P0:	*LD R2, 0x28*	*; R2 ← Mem[0x28]*

Determine the block number in various caches that are affected after each of the above instructions have completed. What will be the TAG field and state of those cache blocks?

(b) Show the resulting code after applying the Software Pipelining technique on the following loop at the C source code level itself (i.e. do not change the code to assembly level). Assume that each operation takes three clock cycles.

```
for (i=1000, i >= 1, i--)
{
        t = x[i] ;
        g = t + 10 ;
        x[i] = g ;
}
```

Question 5 [4 + 6 = 10]

(a) An application running on 10 processors spends 3% of its time in inherially executable portion of code. Compute the Scaled speedup of this application. Do you get the same amount of speedup using Amdahl's law also? Show your analysis in support of your answer.

(b) Draw the structure of a Batcher's 4 x 4 Odd- Even Merging Network. Clearly, explain various steps of the algorithm that are implemented in various sections of the drawn structure. Choosing an appropriate input illustrate the working of this Merging Network. Also, explain the construction of an 8-input Sorting System using the repetitive use of this Merging Network.

OR (for part b)

Develop an algorithm for matrix multiplication on a pipelined mesh architecture. Relate the size of the matrices with the mesh dimensions. Evaluate the complexity of the algorithm by taking into account the computation time as well as the communication time. Illustrate the progress of the matrix computations on the mesh architecture at different steps.

Question 6 [4 + 6 = 10]

(a) Say IC is the total instruction count of a program, CT is the clock cycle time of the processor and CPI is the cycles per instruction for the processor. How will you find the CPU time needed to execute the program? How do the following techniques affect the three parameters: CISC / RISC ISA, Pipelining, Improvement in Fabrication Technology, Compiler Optimizations, Multi-level Memory, Branch Predictor?

(b) Draw the program graph of the 16 instruction nodes mentioned below. How many steps are needed if maximum amount of available parallelism is exploited? Now, assume a **three-issue superscalar processor** that can issue one memory-access instruction, one add/subtract instruction, and one multiply instruction per cycle. Find the minimum number of steps needed to issue these 16 instructions.

1) LOAD R1, A	5) MUL R5, R1, R4	9) MUL R8, R7, R4	13) ADD R11, R6, R10
2) LOAD R2, B	6) ADD R6, R3, R5	10) LOAD R9, E	14) STORE U, R11
3) MUL R3, R1, R2	7) STORE X, R6	11) Add R10, R8, R9	15) SUB R12, R6, R10
4) LOAD R4, D	8) LOAD R7, C	12) STORE Y, R10	16) STORE V, R12

Question 7 [4 + 4 + 2 = 10]

(a) Explain with an illustrative example whether a 1-bit or 2-bits branch history would perform better in predicting the direction of a branch that changes its direction every two executions?

(b) Compare the complexity of prefix computations on a PRAM model and on a linear array.

(c) Illustrate the loop coalescing technique.

---------x---------x---------