(b) Write the advantages and disadvantages of low-order and high-order memory interleaving. Also, compare S-access with C-access memory interleaving.

(c) Write the processor performance equation. How do the following affect various terms of the processor performance equation: Instruction Set Architecture, Better Fabrication Technology, Compiler Optimization, and Instruction Pipelining.

Question 6 [6 + 4 + 4]

(a) Explain various categories of dependence tests.

(b) What are the various causes of cache coherence problem in multi processor systems?

(c) Show with example the role of node duplication scheme in static multiprocessor scheduling.

Question 7 [3.5 x 4 = 14]

(a) Variants of PRAM model

(b) Shared memory Multi-processor models

(c) Loop Vectorization Methods

(d) Unimodular Loop Transformations

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Total No. of Pages: 2

B.E. (COE) 6th Semester

Roll No:.....

END SEMESTER EXAMINATION, May 2015

COE- 315 Advanced Computer Architecture

Time: 3 Hrs.

Max. Marks: 70

Note: Attempt any 5 questions. Attempt all parts of each question together. Assume suitable missing data, if any and specify it clearly.

Question 1 [4 + 10]

(a) What is the relation between a dependency and a hazard? Which techniques a compiler can employ to minimize / remove the effect of various types of dependencies? Explain with example.

(b) For the following reservation table of a pipeline processor, give the list of the forbidden latencies, the collision vector, the state diagram, the minimum average latency and all greedy cycles. Explain the procedure to optimize the MAL. Have you obtained the optimal MAL? If not, achieve it.

	1	2	3	4	5	6	7
S1	X			X			
S2		X					X
S3			X				
S4					X		
S5						X	

Question 2 [4 + 10]

(a) Why do following optimizations increase available parallelism? Also, list the limitation of each technique. (i) Software Pipelining (ii) Loop Unrolling

(b) Draw the structure of a Batcher's 4 x 4 Odd- Even Merging Network. Clearly, explain various steps of the algorithm that are implemented in various sections of the drawn structure.

Question 3 [7 + 7]

(a) Explain the Write-invalidate Snoopy Protocol for Write-back caches.

(b) Explain the difference between Blocking, Non-blocking and Re-arrangeable networks. Show the recursive construction of a 16x16 blocking network.

Question 4 [7 + 4 + 3]

(a) Show that 8x8 Cube network has the same interconnection topology as 8x8 Omega network.

(b) A processor has a non-linear pipeline with 4 stages A, B, C and D. Each instruction goes through different stages in the following order A B C B A D C. Find the bounds on the maximum instruction throughput in a static hazard free schedule.

(c) Differentiate between Amdhal's law and Gustafson law.

Question 5 [5 + 5 + 4]

(a) Draw Illiac Mesh, Torus, Chordal Ring of degree 3, 16 nodes Hypercube, and Cube connected Cycle static networks. Write down their node degree, diameter, and bisection width.

(b) Derive the expression for time response of second order control system subjected to unit step input. (7)

Q4. A unity feedback control system has an open loop transfer function

$$G(s)H(s) = \frac{K}{s(s+2)(s^2+2s+5)}$$

Draw the root locus as the value of K changes from 0 to ∞. Also find the value of K and the frequency at which the root loci crosses the jw-axis. (14)

Q5. Draw the polar plot and find out the crossover frequency and corresponding magnitude for the system given below. (14)

$$G(jw) = \frac{1}{jw(1+jw\tau_1)(1+jw\tau_1)}$$

Q6. Draw the bode plot for the system having the transfer function as follows:

$$G(s) = \frac{10(1+0.1s)}{s(1+0.5s)(1+0.2s\ )}$$

Calculate the gain margin and phase margin also. (14)

Q7. Draw the Nyquist plot for the open loop transfer function given below and comment on stability of the closed loop system. (14)

$$G(s)H(s) = \frac{K}{s^2(\tau s+1)},\ \tau > 0, K > 0$$

Q8. Write notes on any two of the following: (7x2=14)

(a) Synchros

(b) Constant M-N Circles

(c) Geared Drives

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Name..... R. No.....

End Semester Examination, May-2015
VIth Semester, Computer Engineering
Control Engineering (COE-314)

Time: 3:00 hrs M.M:70

Note: Attempt any five questions.

All questions carry equal marks. Assume any suitable data, if missing.

Q1 (a) Calculate the transfer function of the following mechanical system x(s)/F(s). (7)

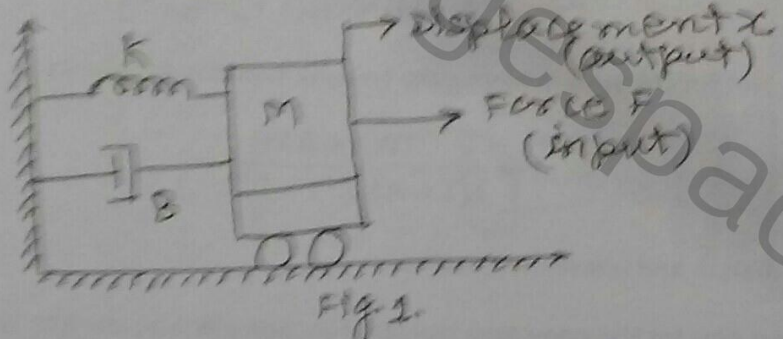

Fig-1.

(b) Calculate the transfer function of the signal flow graph using Mason's gain formula. (7)

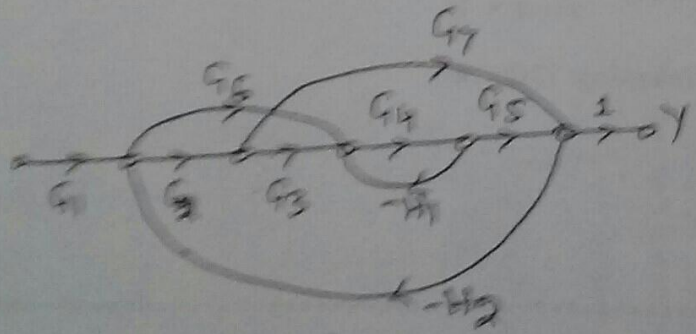

Fig-2

Q2 (a) Derive the transfer function of armature controlled Dc motor with load. (7)

(b) What do you mean by stability? Determine the value of K such that the system is stable. (7)

$$q(s) = s^6 + 3s^5 + 8s^4 + 12s^3 + 20s^2 + 16s + K$$

Q3 (a) Determine the position, velocity and acceleration error constants for type-1 system for unity feedback control whose open loop transfer function is given as follows: (7)

$$G(s)H(s) = \frac{5}{(1+0.2s)(1+0.5s)}$$

Q4. (a) A system has a physical memory of 512 KB and uses a contiguous memory allocation scheme. The following sequence of events occurs in the system: the operating system (300 KB) is loaded, P1 (50 KB) arrives, P2 (50 KB) arrives, P3 (50 KB) arrives, P2 terminates, P1 terminates, P4 (40 KB) arrives, P5 (40 KB) arrives, P3 terminates, P6 (40 KB) arrives, P7 (40 KB) arrives, and P8 (40 KB) arrives. Determine whether the best-fit or the worst-fit strategy will be able to allocate memory to all the processes.

(b) Explain the Segmented paging with an example ? Why it is more popular ? [7+7]

Q5. (a) What is a page fault? How does an operating system handle a page fault?

(b) A process has been allocated three frames. The reference string is as follows: 0 , 9 , 0 , 1 , 8 , 1, 8 , 7 , 8 , 7 , 1 , 2 , 8, 2 , 7 , 8 , 2 , 3, 8 ,3. Determine using whether the LRU algorithm or the second-chance algorithm for page replacement will result in lesser page faults. [7+7]

Q6. (a) Differentiates the following with taking suitable examples (any two)

(i) process & threads (ii) logical file system & basic file system

(iii) FCB & PCB

(b) The cylinders of a hard disk are numbered 0 to 99. The read/write head is currently positioned at cylinder 34 and is moving in the direction of cylinder 99. The disk queue has requests to access blocks on cylinders 73, 41, 65, 11, 59 and 88. Determine whether SCAN scheduling or C-LOOK scheduling will provide a better result. [7+7]

Q7. Write short notes on the following (any two)

(i) DMA (ii) Computer Virus (iii) System calls (iv) Kernel I/O subsystem [7+7]

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Total No. of Page(s): 2

Roll No.....

SIXTH SEMESTER **B.E. (COE)**

B.E. END SEM. EXAMINATION, MAY-2015

COE-313 Operating Systems

Time: 3:00 Hrs. Max. Marks: 70

Note: Attempt any **five** questions.

Q1. (a) How does a process differ from a program? Describe how a process changes its state during its lifetime.

(b) A system has five processes whose details are given below. Calculate the average waiting time of the processes (i) if non-preemptive priority scheduling is used and (ii) if preemptive priority scheduling is used.

Process	Arrival time (ms)	Burst time (ms)	Priority
P1	0	20	7
P2	2	4	0 (highest)
P3	8	10	4
P4	10	6	2
P5	20	10	6

[7+7]

Q2. (a) What is a race condition? How is it related to the critical-section problem?

(b) Modify Peterson's solution so that it works for three processes. Show that the modified solution satisfies the requirements of a solution to the critical-section problem. [7+7]

Q3. (a) What is a deadlock? What are the necessary conditions for a deadlock to occur? What are the different methods to handle deadlocks?

(b) A system has six processes, P1 to P6, and four resource types. The system is in a safe state with Available = [1 1 1 1], Max = $\begin{bmatrix} 2&4&4&3 \\ 2&1&1&2 \\ 5&1&0&5 \\ 2&0&0&2 \\ 2&1&2&3 \\ 5&0&1&5 \end{bmatrix}$ and Allocation = $\begin{bmatrix} 1&3&3&3 \\ 1&0&1&0 \\ 0&0&0&1 \\ 0&0&0&0 \\ 1&1&2&2 \\ 1&0&0&0 \end{bmatrix}$.

Use the resource-request algorithm to show that a request [1 1 1 0] from P1 can be granted. Use the safety algorithm to check if the resultant state will be safe. [7+7]

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(iii) Explain how referential integrity rules can be applied to these relations [6]

Q.5 (a) Consider a 'Video Rental System'. Develop an ER model using all the rules. Consider appropriate keys, entities, relationships, constraints, mapping Cardinalities, generalization/ specialization etc. [10]

(b) Differentiate between DDL and DML. [4]

Q. 6 (a) What are the ACID properties of any transaction? What are the various states through which any transaction may pass.? Explain why each state transition may occur with the help of diagram. [8]

(b) What are triggers and assertions? Explain with the help of suitable examples and write the SQL statements for the same. [6]

Q. 7. Write short notes on any four.

(i) Security
(ii) Data independence
(iii) Views
(iv) Checkpoints
(v) Graph based protocol
(vi) Relational calculus
(vii) Network and hierarchical model

[14]

Total no of pages : 2

Roll no :.....
BE (COE) Sixth Semester

B.E. END SEMESTER EXAMINATION, MAY 2015
COE - 312 : ISDM (Information System and Data Management)

Time : 3:00 Hrs. Max Marks: 70

Note : Attempt any five questions. Assume suitable missing data, if any.

Q.1(a) Explain the log based recovery mechanisms with suitable examples in detail. [8]

(b) What are integrity constraints ? Give the SQL statements to define various integrity constraints. [6]

Q. 2(a) What is an index? What are the various types of indexes that can be created? How many clustered indexes can be created for particular table? If we can create a separate index on each column of a table then what are the advantages and disadvantages of using this approach? [8]

(b) What is serializability ? How it can be maintained using two phase locking protocol ? Give example. [6]

Q.3(a) What is normalization ? What are functional and multivalued dependencies ? Explain the various normalizations which can be done using functional dependencies and multivalued dependencies. [8]

(b) What do you mean by deadlock ? Describe the actions which can be taken to recover from deadlock using suitable example. [6]

Q.4(a) Consider the following database schemas
Hotel (hno, hname, hcity)
Room (rno, hno, type, price)
Booking (hno, gno, datefrom, dateto, rno)
Guest (gno, gestname, gestaddress, gestbill)
Give the relational alzebra expressions and SQL statements for each of the Following

(i) Find the number of guests staying in the 'ABC' hotel on 25/4/2015.
(ii) Find the dates of room number 102 occupied by guest 'Parkash'.
(iii) Find the total income of all the distinct hotels in the month of jan, 2015.
(iv) Find the list of hotels those who have rooms with price 2500 per day. [8]

(b) Answer the following using above database schemas
(i) Identify the foreign keys in the given schemas.
(ii) Is the given schema normalized? If yes, then tell till which NF.

count numbers from 00 to 99 and reset to 00 after reaching 99 and increment every 1s. Assume that the crystal frequency of the 8085 is 2 MHz. Write the 1-second delay routine also. **[7 marks]**

4. [a] Write 8085 assembly code to multiply two 8-bit numbers using the shift and add method. The two numbers are stored in memory locations 2000h onwards. Result of the operation should also be stored in subsequent memory locations. **[7 marks]**

   [b] Write 8085 assembly program to generate a 30% duty cycle PWM waveform with 1 Hz frequency on the SOD pin of 8085 if the SID pin is '0' and 60% duty cycle if SID pin is '1'. The state of the SID pin should be checked at the beginning of every PWM cycle. **[7 marks]**

5. [a] The IOR* and IOW* pins of 8257 DMAC are bidirectional where as MEMR* and MEMW* pins are unidirectional. Why? What is the function of AEN and ADSTB pins of 8257? Explain with a suitable diagram. **[7 marks]**

   [b] If an 8251 USART is operated in asynchronous mode, describe the bit configurations for the mode and command instructions. Write 8085 assembly code to reset 8251 and then transmit data at 9600 bits per second, 8 data bits, no parity and 1 stop bit. Show appropriate signal pin assignments. **[7 marks]**

6. [a] For an 8279 keyboard and display controller connected to an 8085 and mapped as an I/O port at base address 20H, write code to poll the 8279 to find if a key code is available in the FIFO and to read when it is available. Also, explain all the keyboard scan modes. **[7 marks]**

   [b] What is the purpose of OCW1, OCW2 and OCW3 in 8259 PIC? Explain in detail. **[7 marks]**

7. Write short notes on:
   (a) 8254 modes of operation. **[7 marks]**
   (b) 8255 input and output operation in mode 1. **[7 marks]**

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Roll No..... *Date* .....

Sixth SEMESTER B.E. (ECE/COE/ICE)

END SEMESTER EXAMINATION, May-2015

EC/COE/IC-311: Microprocessors

Time: 3:00 Hours **Maximum Marks: 70**

Note: Question 1 is compulsory. *Attempt five questions in all.*

1. [a] Explain the operation of the following 8085 pins: (a) RST OUT, (b) HOLD, (c) Ready, (d) IO/M*, (e) S0 and S1, (f) TRAP and (g) ALE. **[7 marks]**

   [b] Write 8085 assembly program to shift a 16-bit number in BC register pair by 1 bit if CY flag is set and 2 bits if the CY flag is clear. **[3 marks]**

   [c] List all the machine cycles of 8085 and describe the operation of the longest machine cycle. **[4 marks]**

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2. [a] What function does PCHL instruction performs in 8085? Draw the timing diagram for PCHL. **[7 marks]**

   [b] PCHL offers a very unique operation in 8085. However, assume that PCHL instruction is not available to you. Write alternative code sequence to perform identical operation to PCHL. **[3 marks]**

   [c] Explain the contents of the appropriate register after executing the RIM instruction. **[4 marks]**

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3. [a] Design an 8085 system with 16KB EPROM and 16KB RAM, one 8255 (Programmable Peripheral Interface) and two additional output ports using 74373 latches. The latches are connected to two common anode seven segment displays. Draw the interface diagram. Allocate appropriate addresses to all the devices. The peripheral ICs must be IO-mapped. **[7 marks]**

   [b] Write 8085 Assembly language program for the above system, to display a BCD up counter on the two seven segment displays. It should

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