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FIFTH SEMESTER B.E. (COE)
B.E. MID SEM. EXAMINATION, September 2015
COE-301 PRINCIPLES OF COMPUTER GRAPHICS

Time: 1 1/2 Hrs Max. Marks: 20

Note: Answer all the Questions
Assume suitable missing data, if any

Q1. Show the steps how to evolve midpoint approach in order to scan convert an Ellipse in 3rd quadrant. Also show the steps by digitizing the ellipse, where values of a,b are 5,3 respectively.

[3.5, 1.5]

Q2. (a) Scan Fill the polygon (Refer Fig. 1) by vertical line scanning (Left to Right)and

- Constructing the Global Edge Table.
- Traversing the Active Edge Table

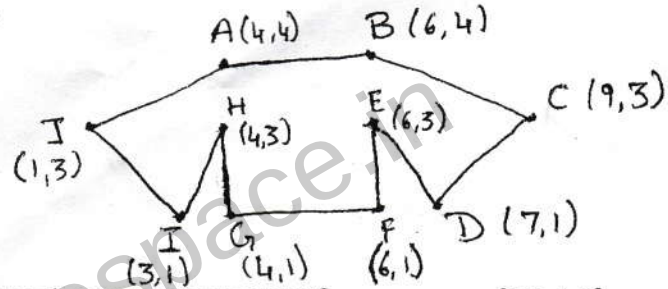

Fig. 1

(b) Write a function that determines whether a polygon is a concave or convex? [3.5, 1.5]

Q3. (a)Reflect the triangle ABC about the line 3x-4y+8=0. The position vector of the triangle ABC is given as A(4,1), B(5,2) , C(4,3).

(b) Perform clipping of the polygon (Refer Fig. 2) using Weiler Atherton clipping algorithm

Clipped Polygon : A B C B E F

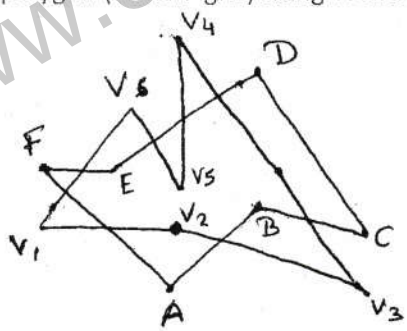

Fig. 2

Subject Polygon
$V_1 V_2 V_3 V_4 V_5 V_6$

V_1	(1,3)	A	(3,2)
V_2	(3,3)	B	(4,4)
V_3	(6,2)	C	(6,3)
V_4	(3,6)	D	(4,6)
V_5	(3,4)	E	(2,4)
V_6	(2,5)	F	(1,4)

[2, 3]

Q4. Perform clipping of the line AB against a triangular window XYZ (Refer Fig. 3) using
(a) Cyrus Beck algorithm and (b) Nicholl lee Nicholl algorithm

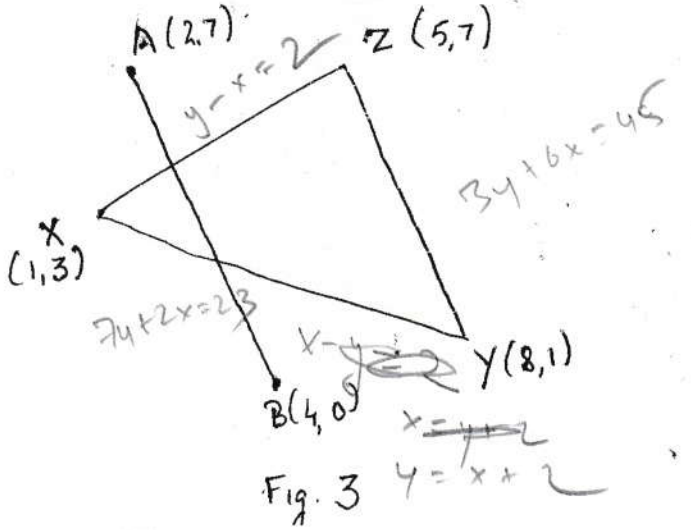

Fig. 3

[2.5X2]

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B.E.(COE) Vth Semester

MID SEMESTER EXAMINATION, SEPTEMBER – 2015
COE – 302 : DMDA (DISCRETE MATHEMATICS
AND DESIGN OF ALGORITHM

Time : 1:30 Hours

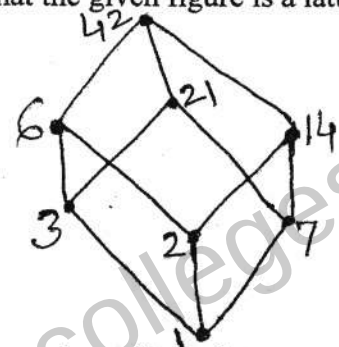
Max Marks : 20

Note : Attempt all questions. Assume suitable missing data, if any.

Q.1 : What is predicate? How will you represent the following statements using predicate calculus.
(a) Mark is poor but happy.
(b) Mark is poor or he is both rich and unhappy. [3]

Q.2 : Show that (RVS) follows logically from the premises (CVD) where
(CVD) -> ~H, ~H -> (A/\ ~B) and (A/\ ~B) -> (RVS)
Also indicate the rules used. [3]

Q.3 : What is a lattice? Prove that the given figure is a lattice or not, where
D= {1,2,3,6,7,14,21,42}



[3]

Q.4 : Construct a set of natural numbers. Show that a set of real numbers between 0 and 1 is not a countably infinite set. [3]

Q.5 : Let R be binary relation on the set of all positive integers such that
R = { (a, b) | (a-b) is an odd positive integer}
Find whether it is equivalence relation or partial ordering relation? [3]

Q.6 : Explain with examples (any two)
(a) Well formed formulas.
(b) Lexicographic order.
(c) Normal forms.
(d) Sets and Multisets. [2.5x2=5]

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Roll. No. 231/CO/13

B.E. MID SEMESTER EXAMINATION September, 2015

COE/EC-303: COMPUTER SYSTEM ARCHITECTURE

Time: 1:30 Hrs. **Max.Marks: 20**

Note: Answer all the questions. Assume any missing information, if any.

Q1 Write 3 address, 2 address, 1 address and 0 address instruction formats for the following instruction

$$x= (A-B+C*(D*E-F)) / (G+H*K) \quad (2)$$

Q2 What are interrupts. Explain the interrupt cycle with flow chart? (2)

Q3 An instruction is stored at location 251 with its address field at location 252. The address field has value 973.A processor register R1 contains the number 9. Evaluate the effective address if the address mode of the instruction is

a) Direct
b) Immediate
c) Relative
d) Index with R1 as index register. (2)

Q4 Explain the difference between

a) Arithmetic shift and Logical shift
b) RISC and CISC
c) Encoder and De-multiplexer
d) Software interrupt and Hardware interrupt (4)

Q5 What is the significance of assembler while designing CPU with Micro-Programmed control unit? Explain with suitable example. (4)

Q6 Design a CPU that meets the following specifications. (6)

- It can access 256 words of memory, each word being 8 bits wide. The CPU does this by outputting an 8 bit address on its output is A[7..0] and reading in 8 bit value from memory on its input D[7..0]
- The CPU contains an 8 bit address register, program counter and accumulator, data register and 3 bit instruction register.
- The CPU must realize the following instruction set. Note that α is a 8 bit value stored in location immediately following the instruction

Instruction	Instruction Code	Operation
LDI	000XXXXXα	AC <-- α
STO	001XXXXXα	M[α] <-- AC
ADD	010XXXXXα	AC <-- AC=M[α]
OR	011XXXXXα	AC <-- ACVM[α]
JUMP	100XXXXXα	PC <-- α
JREL	101XXXXXα	PC <-- PC+ 000AAAAA
SKIP	110XXXXXα	PC <-- PC+1
RST	111XXXXXα	PC <-- 0, AC<--0

MID-SEM EXAMINATION SEPT 2015

BE V SEM EC/COE/IC

EC/COE/IC 304 LINEAR INTEGRATED CIRCUITS

Time: 90 minutes Max. Marks: 20

Note: Attempt all questions; all carry equal marks.

[1] Assuming ideal op-amps, determine an expression for the input admittance $Y_{in}(s)$ of the circuit of Fig. 1. Draw a simple equivalent circuit of the realized admittance function with element values clearly shown.

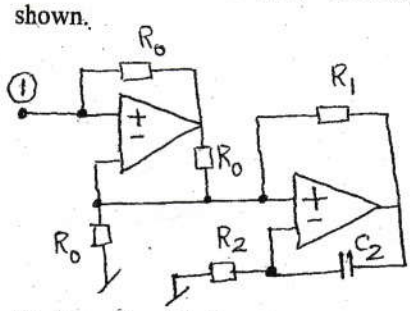

Fig. 1

[2] Assuming ideal op-amps, analyze the sinusoidal oscillator circuit of Fig. 2 and derive its condition of oscillation and frequency of oscillation. Which circuit element should be made variable to obtain variable frequency oscillations?

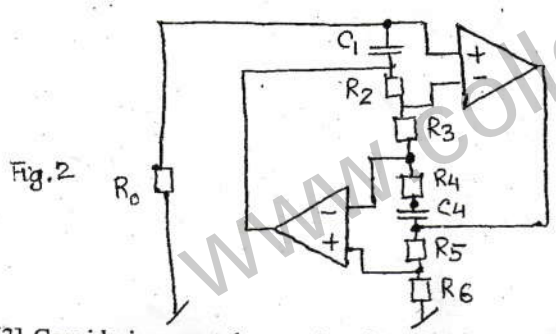

Fig. 2

[3] Considering open loop gain of the op-amp to be finite and frequency-dependent, derive the non-ideal transfer function of the circuit of Fig. 3 and hence, determine the type of filter realized by this circuit. What is the maximum value of the pole Q which can be realized by this circuit?

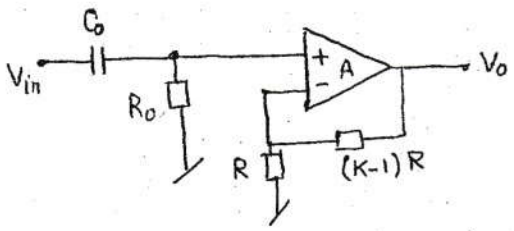

Fig. 3

[4] Fig. 4 shows an active-compensated inverting integrator. Using usual approximation for the non-ideal gains of the two op-amps, show that the non-ideal transfer function of the circuit is given by:

$V_{out}/V_{in} = -(1/sC\,R)\,\varepsilon(s)$

where $\varepsilon(s)$ is the 'error function'. From the error function, deduce an expression for the approximate phase error introduced by the finite gain-bandwidth-products of the op-amps and determine the condition under which this phase error can be made negligibly small.

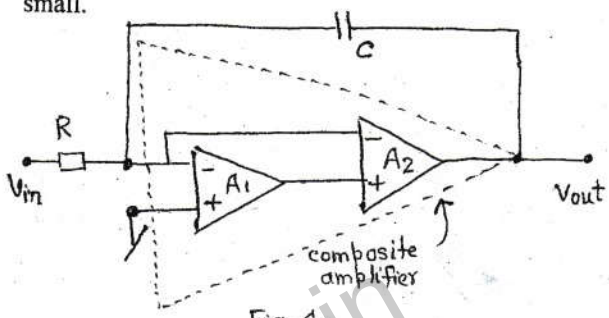

Fig. 4

[5] Explain how the log/antilog module shown in Fig. 5 can be used: (i) as a log amplifier (ii) as an antilog amplifier.

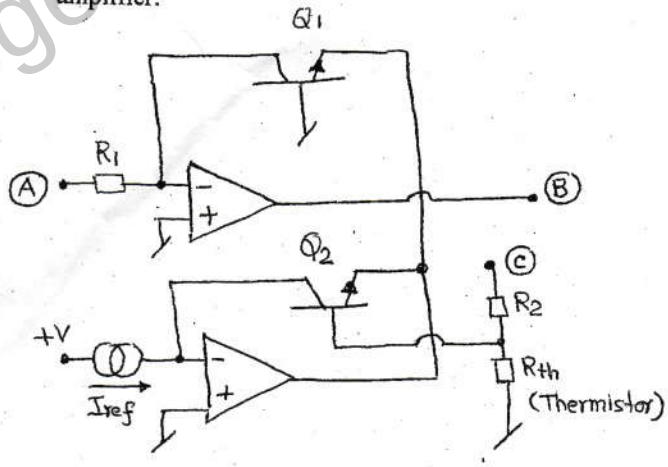

Fig. 5

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FIFTH SEMESTER **B.E. (EC/COE/IC)**

B.E. MID SEM. EXAMINATION, SEPT 2015

EC/COE/IC -305: INDUSTRIAL ORGANISATION AND MANAGERIAL ECONOMICS

Time: 1:30 Hrs. Max. Marks: 20

Note: *Attempt any five questions.*
All questions carry equal marks.
Assume suitable missing data, if any.

1. Why is Fredrick Winslow Taylor called the 'father of scientific management'? Explain his most important contributions to the field of management. [4]

   OR

   Explain major contributions of Henry Fayol to administrative approach to management.

2. What are the important factors that influence choice of plant locations? [4]

   OR

   What information is essential for determining a suitable layout for a manufacturing plant?

3. What are traditional and future oriented performance appraisal methods? Explain briefly. [4]

4. Explain important types of organizational structure with suitable examples. [4]

5. With the help of activities given below draw a network diagram. Determine its critical path, earliest start time, earliest finish time, latest start time, latest finish time, total project duration, total float, free float, and independent float. [4]

Activity	*Duration (in weeks)*
1-2	10
1-3	8
1-4	9
2-5	8
4-6	7
3-7	16

3-7	16
5-7	7
6-7	7
5-8	6
6-9	5
7-10	12
8-10	13
9-10	15

6 What is job evaluation? Why is it necessary for any business organization? [4]

7. Write short notes on any two. [4]

i) MBO

ii) Industrial Psychology

iii) Labour in India

iv) Management skills and levels of Management

v) Production and Productivity

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