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B.E. (COE)

SIXTH SEMESTER

B.E. MID-SEMESTER EXAMINATION, FEB-MAR 2016

COE 311 Microprocessors

Time: 1:30 Hrs. Max. Marks: 20

Attempt any four questions.

1. (a) Define: microprocessor, microcontroller and microcomputer.
   (b) Draw a block diagram of the Intel 8085 microprocessor showing all its pins. [3+2]

2. Describe the use of the following pins of the Intel 8085 microprocessor.
   (a) The bidirectional pins
   (b) ALE
   (c) IO/$\overline{M}$, $\overline{RD}$ and $\overline{WR}$
   (d) READY
   (e) $\overline{RESET\ IN}$ and RESET OUT [5x1]

3. (a) What are 1-byte instructions, 2-byte instructions and 3-byte instructions of the Intel 8085 microprocessor? Explain with examples.
   (b) What are the different addressing modes supported by the Intel 8085 microprocessor? Explain them with examples. Justify the utility of each addressing mode for an assembly language programmer. [2+3]

4. Write a program to find the smallest number greater than 10H in a list stored in the memory locations 2001H through 200AH. Store that number at the memory location 200BH. [5]

5. Study the following program written in the assembly language of the Intel 8085 microprocessor.

```
Loop: MVI A, 10H
      OUT 10H
      DCR A
      JNZ Loop
      HLT
```

   (a) How many bytes will be required to store the machine language equivalent of the program?
   (b) How much time will be required to execute the program? Assume that the microprocessor is operating with a frequency of 3MHz.

(c) Draw the timing diagram for the instruction OUT 10H which is stored in the memory locations 2003-04H showing the signals at the A_{15}-A_8, AD_7-AD_0, ALE, IO/$\overline{M}$, $\overline{RD}$ and $\overline{WR}$ pins. Opcode of OUT is DBH. **[1+2+2]**

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SIXTH SEMESTER **B.E. (ECE)**

MID SEMESTER EXAMINATION, Feb/March 2016

EC– 311: MICROPROCESSORS

Time: 1-½ hrs *Max. Marks: 20*

NOTE: Assume and mention any missing data.
Attempt all questions.

Q 1 a) Write a program for displaying binary up counter at an output port connected at 60H. Counter should count number from 00H to FFH and it should increment after every 1ms. The operating frequency of 8085 is 2MHz. [3]

b) The content of accumulator is 31H; CY=1 and AC=1 after arithmetic addition. What will be the contents of accumulator after the DAA operation? [2]

Q 2 a) Draw the timing diagram for RET instruction. [4]

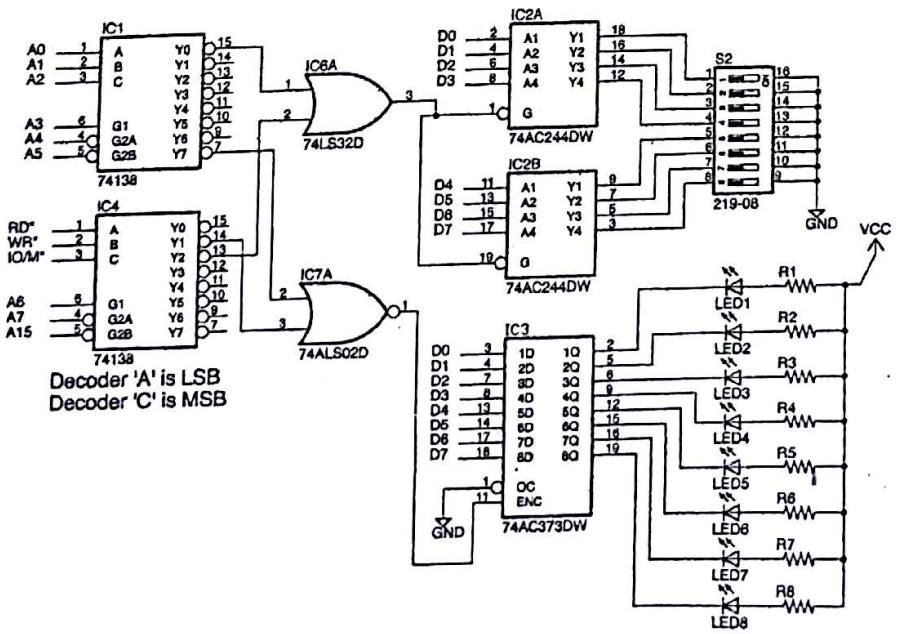
b) The 8085 microprocessor executes program given below, how many times does the 'ADD B' operation takes place? Explain! [1]

```
MVI A, 10H
MVI B, 10H
L1: ADD B
RLC
JNC L1
```

Q 3) a) A set of eight bytes data is stored in the memory location starting as 2070H. Write a program to check each data byte for bit D0 and D7. If D7 or D0 is 1 reject the data byte otherwise store the data byte at memory locations starting at 3070H. [3]

b) Two EEPROM ICs of size 8Kbytes each are interfaced with 8085 microprocessor. One has starting address 2000 H and the other starts at E000 H. Draw the interface diagram. [2]

Q4) What sort of ports are being used in the figure below? Identify the port addresses. Write instructions to read the input port and continue to read it until all the switches are closed. When all the switches are closed, turn on all the LEDs and terminate the program. [5]



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BE (COE) Sixth Semester

B.E. MID SEMESTER EXAMINATION, March 2016
COE - 312 : ISDM (Information System and Data Management)

Time : 1:30 Hrs.

Max Marks: 20

Note : Assume suitable missing data, if any.

Q.1: Differentiate between the following with the help of suitable examples. [10]

(i) DDL and DML
(ii) Logical and physical data independence
(iii) Candidate key and super key
(iv) Relational algebra and Tuple relational calculus
(v) Strong and week entities

Q.2 : Consider the following database schema [9]

MEMBER(MEM_ID, MEM_NAME, BRANCH, YEAR)
BOOK(BOOK_ID, BOOK_NAME, BOOK_AUTHOR, PUBLISHER)
ISSUE(MEM_ID, BOOK_ID, ISSUE_DATE)
RETURN(MEM_ID, BOOK_ID, RETURN_DATE, FINE)

Answer the following queries in relational algebra, tuple calculus and SQL

(i) Find the members those who have not issued any book.
(ii) Find the books returned by "ABC" member on 2.2.2006.
(iii) Find the members those who have issued book by C J date.

Q.3 : Define view. [1]

Total No. of Page(s): 2 Roll No. .....

IXTH SEMESTER B.E. (COE)

B.E. MID-SEMESTER EXAMINATION, FEB-MAR 2016

COE 313 Operating Systems

Time: 1:30 Hrs. Max. Marks: 20

Attempt any four questions.

1. (a) Define: operating system, kernel, system call.
   (b) Why an operating system is called a resource allocator and a control program? [3+2]

2. Calculate the average waiting time of the following processes if (a) shortest-job-first scheduling and (b) shortest-remaining-time-first scheduling are used.

Process	Arrival time (ms)	CPU burst time (ms)
P1	0	10
P2	2	7
P3	4	4
P4	7	2
P5	10	3

[2x2.5]

3. There are *N* chairs in a restaurant. A customer has to wait outside till a chair becomes vacant. After sitting on a chair, a customer can place an order. There is only one waiter in the restaurant who takes the orders and serves the food. The waiter serves one customer at a time. A customer leaves after eating. Write pseudocodes for the customers and the waiter using semaphores. [5]

4. A system has four processes, *viz.* P1 to P4, and four resource types. The system is currently in a safe state with Available = [2 4 4 2],

$$\text{Max} = \begin{bmatrix} 1 & 2 & 2 & 1 \\ 5 & 1 & 0 & 5 \\ 3 & 3 & 4 & 4 \\ 2 & 2 & 2 & 2 \end{bmatrix} \text{ and Allocation} = \begin{bmatrix} 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 2 & 1 & 2 \end{bmatrix}.$$

Use the resource-request algorithm to show that a request [1 0 1 0] from P4 can be granted. Use the safety algorithm to check if the new state will be a safe state. [5]

5. Differentiate between (any two):
   (a) Process and thread
   (b) Semaphore and monitor
   (c) Starvation and deadlock

[2x2.5]

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SIXTH SEMESTER

Roll No .....

B.E. (COE)

B.E. MID SEM. EXAMINATION, FEB-2016

COE-314: CONTROL ENGINEERING

Time: 1½ Hrs.

Max. Marks: 20

Note: Attempt ALL questions. Assume missing data, if any.

1. Find the transfer function of the system whose SFG is drawn in Fig. 1. [4]

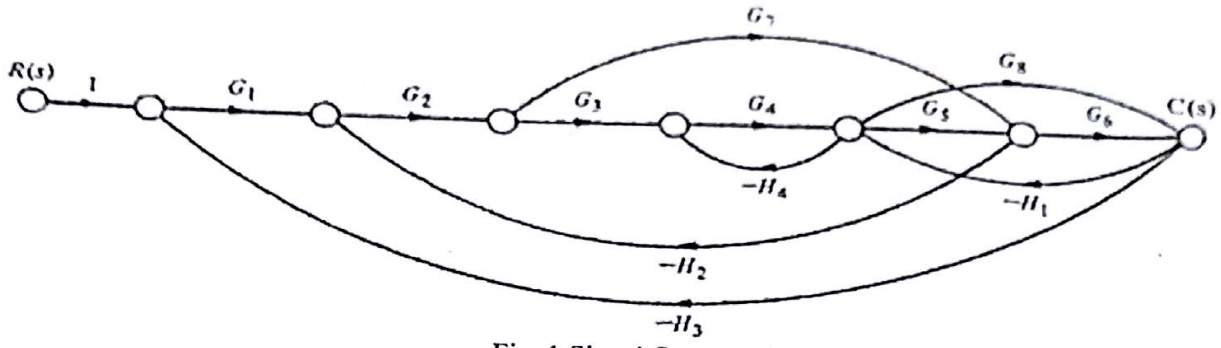

Fig. 1 Signal flow graph

2. Consider the following second-order transfer function: [4]

$$G_P(s)=\frac{K}{(\tau_1 s+1)(\tau_2 s+1)}$$

For a *unit impulse* input, find the output response as a function of time. What is the peak change and when does it occur?

3. Consider a process with the following transfer function: [4]

$$G(s)=\frac{1}{(s+1)(s-2)}\ ,\ H(s)=1$$

Can a PI controller satisfy the necessary condition for stability of this process?

4. Write the differential equations governing the behaviour of mechanical system shown in Fig. 2. Also obtain an analogues electrical circuit based on force-current analogy. [4]

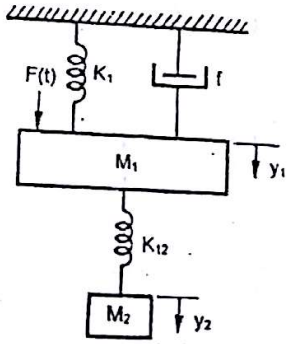

Fig. 2

5. Enumerate the advantages and disadvantages of open-loop and closed-loop system in context with sensitivity and dynamics of system. [4]

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B.E. (COE) 6th SEMESTER MID SEMESTER EXAMINATION, MARCH 2016

COE – 315: ADVANCED COMPUTER ARCHITECTURE

TIME: 1.5 HOURS MAX. MARKS: 20

NOTE: Attempt all questions. Assume suitable missing data, if any, and specify it clearly.

Q 1. A program running on a RISC machine executes 16,000,000 instructions during its execution. The total time it takes to execute an instruction is 200 ns in a non-pipelined system. The total amount of work that needs to be performed on each instruction is **infinitely divisible**. Now, suppose pipelining overhead adds 10 ns to the latency of each pipeline stage. What is the maximum speedup that can be obtained through pipelining? Assume there are no hazards (ideal pipelining). Show your work.

Q 2. A program written in C is executed on two different computers: Computer A and Computer B. Both have a processor that implements the x86 ISA and has 3 GHz clock frequency. During execution of this program, we measure cycles per instruction (CPI) that is found to be 10 on Computer A and 8 on Computer B. On which computer (A or B) this program runs faster? Explain.

Q 3. A dynamic branch predictor is always better than a static one. Refute / Justify with an example.

Q 4. You are designing an ISA (Instruction Set Architecture) for a 6-stage in-order pipelined processor that provides delayed branch instructions. How many branch delay slots would you provide to fully remove the penalty of conditional branches if these get resolved during the 4th stage? Explain.

Q 5. Consider a non-pipelined processor with a clock rate of 2.5 GHz and average CPI of 4. The same processor is upgraded to a 5-stage pipelined processor but due to the internal pipeline delays, the clock speed is reduced to 2 GHz. What is the speedup achieved in this pipelined processor to execute some benchmark program, assume there are no stalls in the pipeline?

Q 6. Keeping a processor pipeline full with useful instructions is critical for achieving high performance. Write the main reasons why a processor pipeline cannot always be kept full?

Q 7. A pipelined processor has a cycle time of 10 ns. A benchmark program exhibits an average CPI of 1.6 on this processor. 10% of the instructions in this program are branches and that an implemented branch prediction scheme is 90% accurate. Every branch mis-prediction costs 2 cycles of delay on this processor. Designer have come up with a new processor design where the cycle time has decreased to 9 ns by increasing the pipeline depth however, the branch mis-prediction penalty has increased to 7 clock cycles and everything else will stay the same. Compute the average CPI on the new processor for the benchmark. Will your benchmark program run faster or slower on this new processor? Show your work.

Q 8. Simplicity of the architecture of RISC machines offered promise of higher performance largely through pipelining and higher clock rates. Despite this, a CISC ISA x86 has not been superseded by RISC architecture. Explain the main technical reason behind this.

Q 9. In a 3-stage pipelined system, stage S1 is used in cycles 1 & 5, stage S2 in cycles 2 & 4, and stage S3 in cycles 3 & 4. Draw the structure of this pipelined system. Show that optimal MAL can be obtained by delaying the usage of Stage 2 scheduled for cycle 4.

Q 10. Comment on the performance of Branch Target Buffer (BTB) in the case of branch instructions using indirect addressing mode.

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