[b] For the Astable multivibrator shown in Fig. 7(b) where the two saturation levels of the op-amp are not same (i.e. they are $+V_{sat1}$ and $-V_{sat2}$ respectively), explain the operation by sketching relevant waveforms and deduce an expression for the frequency of the output waveforms.

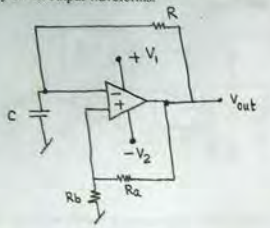

Fig. 7(b)

8. [a] For the emitter-coupled differential pair of Fig. 8(a), assume that all pnp transistors have β =50 and npn transistors have β = 150. Find the value of resistor 'R' such that the current relationships in the entire circuit are satisfied. Do not neglect base currents.

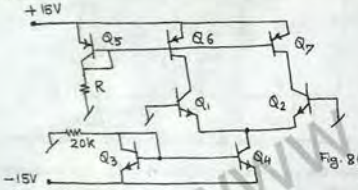

Fig. 8(a)

[b] Determine the input offset voltage and input offset current of the emitter-coupled differential pair.

9. Write technical notes on **any two** of the following.
- **[a]** IC Phase Locked loops
- **[b]** Gilbert multiplier
- **[c]** Voltage regulators
- **[d]** IC Function generators

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Total No. of Page(s): ..... *Roll No.* 304/10/08

Fifth Semester B.E. (ECE/COE/ICE)

B.E. End Sem. Examination, November, 2010

EC-304/COE-304/IC-304: Linear Integrated Circuits

Time: 3:00 Hrs. Max. Marks: 70

Note: Attempt any **seven** questions. Missing data/information, if any, may be suitably assumed and mentioned in the answer.

1. [a] Define input bias current, slew rate, unity gain bandwidth, CMRR and input offset voltage, as applicable to an op-amp.

[b] Determine the voltage gain and input impedance of the circuit shown in Fig.1(b), assuming ideal op-amps. What value of 'α' can make the input impedance of the circuit as infinity?

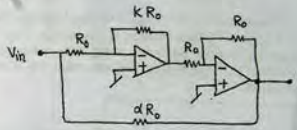


Fig. 1(b)

2. [a] Using $A_1 = A_2 \cong \frac{\omega_t}{s}$, where ω_t is the gain band bandwidth product of the op-amps, show that the circuit of Fig. 2(a) realizes an equivalent impedance between port 1 and ground as shown in Fig. 2(a). What are the values of realized R_o, C_o and L_o.

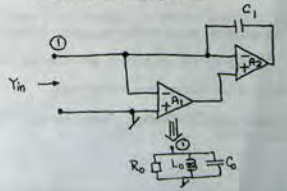


Fig. 2(a)

[b] Fig.2 (b) shows an active-compensated inverting amplifier. Assuming $A_1 = A_2 \cong \frac{\omega_1 \tau}{s}$, show that the approximate phase error of this circuit is given by $\phi \cong \omega^3 \tau_1 \tau_2^2 \left(1 + \frac{R_f}{R_i}\right)$. What is the condition under which the approximation used is valid? How much is the ideal gain of the circuit (i.e. when op-amps are ideal).

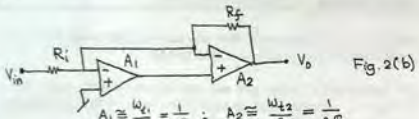


Fig. 2(b)

$A_1 \cong \frac{\omega_{t1}}{s} = \frac{1}{s\tau_1}$; $A_2 \cong \frac{\omega_{t2}}{s} = \frac{1}{s\tau_2}$

3. [a] Write down the transfer functions for second order low pass, high pass, band pass, notch and all pass filters in terms of the parameters H_0, ω_0 and Q_0 where the symbols have their usual meaning. Analyze the circuit of Fig.3 (a) and prove or disprove that by proper selection of V_{in1}, V_{in2} and V_{in3}, one can realize any of these five filter functions from this circuit.

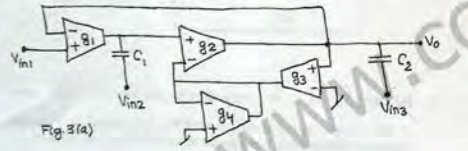


Fig. 3(a)

[b] What are the advantages of OTA-C circuits as compared to op-amp-RC circuits? Devise an OTA-C circuit which should produce an output voltage V_0 given by $V_0(s) = V_1(s) + \frac{1}{s}\left(V_2(s) - V_3(s)\right)$ where V_1, V_2, and V_3 are the input signals. Use a minimum possible number OTAs and passive components.

4. [a] Design a second order active notch filter having center frequency = 100 Hz, bandwidth = 10 Hz and Gain =20 dB.

[b] Assuming ideal op-amps, determine the condition of oscillation and Frequency of oscillation for the oscillator circuit of Fig.4 (b) in terms of K_1, K_2, R and C.

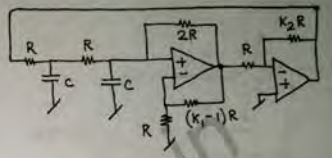


Fig. 4(b)

5. [a] Fig.5 (a) shows a circuit which generates a waveform due to which it can be called a 'tone-burst' oscillator. Verify its operation, sketch the waveforms at V_{01} and V_{02} and calculate the frequencies of the waveforms generated at V_{01} and V_{02}.

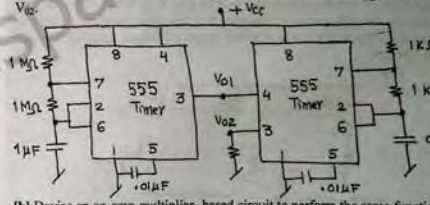


Fig. 5(a)

[b] Devise an op-amp-multiplier- based circuit to perform the same function.

6. [a] Explain how an op-amp can be used to realize (i) a comparator and (ii) 'Schmitt Trigger'.

[b] Using op-amp as a comparator (and any other devices and circuits, if needed) devise a circuit to generate triangular waveform of frequency 1 kHz. Explain its operation and derive an expression for the frequency of the waveform.

7. [a] Determine the relationship between V_{in} and V_0 for the circuit shown in Fig.7(a) assuming ideal op-amps.

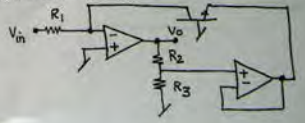


Fig. 7(a)

Number of Pages 2

FIFTH SEMESTER Roll No. .....

B.E.(COE/EC/EE/IC)

END SEMESTER EXAMINATION **NOVEMBER-2010**

COE/EC/EE/IC-305 INDUSTRIAL ORGANIZATION AND MANAGERIAL ECONOMICS

Time: 3 Hours **Max. Marks : 70**

Note : Answer any *FIVE* questions.
Assume suitable missing data, if any.

1[a] Discuss the importance of various types of managerial roles in an organization. 7

[b] Compare scientific management with behavioural thought of management. 7

2[a] Compare project organization and matrix organization. Explain, how does the organizational structure vary with type of industry? 7

[b] Write 14 principles of management given by Henry Fayol. 7

3[a] Vice-Chancellor of your university estimates that the employees are idle 15% of the time. He would like to work sample that has max. error limit 3% and wants to have 95.45% confidence in the results. The value of Z at 95.45% confidence level is 2. 7

[b] Explain normal time, standard time and importance of various types of allowances used to calculate the standard time. 7

4[a] Explain the qualitative methods of forecasting. 7

[b] A firm producing paints. Plans to use simple exponential smoothing to forecast weekly demand and has collected the past data for 15 weeks as shown below:

Week No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Actual Demand	30	35	20	15	10	10	15	20	30	35	30	10	12	20	30

Compute the forecast value using $\alpha = 0.2$ for the 16^{th} week. 7

5[a] Explain loading, sequencing, scheduling, routing, dispatching concerned with production planning and control. 7

[b] A concern is manufacturing a product which is sold for Rs. 10.5 / unit and fixed cost of the assets is Rs. 50,000 with a variable cost of Rs. 6.5/unit. How many units should be produced to break even? How many units must be produced to earn a profit of Rs. 10,000/- what could be profit for sales volume of 20,000 units? 7

6[a] Explain the steps used in work sampling and advantages and disadvantages of work sampling. 7

[b] Mr. Tata is planning to open a new plant at Sanand, Pune and Jamshedpur to produce low cost car components. He has assembled the following fixed cost and variable cost data

Location	*Fixed cost / year (Rs.)*	*Per Unit Costs (Rs.)*		
		Mats.	*Variable*	*Overhead*
Sanand	Rs. 250,000	Rs. 20	Rs. 40	Rs. 40
Pune	Rs. 230,000	Rs. 25	Rs. 70	Rs. 70
Jamshedpur	Rs. 220,000	Rs. 100	Rs. 100	Rs. 100

(i) Graph the total cost lines.

(ii) Over what range of annual volume is each facility going to have competitive advantage?

(iii) What is the volume at the intersection of the Pune and Jamshedpur. 7

7[a] Write notes on various types of plant layout. Compare their merits and demerits. 7

[b] Discuss the importance of decision making in an organization. Write the name of some tools used for decision making. 7

8 Write short notes on any ***Four*** of the following:- **3½ x4=14**

[a] Industrial Psychology

[b] Therblig

[c] Forecasting error

[d] Motion economy

[e] Functional organization

[f] Plant location strategy

[g] GDP of the country

[h] Five year plan (feature of 11th five year plan)

Total Number of Pages 3 Roll No. .....

FIFTH SEMESTER **B.E.(COE**

END SEMESTER EXAMINATION ***NOVEMBER-2010***

COE-302 DISCRETE MATHEMATICS & DESIGN OF ALGORITHMS

Time: 3 Hour ***Max. Marks : 70***

Note : Answer any ***FIVE*** questions.
Assume suitable missing data, if any.

1[a] Show the following implication without constructing the truth table:

$(P \vee (Q \wedge R)) \overleftarrow{\rightarrow} ((P \vee Q) \wedge (P \vee R))$

$(P \overrightarrow{\leftarrow} Q) \Leftrightarrow (P \vee Q) \wedge \neg (P \wedge Q)$ 8

[b] What is a predicate? How do you define any formula in predicate calculus? State the following argument in symbolic form and test its validity.

"If the parcel is not properly addressed or is too large, then the post office will not accept it. The parcel is not too large. If chou wrote the address on the parcel, then it is properly addressed. Hence if chou wrote the address, the post office will accept the parcel". 6

2[a] What is pigeon hole principle? Apply this principle, show that if any 26 people are selected, then we may choose a subset of 4 so that all 4 were born on the same day of the week. 5

[b] Solve the recurrence relation $a_r - 7a_{r-1} + 10a_{r-2} = 3^r$ given that $a_0 = 0,\ a_1 = 1$. 5

[c] Let $X = \{1,2,3,4\}$ a function is defined as $f : X \to X$ such that $f \neq I_x$ and is one –to-one. Find $fof = f^2$ and f^{-1}. 4

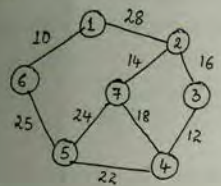
3[a] Define the cardinality of a set. Show that the set of real numbers between 0 and 1 is not a countably infinite set. 5

[b] Generate permutations in lexicographic order of 4 subjects {4,5,6,7}. Find the number of different outcomes when 3 dice are rolled with repetition of numbers. 5

[c] Symbolize the following statement using proposition and prove its validity: 4
If a graduate is well qualified, he will get a good job. A graduate is not well qualified. Therefore, he will not get good job.

B.E.(COE)

...erate the minimum cost spanning tree for the following graph using Prim's and Kruskal's algorithms. **10**



[b] Multiply the following two matrices using strassen's method

$$A=\begin{bmatrix}2&3&4&1\\1&2&3&2\\4&2&1&1\\7&6&2&1\end{bmatrix} \qquad B=\begin{bmatrix}2&1&3&1\\1&2&4&5\\3&1&3&2\\2&3&2&3\end{bmatrix}$$ **4**

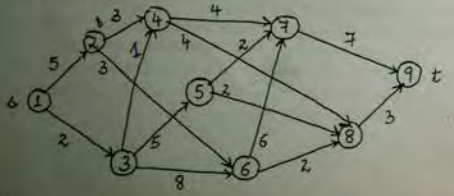
5[a] Given a sequence *(A1, A2, A3, A4)* of *4* matrices to be multiplied. In how many ways the product *A1.A2.A3.A4* can be fully parenthesized? Parenthesize the sequence so that the no. of scalar multiplication is minimum. The dimensions are given below

A_1	5×4
A_2	4×2
A_3	2×3
A_4	3×6

10

OR

Find the minimum cost path from *s* to *t* in the multistage graph in the figure. Do this first using forward approach and then using backward approach write the algorithm in both the cases.

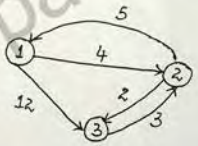


[b] Greedy approach guarantees to produce optimal solution. True or False? Write your comments. **4**

6[a] State the job sequencing problem with deadlines. Describe the greedy method to obtain an optimal solution to this problem. What is the solution generated by greedy method when $n=7, (p_1,p_2 \ldots\ldots p_7)=(5,7,22,20,3,8,32)$ and $(d_1,d_2 \ldots\ldots d_7)=(2,4,5,4,3,2,3)$ **7**

[b] State and analyze the travelling salesman problem. Describe how dynamic programming solution can be obtained to solve this problem. **7**

7[a] Illustrate all pairs shortest paths algorithm with the example given as follows: **7**



[b] Differentiate between dynamic programming and greedy strategy using knapsack problem. Analyze the algorithms using both the approaches. **7**

Total Number of Pages 3

Roll No. .....

FIFTH SEMESTER **B.E.(COE)**

END SEMESTER EXAMINATION ***NOVEMBER-2010***

COE- 303 COMPUTER SYSTEM ORGANIZATION

Time: 3 Hours ***Max. Marks : 70***

Note : Answer any ***FIVE*** questions.
Assume suitable missing data, if any.

1[a] Consider the following register transfer statements for two 4-bit registers R_1 and R_2.

$$xT = R_1 \leftarrow R_1 + R_2$$
$$x'T = R_1 \leftarrow R_2$$

Draw a diagram showing the hardware implementation of the two statements. Use block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2-to – 1 line multiplexer that selects the inputs to R_1. In the diagram, show how the control variables x and T select the inputs of the multiplexer and the load input of register R_1. **8**

[b] What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register? **6**

2[a] A computer uses a memory of 64 K words with one byte in each word. It has the following registers : PC, AR, TR (2 bytes each) and AC, DR, IR (one byte each). A memory reference instruction consist of three words: An one-byte operation code (one word) and a 2 byres address (in the next two words). All operand are one byte. There is no indirect bit.

(i) Draw a block diagram of computer showing the memory and register (with out using a common bus).

(ii) Draw a diagram showing the placement in memory of a typical three word instruction and corresponding one-byte operand.

(iii) List the sequence of micro-operations for fetching a memory reference instructions and then placing the operand in DR. Start from timing signal T_0. **9**

Define the terms critical resistance and critical speed and self-excitation of a DC

OR

[b] Draw and explain a diagram of a bus system for four registers of four bits each using three state Buffers and a decoder. 5

3[a] The control memory has 4096 words of 24 bits each:

(i) How many bits are there in CAR?

(ii) What are the number of inputs in each MUX and how many MUXs are needed? 6

(iii) How many bits are there in each of the four inputs going into the MUX.

[b] Write a program to evaluate the arithmetic statement:

$$Y = \frac{A+B+C*(\frac{D}{E}-F)}{G*H+K}$$

(i) Using a general register computer with three address instructions.

(ii) Using a general register computer with two address instructions.

(iii) Using an accumulator type computer with one-address instructions.

(iv) Using a stack organized computer with zero address operation instructions. 8

4[a] A two –word instruction is stored in memory at an address designated by symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The opened used during the execution of the instruction is stored at an address symbolized by Z. An index register contain the value X. State how Z is calculated from the other address if the addressing mode of the instruction is:

(i) Direct (ii) Indirect (iii) Relative (iv) Indexed. 7

[b] Define Booth algorithm. Show step-by-step process using Booth algorithm to multiply.

(+14) × (+11).

7

5[a] Differentiate between restoring and non-restoring method of fixed point binary division. 7

[b] Distinguish between programmed input and interrupt initiated Input with suitable examples. 7

6[a] Design a parallel priority interrupt hardware for a system with eight interrupt sources. 7

[b] A computer employs RAM chips of 256 x 8 and ROM chips of 1024 x 8. The computer system needs 2K bytes of RAM, 4K bytes of ROM, and four interface units, each with four registers. A memory-mapped input configuration is used. The two highest-order bits of the address bus are assigned 00 for RAM, 01 for ROM, and 10 for interface registers.

[a] How many RAM and ROM chips are needed?

[b] Draw a memory – address map for the system.

[c] Give the address range in hexadecimal for RAM, ROM, and interface. 7

7 Write short notes on the following:

[a] ALU Design

[b] Associative memory

[c] DMA controller

[d] Virtual memory. 3.5x4