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Roll No.:

Fifth Semester

BE(COE/ICE)

Mid Semester Examination, September 2010

COE/ICE-304: Linear Integrated Circuits

Time : 1 ½ Hours

Total Marks : 20

Note: Attempt all questions. All question carry equal marks. Missing data if any may be suitable assumed.

1. What is a Generalised Impedance Converter (GIC)? Find out an expression for Z_{in} when GIC is terminated by a load Z_L. Explain its application in the simulation of low value of grounded resistance, high value of grounded capacitance, a floating inductor, grounded FDNR and grounded FDNC.

2. Find the transfer functions $\left(\frac{V_{01}}{V_{in}}\right), \left(\frac{V_{02}}{V_{in}}\right), \left(\frac{V_{03}}{V_{in}}\right)$, of the circuit shown in Fig. 2, identify the type of filters realizable at V_{01}, V_{02}, V_{03}. Give the expression of filter parameters (H_0, ω_0 and ω_0/Q_0) in each case.

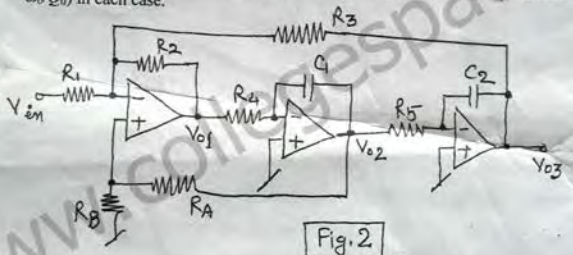

Fig. 2

3. Derive an expression of V_0 for the circuit shown in Fig.3. Show that it can be used as an instrumentation amplifier. Comment on its specific features.

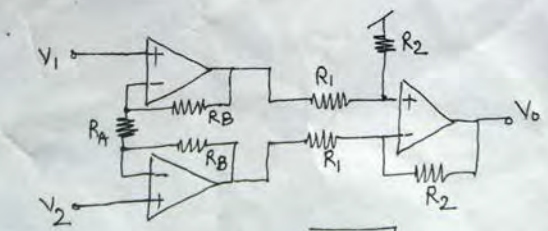

Fig. 3

4. Suggest any configuration for $\frac{I_0}{I_{in}} = K$ where K is a constant.

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Roll No.

September, 2010

BE (V) SEMESTER MID TERM EXAMINATION (COE/ECE/ICE - 305)
INDUSTRIAL ORGANIZATION AND MANAGERIAL ECONOMICS
Course No. 305

Time: 1:30 Hrs. **Max. Marks 20**

Note: 1. Attempt any ten questions
2. Each Question carry equal marks

1. Explain briefly the functions of management.
2. Is Management an art or science, please explain .
3. Distinguish between management and administration
4. What is scientific management? Explain it principles.
5. Discuss Henry Fayol's principles of management.
6. Distinguish between line, staff and functional organization
7. Differentiate between Contingency approach and Systems approach of Management
8. Describe different types of organizational structures.
9. What factors should be considered before choosing a plant location?
10. Discuss the types of plant layouts with suitable examples.
11. Differentiate between a product layout and a process layout of an industrial plant.
12. Where would you recommend the location of the following plants and why?
    a) consumer electronics b) thermal power house of 500mw capacity

Roll No: 304/CO/08 Date:

Mid Semester Examination, September 2010
BE Vth Semester COE

Course No: *COE 301* *Principles of Computer Graphics*
Time: 90 Min MM : 20

Note: Attempt all questions.

Q.1 (a) Find the parametric equation of line passing through (2, 5) and parallel to the vector V=3i+7j. (1)

(b) Generate the Window to View Port transformation matrix using only basic 2D transformation matrices. (3)

Q.2 (a) Find the necessary 2D transformation matrix such that area of ΔABC becomes twice while keeping ∠BAC fixed. Given A (15,16), B(10,8), C(25,12). (3)

(b) Using only the fundamental principles, derive the shearing matrix about any point (h, k). (3)

Q.3 (a) Using midpoint method and symmetry, scan convert the parabola $y=225x^2$. Derive the algorithm for (i) First order differential and (ii) Second order differential. (5)

Q.4 Given the clipping window: (-3,-3), (-3, 3), (3, 3), (3,-3). Use this as the eraser window to find the portions of lines $P_1(-4,2)$, $P_2(2,4)$ and $P_3(-6,3)$, $P_4(2.5,4)$ using the (i) NLN (ii) Cyrus Beck algorithms. (5)

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SEMESTER B.E. (COE)

B.E. MID SEM. EXAMINATION, SEPT. 2010

COE-302 :Discrete Mathematics and Design of Algorithm

Time: 1:30 Hrs. Max. Marks: 20

Note: Attempt ALL questions.

Q. 1. Solve the recurrence relation

$d_n = 2d_{n-1} - d_{n-2}$ with the initial conditions

$d_1 = 1.5$ and $d_2 = 3$ [2]

Q. 2. A survey among 100 students shows that of the three ice cream flavours vanill, chocolate and strawberry, 50 students like vanilla, 43 students like chocolate and 28 like strawberry. 13 of them like vanilla and chocolate, 11 like chocolate and strawberry, 12 like strawberry and vanilla. Also 5 of them like all the three flavours. Find the number of students surveyed who like each of the following flavours.

i) Chocolate but not strawberry.
ii) Chocolate and strawberry but not vanilla.
iii) Vanilla or chocolate, but not strawberry.
iv) Use of formula and draw vein diagram.

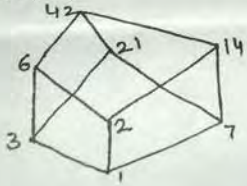
[4]

Q. 3. Let $P(n) = 2n^3 + 3n^2 + n$ is divisible by 6. Prove by mathematical induction. [2]

Q. 4. Explain the following terms (in brief) [6]

(1) Functions and Relations
(2) POSET & Partitions.

Q. 5. Prove that the given figure is a lattice or not. Where $D = \{1,2,3,6,7,14,21,42\}$ [2]



Q. 6. Show that $\bar{p}$ is a tautology implied by $(p \wedge \bar{q})$, $\bar{q} \vee r$ and $\bar{r}$. [2]

Q. 7. Show that $(x)(P(x) \vee Q(x)) \Rightarrow (x)P(x) \vee (\exists x)Q(x)$. [2]

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FIFTH SEMESTER

Roll No.....

B.E. (COE)

MID SEMESTER EXAMINATION, SEPTEMBER 2010

COE – 303: COMPUTER SYSTEM ORGANIZATION

Time: 1:30 Hrs

Max. Marks: 20

NOTE: Attempt All questions.

Assume suitable missing data (if any), and specify it clearly.

Question 1 [8]

Design a CPU (data-path and control path) that meets the following specification:

- It can access 64 words of memory, each word being 8 bits wide. The CPU does this by outputting a 6-bit address on its output pins A[5..0] and reading in the 8-bit value from memory on its inputs D[7..0].
- The CPU contains a 6-bit address registers (AR) and program counter (PC); an 8-bit accumulator (AC) and data register (DR); and a 2-bit instruction register (IR).
- The CPU must realize the following instruction set:

Instruction	Instruction Code	Operation
COM	00XXXXXX	AC ← AC'
JREL	01AAAAAA	PC ← PC + 00AAAAAA
OR	10AAAAAA	AC ← AC v M[00AAAAAA]
DEC	11AAAAAA	AC ← AC –1

Question 2 [2]

Represent the following conditional control statements by two register transfer statements with control functions:

If (P = 1) then (R1 ← R2) else if (Q = 1) then (R1 ← R3)

Question 3 [5]

Implement a 3-bit gray code to binary code converter using 4-to-1 multiplexor. Write the VHDL code for this circuit.

Question 4 [5]

Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages:

S	Cin = 0	Cin = 1
0	D = A + B (add)	D = A + 1 (increment)
1	D = A -1 (decrement)	D = A + (~B) + 1 (subtract)

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