

END SEMESTER EXAMINATION, MAY 2008
EC/COE/IC-311: MICROPROCESSORS

Time: 3:00 Hrs.

Max. Marks: 70

- Note: 1. Attempt five questions in all.
 2. Q. 1 is compulsory.
 3. All questions carry equal marks.
 4. All parts of the same question should be attempted at one place.

- Q1 a)** If the stack pointer points to 0000H, in which memory location will the stack contents be stored if stack is used? [7 * 2 = 14]
 b) Give two examples of instructions with a 6-T state opcode fetch machine cycle.
 c) If Port A is in mode 2, specify how INTR_A will be generated? Explain with the help of logical expression and handshake signal diagram.
 d) Is INTA signal is generated in response to every hardware interrupt signal? Justify your answer.
 e) What do you mean by initialization command word in respect of ICW1 in detail.
 f) Explain the command instructions format of 8251.
 g) Explain how we can load 16-bit count into the counter Register of 8254.

- Q2 a)** Interface 8KB X 8 bit ROM using 2KB X 4 bit ROM as base unit with 8085, and one wait state. [7]
 b) Write an assembly language program for finding out the factorial of a number. [7]

- Q3 a)** Explain the architecture of 8085 with a functional block diagram. [7]
 b) Write an assembly language program for executing the following expression

$$Y = \frac{P * Q}{R},$$

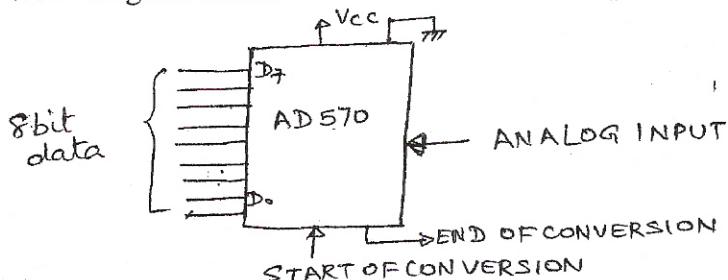
where P, Q and R are 8 bit numbers. [7]

- Q4 a)** Design an up down counter to count from 0 to 9 and 9 to 0 continuously with 1.5 second delay between each count and display the count at one of the output ports. Draw the flow chart and show the delay calculations. 8085 is used with a 2 MHz crystal. [7]
 b) Differentiate between
 i) RST 7 and RST 7.5
 ii) XCHG and XTHL
 iii) CALL 5050H and jump 5050H
 iv) HOLD and HLT
 v) Vectored and non-vectored interrupts
 vi) Port I/O and memory-mapped I/O [7]

Q5 a) Design an interfacing circuit using 8255A to read an A/D converter to meet the following requirements.

- Set Port A in handshake mode to read data from A/D converter.
- Set up Port B as an output port to display data through LEDs.

The block diagram of A/D converter is shown in Fig 1.



[7]

b) Compare fully nested mode and specially fully nested mode of 8259. [3]

c) Initialize 8259 to be selected by B0H and B1H as follows:

Non-buffered system environment, Normal EOI, 8085A system, single 8259 operation, not in SFNM, Call address interval equal to 8. First call address for IR0 must be A000H. Also, IR4 and IR6 must be masked.

[4]

Q6 a) Initialize 8253 such that it generates a negative pulse of approximately 1T state every 1 ms. Consider the crystal of 8085A to be 4 MHz and base address of 8253 to be 10H. Show the calculations of the count. [7]

b) Explain the working of CALL instruction using timing diagram. [7]

Q7 a) Explain the interrupt structure of 8085 with the help of a neat diagram. [7]

b) Explain all the keyboard scan modes of 8279. [7]

Q8 Write short notes on any two:

- DMA controller
- 8085 stack
- OCWs of 8259

[7 * 2 = 14]



COE-312 INFORMATION SYSTEM & DATA MANAGEMENT

Time: 3:00 Hours**Max. Marks : 70****Note :** Answer any **FIVE** questions.

Assume suitable missing data, if any.

- 1[a]** You wish to design a database for storing information about the entertainment industry. Specifically you wish to store information about movies, their directors, and their actors. For movies you wish to store the following information;

The title, release date and the length (running time).

For actors you wish to store their names, birthday, sex(M/F) and awards won (Eg. Oscar for best actor/or Best supporting actress) For directors you wish to store their names and awards won. For any actor or director that has won an award, you wish to be able to look up the following about each award: its name, date and description.

Create an E-R diagram for this data base.

Show entities, relationships and attributes in your diagram. Also, indicate identifiers as well as any weak entities/ or identifying relationships you may have. 10

- [b]** Discuss Data Abstraction. 4

- 2[a]** What are data models? According to you which is the best model and why? 5

- [b]** Differentiate between:

- (i) DBMS and file system
- (ii) Generalization and specialization
- (iii) Centralised and distributed database.

9

- 3[a]** Discuss the desirable properties of a decomposition of a relational schema. 4

- [b] Normalize the following data of personal employees table to 3NF using appropriate relations

Emp-code	Employee name
Dept-code	Department name
Mangr-code	Manager name
Course-code	
Course-title.	

6

- [c] What is BCNF? Illustrate with the help of a suitable example.

4

- 4[a] Consider the following insurance database, where the primary keys are underlined.

Person (driver-id#, name , address)

Car (license, model, year)

Accident (report-number, date , location)

Owns (driver-id#, license)

Participated (driver-id, car, report-number, damage-amount)

Construct the following SQL queries for the relational database:

- (i) Find the total member of people who owned cars that were involved in accident in the year 2000.
(ii) Find the number of accidents in which the cars belonging to "Anand Kumar" were involved.
(iii) Add a new accident to the data base; assume any values for required attributes.
(iv) Update the damage amount for the car with license number "AABB2000" in the accident with report number "AR2197" to Rs.3000.

8

- [b] What is relational algebra? Consider the given relational database.

S-person (S-Mo, S-name, commission)

Product (P-id), Description

Sale (Date, customer-no, S-no, P-id, qty)

Customer (Customer-no, c-name, c-address)

Give a relational-algebra expression for each of the following queries.

- (i) Find names of the salesman who sold product 48.
(ii) Find the names of those customers who bought table lamps (in addition to other products)
(iii) Find names of those sales persons who sold all the products.

6

- 5[a] What is view? How it is related to data independence?

5

- [b] Discuss various mechanism to make the database secure.

3

- [c] List all possible sequences of states through which transaction may pass. Explain why each state transition may occur.

6

- 6[a] Explain the distinction between the terms serial and serializable schedule.

6

- [b] What do you mean by Deadlock? Describe the actions to be taken for the recovery from deadlock.

8

- 7[a] Show that the two phase locking protocol ensures conflict serializability and that transactions can be serialized according to their lock-points.

5

- [b] Consider the following two transactions

T_{31} : read (A)
read (B)
if A=0 then B := B+1;
Write (B)
 T_{32} : read (B)
read (A)
if B=0 then A := A+1;
Write (A)

Add lock and unlock instructions to the transactions T_{31} and T_{32} , so that they observe a two phase locking protocol. Can the execution of these transactions results in dead lock?

4

- [c] Compare the deferred-and immediate-modification versions of the log-based recovery scheme in terms of ease of implementation and overhead cost.

5

- 8 Write short notes on any FOUR:

- Recoverable schedules
- Checkpoint mechanism
- Relational calculus
- BCNF Vs 3NF
- Functional dependency
- Authorization.

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SIXTH SEMESTER**B.E. (COE)**

B.E. END SEM. EXAMINATION, May-2008

COE-313 : OPERATING SYSTEMS

Time: 3:00 Hrs.

Max. Marks: 70

Note: Question No. 1 is compulsory.

Answer any four from the remaining questions.

Assume suitable missing data, if any.

1. Attempt any seven:

- [a] Differentiate between task and thread.
 - [b] Give the basic differences between network operating systems and distributed operating systems.
 - [c] What is Zombie State of a process?
 - [d] Give the structure of Process and Thread objects.
 - [e] What is safe state of a process?
 - [f] What is pipe related to concurrency mechanism in UNIX?
 - [g] What is Thrashing?
 - [h] What are Logic Bombs?
 - [i] Differentiate between Viruses and Worms? [2x7]
- 2.**
- [a] Describe various approaches for designing an operating system. [8]
 - [b] Explain the concept of spooling and buffering in detail. [6]
- 3.**

- [a] Suppose a disk drive has 300 cylinders, numbered 0 to 299. The current position of the drive is 90. The queue of pending requests, in FIFO order is
36, 79, 15, 120, 199, 270, 89, 170

Calculate the average cylinder movements for the following algorithms:

- (i) SSTF (ii) C-SCAN [8]

- [b] How does monitor can be used to solve the problem of synchronization? Discuss with the help of an example. [6]

4.

[a] What are various allocation techniques used in file system? Discuss any one in detail. Also explain how the free space management is carried out in file management system. [8]

[b] Given memory partitions of 100KB, 500KB, 200KB, 300KB and 600KB (in order), how would each of the first-fit, best-fit, and worst-fit algorithms place processes of 212KB, 417KB, 112KB and 426KB (in order)? Which algorithm makes the most efficient use of memory? [6]

5.

[a] What is Critical Section? Give requirements that are to be satisfied by Critical Section. [2]

[b] Give algorithm for producer consumer problem and discuss the solution for the same using semaphores. [5]

[c] Give Dekker's algorithm for two process management of a critical sections. Suggest modifications in this algorithm for N-process management. [7]

6.

[a] Consider a paged virtual memory systems with a two level hierarchy: Main memory M_1 and disk memory M_2 . Assume a page size of four words. The number of page frames in M_1 is 3, labeled a, b and c; and the number of pages in M_2 is 10; identified by 0, 1, 2, ..., 9. The i th page in M_2 consists of word addresses $4i$ to $4i+3$ for all $i = 0, 1, 2, \dots, 9$.

A certain program generates the following sequence of word addresses which are grouped (underlined) together if they belong to same page. The sequence of page numbers so formed is the page trace:

Word trace:

0,1,2,3, 4,5,6,7, 8, 16,17, 9,10,11, 12, 28,29,30, 8,9,10,
 ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓
 Page Trace: 0 1 2 4 2 3 7 . 2

Word trace:

4,5, 12, 4,5
 ↓ ↓ ↓
 Page Trace: 1 3 1

Describe page tracing experiments for above data for the following page replacement policies:

- i) Least Recently Used (LRU)
- ii) Optimal (OPT)
- iii) First in First Out (FIFO). [6]

[b] What is Inverted page Table? Why are segmentation and paging sometimes combined into one scheme? [4]

[c] What is General Resource Graph? Also define Resource allocation Graph and Wait for Graph (WFG).

Draw the General Resource Graph for the following:

- i) Process P_1 holds one unit of R_1 and Process P_2 holds one unit of R_1 . Process P_1 is active and P_2 is waiting to be assigned a unit of R_1 . P_2 is a producer of a consumable resource R_2 . The total number of resources R_1 and R_2 are 3 and 1 respectively.
- ii) Show the graph when P_1 has been assigned its request for one unit of R_1 and R_2 each. [4]

7.

[a] Explain the following CPU scheduling algorithms:

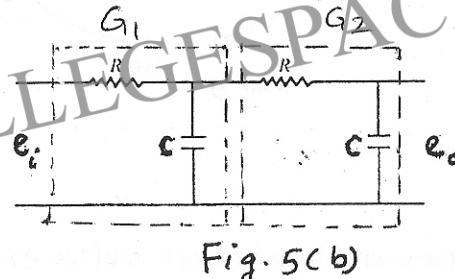
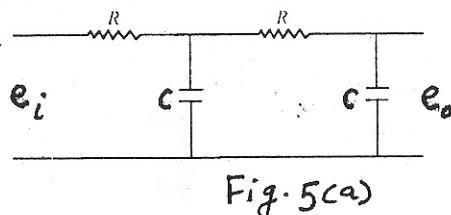
- i) Round Robin
- ii) Priority Scheduling. [5]

[b] Discuss the various models of deadlock. [5]

[c] Differentiate between deadlock and starvation. Give Banker's algorithm for deadlock avoidance. [4]

-----X-----

[b] Derive an expression for transfer function of the circuit shown in Fig.5(a) below. Comment whether this circuit can be represented by two cascade circuits as shown in Fig.5(b). 7



8 Write short notes on any TWO of the following:

- (i) Constant M-N circles
- (ii) Gain margin and phase margin
- (iii) Armature controlled DC-motor.

2x7

Total No. of Pages 4

SIXTH SEMESTER

END SEM EXAMINATION

Roll No.

B.E. (COE)

May-2008

COE-314 CONTROL ENGINEERING

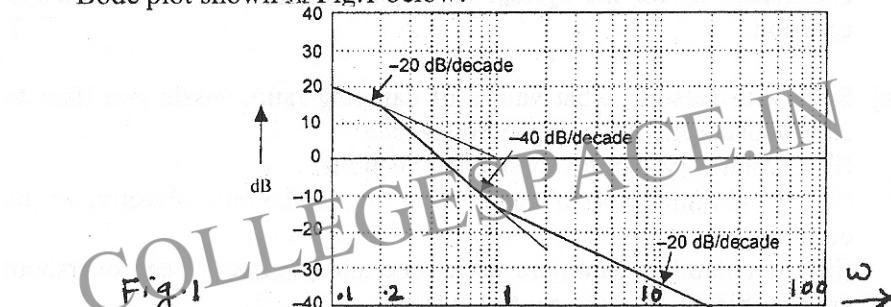
Time: 3:00 Hours

Max. Marks : 70

Note : Answer any **FIVE** questions.

Assume suitable missing data, if any.

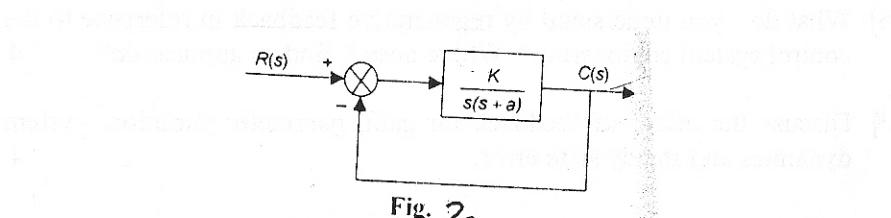
1[a] What do you understand by the terms minimum phase system and non-minimum phase systems. Determine the transfer function from the Bode plot shown in Fig.1 below: 4



[b] What do you understand by Nyquist criterion for stability? Draw the Nyquist plot for (i) a constant function: K, (ii) time delay function: e^{-sT} ,

(iii) first order system and (iv) second order system: $\frac{w_n^2}{s^2 + 2\xi w_n s + w_n^2}$. 10

2[a] Draw the root-contours of the closed loop control system shown in Fig.2 below for the positive value of K 7



- [b] Write the relation between root-loci and transient response. Also, discuss what is an asymptote in reference to root-loci of a closed loop control system. 7

- 3[a] State and explain the situations under which Routh-Hurwitz criterion cannot be used to determine the stability of even linear control systems. Point out the differences between absolute stability and relative stability. Is it a time response method or frequency response method to determine the stability? Point out the advantage of this method. 7

- [b] The open loop transfer function of a closed-loop system is given as

$$G(s)H(s) = \frac{K(s+a)}{s(s+130)(s^2+140s+10^4)}$$

Determine the restriction on the values of gain K and compensation coefficient 'a' for the system to remain stable. Use Routh-Hurwitz criterion. 7

- 4[a] State with reasons, what values of damping ratio, would you like to choose under the following circumstance?

(i) Control system for robotic applications.

(ii) If minimum normalized settling time is the only objective of the control system.

(iii) If obtaining minimum peak time and minimum peak overshoot are the objectives of the control system.

(iv) Navigation control system. 8

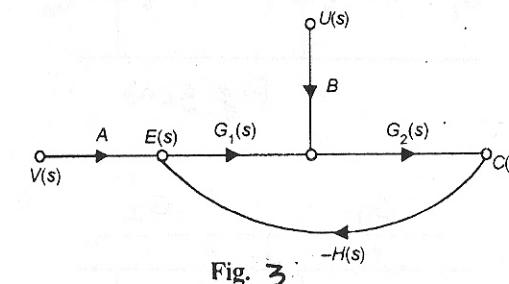
- [b] Derive mathematically and display graphically the time-response of a unity-feedback second-order system to a unit step input for various values of the damping ratio. 6

- 5[a] Compare the effect of a disturbance on the output of a system in case of (i) open loop control system, and (ii) negative feedback control system. 6

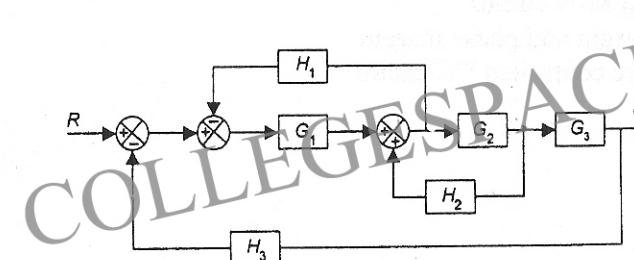
- [b] What do you understand by regenerative feedback in reference to the control system engineering? Where does it find an application? 4

- [c] Discuss the effect of feedback on gain, parameter variation, system dynamics and steady state error. 4

- 6[a] State the Mason's gain formula for obtaining the transfer function of a control system. Using the formula, determine the two transfer function for the following signal flow graph, Fig.3: 7



- [b] Determine the overall transfer function of the system shown in Fig.4 7



- 7[a] What are the various standard signals used for studying the response of the practical control systems? Which one is most widely used and why? 7

Q8)

(a) Consider the following instruction sequence:

```

MOVE R1, #10
MOVE R2, #10
L1: SUB R2, #1
ADD R1, R2
BEZ TAR // BRANCH IF ZERO
JMP L1

```

TAR: -----

For each of the given cases, calculate the branch penalty for a 4-stage (IF, ID, EX, WB) instruction pipeline if the branch condition is detected at the third stage and flushing (does not include filling) the pipeline takes one clock cycle.

- Delayed branching technique used by compiler
- A static prediction is taken assuming 'Branch Taken'

(b) Write explanatory notes on ONE of the following:

- Release consistency versus sequential consistency memory models
- Loop unrolling versus Software Pipelining

[7+7]

TOTAL NO. OF PAGES: 4

B.E. (COE) 6th SEMESTER

COE - 315

ROLL NO:.....

END SEMESTER EXAMINATION, MAY 2008

ADVANCED COMPUTER ARCHITECTURE

MAX. MARKS: 70

TIME: 3 HOURS

NOTE: Attempt total FIVE questions. All question carry equal marks.

Assume suitable missing data, if any, and specify it clearly.

Q1)

[14] Consider the following reservation table for a four-stage pipeline with a clock cycle of 20 ns.

	1	2	3	4	5	6
S1	X					X
S2		X		X		
S3			X			
S4				X	X	

Insert one non-compute delay stage into the pipeline to make a latency of 1 permissible in the shortest greedy cycle.

- What could be the purpose of above modification?
- Show the modified reservation table.
- Draw the block diagram showing interconnection of pipeline stages.
- Draw the state transition diagram for modified table.
- Is the new MAL equal to the lower bound? Justify.
- What is the optimal throughput of this pipeline?
- Derive an expression for the speedup of a non-linear pipeline

Q2)

(a) Use the following notation:

F (Fetch), D (Decode), C (calculate operand address), M_i/A_i (ⁱth stage of execution for multiply / add), W (single write back stage).

Consider the following instruction sequence:

```

I1: ADDF R12, R13, R14
I2: ADD R1, R8, R9
I3: MUL R4, R2, R3
I4: MUL R5, R6, R7
I5: ADD R10, R5, R7
I6: SUB R11, R2, R3

```

Consider a two-issue superscalar architecture with a look-ahead window. Its processing unit has one floating point unit and two integer units. The floating point unit is itself a 5 stage pipeline and the integer unit is a 3 stage pipeline. Calculate the total number of cycles required to execute the above instructions for the following cases:

- In-Order Issue with In-Order Completion
- Out-of-Order Issue and Out-of-order Completion.

(b) Discuss the different ways in which inconsistencies can occur in a cache-based SMP system.

Q3)

[7+7] (a) Given the series of loops below, analyze the loop dependencies for each loop statement and between statements within a loop. Use distance/direction vectors and the applicable dependency tests. Vectorize the loops where possible.

```

Do x = 1,10
  A[x] = PI*A[x+20]
  A[x+10] = A[20-x]
Enddo
Do y=1,N
  B[y,N] = B[1,N] + B[N/2,N] + B[N,N]
Enddo
Do z= 1,20
  A[z] = B[z] + C[z]
  C[z] = A[z+1] + 10
  Do x= 1,10
    D[z,x] = D[z,x-1] - D[z,x+1]
  Enddo
Enddo

```

OR

Use Software pipelining to improve the ILP for the following loop and show the restructured loop along with prologue and epilogue: (Don't convert the statements into assembly language instructions)

```

for(k=0;k<100;k=k+1)
{
  X[k] = X[k] + 1 ;
  Y[k] = Y[k] + X[k];
  Z[k] = Y[k] + 2 ;
}

```

(b) A program runs in 17 seconds on some machine. By making some enhancement in multiplication unit, multiplication operations takes only 0.86 seconds in this program and whole program runs 3.5 times faster. Compute the time take by multiplication operations before enhancement. How much improvement in multiplication operation has been achieved? Compute using Amdahl's law only.

Q4)

[7+7]
(a) Draw an 8×8 Re-arrangeable network using 2×2 switches. Source and destination nodes index ranges from 1 to 8. Show the switch settings for making connection between source node 2 to destination node 1, source node 1 to destination node 5 and source node 3 to destination node 3. Now a request comes for connecting source node 4 to destination node 2. Show that this request may get blocked because of already existing connections. Also, show that switch settings can be modified to find alternate paths for already existing connection so as to serve the new request.

b) The time taken by a computing system to execute N_1 instructions is equal to :

$T_1 = N_1 * (\text{no. of memory access cycles per instruction} + \text{no. of execute cycles per instr}) * \text{Clk-freq}$.
Discuss one technique to reduce each term in this equation.

Q5)

[7+7]
(a) There is multiprocessor system comprising 10 processors P_1 to P_{10} each with a different MIPS rating. $\text{MIPS}(P_i)=1$, $\text{MIPS}(P_i)=2*\text{MIPS}(P_{i-1})$. What is the overall MIPS of the multiprocessor system?
Evaluate the speedup of this multiprocessor system vis-à-vis a uniprocessor system whose MIPS is the average of the MIPS of the ten processors in the multiprocessor system if the following sequential code fragment is to be executed. Ignore communication delays.

```

Do y= 1,955
  A[y] = B[y] + C[y]
Enddo
Do z= 2, 10
  A[z] = A[z+1] + A[z-1]
Enddo
Do x=1,680
  SUM = SUM + A[z]
Enddo

```

(b) Compare an N nodes hypercube with an N nodes CCC in terms of various network parameters and comment upon their scalability.

Q6)

[7+7]
(a) Given: A sequence of references to a single memory blocks by three processors. A read/write from a processor n is written as r_n / w_n .

Stream : $r_1 \ w_1 \ r_1 \ w_1 \ r_2 \ w_2 \ r_2 \ w_2 \ r_3 \ w_3 \ r_3 \ w_3$

Use either MESI protocol or the Write Once protocol for this problem.

Problem specification for MESI:

Calculate the cost of executing the above reference stream on bus-based SMP that supports MESI protocol without cache-to-cache sharing. Assume that all caches are empty to start with and cache hit take a single cycle, misses requiring upgrade or update take 60 cycles and misses requiring whole block transfer take 90 cycles. Assume all cache are writeback. Illustrate the working of the protocol for the above stream.

OR

Problem specification for WRITE-ONCE:

Calculate the cost of executing the above reference stream on a bus-based SMP that supports WRITE ONCE protocol. Assume that all caches are empty to start with. A cache hit takes a single cycle, a bus read operation takes 90 cycles, a write-invalidate operation takes 50 cycles and a read invalidate operation takes 60 cycles. Illustrate the working of the protocol for the above stream.

(b) Compare a dynamic instruction scheduling approach that is based on register tagging with compiler-driven instruction scheduling. Give the advantages and disadvantages of each approach. Which approach is used in a modern processor?

Q7)

[7+7]
(a) Explain the concepts of sorting network and the 0-1 principle. Based on this explain the bitonic sorting algorithm, illustrating for the following given sequence and derive its complexity. Write the algorithm for a 4-dimensional hypercube. 21, 9, 19, 13, 1, 4, 2, 12, 38, 11, 14, 5, 16, 10, 7, 6.

(b) Write an algorithm for implementing the matrix multiplication algorithm on a CWCR PRAM model using $n^3/\log n$ processors. Derive its complexity. Illustrate how the matrix multiplication algorithm would work on a hypercube and compare its complexity with that achieved by the CRCW algorithm.