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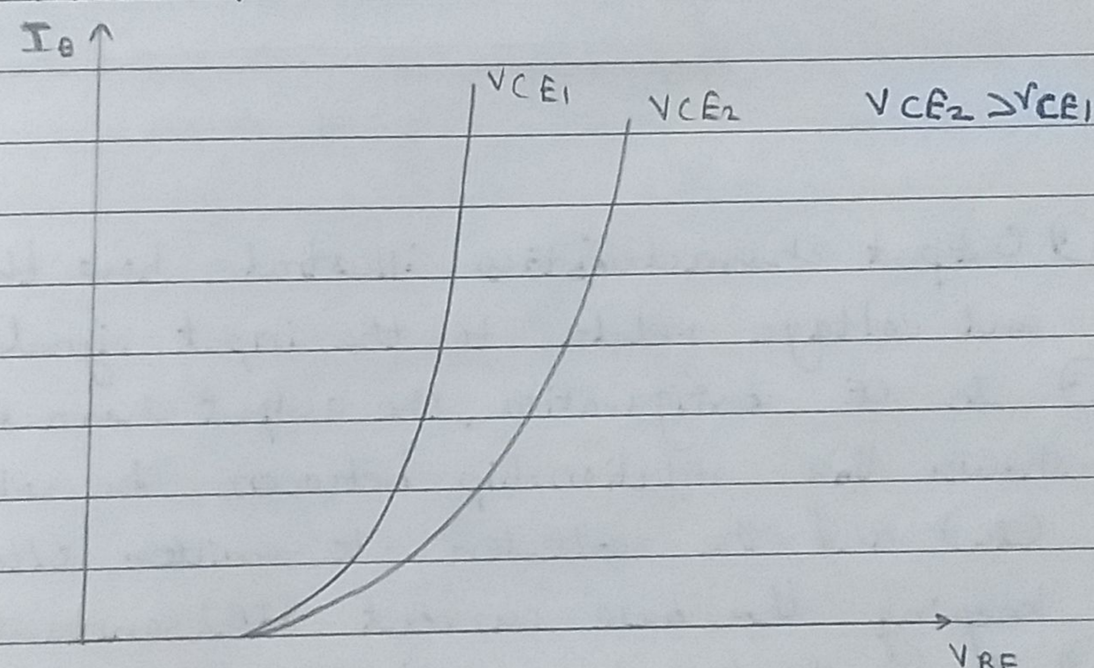
Assignment No - 2

Q.1] Explain input and output characteristics of CE configuration.

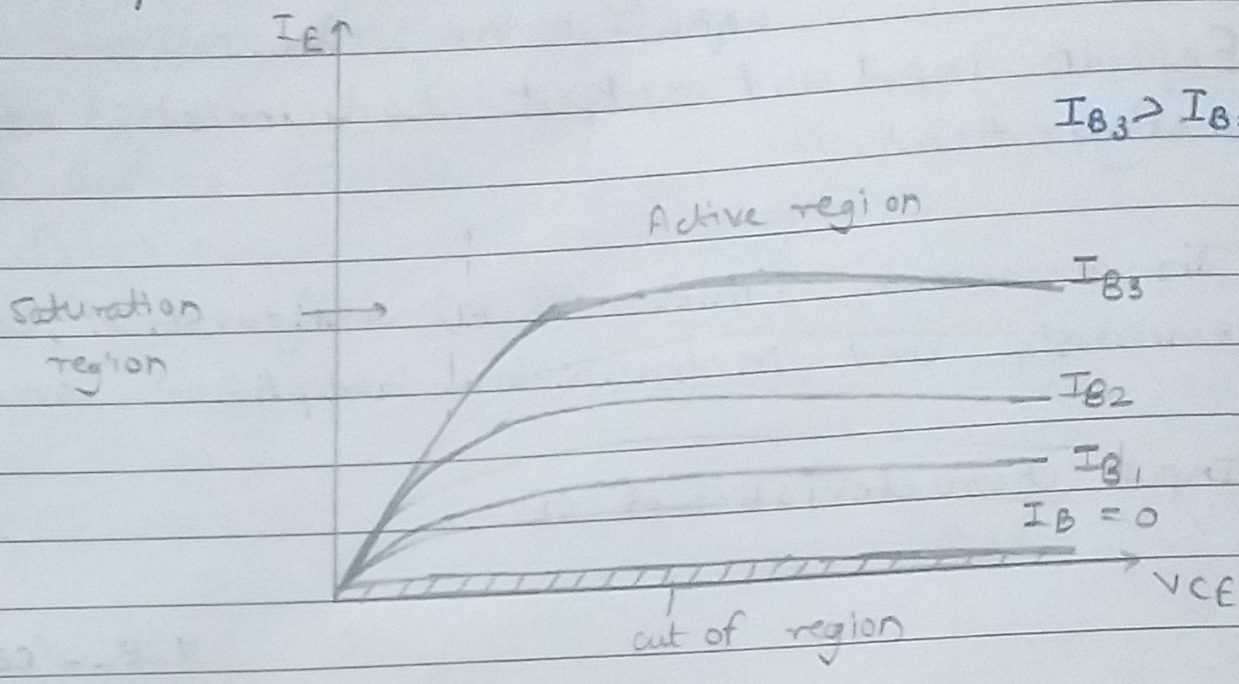
→ In a common Emitter (CE) configuration, which is commonly used in transistor amplifier circuits:

1) Input characteristics of CE -



1. Input characteristics describe how the input current or voltage affects the transistor's behaviour.
2. In CE configuration, the input characteristic typically shows the relationship between the base current (I_B) and the base-to-emitter voltage (V_{BE}), while keeping the collector-to-emitter voltage (V_{CE}) constant.
3. As V_{BE} increases, I_B increases almost exponentially due to the forward-biased junction between the base and emitter.

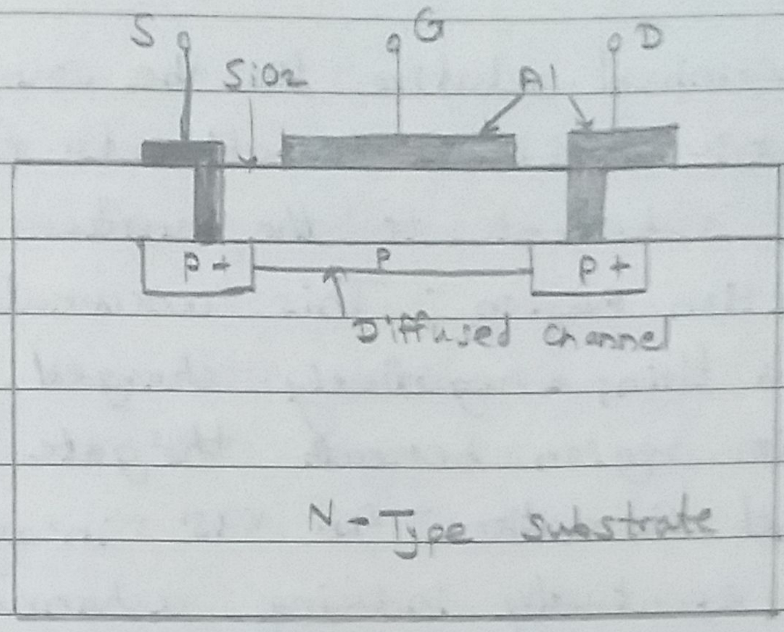
2) Output characteristics of CE -



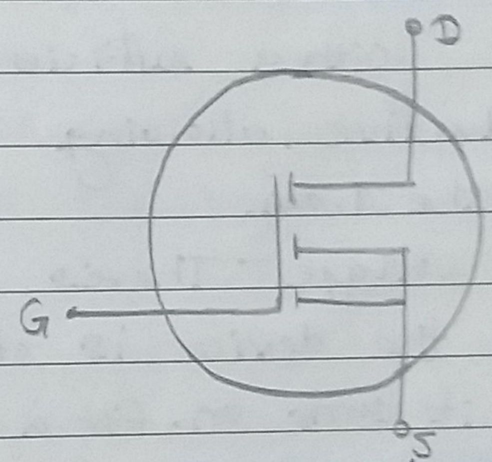
① Output characteristics illustrate how the output current and voltage relate to the input signals.
② In CE configuration, the output characteristics typically shows the relationship between the collector current (IC) and the collector-to-emitter voltage (VCE), while keeping the base current (IB) constant.
③ The output characteristic curve generally shows that the collector current IC increases almost linearly with the collector-to-emitter voltage VCE unit it reaches saturation, where IC levels off due to transistor saturation.

Q.2] Explain construction and operation of P-channel EMOSFET.

→ A P-channel Enhancement-Mode Metal-Oxide-semiconductor Field Effect Transistor (EMOSFET) is a type of FET where current flows between the source and drain terminals when a voltage is applied to the gate terminal.



Structure of p-channel MOSFET



P-channel MOSFET

Construction :-

① Substrate - Typically made of P-type silicon.

② Source and Drain - Regions within the substrate doped with n-type impurities, creating a p-n junction with the substrate.

③ Gate - A metal or heavily doped polysilicon electrodes separated from the substrate by a thin insulating layer (usually silicon dioxide).

④ Body - The region beneath the gate electrode and between the source and drain terminals.

Operations -

① Gate Bias - when a positive voltage is applied to the

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gate terminal relative to the source (VGS <0), it creates an electric field that attracts free electrons from the p-type substrate to the surface beneath the gate.

(2) Depletion Region - This accumulation of electrons from a thin, negatively charged layer called the depletion region beneath the gate oxide.

(3) Channel formation - As VGS increases, the depletion region widens, eventually inducing a channel of electrons in the p-type substrate between the source and drain terminals allowing current to flow.

(4) Conduction - With a sufficient VGS, the channel becomes highly conductive, allowing current to flow from the source to the drain.

(5) Threshold voltage - There's a threshold voltage (Vth) below which the device is off (no channel formed), and above which it turns on. For a P-channel MOSFET, Vth is negative.

Q.3] Define following parameters of Op-Amp.

→

1) BW -

In the context of operational amplifiers (op-Amps), "BW" typically refers to bandwidth. Bandwidth represents the range of frequencies over which an Op-Amp can effectively amplify signals. It's often specified as the frequency range where the gain drops to a certain percentage (eg. -3 dB) of its maximum value. In practical terms, bandwidth determines the frequency range within which an Op-Amp can accurately amplify signals without distortion.

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2) PSRR -

PSRR stands for Power supply Rejection Ratio, which is a measure of an operational amplifier's ability to reject variations in its power supply voltage. It's typically defined as the ratio of the change in the input offset voltage to the change in the power supply voltage. mathematically, it can be expressed as.

$$PSRR = \frac{\Delta V_{\text{offset input}}}{\Delta V_{\text{powersupply}}}$$ initially zero.

where,

ΔV_{ios} = the change in the input offset voltage.

$\Delta V_{\text{power supply}}$ = the change in the power supply voltage.

3) CMRR -

Common mode Rejection Ration, It is the ratio of differential gain to common mode gain. It is ∞ for Ideal Op-amp.

$$CMRR = \frac{A_d}{A_c}.$$

4) Voltage gain -

Open loop voltage gain (A_v). for ideal OP-amp open loop voltage gain is ∞.

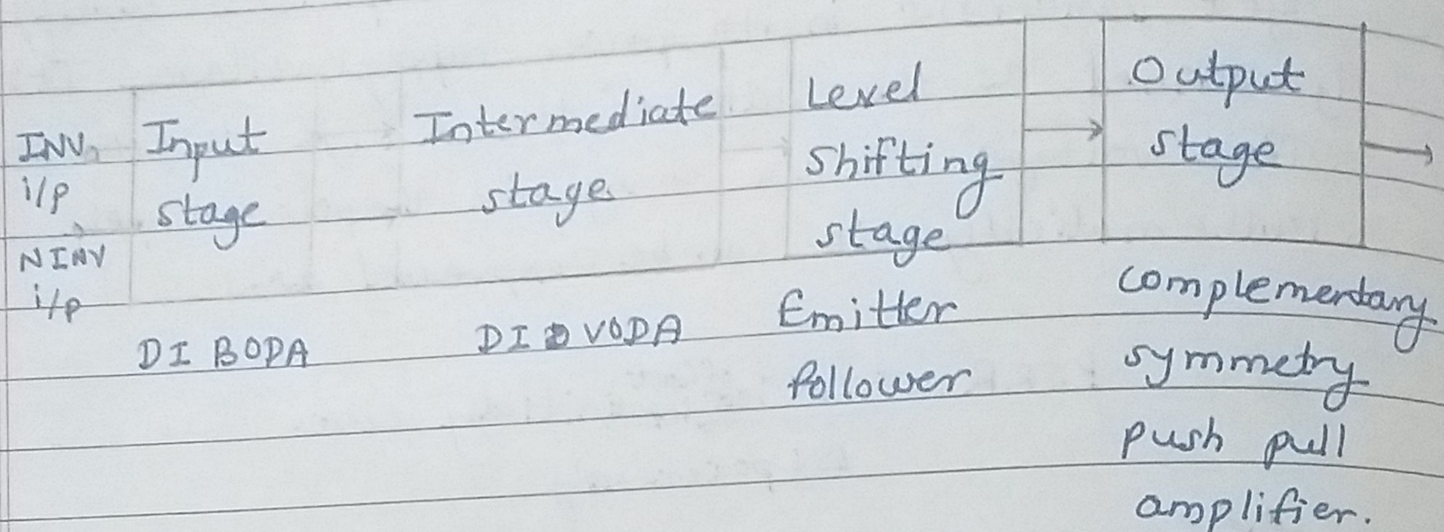
5) Slew Rate - S

Slew rate is denoted by 'S'. It is defined as maximum rate of change of output voltage with time. Ideally value is ∞.

$$S = \left.\frac{dv_o}{dt}\right|_{\text{maximum}}.$$

Q-4] Define ~~an~~ Op-Amp. Draw and explain the functional block diagram of an Op-Amp.

→



① An operational Amplifier consist of foun blocks input stage, intermediate stage, level shifting stage and output stage.

② Input stage - It is dual input balance output differential amplifien (DIBODA). This stage Provides high voltage gain & high impedance.

③ Intermediate stage - It is dual input unbalanced output. differential amplifier (DIVODA). It is also Provides additional gain but has only single output.

④ Level Shifting stage - Due to cascode connecting of two amplifier stages output of intermediate stage gets shifted up from ground level. The level shifted ~~up from ground~~ stage bring back the upshifted output to ground level.

⑤ Output Stage - It is also an high amplifier stage with large current & power gain which uses complementary symmetry push pull amplifier.

Q.5] Prove for an inverting amplifier.

$$AV = -\left(\frac{Rf}{Rs}\right)$$

→ Inverting Amplifier -

① Inverting Amplifier is a negative feedback amplifier and has input given to inverting terminal and non-inverting terminal ground.

② Applying kirchoffs current Law.

$$I_1 = I_B + I_f.$$

$$I_1 = I_f \qquad \because I_B = 0 \text{ ~~for~~ ideal op-amp.}$$

$$\frac{V_{in} - V_a}{R_1} = \frac{V_a - V_o}{R_f}$$

But $V_a = 0$ according to virtual ground concept.

$$\frac{V_{in}}{R_i} = \frac{-V_o}{R_f}$$

$$\boxed{V_o = \frac{-R_i}{R_L} V_{in}}, \quad \boxed{\frac{V_o}{V_{in}} = \frac{-R_F}{R_S}}$$