Design Approach for FPGA based High Bandwidth Fibre Channel Analyser for Aerospace Application

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***Abstract*— Fibre Channel (FC) data transmission protocols are widely used as an interconnecting protocol to cater for the requirement of high-speed data transmission. FC has unique features like high bandwidth, strong anti-interference, flexible topology, distance insensitiveness and low latency. The high-speed, high reliability and low latency of FC communication protocol offers a promising solution for communication protocol in avionics environment. The video / data transmission system performance being critical in aerospace applications, verifying the data flow in the network is vital in order to prevent Hazardous Misleading Information being displayed to the pilot and endangering safety of flight. This paper puts forth a design approach for a receiver module of a Field Programmable Gate Array (FPGA) based high bandwidth Fiber Channel Analyser (FCA). The proposed design is to be implemented using Xilinx Spartan-6 FPGA SP605 evaluation board. The receiver module design addresses the requirements of transmission of soft real time video with resolution (VGA) and link speed with the incorporation of ethernet interface. The concept of developing a high bandwidth FCA for enhanced speed and quality of data, audio and video transmission in avionics system is critical and need of the hour. The outcome of such an effort can be utilized for multiple aerospace applications.**

Keywords – FPGA, Fiber channel, Protocol, Analyser, Avionics, Communication, Aerospace, Network, Transmission, Topology, Receiver module, Latency, Resoultion.

I. INTRODUCTION

Fibre Channel communication technology is the high-speed serial data transmission as compared to other technologies. FC is being explored for the modern aircraft applications for transmission of data, audio and video at various speed. High-bandwidth and strong anti-interference features of FC makes advantage for high speed communication. Avionics environment demands high speed interconnecting medium for transferring huge volume of data between the end systems [1].

The video transmission over FC in avionics systems is considered critical and complex among all the types of data transmission. Errors in FC communication might degrade the quality of video and add latency. The aircraft cockpit display systems like Primary Flight & Multifunction Displays do not show any Hazardous Misleading Information that could result in hazardous or catastrophic situations in real time to the flight or mission. Therefore, testing and validation becomes an inseparable part of integration process of any avionics video system.

This paper proposes a design approach of a receiver module that is capable of receiving Video Graphic Array (VGA) with resolution of 640 x 480 at the nominal rate 1.0625 Gbps through fibre optical link by using ethernet interface to host Personal Computer (PC) in soft real time.

II. PROPOSED HIGH BANDWIDTH FCA FOR AVIONICS DIGITAL VIDEO BUS (ADVB) PROTOCOL

The design approach for the high bandwidth Fibre Channel Analyser in the current study is summarized in the block diagram shown in Fig. 1.

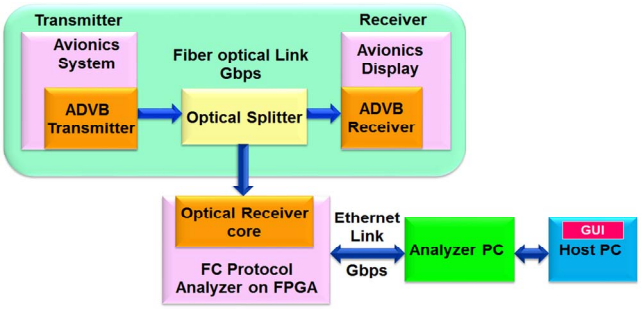

Fig 1. High bandwidth FC Analyser system

The proposed FC Analyser system consists of an avionics system with an FC transmitter at one end and avionics display with an FC receiver at another end. The communication between these two systems is achieved through an fibre optical link. The FPGA protocol analyzer (FC analyzer) will be connected to the fibre optical link. The FC analyzer is used for analyzing the data flow in the communication link ranging up to 1.0625 Gbps. The FC

analyzer receives high speed serial data via the optical receiver, buffers data to the external memory, packetizes it into Institute of Electrical and Electronics Engineers (IEEE) 802.3 frame format and transmits data to the host PC. The communication between the FC analyzer and host PC will be achieved via the ethernet link at a specified data rate (Gbps). The Graphical User Interface (GUI) application for window-based platform will be executed on the host PC, which will accept and process the received packets for decoding, displaying and checking of the FC data in soft real time.

III. Architecture of FC Protocol

FC communication system functions in three different topologies [2].

- Point to Point - Two FC nodes are connected directly
- Arbitrated loop – Capable of connecting multiple devices in a loop manner
- Switched fabric - Devices are connected through switch

Fibre Channel Protocol (FCP) possess multi-layer protocol architecture. It consists of 5 layers that includes FC-0: physical layer, FC-1: encode / decode layer, FC-2: framing protocol / flow Control, FC-3: common services and FC-4: Upper Level Protocol. In addition, there is one more layer, though it is not typically considered part of the basic architecture FC- Arbitrated Loop (AL) layer [3]. FCP offers its functionality in different classified levels. The FCP architecture is shown in Fig. 2.

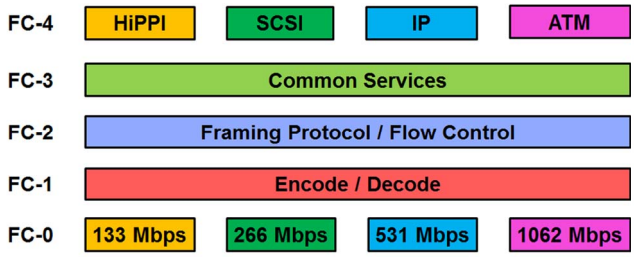

Fig 2. Architecture of Fibre Channel Protocol

FC-0 layer is the physical interface that includes fibre, connectors, parameters related to optical medium and data transmission speed. In addition, the system safety is specified for the laser data link and optical fiber control system. The optical fiber can be a one or multi-mode of operation.

FC-1 layer consists of transmission protocol rules, which includes encoding & decoding instructions for serial data, disparity and the special characters. The 8b/10b encoding scheme offers superior transmission characteristics with low latency.

FC-2 layer containing a standard of signaling protocol and also performs as transport mechanism for FC. The subsequent building blocks are laid down by the standards to aid in transport of data through connection such as protocol, frame, exchange and sequence.

FC-3 layer represents the common services. It is amenably defined for the future use and it offers service required for advanced features such as multicast, striping and hunt groups.

FC-4 layer defines the standards for mapping of Upper Level Protocols (ULP) over FC data structures. Because of its high speed, low overhead and reliability these ULP are used to transport Internet Protocol (IP), Small Computer System Interface (SCSI), IEEE 802.3 and Intelligent Peripheral Interface (IPI).

IV. Structure of FC Frames

A frame is an important unit of data transfer at FC-2 layer. A Fibre Channel frame (FCF) consists of five parts: Start of Frame (SOF), frame header, payload, Cyclic Redundancy Check (CRC) and End of Frame (EOF). The SOF and EOF act as a delimiter in order to set the signal of a 4-byte word used for sequence control. The frame header consists of 24 bytes length and contains address information and sequence number of each frame. The data payload in an FC frame contains, up to 4 to 2112 bytes per frame of actual data [4]. The CRC checksum facilitates error detection in the frames received. In addition, the 4-byte word is used for error handling. Prior to encoding at the FC-1 layer, the sender calculates the CRC checksum. After decoding at the FC-1 layer, the receiver calculates the checksum. The Ideal Ordered Sets shown at the two ends of the frames are to keep synchronization in FC connection. The FCF structure is shown in Fig. 3.

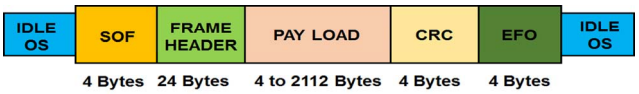

Fig 3. FCF structure

V. Bandwidth Calculation

In the proposed design approach of a receiver module for VGA resolution of 640 x 480, the bandwidth calculation based on VGA frame is as follows (Fig. 4).

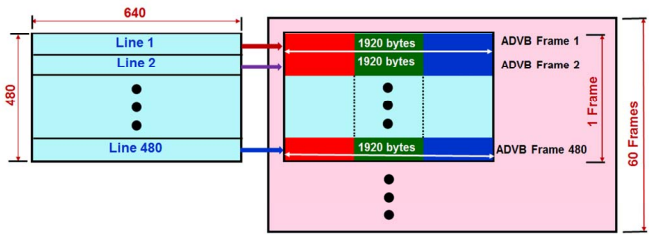

Fig 4. Details of VGA frame

Bandwidth (BW) is calculated using [5] equation No. 1

$$BW = tbvf \times fps \times protocol\ overhead \times 8b10b \quad (1)$$

Where tbvf denotes total bits in the video frame, fps denotes frames / second, 8b10b denotes 8-bit to 10-bit encoding structure. The protocol overhead is approximated = 5%.

For VGA image resolution of 640 x 480, each of the 640 RGB pixel per line requires 3 bytes, totaling to 1920 bytes per line with 60 Hz frequency. Each frame has a maximum limit of 2112 bytes of payload. Hence, the VGA video lines are well within the limit. The VGA resolution of 640 x 480 RGB video frame requires 580.608 Mbps of data transfer. The ARINC 818 Avionics Digital Video Bus standard fiber channel link rate is 1.0625 Gbps. The ethernet maximum data transfer rate is 1 Gbps (125 Mbytes) and the data loading is 58.0608 percent out of 100 percent.

VI. PROPOSED ARCHITECTURE OF THE RECEIVER

The following functionalities are proposed to be part of the receiver module:

- The system should receive fiber channel serial data at the nominal rate of 1.0625 Gbps.
- The received data should be decoded and converted from serial to parallel 32-bit wide.
- The frames of user defined length should be detected in trigger detect block and stored in the memory.
- The received data from FPGA should be stored and buffered for further transmission to host PC in soft real time. The communication between FPGA and host PC is through ethernet.

The receiver module consists of Small Form Factor Pluggable (SFP) Transceiver, Gigabit (GTP) Transceiver, Trigger Detect Blocks (TDB), 32-bit First-In First-Out (FIFO), Memory Data Handler (MDH), Memory Controller Core (MCC), 32-bit to 8-bit First-In First-Out, Ethernet Packetizer (EP), Tri-Mode Ethernet Medium Access Controller Core (TEMAC), User Datagram Protocol (UDP) packet validation & Trigger Generation, Ethernet Physical Interface (EPI) and Graphical User Interface (GUI) that are as shown in Fig. 5. The functions of these blocks are described briefly as follows.

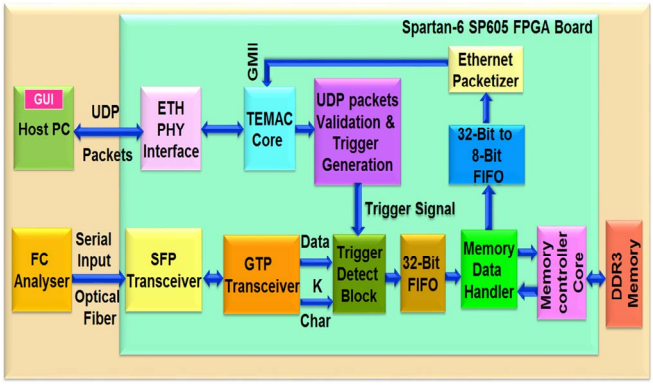

Fig 5. Proposed block diagram of receiver module

A. Small Form-factor Pluggable Transceiver

The SFP transceiver module receives the serial data from the FC analyzer through an optical fibre. The received serial data is converted from optical to electrical signals.

B. Gigabit Transceiver

The serial data received from SFP transceiver is converted to parallel data & 'K' character of 16-bit. Subsequently, it is converted into 32-bit data for alignment of even bytes. The output of GTP transceiver is sent to TDB.

C. Trigger Detect Block

On detection of a positive edge trigger, the TDB carries out a comparison of the parallel output data received from GTP transceiver with the user defined data reference value (read packets) stored in the host PC via ethernet interface. On finding the match between received data and user defined (reference) data, the TDB gives output signal to write the data into 32-bit FIFO.

D. 32-bit First-In First-Out

Memory structure is dominant mechanism to control the flow of data between source and destination. It is programmed as 32-bit FIFO of write buffer module. When TDB enable signal changes from low to high, the data is read and incoming data is written into the FIFO. The 32-bit FIFO output signal is fed to the memory data handler.

E. Memory Data Handler

This module is designed to receive the frames from 32-bit FIFO. The data is transmitted and received from the memory controller core block for the read / write operations to an external storage device. The handler also receives the request from ethernet for read / write operations.

F. Memory Controller Core

The MCC module scheme has been integrated in Xilinx FPGA board as a memory controller unit to be interfaced with DDR3 memory by using Memory Interface Generator core. The FPGA board offers continuous communication between MIG core & DDR3 memory to perform read and write operations. The MIG tool is used to configure different ports for read and write operations. The DDR3 is configured for 333 MHz data rate. After the entire data has been read from the memory, read complete signal is fed to TDB to notice the next trigger.

G. 32-bit to 8-bit First-In First-Out

The 32-bit to 8-bit FIFO is programmed as a read buffer. UDP data fields are byte oriented, hence need to be converted from 32-bit into 8-bit data in order to map the data into UDP. The conversion from 32-bit to 8-bit data is performed by this FIFO module. The converted data read from the memory is stored in the FIFO.

H. Ethernet Packetizer

The UDP frames are generated by this module, after the captured data is completely written into memory. The MAC, IP & UDP header are generated on detection of a positive edge write capture signal, with calculation of IP Checksum. A 32-bit status data follows the header data, indicating the ethernet packet number and additional status.

I. Tri-EMAC Core

In this design approach, the FPGA TEMAC Core generator family is used for ethernet protocol communications. TEMAC - FPGA is interfaced using AMBA Crosslink Interface (AXI4) stream protocol. The AXI4 has a master and slave. TEMAC core has been programmed for an operational speed rate 1 Gbps. The receiver module is accessed through the TEMAC. In the TEMAC block the Preamble, start of frame and frame check are generated. The check sequence fields for the ethernet packets are coded using AXI4-Stream, which is a protocol designed to transport arbitrary unidirectional data streams.

J. UDP packet validation & Trigger Generation

This module receives the UDP and validates these packets to segregate the targeted UDP from other packets. These packets are validated by checking IPv4, ethernet type, destination & source IP, port destination number of first 8 bytes namely reference signal, signature and payload of the frame. The packets are valid only when the said parameters match with the input reference. Data reference, length and values of the valid packets are stored for further handling. The last 4 bytes are command signal of the packet, which is used to generate a trigger signal and the same is fed to the TDB for several clock cycles.

K. Ethernet Physical Interface

This module is used for ethernet communication of 1 Gbps, also designed to work in Gigabit Media Independent Interface with physical address.

L. Graphical User Interface

As mentioned earlier (Sec. II), it is proposed to introduce customized GUI application between FPGA and host PC that is capable of monitoring the frames and providing trigger signal to FPGA. The GUI application is a window-based platform of Microsoft Visual Studio that interfaces with the host PC through ethernet to achieve the intended task. The tasks of the GUI include (1) Start capture signal of UDP packet to FPGA (2) Data length & reference (3) Total number of frames captured (4) Frame numbers (5) Current frame error status (6) Total words in current frame (7) Data log progress bar and (8) Decode the stored data & display.

The overall flowchart highlighting the functionality of the proposed receiver module is shown in Fig. 6.

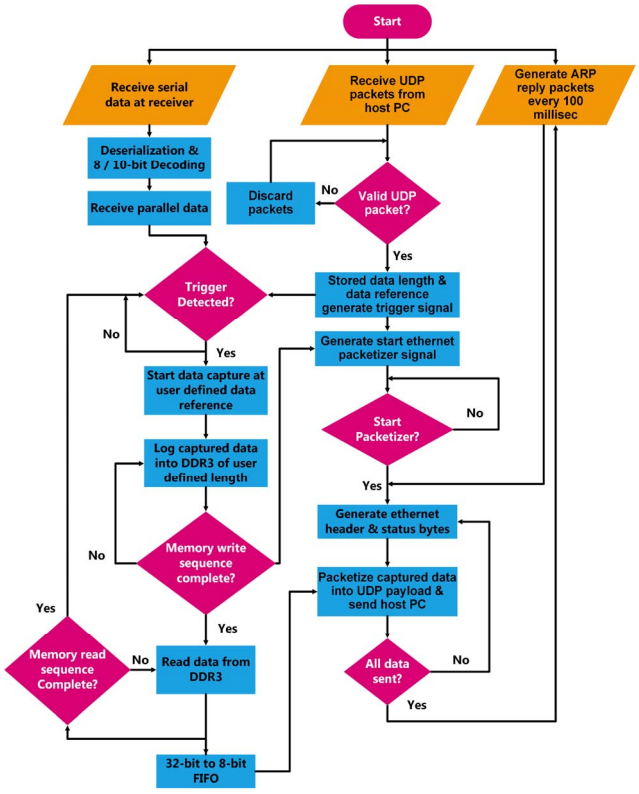

Fig 6. Proposed receiver module flowchart

VII. RESULTS

Test was carried out in order to check the functionalities of few blocks (i.e SFP, GTP, Trigger Detect Block, 32-bit FIFO, Memory data handler and Memory controller core through a fiber optical link) of receiver module for FCA. The Very High Speed Integrated Circuit Hardware Description Language (VHDL) coded frames were generated by Xilinx spartan-6 FPGA for transmission to host PC. The test setup of the proposed design receiver module is shown in Fig. 7.

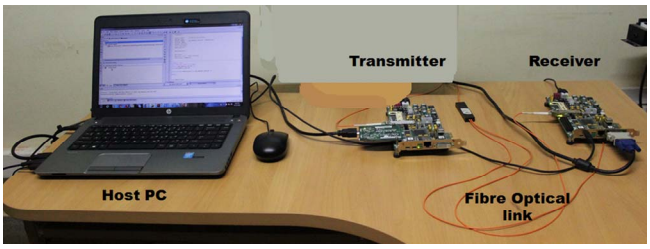

Fig 7. Test setup

The Wireshark tool was used to monitor and check the UDP packets transmitted between FPGA and host PC. The tool showed that the received packets were captured and transmitted as per design. The transmitted data from FPGA to host PC is shown in Fig. 8.

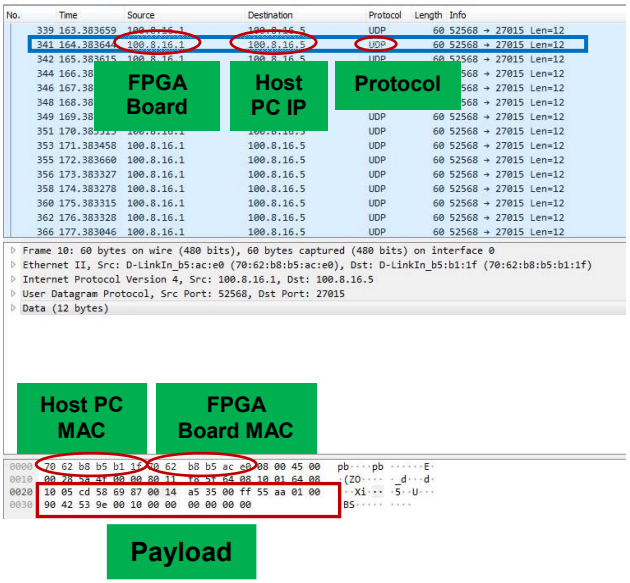

Fig 8. Received UDP frames

The source IP address (FPGA) and MAC is identified as 100.8.16.1 and 70 62 b8 b5 b1 1f respectively. Similarly, the destination IP address (host PC) and MAC is identified as 100.8.16.5 and 70 62 b8 b5 ac e0 respectively. The UDP is used for the data transfer through ethernet. The header and payload of the FC frame are represented by the payload of ethernet frame.

VIII. CONCLUSION

A design approach of FPGA based high bandwidth FCA for aerospace application, with link rates in the range of 1.0625 Gbps using the Xilinx Spartan-6 FPGA evaluation board was proposed in this paper. The design of the receiver module addressing the requirements of transmission of VGA resolution of 640 x 480 through fibre optical link using ethernet interface to host PC in soft real time was presented. Functionality checks were carried out on few blocks of the receiver module. The Wireshark tool showed that the received UDP packets were captured and transmitted as per design between FPGA and the host PC.

Further work envisaged to realize the full-fledged high bandwidth FC Analyser includes transmission of Avionics Digital Video Bus (ADVB) frames of VGA in soft real time and Cyclic Redundancy Check (CRC) of each frame to be implemented in a customised GUI application via ethernet interface to a host PC.

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