

Construction Analysis of Flip Chip Package for Aerospace Application

Zhao Liyou*, Kong Zebin, Li Zhen, Wang Kunshu

Centre for components reliability
Shanghai Aerospace Technology Foundation
Shanghai China

*Email: zhaoliyou0617@163.com

Abstract—Eight typical flip chip packages were adopted in this study, two domestic, six imported, and five of the six imported were models with experience of aerospace application. The construction and material of these flip chip packages were analyzed, and similarities and differences between the domestic and the imported packages were compared. Construction analysis criteria of flip chip package for aerospace application were summarized based on these results. The results of this study could play an important guiding role in construction analysis of aerospace flip chip package components.

Keywords—*flip chip package; construction analysis; aerospace application*

I. INTRODUCTION

Flip chip technology is a means of chip assembly that a chip is attached face down to a substrate by bumps. This advanced flip chip interconnect technology can significantly improve the performance of high-speed systems and raise the integration of packages. As aerospace electronic systems develop toward multifunction, miniaturization, and high speed, flip chip packaged components are wildly applied in aerospace, and these flip chip packages are basically imported [1]. A comparison of construction and material between the imported and the domestic flip chip packages can show deficiency of the domestic packages, thus beneficial for promoting its future application in aerospace, but there have been few reports on this area by far.

Construction analysis is a key part of reliability evaluation before aerospace application of components, which is to obtain the component information of construction, material, and process by a series of destructive and non-destructive tests, and evaluate their aerospace applicability [2-4]. Existing stands mainly provide construction analysis methods of general packages which adopt the wire bonding or the tape automated bonding. It is necessary to investigate construction analysis methods of the flip chip package.

This study adopted typical flip chip components at home and abroad, and a comparison of package construction and material was carried out. Construction analysis criteria of the flip chip package for aerospace application were summarized based on the comparison results.

II. EXPERIMENTS AND ANALYSIS

Eight flip chip package components were adopted in this study, shown in Table I. Six of the components were imported, and five of the six imported were models with experience of aerospace application. The other two were domestic and intended for aerospace application.

TABLE I. THE ADOPTED FLIP CHIP PACKAGES

Components	Company	Application	Code name
FPGA	Domestic	—	Domestic I
FPGA	Domestic	—	Domestic II
Microprocessor	TI	Satellite X	Imported I
Microprocessor	TI	—	Imported II
Microprocessor	TI	Satellite X	Imported III
FPGA	XILINX	Satellite X	Imported IV
DSP	TI	Satellite X	Imported V
FPGA	XILINX	Satellite X	Imported VI

A. Marking

Laser marking was used in the domestic packages. The lid coating was penetrated during marking to cause the lid substrate bare, as shown in Fig. 1. When the working or test environment is seriously corrosive, the lid is vulnerable to corrosion, so construction analysis should require optimization of the marking process or protection of the lid. Both ink marking and laser marking were used in the imported packages, and the penetration of lid coating was not found, as shown in Fig. 1.

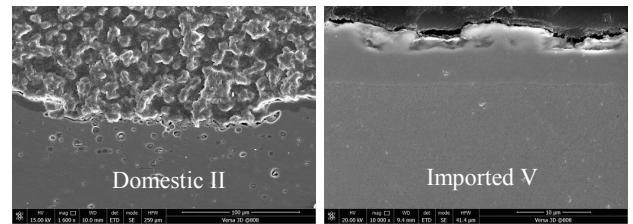


Fig. 1. Typical cross-section images of marking

B. Lid

Table II showed the material of lid substrate and coating. The lid material of the domestic packages was Al-Mg alloy, and the imported packages adopted Kovar, Al-Mg or Cu alloy lid. Ni/Au or Ni/Au/Ni/Au coating was used in the Kovar lid, and Al₂O₃ coating in Al-Mg lid, Ni coating in Cu lid. The domestic and the imported II, IV, V, VI packages stuck lids on

chips (and substrates) using thermal interface materials. EDS analysis indicated that the thermal interface materials were polymer filled with Al_2O_3 and SiO_2 particles.

TABLE II. MATERIALS OF LID SUBSTRATE AND COATING

Code name	Substrate	Coating	Thickness of coating (μm)
Domestic I	Al-Mg	Al_2O_3	7
Domestic II	Al-Mg	Al_2O_3	8
Imported I	kovar	Ni/Au	2.8/2.4
Imported II	Al-Mg	Al_2O_3	8
Imported III	kovar	Ni/Au/Ni/Au	4.1/1.2/4.4/2.0
Imported IV	Cu	Ni	6
Imported V	Cu	Ni	8
Imported VI	Cu	Ni	5

The imported I and III packages employed classical sealing methods. A kovar frame was first welded to the Al_2O_3 substrate using AgCu solder in the imported I. Then, the kovar frame and the lid were welded together by parallel seam sealing. The lid was welded directly to the Al_2O_3 substrate using AuSn solder in the imported III package. To realize welding of kovar to Al_2O_3 , ceramic metallization was conducted in the imported I and III, and the first metallization layer was W, then the Ni layer on it.

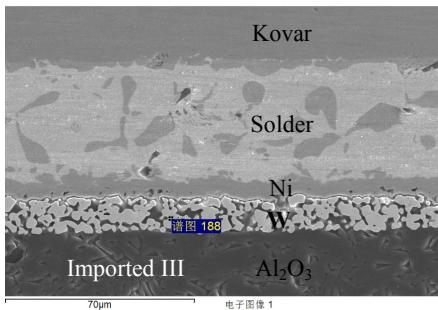


Fig. 2. The cross-section image of ceramic metallization

C. Bump

Table III showed the analysis results of bumps in this study. The imported packages adopted SnPb or SnAg bump solder, and SnAg was used in bumps of the domestic packages. Flip chip bumps usually employed Sn63Pb37 eutectic solder in the past for its excellent properties, but Sn63Pb37 usually melt during surface mounting of components, thus resulting in short circuit of bumps. In this study, non-eutectic SnPb bumps were used in the imported packages. Non-eutectic SnPb may also melt during surface mounting, but because of its higher melting point and larger viscosity coefficient, short circuit of bumps can be inhibited well. SnAg solder has better fatigue resistance and tensile strength than Sn63Pb37, but the wettability is relatively poor.

TABLE III. THE ANALYSIS RESULTS OF BUMPS

Code name	Material	Dimension (width/height μm)	Spacing (μm)
Domestic I	SnAg	111/77	381
Domestic II	SnAg	90/93	252
Imported I	Sn78Pb22	120/70	227
Imported II	Sn75Pb25	116/109	365
Imported III	Sn72Pb28	112/70	190
Imported IV	Sn58Pb42	126/99	346
Imported V	SnAg	101/82	244
Imported VI	Sn71Pb28	135/101	190

There are four major classes of flip chip bumps, namely, meltable solder bump, partially meltable bump, non-meltable bump, and polymeric adhesive bump. Meltable solder bump would melt during flip chip bonding if the reflow temperature reaches the solder liquidus temperature. Sn content is usually high in the meltable solder bump, which can exhaust Cu metallization in a short time, resulting in separation of intermetallic compounds from under bump metallization (UBM) [5]. Thickening of Cu metallization is adopted to solve this problem, and if the exhaustion of Cu metallization does not occur, intermetallic compounds would grow along Cu metallization. The domestic I and the imported I, II, and III employed the meltable solder bump, as shown in Table III and Fig. 2. Another method to prevent the exhaustion of Cu metallization is to use UBM which reacts with Sn slowly, such as the imported IV, V, and VI. The bump with a high Pb solder stud and a low melting point solder tip is known as partially meltable bump. The high Pb solder stud does not melt, and the low melting point solder melt during flip chip bonding. A Cu stud with a low melting point solder tip is also of partially meltable bump, such as the domestic II. The other two classes of flip chip bumps were not included in this study, which have no experience of aerospace application interiorly. Dimension and spacing of the domestic packages are similar to that of the imported, width around 100 μm , height over 70 μm , and spacing over 70 μm .

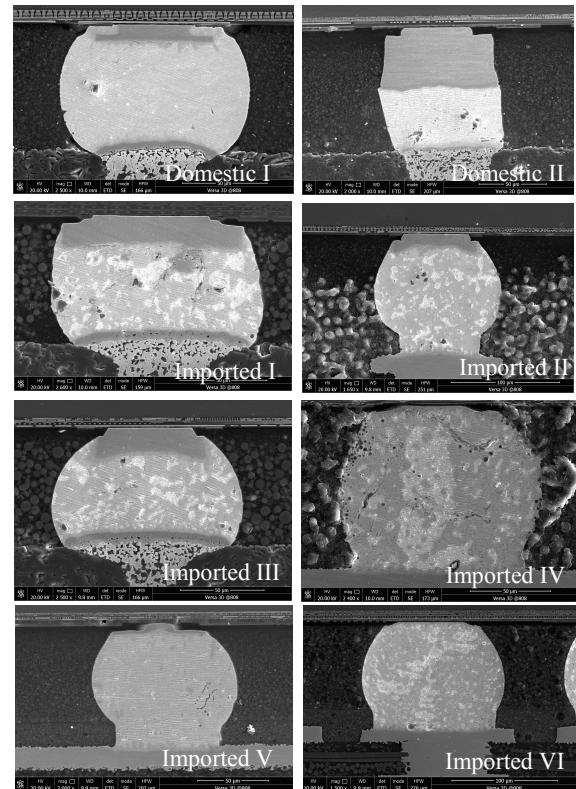


Fig. 3. Cross-section images of bumps

D. UBM

UBM between the bump and the aluminum pad is composed of an adhesion layer, a diffusion barrier and a wettable layer. Previous reports indicated that the adhesion

layer is usually Cr, Ti, Ti-W or Al, the diffusion barrier is usually Cr, Cr-Cu, Ti, Ti-W or Ni-V, and the wettable layer is usually Cu or Ni [6]. Table IV showed the UBM of the packages in this study. Ti/Cu UBM was adopted in the domestic packages and the imported packages employed Al/Ni-V/Cu or Ti-W/Cu.

TABLE IV. UBM OF THE ADOPTED PACKAGES

Code name	UBM	Code name	UBM
Domestic I	Ti/Cu	Imported III	TiW/Cu
Domestic II	Ti/Cu	Imported IV	Al/NiV/Cu
Imported I	TiW/Cu	Imported V	TiW/Cu
Imported II	TiW/Cu	Imported VI	Al/NiV/Cu

E. Underfill

Underfill was used to redistribute the thermomechanical stress created by the Coefficient of Thermal Expansion (CTE) mismatch between the chip and the substrate, as shown in Fig. 4. The interface between the underfill and the chip was well in all the adopted packages of this study. There was a polyimide layer on the chip of all the imported packages, which had an effect of moisture proof and decreasing chip surface stress caused by the CTE mismatch between the chip and the solder (or underfill). The domestic I did not employ this polyimide layer. Construction analysis should require supplement of this protection or evaluation of the reliability by scientific tests before aerospace application.

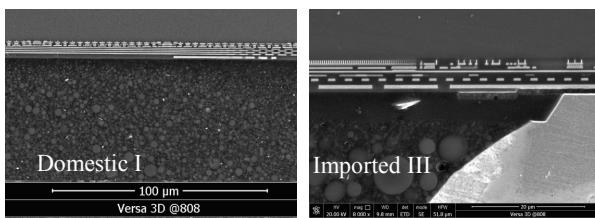


Fig. 4. Cross-section images of underfill

External visual was conducted after delidding of packages to inspect filling quality of underfill. Underfill should be neither too much, nor too little. Too much will affect heat radiation, and too little can fail to provide adequate functionality. It can be seen from the top of chip that underfill distributes all around the chip in this study, as shown in Fig. 5.



Fig. 5. External visual images of filling quality of underfill

F. Substrate

There were two types of substrates in this study, ceramic and organic. The ceramic material was Al_2O_3 , the wire metallization was W, and the hole metallization was Mo-W. Vertical interconnection in the ceramic substrate was achieved by stacking of a necessary numbers of substrate layers, but a good alignment of metallization was difficult, due to the stacking process by high pressure mechanical press. From the

Fig.6, it can be seen that the connected metallization hole of different layers in substrate is not in a good alignment for one domestic flip chip package, and it is much better for the imported packages. Construction analysis should require improvement of the substrate quality. The pad material of ceramic substrate in this study was Ni, which can react with Sn to form Ni_3Sn to complete welding.

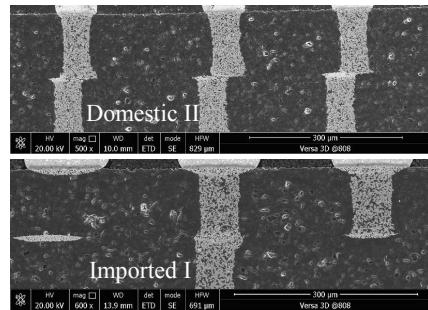


Fig.6. The alignment quality of metallization in ceramic substrate

The organic substrate of the imported package in this study had a core at the center that employed ordinary PCB technology and build-up layers on both side of the core that employed micro-via hole for layer to layer connection, as shown in Fig. 7. The role of core was to provide mechanical rigidity and power layers with containing thick Cu conductor plane. Build-up layers were processed sequentially put over on both side the core to provide high density wiring for flip chip bonding. The through holes in the core were filled with organic resin.

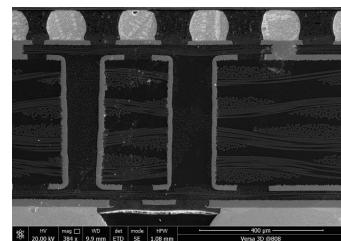


Fig.7. Cross-section image of organic substrate

G. Lead

Table V showed types and materials of leads in this study. The results indicated that flip chip package can employ different types of leads, including BGA, CGA, and PGA. BGA materials are generally of two kinds, lead and lead-free. Compared with BGA, CGA leads have higher reliability in a thermal stress environment. One domestic package adopted CGA leads, and there Sn76Pb23 solder column was welded on W/Ni metallization of substrate using 63Sn37Pb eutectic solder. PGA was developed on the basic of DIP, to realize multi-lead and raise packaging density. One domestic package and one imported package adopted PGA leads. Pins were welded on W/Ni metallization of substrate using AgCu solder in PGA. The pin material was kovar alloy, the coating material was Ni/Au.

TABLE V. TYPES AND MATERIALS OF LEADS

Code name	Types	materials	
Domestic I	PGA	Kovar	Ni/Au coating
Domestic II	CGA	Sn76Pb23	Sn63Pb37

Imported III	PGA	Kovar	Ni/Au coating
Imported I	BGA		Sn63Pb37
Imported II	BGA		Sn73Pb27
Imported VI	BGA		Sn96Ag4

III. CONSTRUCTION ANALYSIS CRITERIA

The construction analysis criteria of flip chip packages for aerospace application were summarized based on above experimental results. Failure cases and existing standards of flip chip packages, such as national military standard, American military standards, and aerospace standard were also referred during the summary.

A. Marking

The marking should be complete and meet the corresponding requirements of GJB597A-1996. The lid coating should be not penetrated for the laser marking when used in seriously corrosive environment, or else a necessary protection of marking should be conducted.

B. Lid

Lid material should have experience of aerospace application. The lid coating should have good adhesion to the substrate. The coating material and thickness should meet MIL-PRF-38535K corresponding requirements. Sealing should adopt aerospace common process and material. The lid bonding quality should meet GJB548B method 2030 ultrasonic inspection requirements.

C. Bump and UBM

The bump and UBM should employ construction and material with experience of aerospace application. The flip chip package should meet GJB548B method 2017 internal visual requirements. The interface bonding of different materials should be well. The flip chip package should meet GJB548B method 2011 bond strength or 2031 pull-off test requirements.

D. Underfill

The hermetic package should meet GJB548B-2005 method 1018 internal gas analysis requirements. The moisture sensitivity level of non-hermetic package should meet the requirements of application, and manufactures should provide reasonable transport, storage and using conditions. Generally, the height of underfill can not be lower than 1/3 of the chip, and there are no underfill remains on the upper surface of chip. When the ceramic substrate with non-meltable bumps is used, the underfill quality should meet GJB548B method 2030 ultrasonic inspection requirements. The flip chip package which employs a ceramic substrate with meltable bumps or an organic substrate should meet J-STD-020 ultrasonic inspection requirements.

E. Substrate

The substrate and metallization material generally should have experience of aerospace application. The organic substrate should meet GJB362B-2009 requirements. The hole

and wire metallization in ceramic substrate should have no quality defect. The connected metallization of different layers should be in a good alignment.

F. Lead

The lead and coating material should meet MIL-PRF-38535 requirements. The lead pitch and dimension should meet MIL-STD-1835 requirements, or coincide with that of packages which have experience of aerospace application. Solder ball and column leads should meet the mechanical property requirements in GJB7677. Pin grid array should meet GJB 548B lead pull test requirements.

IV. CONCLUSION

A comparison was conducted on construction and material between the domestic and the imported flip chip packages. The domestic flip chip packages adopted construction and material roughly the same as the imported. The lid coating of one domestic flip chip package is penetrated during laser marking to cause the lid substrate bare. When the working or test environment is seriously corrosive, the construction analysis should require optimization of the marking process or protection of the lid. A polyimide layer used in the imported device is not adopted on one domestic chip surface, which has an effect of moisture proof and decreasing chip surface stress. Construction analysis should require supplement of this protection or evaluation of the reliability by scientific tests before aerospace application. The connected metallization hole of different substrate layers is not in a good alignment for one domestic flip chip package, and it is much better for the imported package. Construction analysis should require improvement of substrate quality. The construction analysis criteria of the flip chip package for aerospace application were summarized in this study, and the results can be used as the reference for the construction analysis of aerospace flip chip packages.

- [1] Q. Zhang, Y.L. Zeng, W.M. Zhu, "Quality assurance analysis of aerospace Non-hermetic ceramic flip chip package FPGA," Quality and Reliability, vol. 2, pp. 55-58, 2013.
- [2] X. Gong, "Structural analysis of DC/DC power modules for aerospace application," Electronic Product Reliability and Environmental Testing, vol. 28, pp. 23-28, 2010.
- [3] Y.W. Zhang, L.D. Jiang, Z.Q. Chen, "A new method for reliability evaluation of device-construction analysis (CA)," Electronic Product Reliability and Environmental Testing, vol. 10, pp. 1-3, 2003.
- [4] L. Zhang, H. Xia, X. Gong, "Structure analysis of space components," Electronic Product Reliability and Environmental Testing, vol. 30, pp. 53-57, 2012.
- [5] L. Wang, D.P. He, D.Q. Yu, J. Zhao, H.T. Ma, "Current research on the reaction between solder bump and under bump metallurgy system in flip chip," Materials Review, vol. 19, pp. 16-19, 2005.
- [6] J.H. Guo, S.D. Wang, Z.H. Zhang, T. H, S.L. Jia, "UBM of bumps for flip chip," Semiconductor for Technology, vol. 26, pp. 60-64, 2001.