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EDUCATION & AWARDS

The University of Texas at Austin - Austin, TX
Integrated Masters of Engineering - Architecture, Computing Systems, and Embedded Systems *GPA: 3.90* **Aug. 2024 - Dec. 2025**
Bachelor of Science - Electrical and Computer Engineering *GPA: 3.80* **Aug. 2020 - May 2024**

Awards: March Economic Madness Winner - *The IC2 Institute* **Mar. 2022**
CS Research Mentorship Program (CSRMP) Class of 2023A - *Google* **Jan. 2023 - May. 2023**

RELEVANT COURSEWORK

Computer Architecture • VLSI • ASIC Design Lab 1 • Computer Perf. & Benchmarking • Digital Logic Design • Embedded Systems • Circuit Theory
Software Design and Implementation I/II • Algorithms • Matrices/Matrix Calculations • Linear Systems and Signals • Concurrent and Distributed Systems

TECHNICAL SKILLS

SystemVerilog • Verilog • Python • C/C++ • UVM • Synopsys Verdi • Cadence Tools • Git • Assembly

WORK EXPERIENCE

ARM Austin, TX – *Incoming SoC Design Engineer Intern* **May 2025 - Aug 2025**

Microsoft Seattle, WA – *Silicon Engineering Intern* **May 2024 - Aug 2024**

- Worked on Azure Artificial Intelligence Silicon Engineering (AiSiE) under Cluster DV team for verification of AI GPU chip working with coverage, connectivity, and performance
- Developed functional coverage test plan, implemented in SystemVerilog, and reviewed in weekly coverage tests using Verdi to verify module enabling multicast writes from direct memory access control block to target memory systems
- Created and setup workflow for formal connectivity check tests and extraction of signals to verify and find valid paths in design using VC Formal
- Developed Python scripts to decode SRAM block addresses and measure bandwidth, while optimizing stimulus tests to improve direct memory access control block performance results by 20%, aligning with architectural specifications

Amazon Web Services (AWS) Seattle, WA – *SDE Embedded Intern* **May 2023 - Aug 2023**

- Worked on AWS EC2 Commercial Software Services team to deliver timely resolutions and optimize performance for SAP customers' applications and infrastructure running on AWS resources including EC2 Instances and EBS Volumes
- Utilized Python lambda functions and AWS System Manager Automation Documents to develop a storage configuration check system for SAP HANA databases, providing customers insights into SAP application misconfigurations

Advanced Micro Devices (AMD) Austin, TX – *Design Verification Engineering Co-op/Intern* **Jan. 2023 - May 2023**

- Worked on Foundry Technology and Operations (FTO) Advanced Technology team creating testing model and testbenches to enable ATE pattern generation in C++ and SystemVerilog for verification of FTO's three nanometer chiplet test chip technology
- Developed a Python-based Regression Analysis Tool to consolidate, execute, and optimize multiple patterns/test case results into a singular process, improving runtime from 3-6 minutes to 30 seconds

PROJECTS

AES Module Tapeout - *ASIC Design Lab 1 Final Project* **Jan. 2025 - May 2025**

- ASIC tapeout of provided AES encryption core targeting high performance within 345μm × 345μm die area limit completing full RTL-to-GDSII flow: synthesis, floorplanning, power planning, APR, clock tree synthesis (CTS), chip signoff, and resolvingDRC/LVS using Cadence and Synopsys tools
- Pushed design to timing and power limits, achieving maximum frequency by optimizing clock paths, minimizing IR drop with robust power grid design, and resolving all setup and hold violations
- Integrated scan chain passing all DRC and LVS checks and implemented decap and filler cells to meet physical and design closure requirements

Benchmarking M3 Pro GPU – *Grad Computer Performance Evaluation and Benchmarking Final Project* **Feb. 2024 - May 2024**

- Compared Apple's M3 Pro GPU to NVIDIA's RTX 3080 GPU compute performance with metrics such as throughput, arithmetic intensity GLOP/s, and L2 Cache Miss Rate
- Evaluated and developed GEMM/GEMV benchmarks for 512, 1K, 2K dimensions utilizing Metal and CUDA framework for each GPU respectively and tested open sourced SHOC Benchmarks utilizing OpenCL and CUDA
- Results of SHOC benchmarks found NVIDIA to outperform the M3 Pro and GEMM/GEMV results varying for key metrics

All Digital Phase Locked Loop – *Grad VLSI 1 Final Project* **Oct. 2023 - Dec. 2023**

- Researched and designed an All Digital Phase Locked Loop (ADPLL) on a 45 nm technology node that meets high performance specifications
- Explored two different designs using a XOR Digital Phase Detector/Time to Digital Converter, Digital Loop Filter, and Digital Controlled Oscillator
- Conducted synthesis, timing analysis, and exhaustive functionality tests, including in-depth assessments of phase noise, lock time, area, and jitter using Synopsys VCS and Cadence Innovus