

UART PROJECT

TEAM NAME : **BJT**

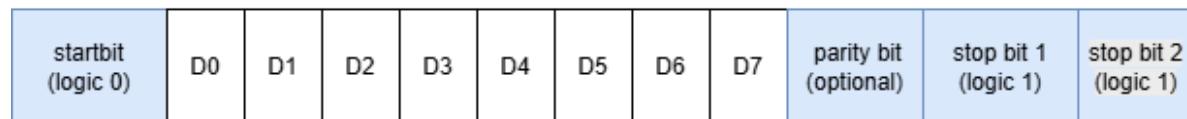
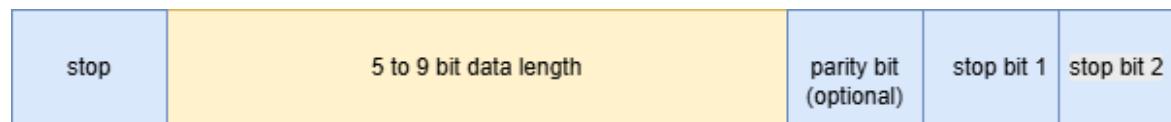
TEAM MEMBERS:

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Objective

To design and implement a UART system using Verilog that includes a baud rate generator, framing logic, and parity-based error detection, and to verify its operation using various test cases to ensure proper timing between transmitter and receiver.

UART frame format



- Start bit is 0
 - Informs receiver new frame is starting
- Data bits
 - 8bits(can be 5-9 bits)
 - LSB will be transmitted first
- Parity bit
 - 1 or 0 based on parity type
- Stop bit 1 is 1
- Stop bit 2 is 1
 - Indicate end of frame

1.Baud rate

The number of bits transmitted/received per second.

Its calculated by

$\text{Clk_cycles_tx} = \text{system clock frequency}$

Baud rate

$\text{Clk_cycles_tx} \rightarrow$ number of clock cycles for transmitting a bit

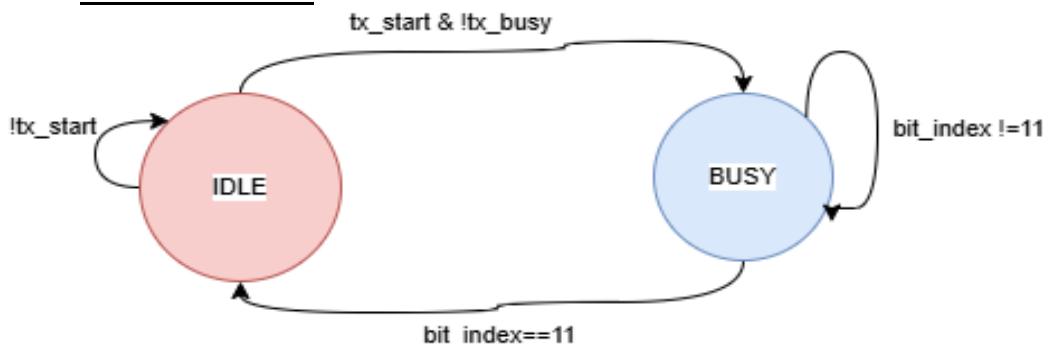
$\text{Clk_cycles_rx} = \text{system clock frequency}$

Baud rate $\times 16$

$\text{Clk_cycles_rx} \rightarrow$ number of clock cycles per oversampling tick

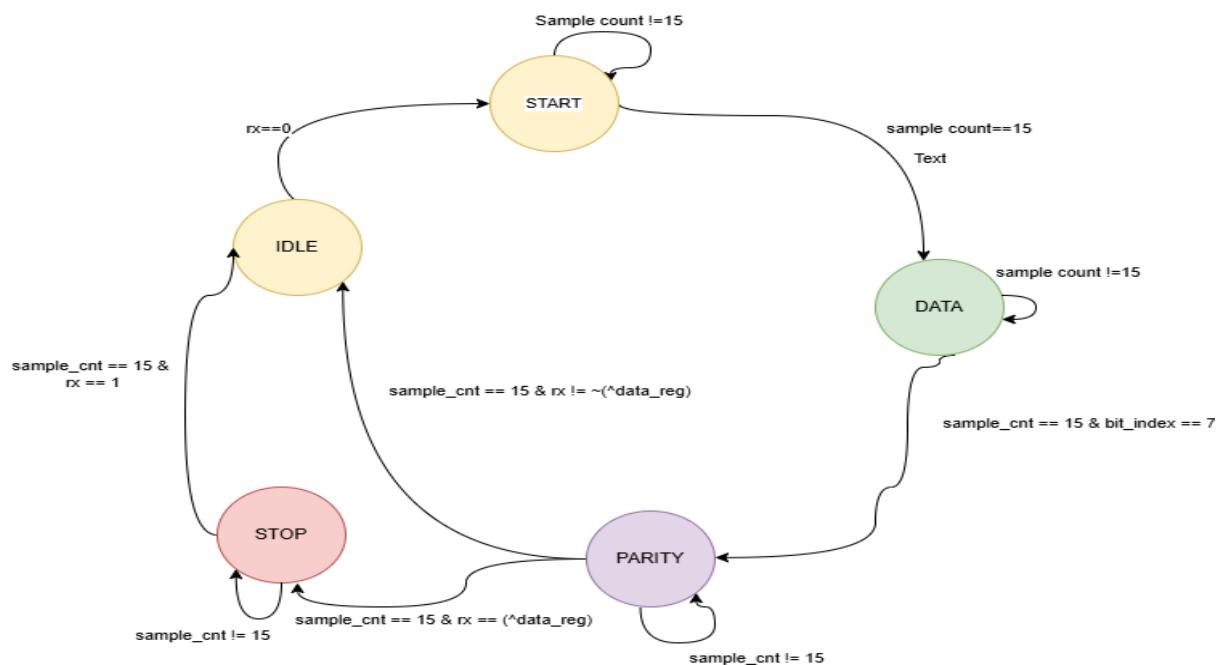
Generally, system clock frequency is **50MHZ** and baud rate is **9600**

2.UART Transmitter



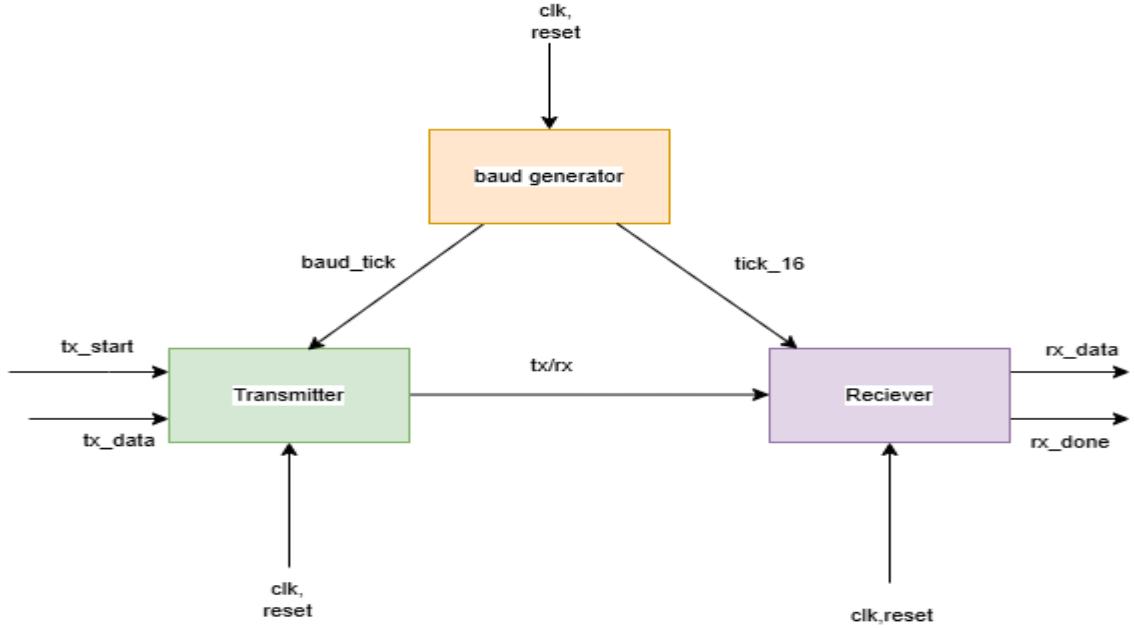
- tx_start → starts transmission
- tx_data → input parallel data
- tx_busy → indicates transmission is in progress
- tx → serial output line from transmitter

3.UART Receiver



- rx → serial input line of receiver
- rx_data → received data
- rx_done → indicates a frame of data is received

Block diagram of UART



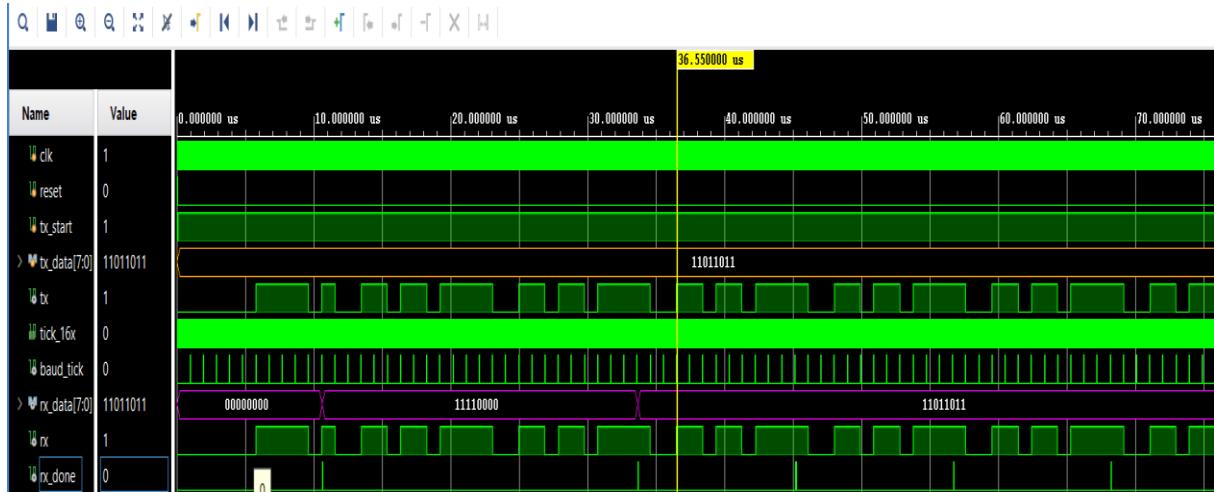
TEST CASES

1. continuous transmission

Applied signals

`tx_data=8'b1111000`

`tx_data=8'b11011011(2nd data byte)`



2. Error detection (parity based)

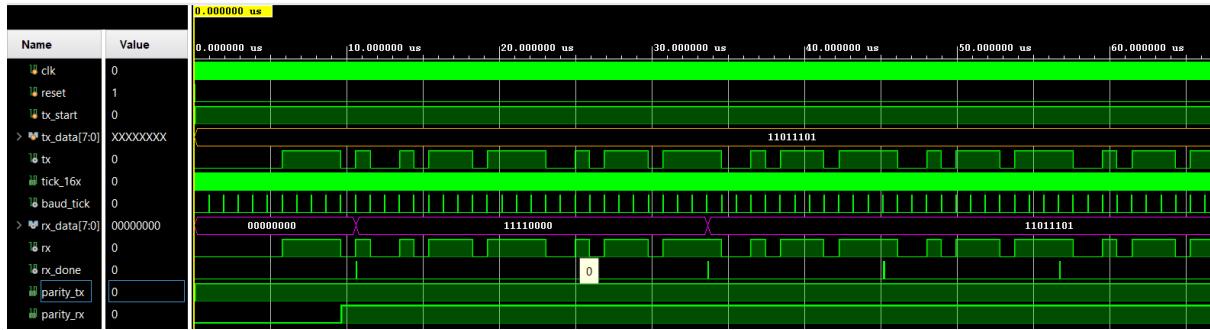
odd parity = $\sim(\text{^data_reg})$

1st data byte is 11110000

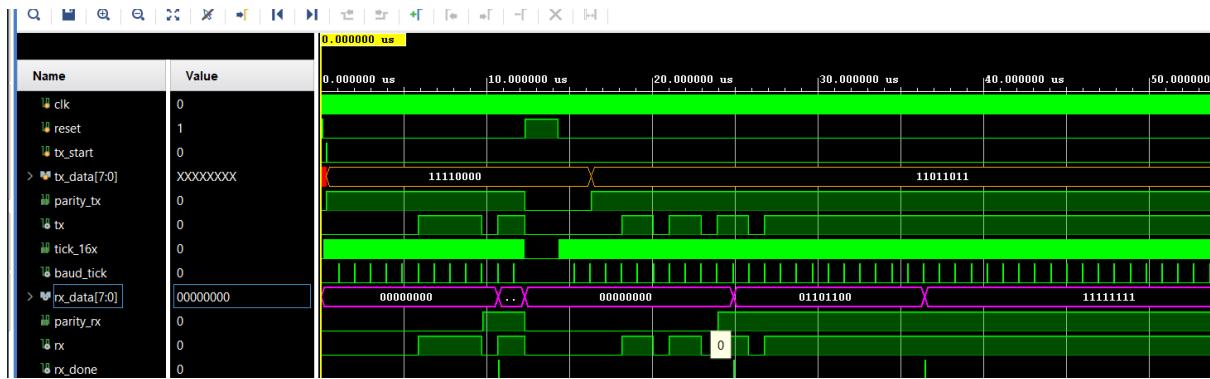
Parity=1

2nd data byte is 11011101

Parity=1



3. Reset applied between 2 frames



Because reset is asserted in between the transmission, the receiver could not detect the start bit ,therefore received incorrect data.

- **Conclusion**

UART is designed using Verilog .It supports serial data communication,tested by different test cases such as parity check,reset in between transmission and transmission of two consecutive data frames and it operates correctly in all these conditions.

Future scope:

Design can be enhanced by adding FIFO and adding test case such as variable data length ranging 5 to 9 bits.