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Development of a thermal resistance model for chip-on-board packaging of high power LED arrays

Minseok Ha, Samuel Graham *

Georgia Tech, Mechanical Engineering, 771 Ferst Dr., Atlanta, GA 30332, United States

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ABSTRACT

The performance of high power LEDs strongly depends on the junction temperature. Operating at high junction temperature causes degradation of light intensity and lifetime. Therefore, proper thermal management is critical for LED packaging. While the design of the heat sink is a major contributor to lowering the overall thermal resistance of the packaged luminaire, another area of concern arises from the need to address the large heat fluxes that exist beneath the die. In this study we conduct a thermal analysis of high power LED packages implementing chip-on-board (COB) architecture combined with power electronic substrate focusing on heat spreading effect. An analytical thermal resistance model is presented for the LED array and validated by comparing it with finite element analysis (FEA) results. By using the analytical expression of thermal resistance, it is possible to understand the impact of design parameters (e.g., material properties, LED spacing, substrate thickness, etc.) on the package thermal resistance, bypassing the need for detailed computational simulations using FEA.

1. Introduction

LEDs are being developed as the next generation solid state lighting source due to their high efficiency and long lifetime, with a potential to save $15 billion per year in energy cost by 2020 [1]. Since the total luminous flux generated by a single LED is considerably lower than other light sources, to be competitive the total light output must be increased with higher forward currents and packages which employ multiple LEDs. However, both of these solutions can result in an increase the junction temperature, which degrades the performance of the LED. In general, as the operating temperature of LEDs increase, the light intensity decreases, the lifetime is reduced, and the output wavelengths can shift. Thus, the ability to thermally manage and control the junction temperature of LEDs has become paramount in the overall development of high power and high efficiency LED solid sate light sources.

There are three major parameters that impact the junction temperature of a LED which are the input power, thermal resistance between the die and the thermal reservoir, and the temperature of the thermal reservoir (e.g., ambient temperature). Typically, the power input to the die and the temperature of the thermal reservoir are not controlled by the thermal management scheme implemented in the packaging of the LED based luminaire. Rather, these are controlled more by the maximum rating of the die and the intended application environment of the luminaire. On the other hand, the thermal resistance which exists between the junction and the thermal reservoir are in part, thermal design parameters which can be optimized to minimize the junction temperature for a given application. Major components of the thermal resistance between the junction and thermal reservoir (e.g., the ambient) are shown in Fig. 1b. While the design of the heat sink is a major contributor to lowering the overall thermal resistance of the packaged luminaire, another area of concern arises from the need to address the large heat fluxes which exist beneath the die since LED package has limited path of heat dissipation (see Fig. 1). Typical heat fluxes of high power LED chips can range from 100 to 500 W/cm^2 provides a challenge for passive thermal management strategies. While the overall power output of a single die is low (e.g., <5 W), the large heat fluxes must be appropriately addressed by thermal spreading in the substrate to effectively limit the junction temperature rise.

At present commercially available surface mount LEDs typically provide a junction to package thermal resistance for single or multi-chip module LEDs [2–4]. While this allows for some thermal design of solid state lighting sources, little is broadly understood concerning the details of the heat transfer process within the package and techniques which can be used to address heat spreading, especially in high power LED arrays chip LED arrays [5–9]. It is possible to address the spreading requirements of high powered LED die through the use of power electronic substrates for efficient heat dissipation, especially when the die are directly mounted to the power substrate in a chip-on-board (COB) architecture. However, the thermal design process utilizing COB architectures on power electronic substrates relies heavily on the use of finite element analysis which requires time consuming calculations when

* Corresponding author.
E-mail address: sgraham@gatech.edu (S. Graham).

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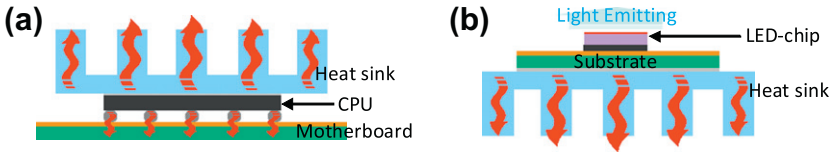

Fig. 1. Schematic of thermal path of (a) general power electronics and (b) LED package.

exploring the parametric design space. This is necessary due to the lack of analytical models which can account for the complex nature of the heat flow through a multilayer power electronic substrate and through the heat sink to the ambient temperature reservoir. Additional complications come into play when moving from a single LED heat source to an array of LEDs where thermal cross talk may impact the overall temperature rise in the array. Thus, a need exists to develop tools which can account for details of the heat dissipation process in COB LED arrays in order to allow for faster design and optimization of high power LED luminaires.

In this study, high power LED-chips (>1 W/die) implementing COB architectures were designed and analyzed using both FEA and a new analytical solution. Substrates for these packaging configurations include two types of power electronic substrates; insulated-metal-substrates (IMS) and direct-bonded-copper (DBC). To understand impact of these substrates on operating temperature, the thermal impedance of the dielectric layer as well as the heat spreading in the copper circuit, dielectric layer, and bottom metal substrate layers were studied. In the analysis of the COB architectures, several lead free solders and thermal interface materials were considered as die attach materials. The analysis starts with a single-chip LED package and is extended to address multi-chip arrays on power substrates. The power substrates were attached to a fixed heat sink design as the optimization of the heat sink was not considered at this time. However, without loss of generality, the model which was developed can account for the contributions of the heat sink to the overall thermal resistance.

2. Modeling of LED packages

2.1. Single chip LED package

The basic model used to analyze the COB architecture is shown in Fig. 2. Since developing an analytical model for multi-chip LED arrays is very complicated, attempts were first made to develop a solution for single chip packages and extend the result to the arrays. A comparison between full three dimensional FEA and analytical modeling results were made to show the utility of this approach. The LED-chip under consideration in this model is made in a vertical thin film (VTF) structure, and attached to a Si die using Au–Si eutectic bonding. Due to the very thin thickness of these layers, their contribution to the overall thermal resistance was much negligible based on FEA results. Thus, to simplify the model, we replaced the LED chip and Au–Sn eutectic bonding with a uniform heat flux boundary condition on top of the Si die as shown in Fig. 4. The Si die was attached to the power electronic substrate, DBC or IMS, with interface materials having the properties of lead-free solders (In, Au–20Sn, or Sn–3.5Ag). Finally, the packaged LED was attached to a heat sink using thermal grease as the thermal interface material. Although the contact resistance should be considered for the TIM and the die-attach resistance, it is neglected because of difficulties in finding solutions. The materials, dimensions, and thermal conductivities of materials are summarized in Table 1.

We assumed that materials are homogeneous and isotropic, and their thermal conductivities are independent of temperature. The heat sink design used is based on a commercially available heat sink with natural convection boundary conditions (see Figs. 3 and 4). All surfaces around the die and substrate are adiabatic except the top of the Si die. This assumption is reasonable because most of the heat generated in LEDs is dissipated by conduction through the back side of the LED through the heat sink (>90%). The heat dissipation by convection around the die and substrate is negligible because of the very small surface areas involved and the large resistance presented by natural convection heat transfer coefficients. For the heat sink, a uniform convective heat transfer coefficient, $h = 10\ \mathrm{W/m^2\,K}$, at 25 °C ambient temperature was assumed.

Before developing the analytical expression for the thermal resistance model, the system in Fig. 5 was divided into several components for the simplification of the problem. This was achieved by dividing the system into three components; the Si die and die-attach, power electronic substrate and TIM, and the heat sink.

For the boundary condition between Si die and substrate, a uniform heat flux was assumed to exist. The heat flux between Si die and substrate are plotted based on FEA simulations and shown in Fig. 6. Although there is some deviation from spatial uniformity of the heat flux under the die, it is not significant except at the very edge. For the boundary condition between TIM and heat sink, two different assumptions were also used with respect to the components. For the substrate and TIM-component, a uniform temperature at the bottom of the component was assumed to allow for the calculation of the component thermal resistance. FEA results

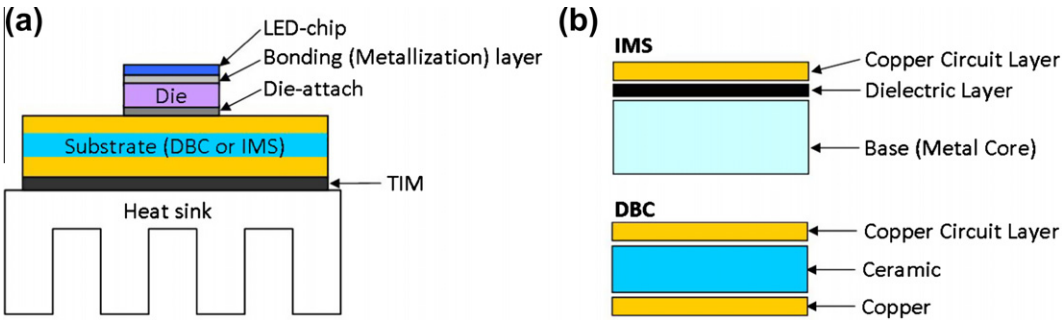

Fig. 2. (a) The structure of the simplified LED package and (b) the structures of IMS and DBC substrate.

Table 1
Structural dimensions and properties of materials analyzed 25 °C [7,10].

	Thickness (μm)	Size	Materials		Thermal conductivity (W/m^2 K)
LED-chip	4	1 mm × 1 mm	GaN		130
Metallization	10	1 mm × 1 mm	Au–Si eutectic bonding		27
Si die/submount	375	1 mm × 1 mm	Si		124
Die-attach	50	1 mm × 1 mm	Lead	100In	82
			Free	Au–20Sn	57
			Solder	Sn–3.5Ag	33
Substrate	–	1 cm × 1 cm	Copper		385
			DBC	AlN	180
				Al_2O_3	30
			IMS	Dielectric	1.1
				Al	150
TIM	50	1 cm × 1 cm	Thermal grease		3
Heat sink	–	–	Al		150

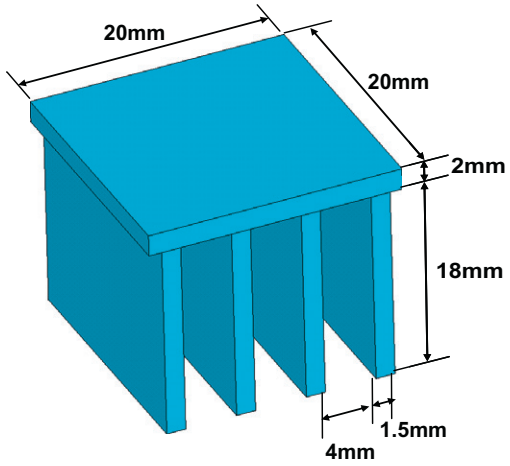

Fig. 3. The structure and dimensions of the heat sink.

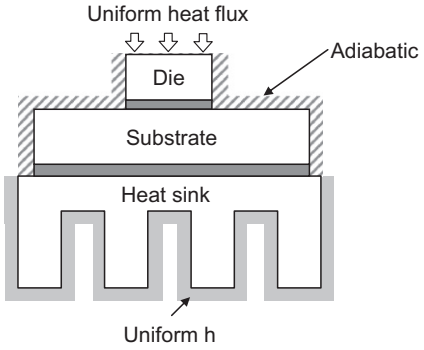

Fig. 4. Boundary conditions used in this study; uniform heat flux on top of the die, uniform convection heat transfer coefficient around heat sink, and all other surfaces adiabatic.

show that the temperature distribution at the bottom of TIM varies less than 1 °C making this assumption satisfactory. When calculating thermal resistance of heat sink, however, using a uniform heat flux with a specific heat conducting area which can be determined by a heat spreading characteristics was found to be a better assumption.

2.2. Analytical expressions of thermal resistance

To develop analytical expressions for the component thermal resistances described above, the heat flux on the top of the Si die is assumed to be uniform and heat flux area does not change as it moves through the Si die and die-attach. Therefore, the thermal resistance of die and die-attach can be expressed using one-dimensional thermal resistance model for heat diffusion;

$$R_{Die} = \frac{t_{Die}}{k_{Die}A_{Die}} \tag{1}$$

$$R_{Die\text{-}attach} = \frac{t_{Die\text{-}attach}}{k_{Die\text{-}attach}A_{Die\text{-}attach}} \tag{2}$$

where t is the thickness, k is the thermal conductivity, and A is the size of the heat flux area (see Fig. 7).

To estimate thermal resistance of the power electronic substrate, a three-dimensional heat equation was solved to account for the heat spreading effect. Power electronic substrate such as DBC substrate and IMS consists of three layers. While it is possible to solve the boundary value problem for each layer, the problem becomes more tractable by solving for the heat transfer through the three layer power electronic substrate plus the thermal interface material while assuming a uniform temperature on the bottom side of the thermal interface material.

The single layer solution in cylindrical system was derived first by Kennedy [11]. Although the solutions with different geometry and boundary conditions have been derived so far, there are not many solutions for multi-layer heat spreading problem. The only analytical solution for four-layer structure was derived by Palisoc and Lee [12,13]. However, the solution is very complex and requires large amount of calculation that is not suitable for parametric study. Also, since it is solved for an infinite plate problem, the solution does not account for the effect of a finite substrate size. Yovanovich et al. calculated thermal resistance of various geometries and various boundary conditions [14–20]. However, their analytical solutions are applicable only up to two layers. They used the effective thermal conductivity for more than two layers. It gives overall tendency of thermal resistance of multi-layer structure with various boundary conditions, but shows large errors in some cases. Masana [21–23] calculated thermal resistance using spreading angle, based on analytical analysis and this solution is simple and gives quite accurate result. Also it is possible to solve with strip heat source and eccentric heat source, and is not restricted by the number of layers. Although this method is reliable in most cases, it gives large errors if a layer with very small thermal conductivity exists among the multi-layers. If we have simple analytical solution for four-layer problem, we can analyze the system more precisely. Therefore, exact analytical solution of a four-layer problem was derived and compared with other solutions. We solved the multi-layer structure with circular disks instead of rectangular disks because the problem is simplified into

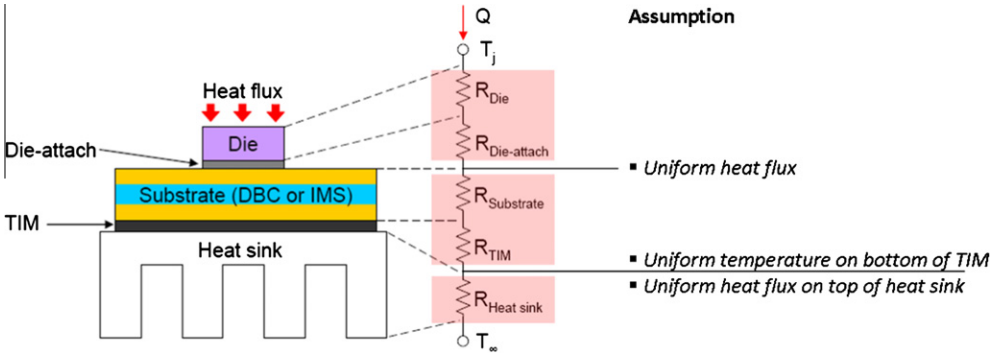

Fig. 5. Thermal circuit for LED package and assumptions when dividing into components.

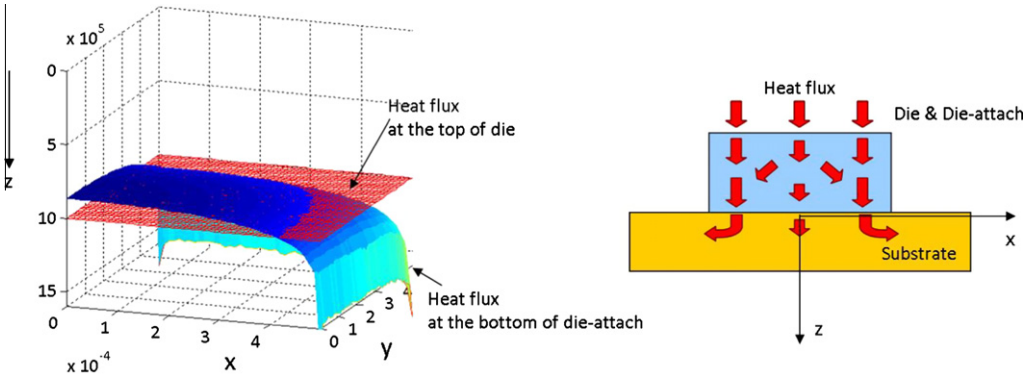

Fig. 6. Heat flux at the top of die and at the bottom of die-attach. Due to heat spreading in substrate, heat flux at the edge is large.

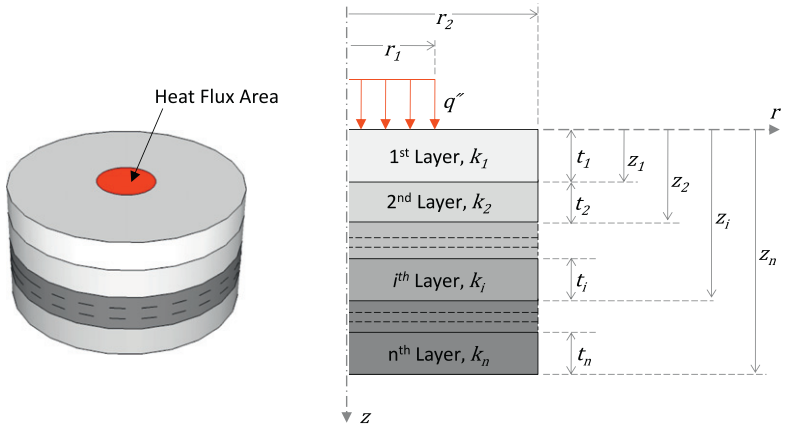

Fig. 7. The schematic of multi-layer circular disk.

two-dimensional problem due to circular symmetry. The expression for this thermal resistance is given in the following equation:

$$R_{multi\text{-}layer} = \frac{1}{\pi r_2^2}\left(\sum_{i=1}^{n}\frac{t_i}{k_i}\right) + \frac{2}{k_1\pi r_1}\sum_{l=1}^{\infty}\frac{J_1\left(\frac{r_1}{r_2}\alpha_l\right)}{\alpha_l^2 J_0^2(\alpha_l)}\varphi_n \tag{3}$$

where α_l is the roots of the zero-order Bessel function, $J_0(x)$; the summation is conducted over ascending values of α_l, which is approximated using Stokes approximation [18–24]. A modified Stokes approximation is

$$\alpha_l = \frac{\beta_l}{4}\left(1 - \frac{6}{\beta_l^2} + \frac{6}{\beta_l^4} - \frac{4716}{5\beta_l^4} + \frac{3902,418}{70\beta_l^4}\right) \tag{4}$$

where $\beta_l = \pi(4l+1)$ and $l \geqslant 1$. φ_n is determined by total number of layers, n, and in case of four-layer it can be calculated using following relationship:

$$\varphi_4 = \frac{\left[\begin{array}{c}\frac{\tanh(t_1\lambda_l)}{k_1}+\frac{\tanh(t_2\lambda_l)}{k_2}+\frac{\tanh(t_3\lambda_l)}{k_3}+\frac{\tanh(t_4\lambda_l)}{k_4}\\ +\frac{k_2}{k_1k_3}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)+\frac{k_2}{k_1k_4}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_4\lambda_l)\\ +\frac{k_3}{k_1k_4}\tanh(t_1\lambda_l)\tanh(t_3\lambda_l)\tanh(t_3\lambda_l)+\frac{k_3}{k_2k_4}\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)\tanh(t_4\lambda_l)\end{array}\right]}{\left[\begin{array}{c}\frac{1}{k_1}+\frac{\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)}{k_2}+\frac{\tanh(t_1\lambda_l)\tanh(t_3\lambda_l)}{k_3}+\frac{\tanh(t_1\lambda_l)\tanh(t_4\lambda_l)}{k_4}\\ +\frac{k_2}{k_1k_3}\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)+\frac{k_2}{k_1k_4}\tanh(t_2\lambda_l)\tanh(t_4\lambda_l)+\frac{k_3}{k_1k_4}\tanh(t_3\lambda_l)\tanh(t_4\lambda_l)\\ +\frac{k_3}{k_2k_4}\tanh(t_1\lambda_l)\tanh(t_2\lambda_l)\tanh(t_3\lambda_l)\tanh(t_4\lambda_l)\end{array}\right]} \tag{5}$$

where $\lambda_l = \alpha_l / r_2$. When calculating the thermal resistance, we used the maximum temperature of the top surface at the center, rather than the average temperature of heat flux area.

The thermal resistance of the heat sink can be easily estimated by using the result of the FEA for the single chip model. This is because the thermal resistance of the heat sink of a fixed geometry with a concentrated heat source does not change greatly with the variable parameters found in the other components (i.e., Si die and thermal interface as well as the substrate and thermal interface components). Thus, the thermal resistance of the heat sink was calculated using FEA analysis for the single chip chases. An analytical model, which accounts for heat sink thermal resistance and heat spreading at the top of the heat sink, however, is necessary for characterizing multichip LED modules.

For the multichip LED array, a $N \times N$ LED-array based using a COB structure was used to develop the thermal circuit model (see Fig. 8). The power input q was assumed the same the same for all LEDs. The thermal resistance of the total system can be estimated by using in the following equation:

$$R_{tot} = R_{Die} + R_{Die\text{-}attach} + [R_{Substrate} + R_{TIM}] + N \times R_{Heatsink} \tag{6}$$

where R_{Die} and $R_{Die\text{-}attach}$ can be calculated using the expressions used for a single chip-LED package (Eqs. (1) and (2)). $[R_{Substraet} + R_{TIM}]$ can be calculated using Eq. (3) with $n = 4$. To determine r_2, that is the radius of the substrate, the mid-surface between the LEDs can be assumed adiabatic (see Fig. 9). Therefore, if the array is arranged with uniform distance, r_2 can be determined by in the following equation:

$$r_2 = \frac{\text{Pitch}}{\sqrt{\pi}} \tag{7}$$

The last term in Eq. (6), $N \times R_{Heatsink}$, must account for the thermal spreading resistance affected by the placement of LEDs. The thermal resistance of the heat sink including thermal spreading resistance can be calculated by Muzychka's solution [16] (see Fig. 10).

The solution for the temperature distribution on the heat sink can be obtained using superposition. For N discrete heat sources, the surface temperature distribution is given by

$$T(x,y,0) - T_f = \sum_{i=1}^{N} \theta_i(x,y,0) \tag{8}$$

where

$$\theta_i(x,y,0) = A_0^i + \sum_{m=1}^{\infty} A_m^i \cos(\lambda x) + \sum_{n=1}^{\infty} A_n^i \cos(\delta y) + \sum_{m=1}^{\infty}\sum_{n=1}^{\infty} A_{mn}^i \times \cos(\lambda x)\cos(\delta y) \tag{9}$$

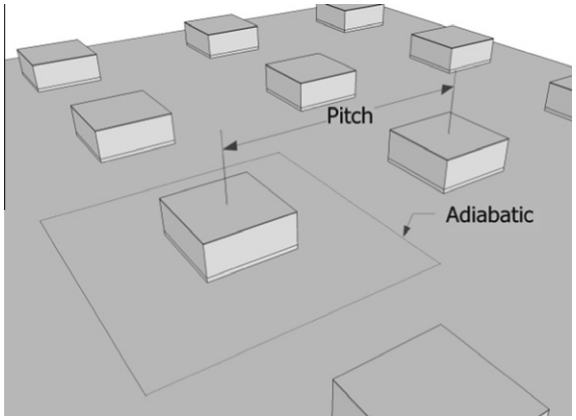

Fig. 9. The schematic of the array of multiple LEDs. LEDs are placed evenly in the substrate and the distance between the adjacent LEDs is defined as pitch.

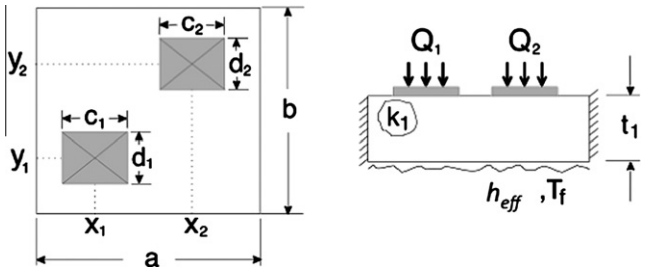

Fig. 10. Isotropic plate with eccentric heat source [16].

$$A_m^i = \frac{2Q_i\left[\sin\left(\frac{(2x_i+c_i)}{2}\lambda_m\right) - \sin\left(\frac{(2x_i-c_i)}{2}\lambda_m\right)\right]}{abc_i k_1 \lambda_m^2 \phi(\lambda_m)} \tag{10}$$

$$A_n^i = \frac{2Q_i\left[\sin\left(\frac{(2y_i+d_i)}{2}\delta_n\right) - \sin\left(\frac{(2y_i-d_i)}{2}\delta_n\right)\right]}{abd_i k_1 \delta_n^2 \phi(\delta_n)} \tag{11}$$

$$A_{mn}^i = \frac{16Q_i \cos(\lambda_m x_i)\sin\left(\frac{1}{2}\lambda_n c_i\right)\cos(\delta_n y_i)\sin\left(\frac{1}{2}\delta_n d_i\right)}{abc_i d_i k_1 \beta_{m,n} \lambda_m \delta_n \phi(\beta_{m,n})} \tag{12}$$

and $\lambda = \frac{m\pi}{a}, \delta = \frac{n\pi}{b}, \beta = \sqrt{\lambda^2 + \delta^2}, \phi(\zeta) = \frac{\zeta \sinh(\zeta t_1) + h_{eff}/k_1 \cosh(\zeta t_1)}{\zeta \cosh(\zeta t_1) + h_{eff}/k_1 \sinh(\zeta t_1)}$ and ζ is replaced by λ, δ, and β. Since our concern is the maximum junction temperature of the system, if we put the location of x, y as the center of the innermost LED in the array, the maximum $N \times R_{Heatsink}$ can be obtained by

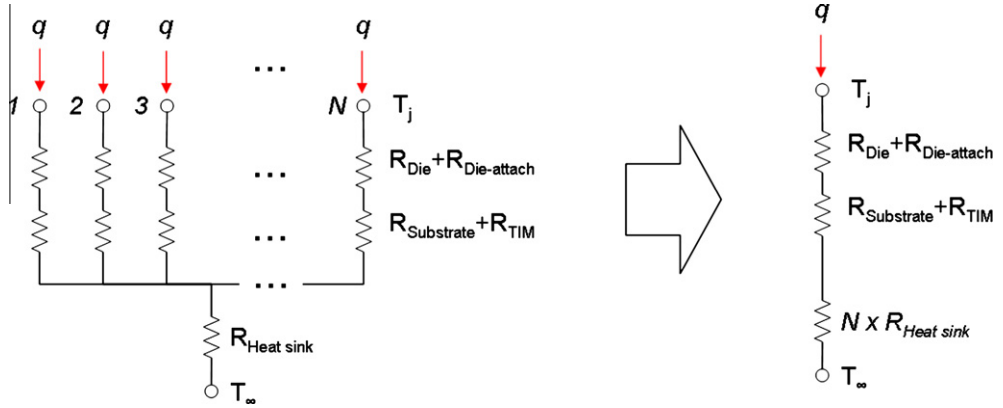

Fig. 8. The equivalent thermal resistance model of LED array. If the power used and structure is the same, it can be simplified as the right side.

$$N \times R_{Heatsink} = \frac{T(x,y,0)}{\sum_{i=1}^{N} Q_i} \quad (13)$$

2.3. Results and discussions for single chip LED package

Fig. 11 displays the FEA temperature result from the analysis of a single chip LED dissipating 1 W on a 375 μm thick Si die, 50 μm of Au–20Sn solder, a Cu–AlN–Cu DBC substrate, and 50 μm of thermal grease attached to the heat sink from Fig. 2. Only a quarter of the geometry was modeled due to the two fold symmetry of the problem. In addition to the DBC substrate, and IMS substrate with 127 μm (Cu)/75 μm (dielectric)/1000 μm (Al base) was also investigated to compare its thermal performance. Since the heat spreading within the power electronic substrate is critical to lowering thermal resistance, a parametric study which included changes in dielectric material properties as well as copper circuit layer thickness and size was investigated. These results are presented in Figs. 12 and 13.

Thermal resistance of die and die-attach calculated using Eqs. (1) and (2) are compared with thermal resistance estimated using FEA analysis (see Fig. 12). Overall, very good agreement is seen between the simple model and the FEA analysis. The linear increase in thermal resistance with die thickness is expected and the reduction in thermal resistance when comparing a Si to SiC die is also observed. The die attach material has a low thermal conductivity compared to both die materials; however, thermal resistance is not significant because it is much thinner than the die. With the typical thickness of the die attach being 50 μm, the difference of thermal resistance between Au–20Sn (57 W/mK) and using 100In (82 W/mK) was found to be less than 0.7 °C/W.

The heat spreading effect is observed in the power electronic substrate when considering the copper circuit layer, dielectric layer, and metal substrate. Due to the heat spreading effect, the thickness of copper in the copper circuit layer and its lateral dimensions are very important to reduce the thermal resistance. As shown in Fig. 13, as the copper circuit layer thickness increases, the thermal resistance of an IMS substrate when compared to a DBC using AlN or Al_2O_3 decreases substantially. This is a result of the ability of the copper circuit layer to reduce the local heat flux which reduces the temperature drop across the subsequent dielectric layer. This effect is also seen when varying the lateral size of the copper circuit layer with a fixed die size of 1 mm × 1 mm. For a fixed DBC thickness of 127 μm (Cu)/381 μm (ceramic)/127 μm (Cu) and IMS thickness of 127 μm (Cu)/75 μm (dielectric)/1000 μm (Al base), as the lateral size reaches a factor of 10 greater than the die size, the thermal resistance between the 3 substrate types begins to diminish. Thus, the results show that the copper circuit layer thickness design is critical in the control of the package thermal resistance (see Fig. 14).

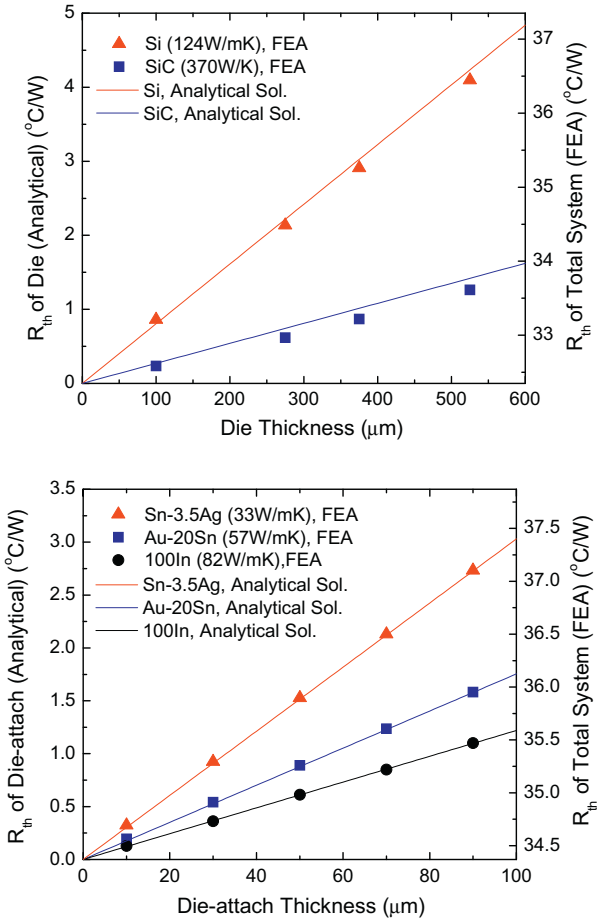

Fig. 12. Validation of thermal circuit model of die and die-attach. The relative changes with respect to the thickness are compared (left and right *y*-axis has the same scale). The simulation conditions shown in Fig. 11 were used, and only thickness of die and die-attach were changed.

The thermal resistance of LED-array as a function of pitch was estimated by the analytical method and compared with the FEA result (see Fig. 15). The results obtained by the two different meth-

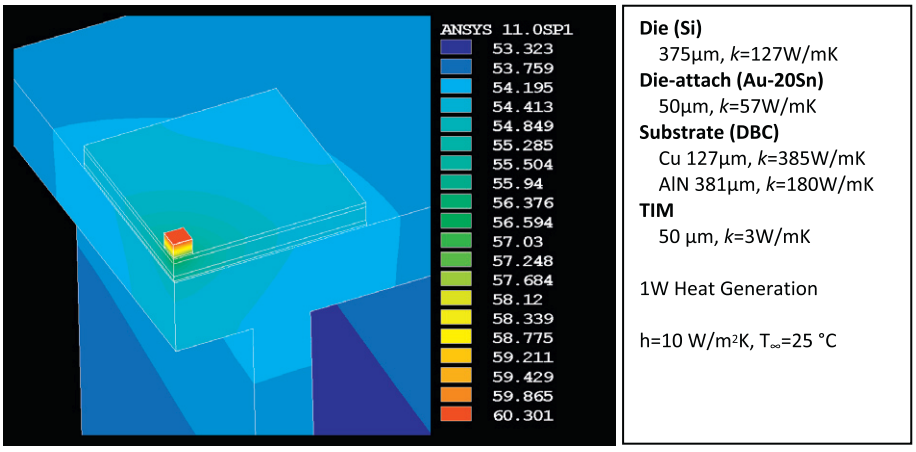

Fig. 11. The contour plot of temperature distribution in LED package. The simulation conditions are shown in the right.

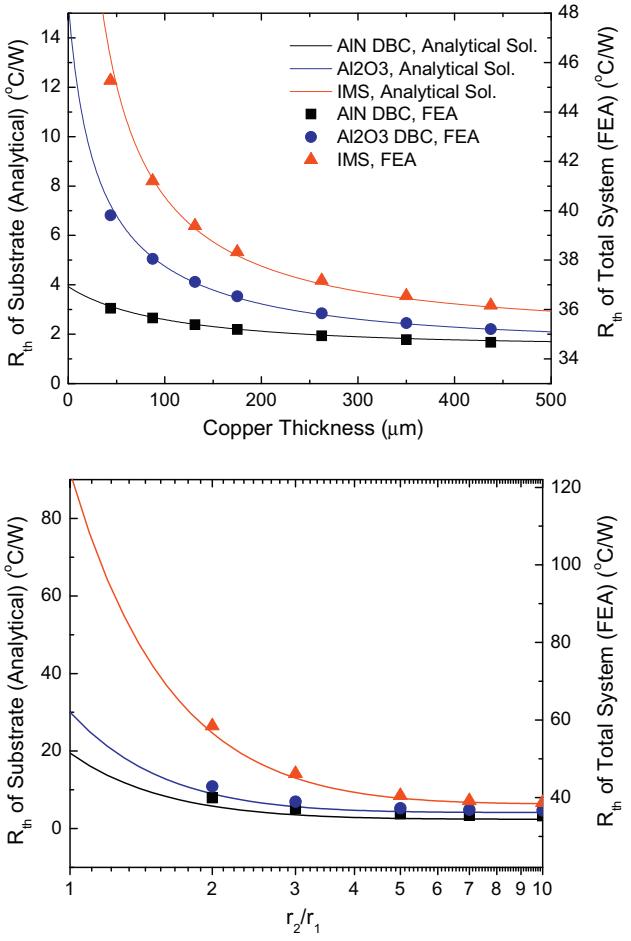

Fig. 13. The validation of thermal resistance model. 1 mm^2 heat source is placed at the center of substrate. Fixed substrate size, 1 cm^2, used for the first plot and fixed copper thickness, 127 μm, for the second plot. Three different substrates are used; AlN DBC, Al_2O_3 DBC, and IMS. 381 μm of ceramic was used for DBC, and 75 μm of dielectric and 1000 μm of base for IMS. 50 μm of thermal grease (3 W/m^2 K) is used for TIM. Uniform heat flux at top surface and uniform temperature at bottom surface were assumed. Left and right *y*-axis has the same scale.

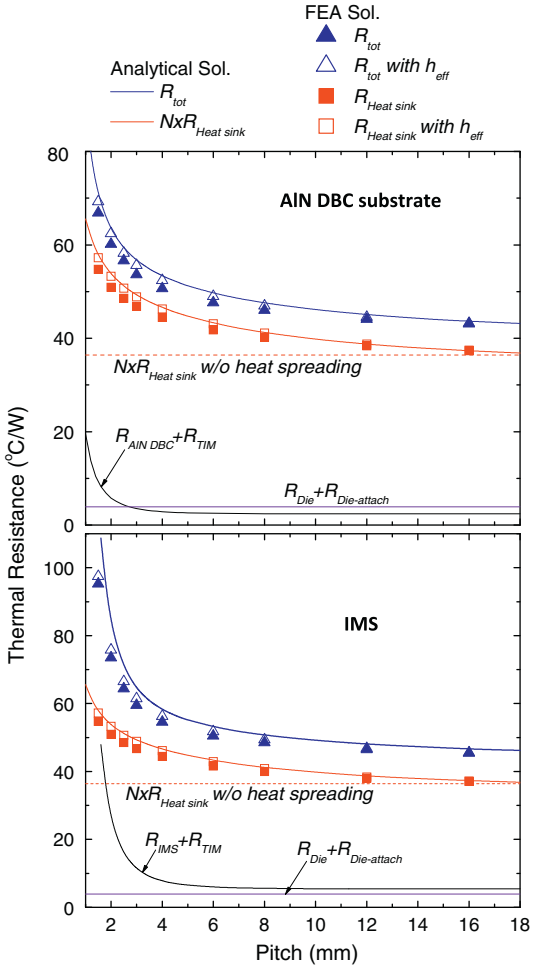

Fig. 15. The thermal resistance of LED-array as a function of pitch. Lines are analytical results and symbols are FEA results. The conditions shown in Fig. 11 were used for the LED-array with AlN DBC substrate. 127 μm copper, 50 μm and 1.1 W/mK dielectric, and 1 mm Al base is used for IMS.

ods agree well. The total thermal resistance of the system is the sum of the three components. The violet solid line is the thermal resistance of the die and die-attach. Since its geometry and thermal conductivity does not change, it remains constant as 3.9 °C/W. The black solid line is the thermal resistance of the substrate. When the pitch is small, the thermal resistance of the substrate is large because the heat does not spread enough. Once the pitch is larger than a certain distance, the restriction of the heat spreading in substrate becomes negligible. Approximately, it is 6 mm for a 127 μm (Cu)/381 μm (ceramic)/127 μm (Cu) DBC substrate and 9 mm for 127 μm (Cu)/75 μm (dielectric)/1000 μm (Al base) IMS achieving less than 5% difference compared to the infinite pitch. From this

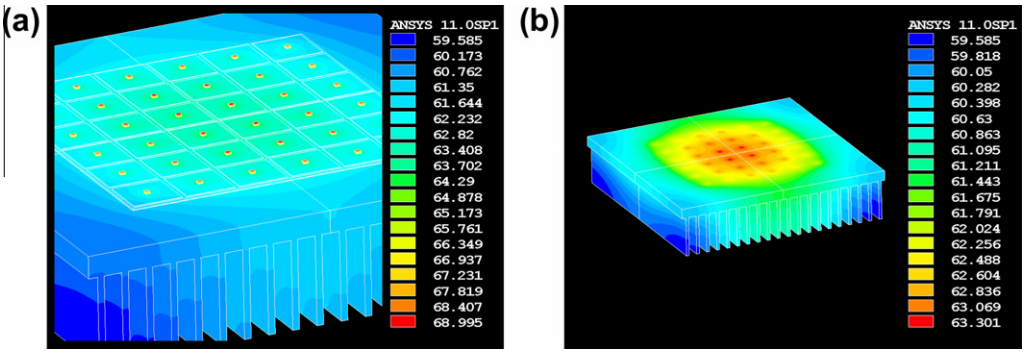

Fig. 14. The contour plot of temperature distribution by FEA. (a) Entire structure and (b) only heat sink. The 6 by 6 LED array based on COB structure was modeled. The condition shown in Fig. 11 is used except the substrate size and the heat sink size. The substrate size is 72 smm × 72 mm, and the distance between two adjacent LEDs, pitch, is 12 mm. The base plate of the heat sink is 110 mm × 110 mm with 5 mm thickness, and 20 straight fins have 1.5 mm thickness and 20 mm height. 1 W power input was applied in each LED.

approximation, we assumed that the heat conducting area is 36 mm^2 between DBC package and the heat sink and 81 mm^2 between IMS package and heat sink. The red[1] solid line is the thermal resistance of the heat sink. The square of the pitch is used as heat flux area if it is smaller than typical heat flux area. The red dashed is the thermal resistance of heat sink without thermal spreading resistance, which means the heat flux area is the entire top surface of the heat sink. It is the lowest thermal resistance of the heat sink. The black solid line is the total thermal resistance of the system and it is the sum of the other three solid lines. To calculate the thermal resistance in analytical solution, convection coefficient h (with fin) was converted into equivalent convection coefficient h_{eff} (without fin)

The pitch of the LEDs in the array is an important factor in determining the thermal resistance of LED-array. Although the larger pitch can achieve a lower thermal resistance, the pitch is usually determined by considering other factors such as optics. For effective thermal management of the system, it is best to minimize the interference of heat spreading in the substrate level. This depends on the type of substrate, the thickness of each layer, etc., and typically 6 mm for a DBC substrate and 9 mm for a IMS is the minimum pitch preventing drastic increase of thermal resistance if we use copper circuit layer thicker than 127 μm, which is in the range of concern for the industrial use.

So far, we assumed that the copper circuit layer has the same size with a substrate. Although this assumption is reasonable because practically the etched area of copper circuit layer in power electronic substrate is as small as possible, it is not always acceptable. Further FEM simulations show that the etched area has little effect on the thermal resistance for DBC substrate, however has very large effect for IMS. In case of IMS, the lateral size of copper circuit layer behaves like the lateral size of substrate. Therefore, IMS must have enough large copper circuit area for proper thermal management.

3. Discussion and conclusions

In this study, the thermal resistance of high power LEDs implementing COB architecture was analyzed by FEA and analytical analysis. In the die and die-attach layers, the thermal resistance is very sensitive to the thermal conductivities and the layer thickness because of the very high heat flux transported through them. The die and die-attach can be assumed as one dimensional heat flux structures and their thermal resistances were developed based on one-dimensional thermal resistance for conduction in a plane wall. As die material, Si is a good choice because alternative materials like SiC are extraordinary expensive. Using thin layers of Si could be economical way to reduce thermal resistance of die rather than using SiC. In the case of die-attach layers, the effect of thermal conductivity of the die-attach on the thermal conductivity is not significant. Any void or delimitation could be more critical than the thermal conductivity of the die-attach material. Au–20Sn is mostly used for the die-attach material of high power LEDs because of its excellent wettability, excellent resistance to corrosion, high thermal conductivity, high joint strength, and fluxless process. Also, the CTE matches well with other package material such as Si, ceramics, Copper and Moreover, the excellent wettability makes very thin die-attach possible, from a few microns to 10 μm.

Power electronic substrates can dissipate heat very efficiently compared to a conventional FR4-PCB, and this is because of low thermal impedance of dielectric layer and effective heat spreading in thick copper circuit layer. In the case of a DBC substrate, ceramics are used as the dielectric material, which have very high thermal conductivities; AlN is 180 W/mK and Al_2O_3 is 30 W/mK. In the case of IMS, although the dielectric has very low thermal conductivity, 1–2 W/mK, low thermal impedance can be achieved by using very thin layers. These substrates can take advantage of the use of "heavy copper". By spreading heat in a thick copper circuit layer, effective heat transfer can be achieved. From the analysis, it was found that the most important parameters in substrates are the thickness of the copper circuit layer and the lateral size of the substrate. Thick copper layers can dramatically reduce thermal resistance and at the same time it requires a large substrate area. However, in case of AlN DBC substrates, the impact of copper thickness is negligible. Although AlN DBC substrates show better thermal performance than Al_2O_3 DBC substrate or IMS, it is more expensive than others.

The thermal conductivity and thickness of the TIM are not critical factors in determining the thermal resistance of the package. That is because the heat flux density is reduced after passing through the power substrate to only 2–6% of that of die level due to heat spreading in substrate. Solder can be used to mount the SMT package on the substrate or the board; however it is not suitable for the substrate of COB array because of large contact area. The large contact area may cause non-uniform thickness and voids, which are damaging for reliability and thermal management. The most common is thermal grease, typically silicone grease filled with aluminum oxide, zinc oxide, or boron nitride. Another type is the phase-change materials (PCM). These are solid at room temperature but liquefy and behave like grease at operating temperatures. The main advantage of PCM is that they can achieve low thermal contact resistance at operating temperature while they are easy to handle and are not messy at room temperature.

The thermal resistance of LED-array largely depends on the pitch, which is the distance between two adjacent LED-chips, as well as other parameters that mentioned previously. The design shows that LED-chips placed evenly on the heat sink have the lowest thermal resistance and it increases gradually as the pitch decreases. Although the placement of LED-chip on the substrate depends on other design considerations, the pitch should be larger than the distance which causes significant incensement in the thermal resistance by the interference of heat spreading in the substrate level. The value varies with the type of substrate and the thickness of each layer in the substrate as well as heat source size. The analytical solution derived in this study can provide simple and easy way to find the response with respect to the change of each design parameter.

The optimized thermal design is not always acceptable because the design is restricted by other design considerations, cost and so on. The optimized design should be determined by considering trade-offs with all other factors. The general guideline for the thermal management of LED-array implementing COB technology can be provided by this study. After determining the general design by using analytical solutions, the specific design can be examined by FEA or experimental methods.

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