

## Project #1 Simulation of a PN Junction

Due: Oct. 31, 2017 in class

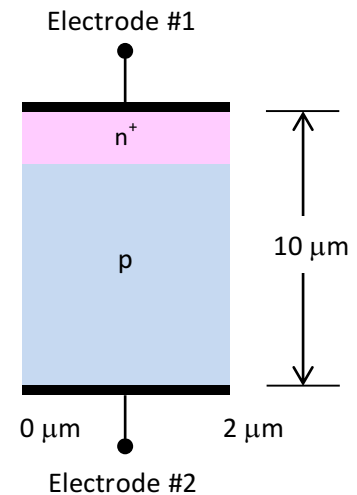
An N<sup>+</sup>P junction is fabricated on a P-type silicon substrate with  $N_a = 8 \times 10^{15} \text{ cm}^{-3}$ . The N<sup>+</sup> region has a concentration of  $N_d = 2 \times 10^{18} \text{ cm}^{-3}$  and a junction depth of  $x_j = 1 \text{ }\mu\text{m}$ . The total device depth is  $10 \text{ }\mu\text{m}$  (from top to bottom contact).

Use Sentaurus to simulate and view the results for the following conditions:

### 1. Zero Bias, Uniform Doping Profiles (10 points)

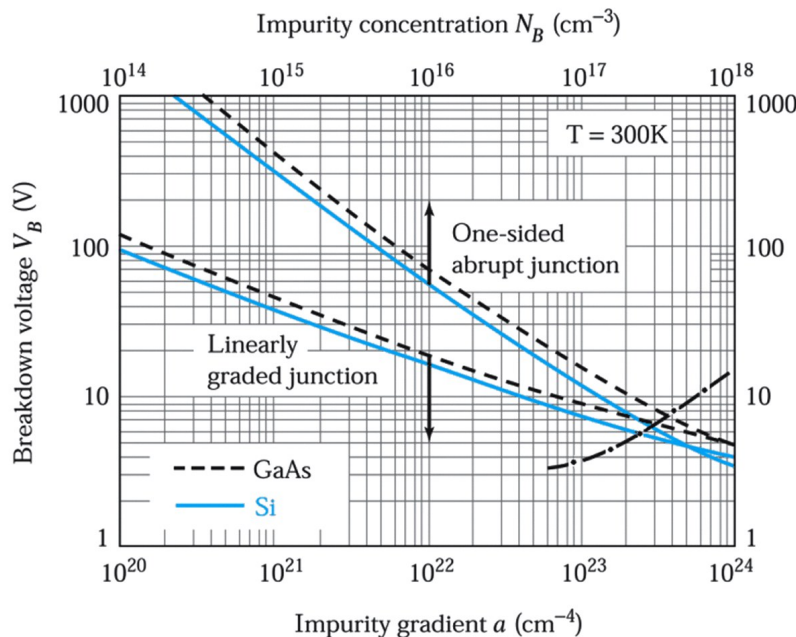
Using uniform doping profiles, verify the 1D and 2D impurity concentrations of the junction. Plot the 1D electrostatic potential across the junction to estimate the built-in potential and depletion region width. Compare the results with the theoretical values. [3+4+3]

You may want to use a non-uniform mesh, which is denser in the top  $2 \text{ }\mu\text{m}$  of the device.



### 2. Reverse Bias, Uniform Doping Profiles (10 points)

Simulate the diode under reverse bias. Plot the reverse IV characteristics and extract the breakdown voltage. Compare your result with the following figure. What is the maximum electric field in the junction just before breakdown? [4+2+2+2]



Source: Sze and Lee, Semiconductor Devices, 3<sup>rd</sup> Ed.

### 3. Forward Bias, Uniform Doping Profiles (8 points)

Plot the IV relation for this diode under a forward bias between 0 and 1 V. Identify and explain what happens as the forward bias is raised above 0.7V.

*Hint: Examine the change in the IV relation with increasing voltage and determine the cause of this change.* [4+4]

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### 4. High Temperature, Uniform Doping Profiles (9 points)

The junction temperature is raised to 600°C. Simulate this junction up to a reverse bias of 10V and a forward bias of 1V. Plot and explain the IV characteristics. **[4+5]**

### 5. Gaussian $n^+$ Doping Profiles (18 points)

Using a Gaussian profile for the  $N^+$  region with peak concentration of  $2 \times 10^{18} \text{ cm}^{-3}$ , peak position of  $y = 0 \text{ } \mu\text{m}$ , junction depth of  $0.5 \text{ } \mu\text{m}$ , the doping concentration at that depth is  $1 \times 10^{18} \text{ cm}^{-3}$ , and a Gauss factor of 0.8, verify the 1D and 2D doping concentration of the junction. Plot the 1D potential across the junction to estimate the built-in potential and depletion width at equilibrium. Compare the built-in potential with the theoretical value. Compare the built-in potential and depletion width to those of the uniformly doped diode (Part 1). Plot the IV relation of the diode between -2V and 1V and compare with that of the uniformly doped diode (Parts 2 and 3). Bonus: Estimate the minority carrier diffusion lengths  $L_n$  and  $L_p$ . **[3+3+3+3+3+3 + (bonus 3)]**

### Sentaurus Files

1. You have to make following changes to take avalanche breakdown into consideration. In sdevice.cmd file change the physics to the following

```
Physics {  
    Temperature=@<temp>@  
    AreaFactor = 1e3 * AreaFactor to convert current into mA  
    EffectiveIntrinsicDensity( Slotboom )  
    Mobility ( DopingDep eHighFieldSaturation hHighFieldSaturation )  
    Recombination(SRH(DopingDep) Auger Avalanche(ElectricField))  
}
```

2. Use the MathSection\_des.cmd and PlotSection\_des.cmd files from folder.

#### Hints:

1. You can start from Project 0 and modify that because the structure (like doping placement, electrodes) is similar.
2. Choose smaller grid point separation for regions close to the junction and then you can gradually increase the spacing as you go towards the surface of the wafer.
3. For the Bonus in Part 5, measure the minority carrier concentration in the N and P regions to calculate  $L_p$  and  $L_n$ . One option is to determine the minority carrier distribution as a function of position under a bias and find  $L_p$  and  $L_n$  from a curve fit.

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### Report Format

The formal report should have details of the design steps taken (such as processes, physical and electrical parameters, etc.). Use tables, and graphs as needed. Your report should include sufficient information for someone else to repeat your design.

- All reports must be typed
- Include a cover page on your reports
- No more than 10 pages excluding the cover page, but including all tables, plots, code, references
- Use 1.5 or double-spacing
- Use 12 pt font
- Label all graphs and tables. Include descriptive captions

**Each team member signs the cover page on the report.** By signing your name, you acknowledge that you: (a) have participated in the project; and (b) have contributed to and are accountable for the report being submitted.

Plagiarism is a serious offence. Academic honesty is very important. Plagiarism, if detected, will be dealt with formally. (<http://academicintegrity.utoronto.ca/>)

### Marking Scheme

Responses to questions: 55 (+ 3 bonus)

*Each of the underlined action items in the project description is assigned a mark as indicated in the brackets.*

Presentation (writing style, grammar, clarity, figures): 15

Formatting: 5

**Total: 75**

Late Penalty: 10 points per day, including weekends.