Sardar Vallabhbhai Patel Institute of Technology, Vasad

Digital Fundamentals

Assignment 5

Combinational and Sequential Circuits

1. Draw the logic diagram of a 2-to-4-line decoder with only NOR gates. Include an enable input.
2. Construct a 16*1 multiplexer with two 8*1 and one 2*1 multiplexers.
3. Implement the following Boolean functions with 8*1 multiplexers.

$$F(A, B, C, D) = \Sigma(0, 3, 5, 6, 8, 9, 14, 15)$$

4. Implement the following Boolean functions with 8*1 multiplexers.

   F (A, B, C) = Σ (0, 2, 6, 7)
5. Discuss D-type edge- triggered flip-flop in detail.
6. Design a counter with the following binary sequence:0,4,2,1,6 and repeat (Use JK flip-flop)
7. Design a counter with the following binary sequence:0,1,3,7,6,4, and repeat.(Use T flip-flop)
8. With neat sketch explain the operation of RS latch.
9. Show the logic diagram of clocked D.
10. With logic diagram and truth table explain the working JK Flip flop. Also obtain its Characteristic equation. How JK flip-flop is the refinement of RS flip-flop?
11. Explain the working of the Master Slave J K flip-flop.
12. Write short notes on
    1. Clocked R-S flip flop
    2. JK Flip flop
    3. D Flip Flop
    4. T Flip Flop