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Assignment : 4

2] What is half adder? What is disadvantage of it over full adder?

⟹ A half adder is an adder which adds two binary digits together resulting in a sum and carry.

- We assign symbole x and y to the two inputs.

x	y	c	s
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

From the truth table,

$S = x'y + xy'$ and $c = xy$

$\therefore S = x \oplus y$

- The disadvantage of half adder is it can only add two 1-bit numbers given as input but do not add the carry obtained from previous addition, while the full adder along with two 1-bit number can also add the carry obtained from previous addition.

3] With necessary sketch explain full adder in detail Also explain a full adder be designed using two half adder and an OR gate.

=> A full adder is a combination ckt. Consisting of three inputs and two outputs.
- Two inputs variables are denoted by x and y, represent the two significant bits to be added.
- The truth table of full adder is given beloow.

Input			Output	
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

From the truth table

$S = x'y'z + x'yz' + xy'z' + xyz$

$= x'(y'z + yz') + x(y'z' + yz)$

$= x'(y \oplus z) + x(yz' + y'z)'$

$= x'(y \oplus z) + x(y \oplus z)'$

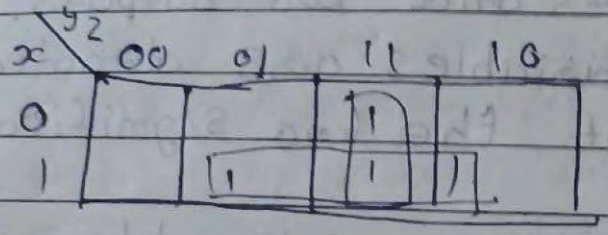
$S = x \oplus y \oplus z$

$C = x'yz + xy'z + xyz) + xyz$

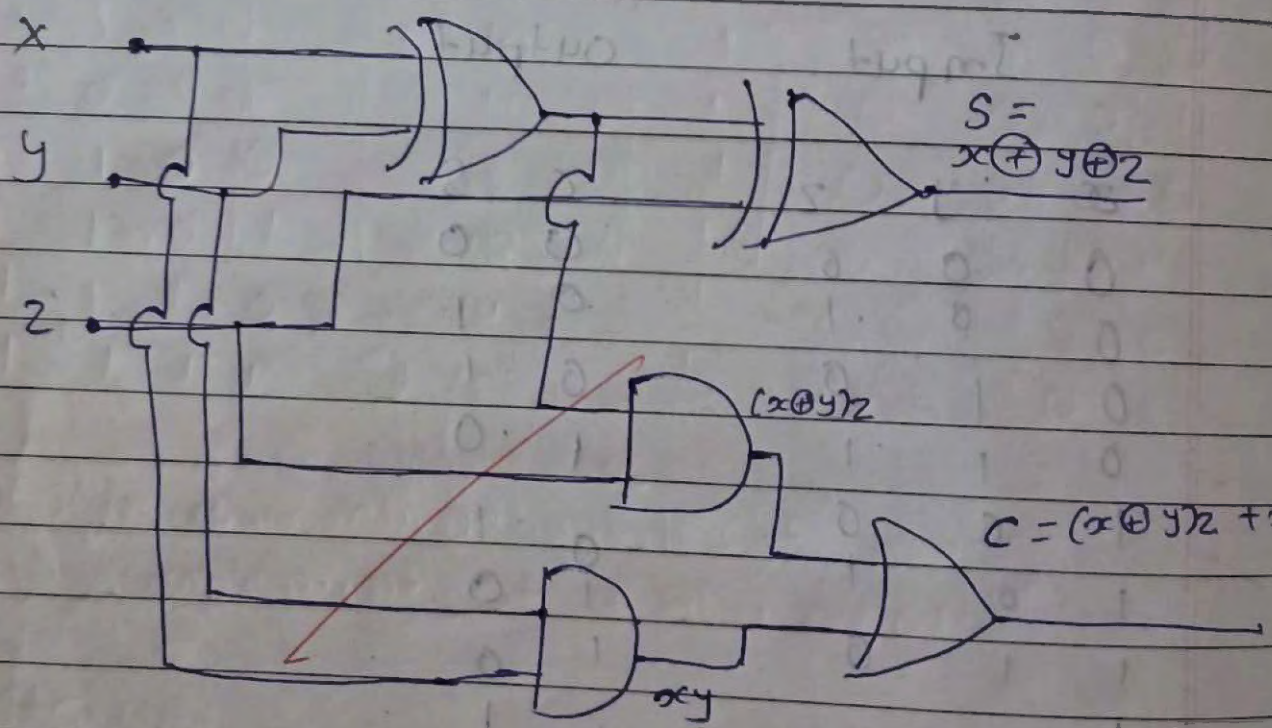
$= (x'y + xy')z + xy(z + z')$

$= (x \oplus y)z + xy$

Using K-Map



$C = xz + xy + yz$



4] Design half adder NAND gate only

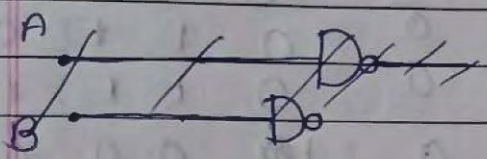
=> For half adder as known.

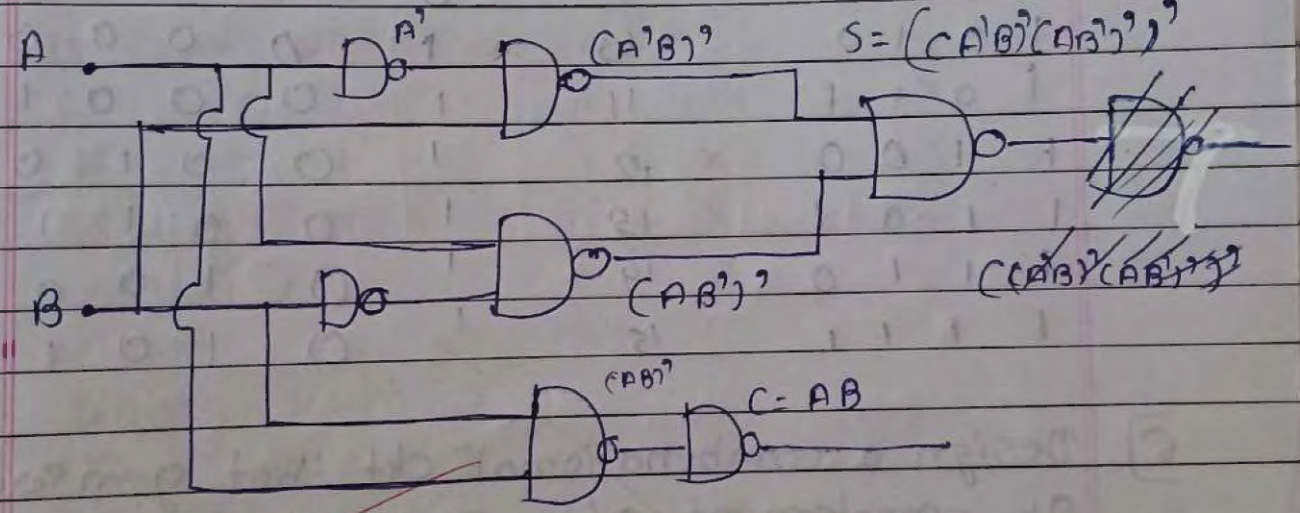
$S = A'B + AB'$ ——— (1) $C = AB$ (2)

$= A \oplus B$

$= ((A'B + AB')')'$

$= ((A'B)'(AB')')'$





5] Design ckt of 4-bit binary which indicates if the four bit input is BCD or not. If its BCD, then output must be high.

Binary code A B C D	Desimal numbers	BCD code B_4 B_3 B_2 B_1 B_0
0 0 0 0	0	0 0 0 0 0
0 0 0 1	1	0 0 0 0 1
0 0 1 0	2	0 0 0 1 0
0 0 1 1	3	0 0 0 1 1
0 1 0 0	4	0 0 1 0 0
0 1 0 1	5	0 0 1 0 1
0 1 1 0	6	0 0 1 1 0
0 1 1 1	7	0 0 1 1 1
1 0 0 0	8	0 1 0 0 0
1 0 0 1	9	0 1 0 0 1
1 0 1 0	10	1 0 0 0 0
1 0 1 1	11	1 0 0 0 1
1 1 0 0	12	1 0 0 1 0
1 1 0 1	13	1 0 0 1 1
1 1 1 0	14	1 0 1 0 0
1 1 1 1	15	1 0 1 0 1

6] Design a combinational ckt that generate 9's complement of a BCD output.

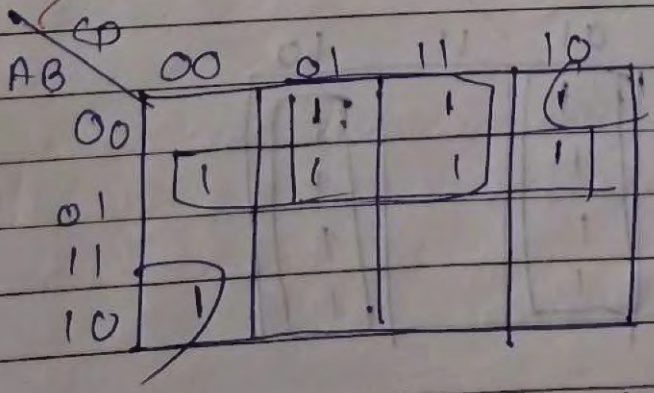
⇒ Here,

Four all functions don't care condition

$d = AB'CD' + AB'CD + ABC'D' + ABC'D + ABCD' + ABCD$

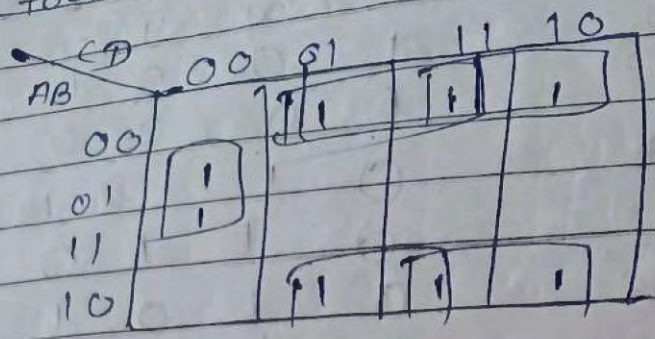
A	B	C	D	W	X	Y	Z
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	1	0	0	1
0	0	1	1	0	1	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	0	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	1	0
1	0	0	1	0	0	0	1
1	0	1	0	0	0	0	0
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X
				X	X	X	X

Using k-map
four ∞,



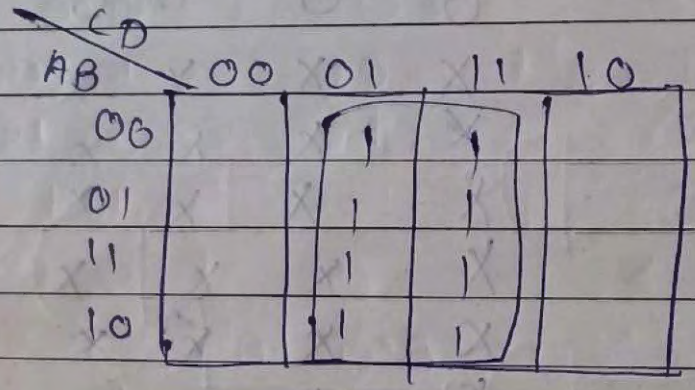
$$W = A'B + A'D + A'C + AB'C'D'$$

for x,



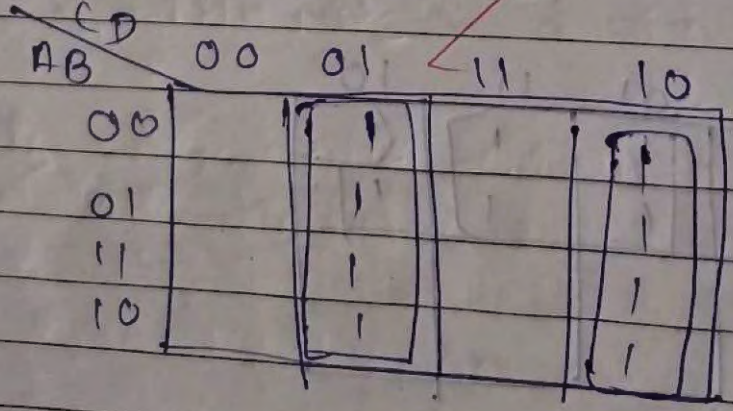
$x = Bc'D' + BD + B'C$

for z,



$z = D$

for y,



$y = cD + cD' = C \oplus D$

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	A	B	C	D	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1
2	0	0	1	0	1	1	1	0
3	0	0	1	1	1	1	0	1
4	0	1	0	0	1	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	0	1	1	1
9	1	0	0	1	0	1	0	1
10	1	0	1	0	0	1	1	0
11	1	0	1	1	0	1	0	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	1	0
15	1	1	1	1	0	0	0	1

$w = A'B + A'D + A'C + AB'C'D'$

$x = BC'D' + B'D + B'C$

$y = C \oplus D$

$z = D$

8) Design a combinational ckt. that accept a 3 bit binary number and generates an output equal to square of input.

	Input			Output					
	P	B	C	x_5	x_4	x_3	x_2	x_1	x_0
0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	1
2	0	1	0	0	0	0	1	0	0
3	0	1	1	0	0	1	0	0	0
4	1	0	0	0	1	0	0	0	0
5	1	0	1	0	1	1	0	0	1
6	1	1	0	1	0	0	1	0	0
7	1	1	1	1	1	0	0	0	1

$x_5 = AB\bar{C} + ABC$

$x_5 = AB$

$x_4 = A\bar{B}\bar{C} + A\bar{B}C + ABC$

$= A\bar{B} + ABC = A(\bar{B} + BC) = A(B + C)$

$x_4 = AB + AC$

$x_3 = \bar{A}BC + A\bar{B}\bar{C} = C(\bar{A}B + A\bar{B})$

$x_3 = (A + B)C$

$x_2 = \bar{A}B\bar{C} + AB\bar{C} = B\bar{C}$

$x_1 = 0$

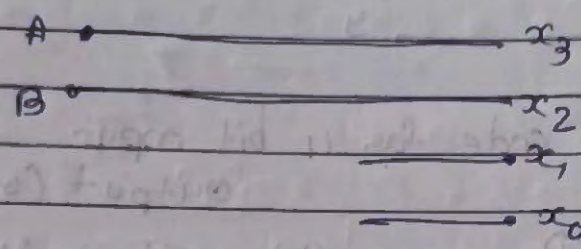
$x_0 = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$

$= \bar{A}C + AC$

$x_0 = C$

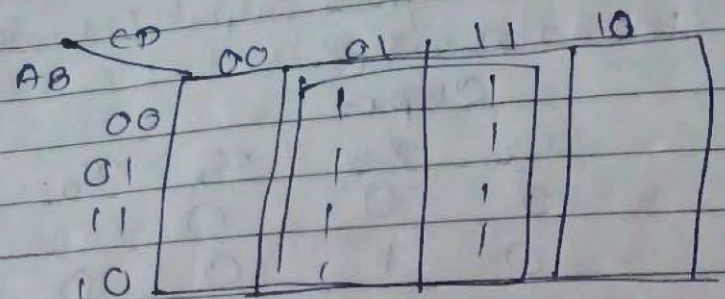
9] Construct a ckt that gives output 1 time of two bit binary variable input.

	Input		Output			
	A	B	x_3	x_2	x_1	x_0
0	0	0	0	0	0	0
1	0	1	0	1	0	0
2	1	0	1	0	0	0
3	1	1	1	1	0	0



10] Design a ckt which has 4 bit binary input output 1 when input logic is in odd no.

	A	B	C	D	Output (Y)
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	0
9	1	0	0	1	1
10	1	0	1	0	0
11	1	0	1	1	1
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	0
15	1	1	1	1	1



$Y = D$

12) BCD to Gray code for 4 bit input

	Input				output (Gray code)			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

W =

AB \ CD	00	01	11	10
00				
01				
11	1	1	1	1
10	1	1	1	1

$W = A$

X =

AB \ CD	00	01	11	10
00				
01	1	1	1	1
11				
10	1	1	1	1

$X = A'B + AB' = A \oplus B$

Y =

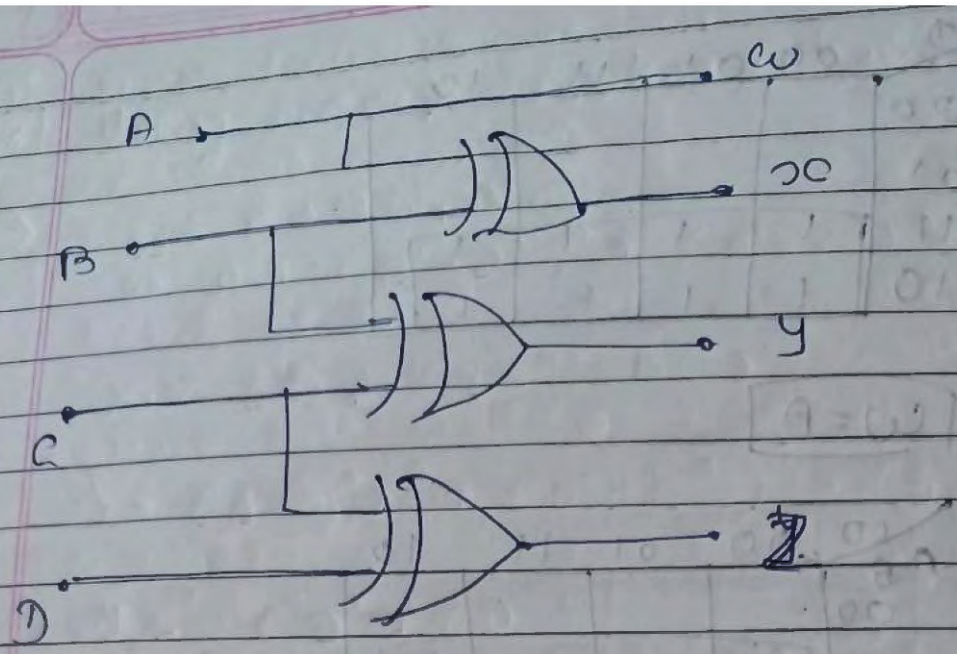
AB \ CD	00	01	11	10
00			1	1
01	1	1		
11	1	1		
10			1	1

$Y = BC' + B'C = B \oplus C$

Z =

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	1			1
10	1			1

$Z = C'D + CD' = C \oplus D$



16] BCD to excess 3-code using min no. of NAND gate.

⇒

	Input				Output			
	A	B	C	D	w	x	y	z
0.	0	0	0	0	0	0	1	1
1.	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0
10	1	0	1	0	x	x	x	x
11	1	0	1	1	x	x	x	x
12	1	1	0	0	x	x	x	x
13	1	1	0	1	x	x	x	x
14	1	1	1	0	x	x	x	x
15	1	1	1	1	x	x	x	x

w =

AB \ CD	00	01	11	10
00		1	1	1
01	X	1	X	X
11				
10	1	1	X	X

$w = A + BD + BC$

$w = [A' . (BD)' (BC)']'$

x =

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	X	X	X	
10		1	X	X

$x = B'D + B'C + BC'D'$

$x = [(B'D)' (B'C)' (BC'D')']'$

y =

AB \ CD	00	01	11	10
00	1		1	
01	1		1	
11	X	X	X	X
10	1		X	X

$y = C'D' + CD = [(C'D')' (CD)']'$

z =

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10	1		X	X

$z = D'$

18] Using g(6) we know that,

$\Rightarrow W = A + BD + BC$

$\Rightarrow A + (B' + D')' + (B' + C')'$

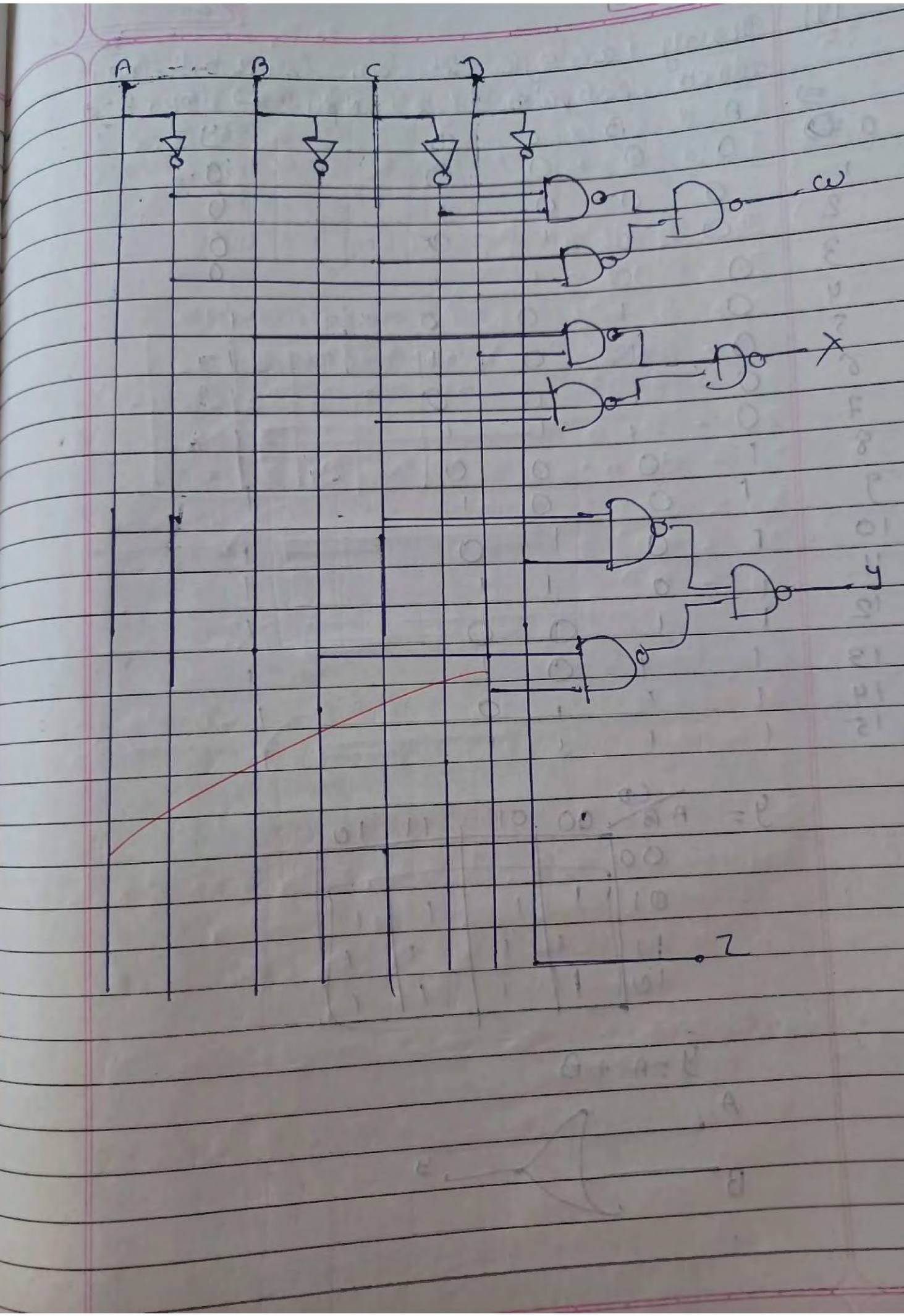
$X = B'D + (B'C') + BC'D'$

$X = (B + D')' + (B + C')' + (B' + C + D)'$

$Y = C'D' + CD$

$Y = (C + D)' + (C' + D')'$

$Z = D'$


A
B
C
D
w
x
y
z

[9] Desing a logic ckt. for four-bit inputs which provides high output if input is > 3

⇒	A	B	C	D	y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	1
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

$y =$

AB \ CD	00	01	11	10
00				
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$y = A + B$