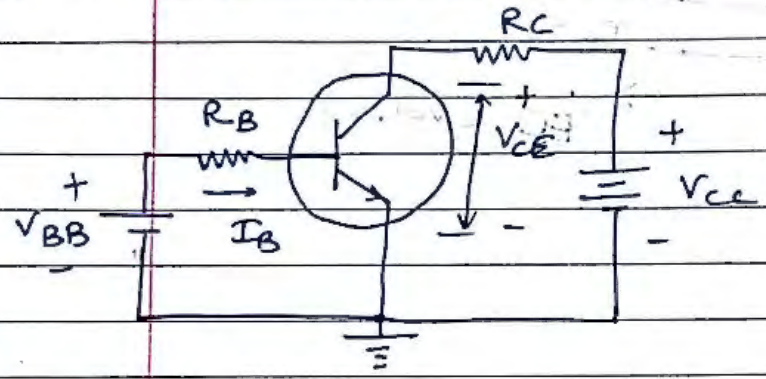
Chapter-2 BJT (Bias circuits)

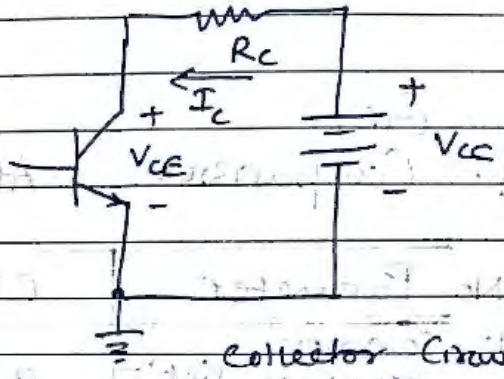
(by. Amit A. Patel)

Q. What is DC load line & Explain with necessary diagram.

→ To understand concept of load line consider the common emitter configuration.



→ To plot load line consider collector circuit



Collector Circuit

→ Apply KVL in collector circuit

$$V_{CC} - V_{CE} - I_C R_C = 0$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

$$I_C = \left(\frac{-1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C}$$

Compare above equation with $Y = mx + c$

here $Y = I_C$, $X = V_{CE}$, $m = \frac{-1}{R_C}$, $c = \frac{V_{CC}}{R_C}$

→ Now substitute $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C}$ (Represent A point)

→ if $I_C = 0$, we get $V_{CE} = V_{CC}$ (Represent B point)

→ Why word DC load line?

→ DC means the line is drawn at dc operating conditions, without any ac signal at the input.

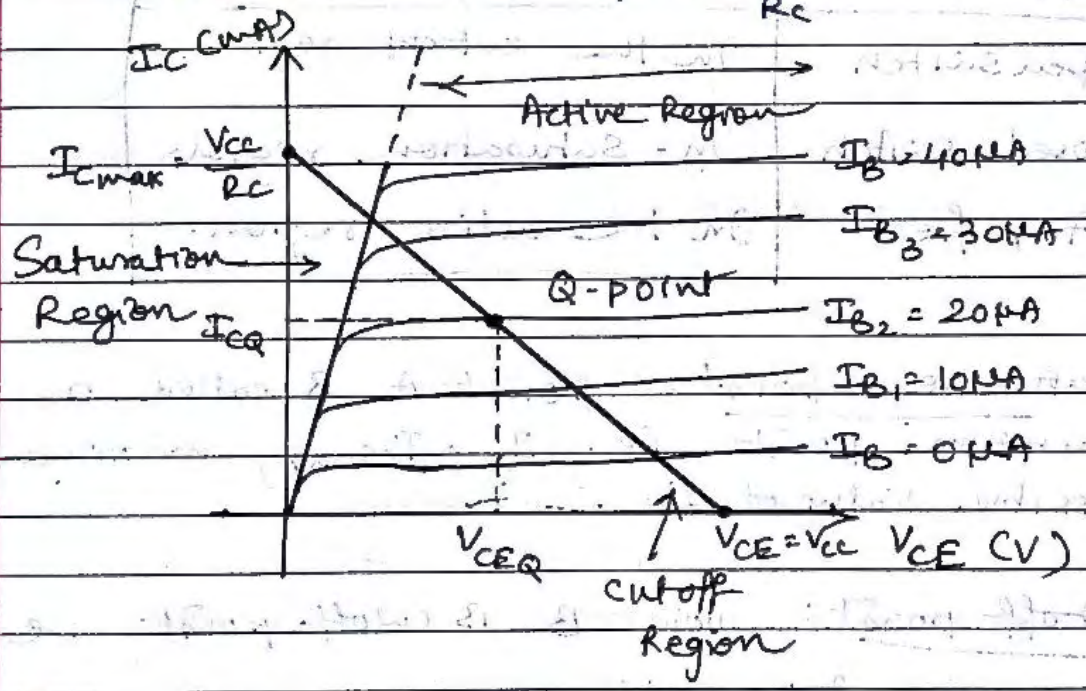
→ & the word load line is because slope of line is $-\frac{1}{R_C}$, where R_C is load resistance.

DC loadline

line is drawn under DC operating condition

slope of line depends on the load resistance R_C

slope = $\frac{-1}{R_C}$



Operating point or the Quiescent point (Q-point) or Bias point:

→ Q. point is the point on load line which represents the dc current through a transistor (I_{CQ}) & the voltage across it (V_{CEQ}), when no ac signal is applied at the input.

→ DC load line is set of infinite Q. point. Designer chose any point on load line as

operating point depending on application.

→ If transistor is used for amplification then Q point should be at the center of load line.

co-ordinates of Q point are:

$$Q = (V_{CEQ}, I_{CQ})$$

Position of Q-point & application

	Application	Position of Q-point
1.	Open switch	In the cut-off region
2.	closed switch	In saturation region
3.	Amplifier	In the active region.

Saturation point: point A is called a saturation point i.e. $I_C = I_{C(max)}$ maximum possible value of I_C.

cut-off point: point B is cutoff point i.e $I_C = 0mA$ & $V_{CE} = V_{CC}$.

Q. Why Biasing Circuits are required? (Jan '19)

* Factors affecting the stability of Q-point

→ ideally Q-point is expected to be "stable" i.e. should not shift up or down on the load line. But practically it is not so.

→ In fact Q-point is quite unstable & keeps changing its position on the dc load line.

→ factors affecting the stability of Q-point are:

1) change in temperature.
2) change in the value of β_{dc}

→ Q. point instability is not desirable because it will introduce distortion in amplified signal.

BIAS STABILIZATION:

→ Bias stabilization is a process of stabilizing the position of the Q-point or bias point.

→ So we need to design a biasing circuit which will keep the position of Q-point stable on the load line.

→ first we will see effect of various parameters on the stability of the Q-point.

Q-point instability due to Temperature.

→ Junction temperature of a transistor is dependent on the amount of the current flowing through transistor. Due to increase in temperature the following parameters of a transistor will change.

1. V_{BE}
2. β_{dc}
3. I_{CBO}

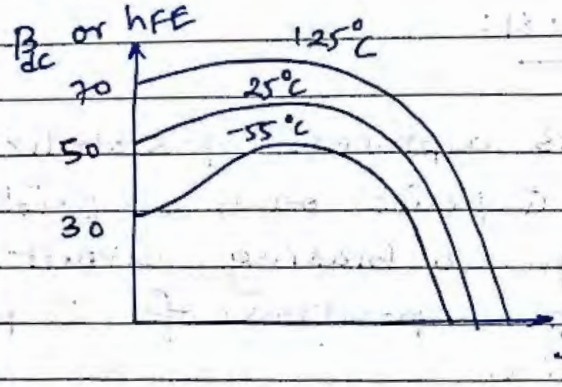
1. Change in V_{BE}:

→ V_{BE} decreases at the rate of 2.5mV/°C with increase of temperature. So I_B increases which changes I_C & Q-point changes.

2. Change in current gain β_{dc}:

→ As $I_C = I_B \cdot \beta_{dc}$

So, as β_{dc} changes, I_C changes & Q-point also changes. As temperature increases β_{dc} increases.



β_{dc} depends on
1) transistor
2) I_C
3) Temperature

3. Change in Reverse saturation current (I_{CBO})

$$I_C = \beta_{dc} I_B + (1+\beta_{dc}) I_{CBO}.$$

→ So I_{CBO} changes then I_C changes & hence Q. point changes.

→ To overcome this problem biasing circuit must include some kind of "temperature compensation" or "temperature stability".

Q. What is Stability factors? Explain (Jan '19)
Stability factors:

→ Q. point of amplifier depends on following parameters:
1) I_{CBO}
2) β_{dc}
3) V_{BE}

1. Stability Factor:

$$S = \frac{\Delta I_c}{\Delta I_{co}} \Big|_{\text{constant } V_{BE} \& \beta_{dc}}$$

or $S = \frac{\partial I_c}{\partial I_{co}}$

2. Stability factor:

$$S' = \frac{\Delta I_c}{\Delta V_{BE}} \Big|_{\text{constant } I_{CBO} \& \beta_{dc}}$$

or $S' = \frac{\partial I_c}{\partial V_{BE}}$

3. Stability factor:

$$S'' = \frac{\Delta I_c}{\Delta \beta_{dc}} \Big|_{\text{constant } I_{CO} \& V_{BE}}$$

or $S'' = \frac{\partial I_c}{\partial \beta_{dc}}$

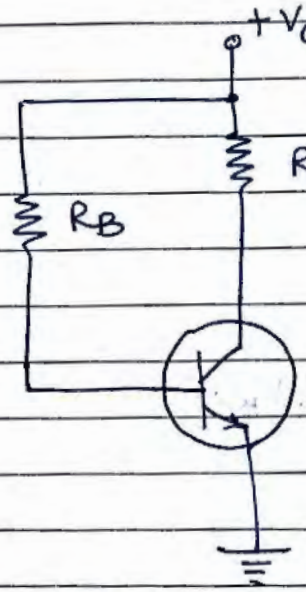
Total change in collector current

$$\Delta I_c = S \Delta I_{CBO} + S' \Delta V_{BE} + S'' \Delta \beta_{dc}$$

STABILIZATION (BIASING) TECHNIQUES

1) Fixed bias circuit (Base bias)
2) collector to Base bias circuit (collector feedback bias)
3) Voltage divider Bias (VDB)
4) Emitter feedback Bias.

Q. Write short note on Base bias circuit. (Fixed Bias Circuit)



Base bias circuit for n-p-n transistor.

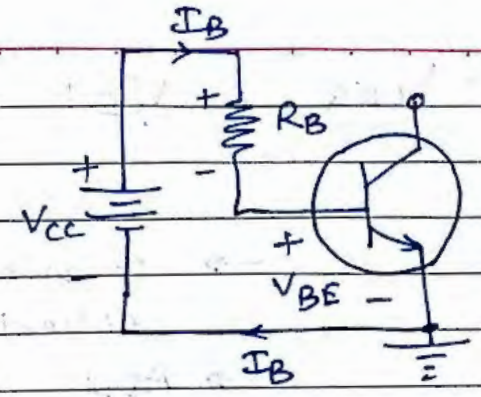
→ here in Base bias circuit only one power supply (V_{CC}) is used to supply power to collector as well as base.

Analysis of fixed bias circuit:

→ Here we need to analyse base circuit & collector circuit

Step-1

→ Expression for Base current:



→ consider the base circuit, here collector is assumed to be open circuited.

→ Apply KVL to Base circuit.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

→ for silicon transistor $V_{BE} = 0.7V$ & for Ge transistor $V_{BE} = 0.3V$.

→ So, $V_{BE} < V_{CC}$, so we can neglect

$$I_B = \frac{V_{CC}}{R_B}$$

→ Here V_{CC} & R_B both are of fixed value. so, I_B remains constant, so this biasing circuit is "fixed bias circuit".

step-2 Expression for I_C or I_{CQ}:

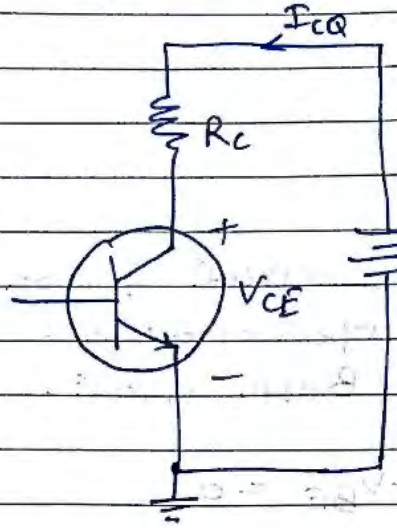
→ fixed bias circuit is designed to operate in the active region.

$$I_C = \beta_{dc} I_B + I_{CEO}$$

$$I_{CEO} << \beta_{dc} I_B$$

$$I_{CQ} = \beta_{dc} I_{BQ}$$

Step 3 Expression for V_{CEQ} or V_{CE}:



→ Consider the collector circuit

→ Apply KVL to collector circuit

$$V_{CC} - I_{CQ}R_C - V_{CEQ} = 0$$

$$V_{CEQ} = V_{CC} - I_{CQ}R_C$$

→ I_{CQ} & V_{CEQ} will give us co-ordinates of Q-point.

Stabilization of Q-point:

As temperature ↑, I_{CBO} ↑, so I_C ↑ because

$$I_C = \beta I_B + (1+\beta) I_{CBO}.$$

→ Here in fixed bias I_B is constant, so, I_C will keep rising with change in temperature.

→ fixed bias circuit can not automatically keep I_C constant & stabilize the Q-point.

Advantages:

→ Circuit is simple & has less number of components.

→ It gives very good flexibility as the Q-point can be set at any point in active Region by adjusting value of R_B.

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DB advantages : (of fixed Bias Circuit)

→ very poor thermal stability.

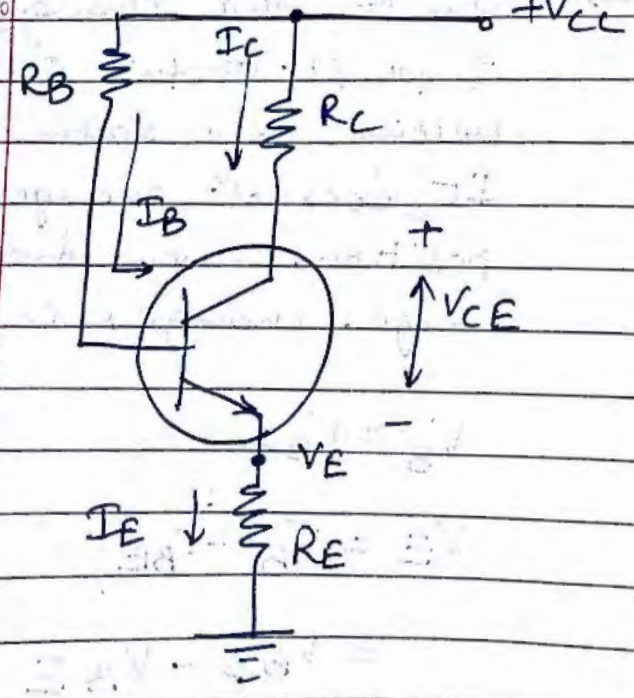
$S = (1+\beta_{dc})$

→ with change in β_{dc} due to change in temperature the operating point keeps on changing.

Q. Write short Note On:

Emitter Feedback Bias:

→ Here Resistor R_E is added in to fixed Bias circuit



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Stabilization of Q-point.

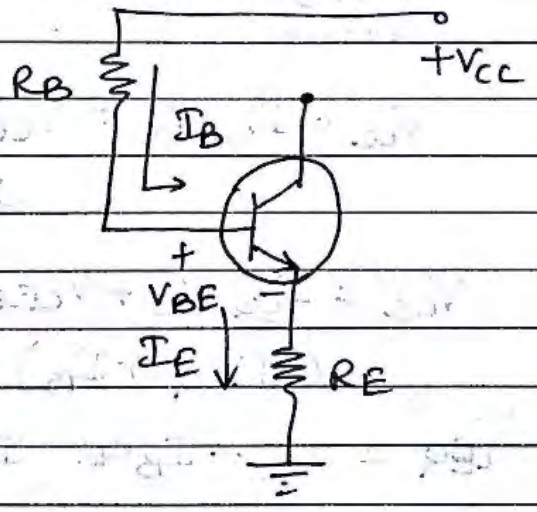
→ If I_C tends to increase due to either rise in temperature or change in β_{dc} due to replacement of transistor, then I_E will also increase.

→ As I_E increases, voltage drop across R_E i.e. V_E will increase.

→ But V_B is constant, so V_{BE} decreases, this will reduce the I_B & therefore the increased I_C will be reduced towards its desire value. Thus Q-point stabilized.

Analysis:

Expression for I_{CQ}:



Base circuit

Apply KVL.

$V_{CC} = I_B R_B + V_{BE} + I_E R_E$ — (1)

$I_E = I_C + I_B$ — (2)

$I_C = \beta_{dc} I_B$ — (3)

$I_E = \beta_{dc} I_B + I_B$.

→ Substitute value of I_E & I_C from eq. (2) & (3) in (1).

$V_{CC} = I_B R_B + V_{BE} + (\beta_{dc} I_B + I_B) \cdot R_E$

$V_{CC} = I_B R_B + V_{BE} + \beta_{dc} I_B R_E + R_E I_B$.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E + \beta_{dc} R_E}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta_{dc}) R_E} \quad \text{---(4)}$$

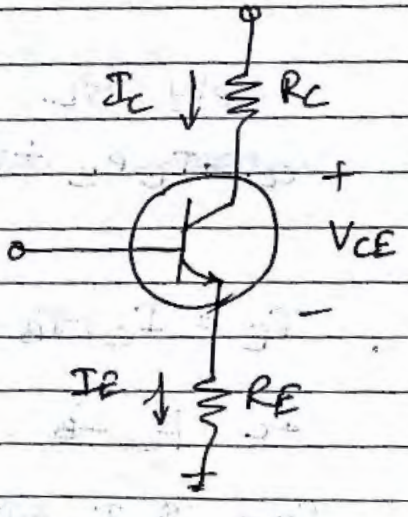
Step 2 Expression for I_{CQ}:

$$I_{CQ} = \beta_{dc} I_B$$

put value of I_B from eq. (4) in above,

$$I_{CQ} = \frac{\beta_{dc} (V_{CC} - V_{BE})}{R_B + (1+\beta_{dc}) R_E}$$

Step 3 Expression for V_{CEQ}:



→ Apply KVL to collector circuit

$$V_{CC} = I_{CQ} R_C + V_{CEQ} + I_E R_E$$

$$V_{CC} = I_{CQ} R_C + V_{CEQ} + (I_{CQ} + I_B) R_E$$

$$V_{CEQ} = V_{CC} - I_B R_E - I_{CQ} (R_C + R_E)$$

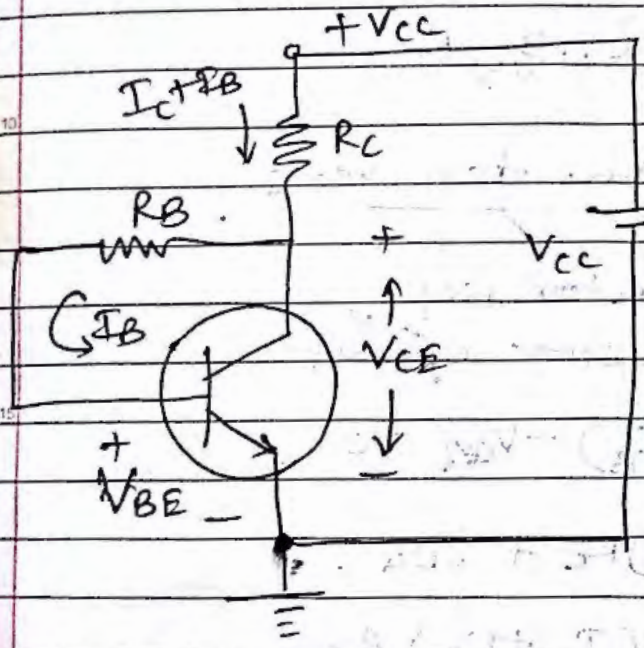
Assuming $V_{CC} >> I_B R_E$

$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E)$$

Q. Write short note on
Collector Feedback Bias: (Collector to Base Bias)

→ collector to Base bias circuit is improvement over the fixed bias circuit.

→ R_B is now connected to the collector, not to supply.



→ Current flowing through RC is sum of I_C & I_B

Step-1 Expression for Base current.

$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0.$$

$$V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

But $I_C = \beta_{dc} I_B$.

$$V_{CC} = (R_B + R_C) I_B + \beta_{dc} I_B R_C + V_{BE}$$

$$V_{CC} = (R_B + R_C + \beta_{dc} R_C) I_B + V_{BE}$$

$$I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + R_C + \beta_{dc} R_C}.$$

collector current at Q-point is I_{CQ}.

Step-2 Expression for collector current.

collector current $I_{CQ} = \beta_{dc} I_{BQ}$

$$I_{CQ} = \frac{\beta_{dc}(V_{CC} - V_{BE})}{(R_B + (1+\beta_{dc})R_C)}$$

Step-3 Expression for V_{CEQ}.

→ now consider collector loop.

→ Apply KVL to collector circuit

$$V_{CC} - R_C(I_C + I_B) - V_{CEQ} = 0$$

$$V_{CC} = (I_C + I_B)R_C + V_{CEQ}$$

$$V_{CEQ} = V_{CC} - (I_C + I_B)R_C$$

→ V_{CEQ} is voltage across collector to emitter at Q-point.

Q-point Stabilization:

→ We know that Q point stability is affected by change in β_{dc} or I_{CEO} due to changes in temp or due to piece to piece variations in characteristics.

→ due to change in β_{dc} & I_{CEO} I_C changes

$$I_C = \beta_{dc} I_B + I_{CEO}$$

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STABILIZATION OF Q-POINT TAKES PLACE AS BELOW.

→ If temp ↑, β_{dc} & I_{CEO} ↑, so I_C ↑, voltage drop across R_C i.e. $I_C R_C$ ↑,

$V_{CE} = V_{CC} - (I_C + I_B) R_C$, so, V_{CE} ↓,

As $I_B = \frac{V_{CE} - V_{BE}}{R_B}$, I_B ↓, this reduces I_C because $I_C = \beta_{dc} I_B$, so increase in I_C is compensated.

→ so I_C maintained constant, irrespective of change in β_{dc} or I_{CEO}, & Q point stabilized.

Advantages:

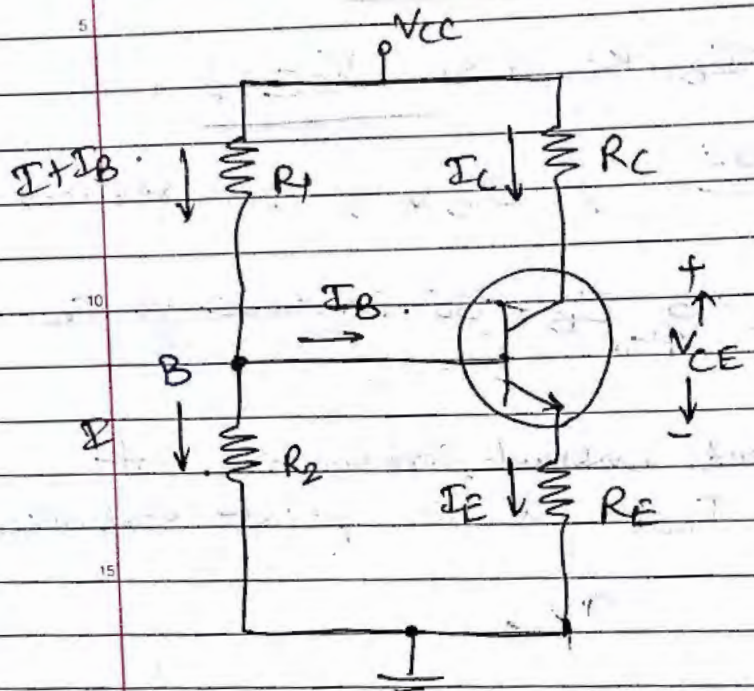
→ Improvement in stability.
→ needs only one dc power supply.
→ Advantages of negative feedback.

Disadvantages:

→ Poor thermal stability for small value of R_C.
→ complicated circuit design
→ voltage gain reduced due to negative feedback.
→ Q-point stability is not as good as expected.

Q. Write short note on VOLTAGE DIVIDER BIAS (VDB).

→ Circuit Diagram for voltage divider Bias is shown in fig. below.



Voltage divider Bias.

→ Due to presence of R_1 & R_2 which divides voltage V_{CC} circuit name is given as voltage divider circuit.

→ R_1 & R_2 form voltage divider, to apply fixed voltage V_B to the Base

→ R_E is connected in the emitter circuit.

Bias stabilization using voltage divider Bias.

→ I_E ↑ due to change in Temperature or β_{dc}

→ I_C ↑ then I_E ↑

→ So drop across R_E ↑ ($V_E = I_E R_E$)

→ But V_B constant so V_{BE} ↓

→ As V_{BE} ↓, I_B ↓

→ So, I_C also decreases. Thus compensation for increases in I_C is achieved.

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Consider Base Circuit:

Voltage at Base terminal is V_B.

$$V_B = V_{R_2} = \frac{R_2 \times V_{CC}}{(R_1 + R_2)}$$

Consider collector circuit

Voltage across emitter resistance R_E

$$V_E = I_E R_E = V_B - V_{BE}$$

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

Apply KVL in collector loop.

$$V_{CC} = I_C R_C + V_{CE} + R_E I_E$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Steps for simplified Analysis

1) $V_B = \frac{R_2}{R_1 + R_2} V_{CC}$
2) $V_E = V_B - V_{BE}$
3) $I_E = \frac{V_E}{R_E}$
4) $I_C \approx I_E$
5) $V_C = V_{CC} - I_C R_C$
6) $V_{CE} = V_C - V_E$

Advantages of VDB:

→ It has smallest value of S among all biasing circuit.
→ loss of signal gain is avoided as R_E is connected
→ R_E introduce negative feedback, so circuit is more stable.

Disadvantages of VDB:

→ The ratio (R_B/R_E) needs to be low for better Q point stabilization. so R_E should be high & R_B low, which reduces input Resistance.
→ Reduction in gain due to negative feedback if R_E is unbypassed.

COMPARISION OF BIASING CIRCUITS.

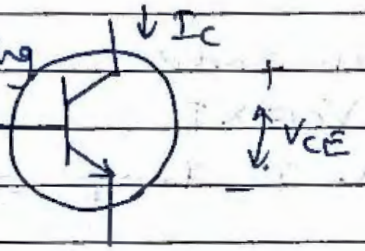
	Parameter	Base Bias	Emitter Bias	Voltage Divider Bias.
1.	Circuit Diagram	-	-	-
2.	Emitter Resistor	Not used	used	used
3.	Feedback	Not present	Present	Present
4.	Thermal Stability	Poor	Good	Very Good
5.	Power supply	Single polarity	Single polarity	Single polarity
6.	Application	Switch Digital Application	IC, driver, Amplifier	Amplifier

Q. What is transistor power dissipation & thermal Runaway.

Transistor power Dissipation:

→ In all power amplifier, we need to use power transistors. These are operated in active region.

→ So, large voltage (V_{CE}) appears across transistor & large current (I_C) flows through it.



Power dissipation

$P_d = I_C \cdot V_{CE}$

→ P_d is measured in Watts.

→ This P_d increases temp of power transistor & Power dissipation is done in form of heat.

→ As P_d ↑, temp of device is ↑

↪ Device temp. should not rise above max. limit i.e. T_{jmax} specified by junction, otherwise

→ device can damage permanently

Q. Thermal Stabilization

Thermal Runaway

→ The collector region of a transistor dissipate heat. As the amount of power dissipated in transistor ... increases junction temperature increases.

→ The maximum power that a transistor can dissipate without getting damaged depends on max. temp that a collector-base junction can withstand.

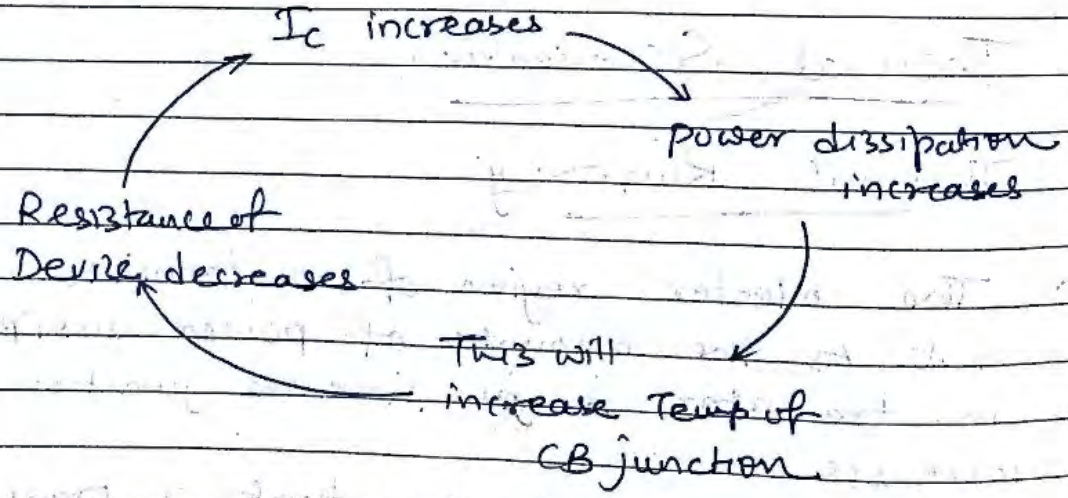
→ Temperature of collector - Base junction increases due to.

1) Due to increase in the ambient (surrounding) temp.
2) Due to the internal heating.

→ Internal heating process is cumulative

1. As I_C ↑ , power dissipated in collectorbase junction ↑ , $P_D = V_{CE} \times I_C$.
2. As Power dissipation ↑, Temp of CB junction increases
3. As Junction Temp ↑, internal resistance ↓
4. As internal resistance ↓ , I_C ↑.

→ This becomes cumulative process which will finally damage the transistor due to excessive internal heating.



How to avoid Thermal Runaway:

→ Never exceed the I_C beyond certain max. value specified by manufacturer.

→ Never exceed the internal power dissipation above the max. value specified by manufacturer.
→ Use heat sink to reduce the heat into atmosphere.

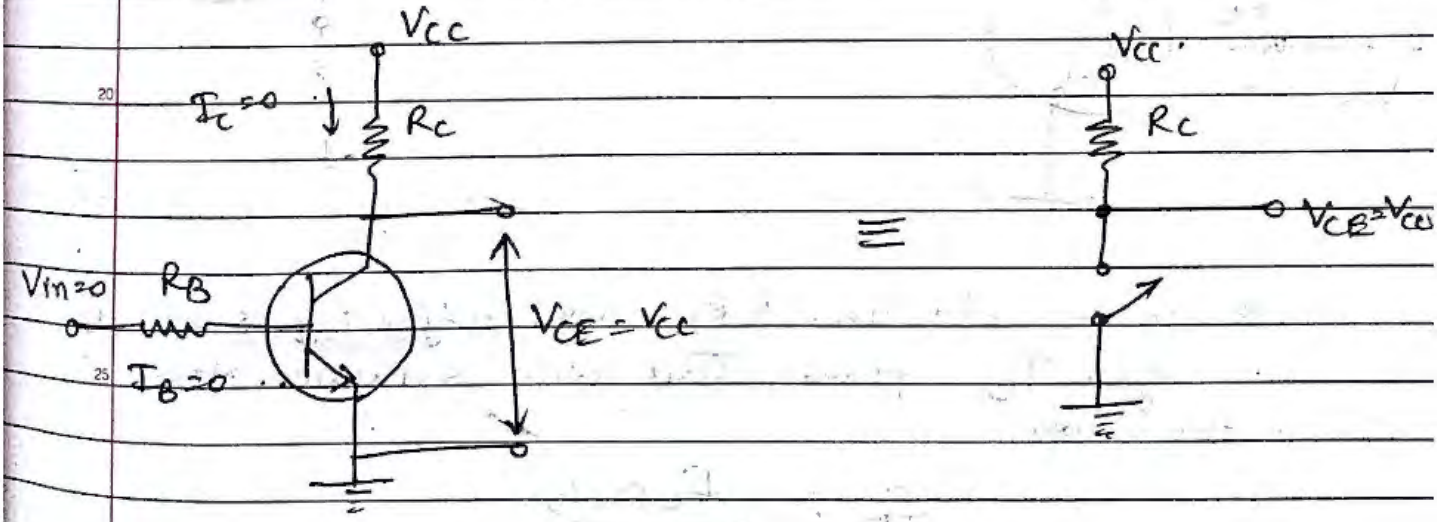
Q. Draw & Explain Transistor as Switch.

→ Transistor can be used for two applications.
1. Amplifier 2. as a switch.

→ for Amplification, transistor is Bias in active region.
→ for switch open transistor bias in cutoff "
→ for switch closed Transistor bias in saturation"

Transistor in cutoff region:

(transistor as an open switch).



→ In cutoff region both junctions (CB junction & BE junction) are in reverse Biased.

→ Voltage drop across the transistor (V_{CE}) is high.

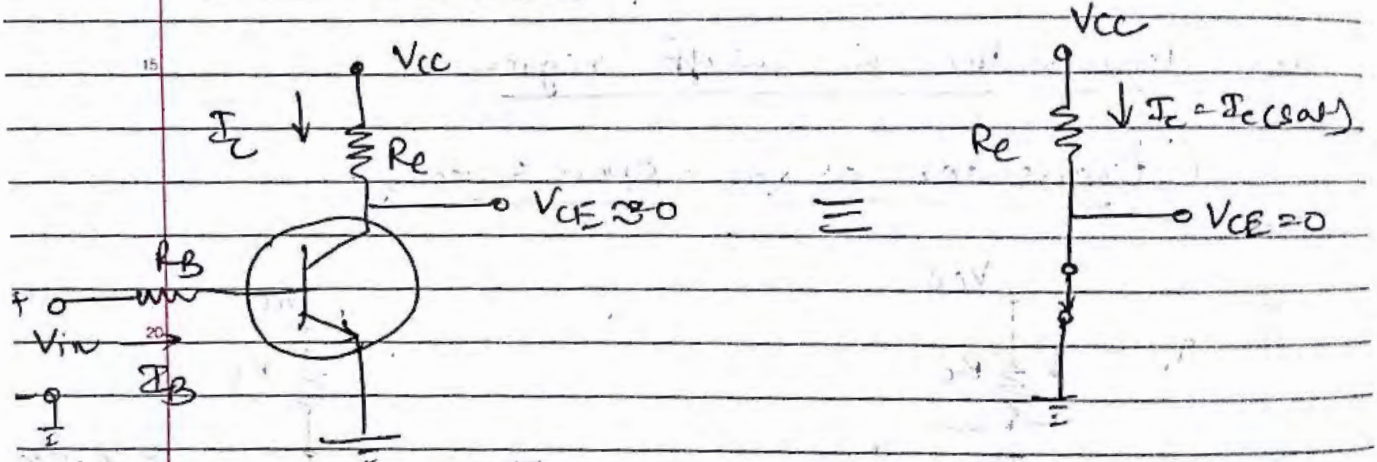
→ $V_{in} = 0$, so $I_B = 0$, $I_c = 0$

so, $V_{CC} = I_c R_c + V_{CE}$

As $I_c = 0$, $\boxed{V_{CC} = V_{CE}}$

→ This shows resistance offered by transistor is infinite & transistor operates as open switch.

* Transistor in Saturation Region: (Transistor as closed switch)



→ Value of V_{in} & R_B are adjusted such as large I_B flows. This will saturate the transistor.

$$I_B \geq \frac{I_{c(sat)}}{\beta}$$

→ In saturation region both junctions are in forward biased.

→ V_{CE} is very small of the order of 0.2V to 1V.

→ I_c is very large.

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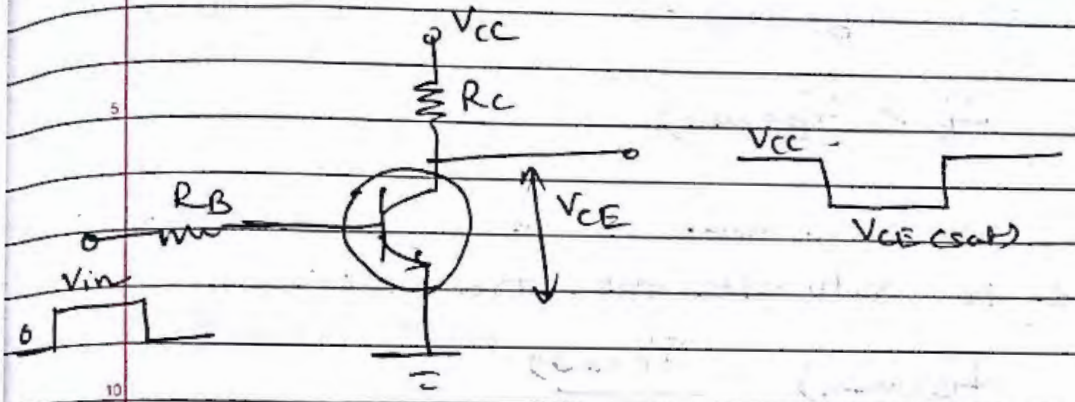
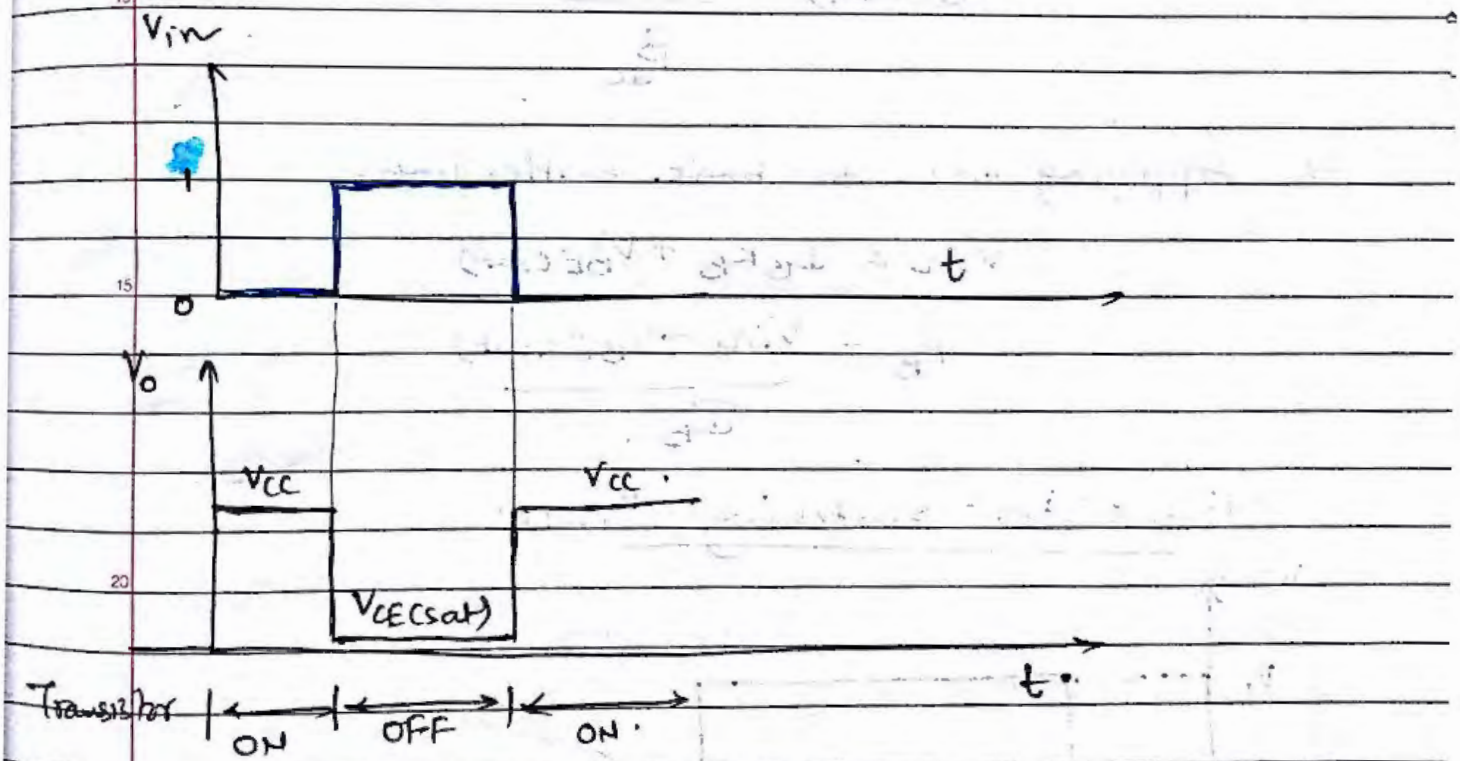
Switching waveforms of an ideal transistor switch:





→ To design Biasing Circuit.

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

$V_{CE(sat)} = 0V$ assumption.

$$I_{C(sat)} = \frac{V_{CC}}{R_C} \Rightarrow \boxed{R_C = \frac{V_{CC}}{I_{C(sat)}}}$$

let
$V_{in} = 5V$, transistor is saturated by supplying a base current I_B, which is greater than a value called $I_{B(min)}$.

$$I_B \geq I_{B(min)}$$

$I_{B(min)}$ is minimum value of base current required to saturate the transistor.

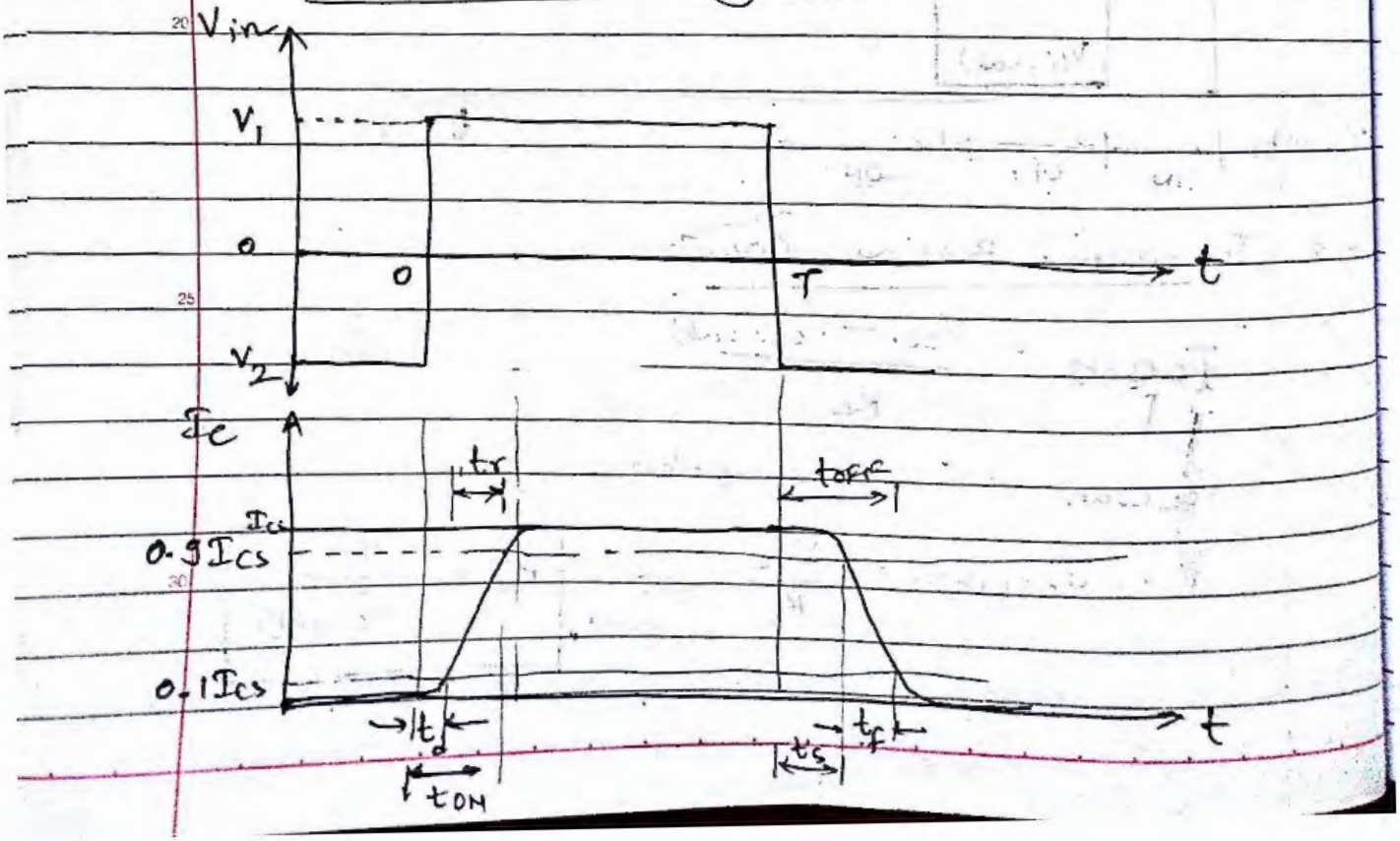
$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{dc}}$$

→ Applying KVL to base emitter loop.

$$V_{in} = I_B R_B + V_{BE(sat)}$$

$$R_B = \frac{V_{in} - V_{BE(sat)}}{I_B}.$$

Transistor switching Times.



The practical transistor does not switch its state instantaneously. It needs finite time to turn on & to turn off completely.

→ Consider practical transformer being driven by pulse waveform as shown in fig. Various delays are as below.

1) Turn on time: $t_{ON} = t_d + t_r$, it is sum of two time intervals delay time t_d and rise time t_r. It is a time between high base voltage is applied & collector current reaches 90% of its max. value

2) Delay Time: Time required for collector current to attain 10% of the maximum value of I_C. $I_{C(max)} = I_{CS}$ (saturation value of I_C)

$$I_{CS} = \frac{V_{CC}}{R_C}$$

3) Rise Time: Time required for collector current I_C to increase from 0.1 I_{CS} to 0.9 I_{CS}.

4) Turn off Time: Time taken by collector current to reduce I_{CS} to 10% of I_{CS} after input switch from V_1 to V_2

$$T_{OFF} = t_s + t_f$$

5) Storage time: t_s

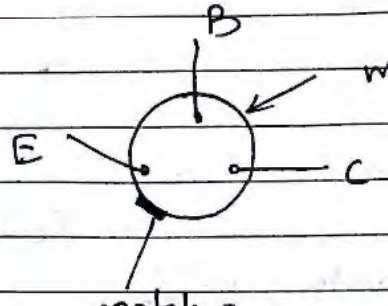
Time interval between transistor input waveform from V_1 to V_2 and & time when I_C reduced to 90% of I_{CS}.

Fall Time : (t_f)

It is defined as the time required for I_C to fall from 90% to 10% of the maximum value of I_C i.e. I_{CS}.

Q. How to Test transistor using multimeter

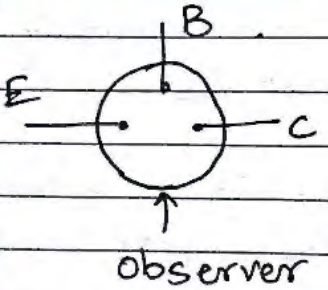
Identification of transistor leads -

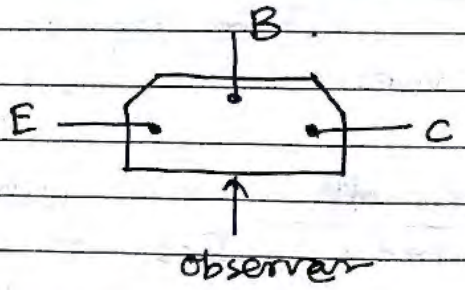


Bottom view of transistor.

→ Terminal close to notch is emitter.
→ Central terminal is Base
→ remaining is collector

→ If transistor donot have notch, then.

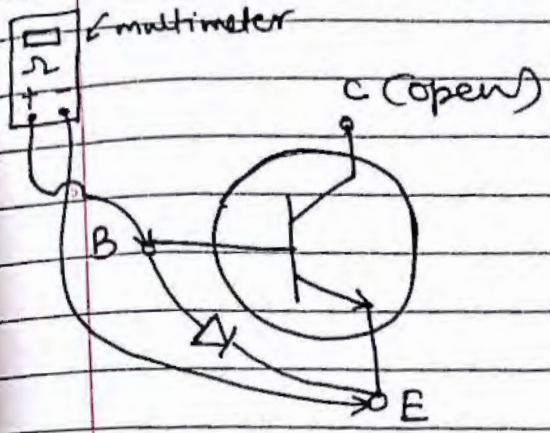




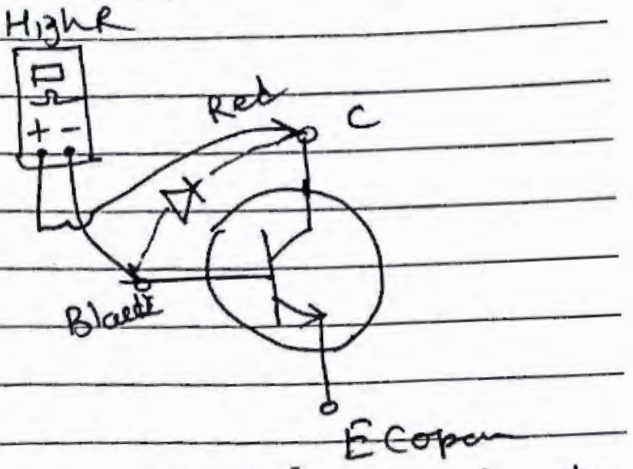
→ Lead on left hand side is emitter, central is base & remaining is collector.

→ for Base first (BF) series transistors, the procedure is same only one change, left most terminal is base, central is emitter & remaining is collector.

Transistor Testing using a multimeter.



checking BE junction



checking CB junction

1) checking BE junction:

Red of multimeter (positive terminal +ve) is connected to base & Black of multimeter (-ve) is connected to emitter then internal battery of multimeter will forward Bias BE junction & resistance is low about 100 Ω to 1KΩ.

2) checking CB junction:

Red terminal of multimeter (+ve terminal) connected to collector & Black terminal i.e. (-ve terminal) of battery connected to Base. Then, resistance displayed will be high about 100 KΩ.

If both junction resistances are closed to their expected values then NPN transistor is okay.