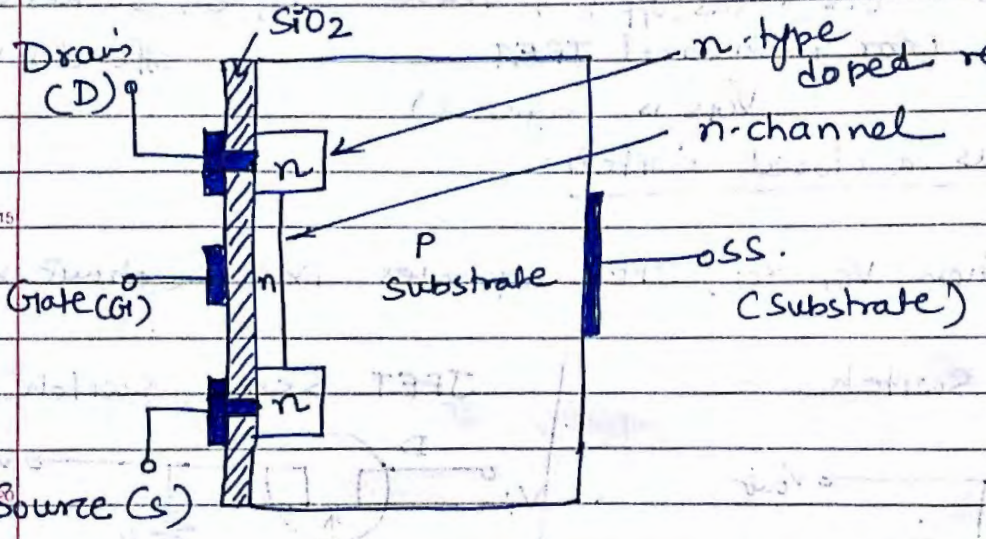
MOSFET. (Metal oxide Semiconductor field effect transistor)

Types of MOSFET.

→ Depletion type MOSFET.
→ Enhancement type MOSFET.

Q. Draw & Explain construction of Depletion type MOSFET (D-MOSFET)



Construction of n-channel D-MOSFET.

→ p-type of semiconductor material (Silicon) is used as a substrate.
→ Drain & source terminals are connected to n-type material through metallic contacts.
→ The gate terminal is insulated from the n-channel by thin Silicon di-oxide (SiO_2).
→ Depletion MOSFET. is normally ON MOSFET.

It means it conducts when no gate voltage applied.

Q. Explain operation of Depletion MOSFET:

OR

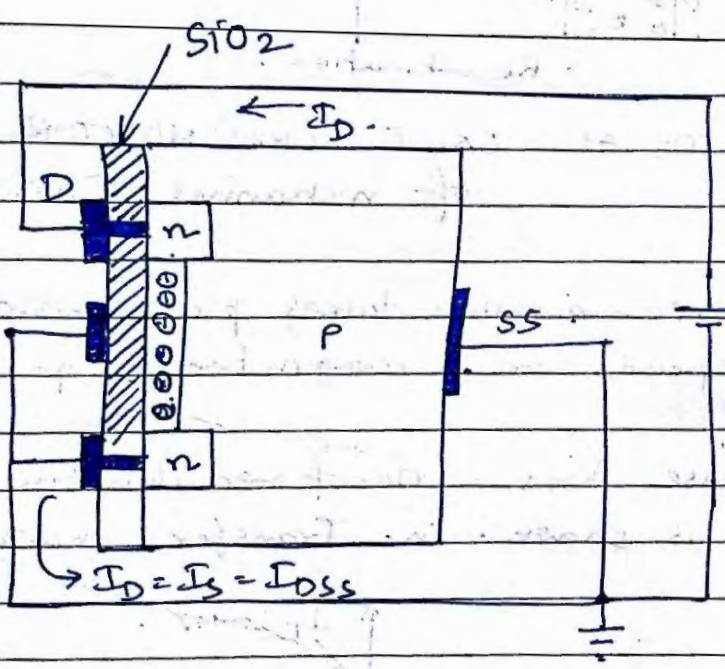
Explain construction, operation & characteristic of n-channel DMOSFET.

case·1 Operation with $V_{GS}=0V$.

→ Gate, source & substrate terminals are connected together to the ground point. Thus $V_{GS}=0$.

→ positive V_{DD} applied to drain, due to this electrons from channel attracted to the drain & drain current starts flowing.

→ I_D at $V_{GS}=0$ is I_{DSS}.



n-channel depletion type MOSFET with $V_{GS}=0$

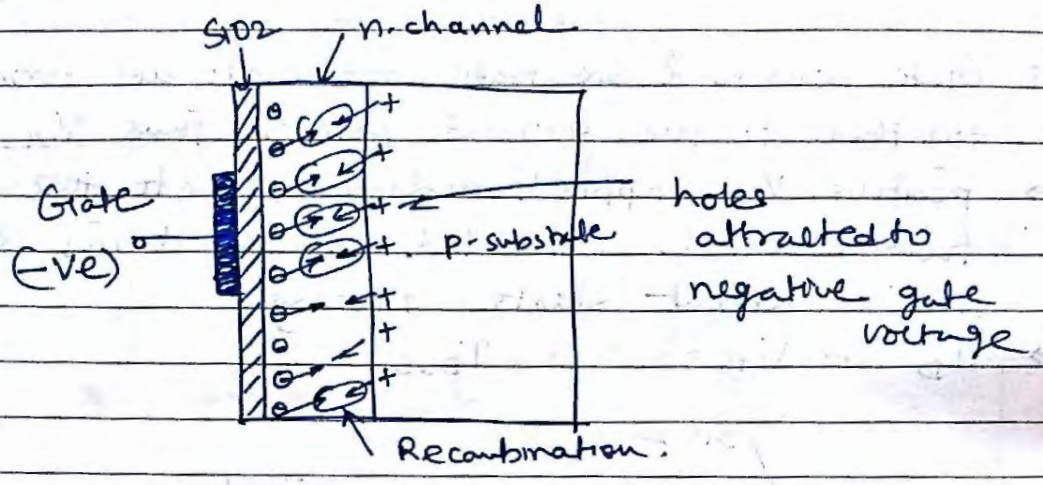
case·2. Operation of depletion MOSFET with negative V_{GS}.

→ As negative gate to source voltage applied it repels electrons to p-type substrate &

attracts holes from substrate.

→ these holes recombines with electrons inside channel. This will reduce the number of free electrons available for conduction.

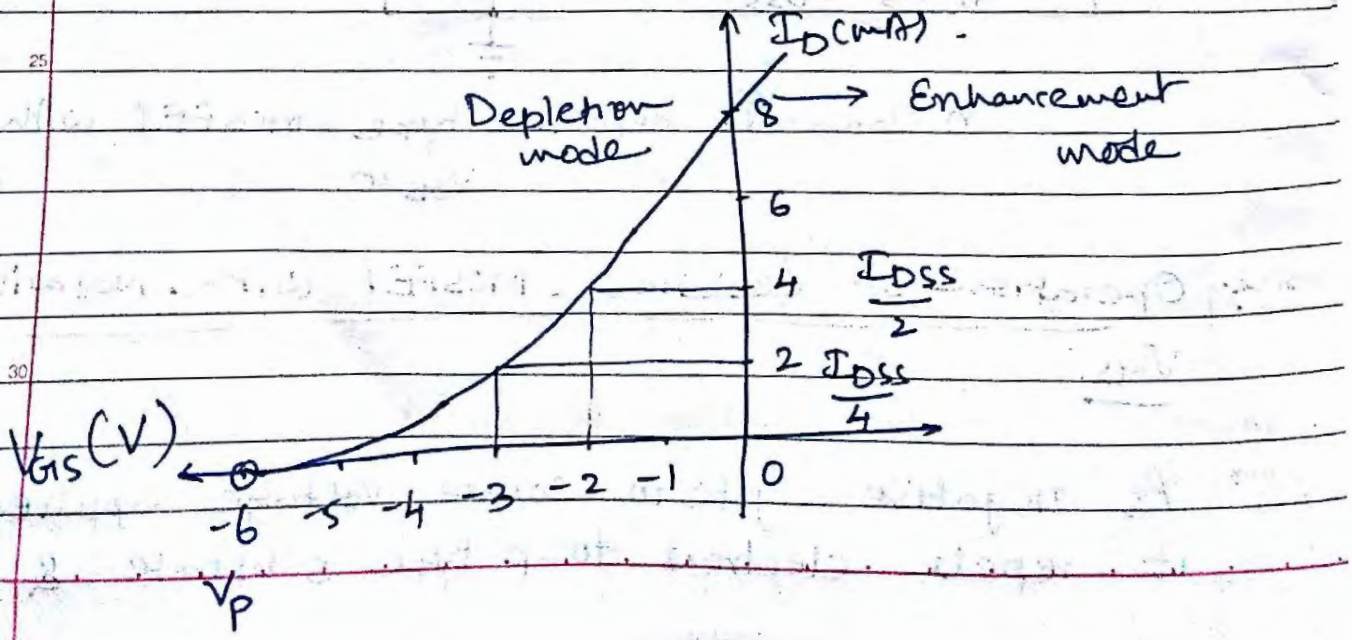
→ so, drain current decreases with increase in negative value of V_{GS}.



METAL OXIDE SEMICONDUCTOR STRUCTURE of n-channel DMOSFET.

→ number of recombination takes place inside channel depends on magnitude of negative V_{GS}.

→ As we increase V_{GS}, no. of recombination ↑ & I_D ↓. This is shown in Transfer characteristics.



transfer characteristics shows that

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Case 3 Effect of positive gate to source voltage:

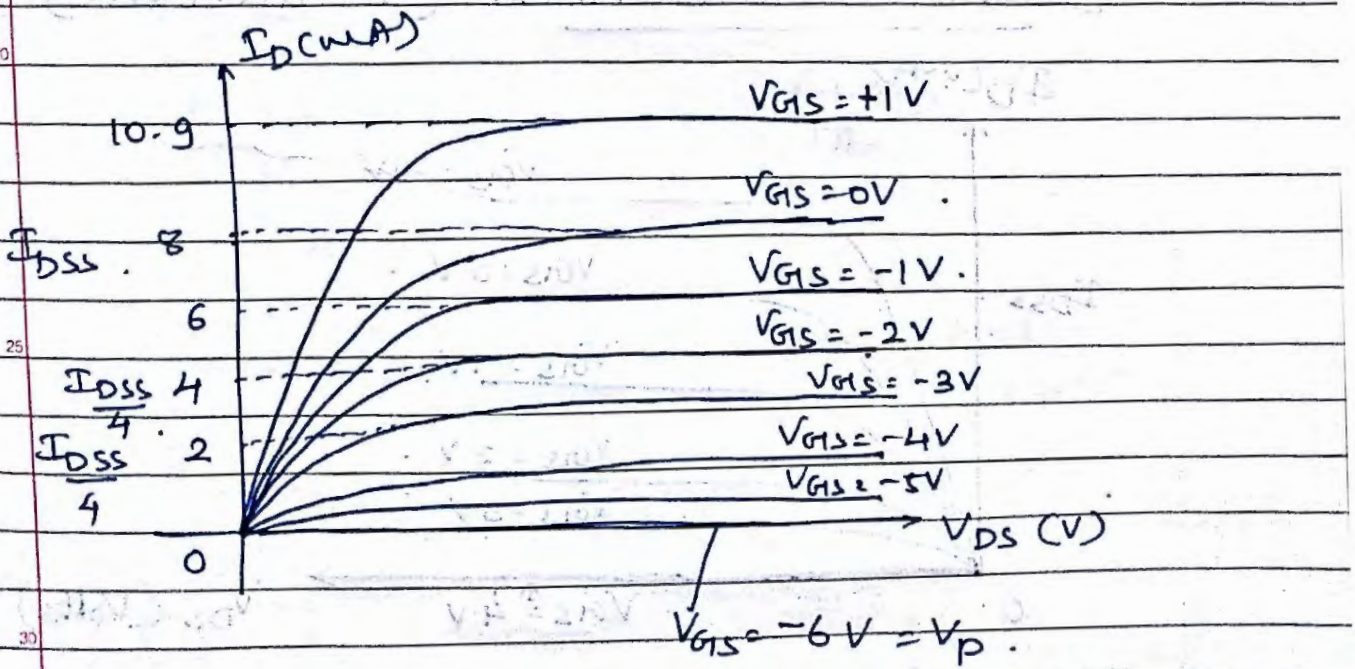
→ If gate voltage is made positive with respect to source, then positive V_{GS} will attract additional electrons (free electrons) from p-type substrate.

→ Due to these accelerated electrons drain current will increase due to positive V_{GS}.

→ positive V_{GS} is enhancement region.

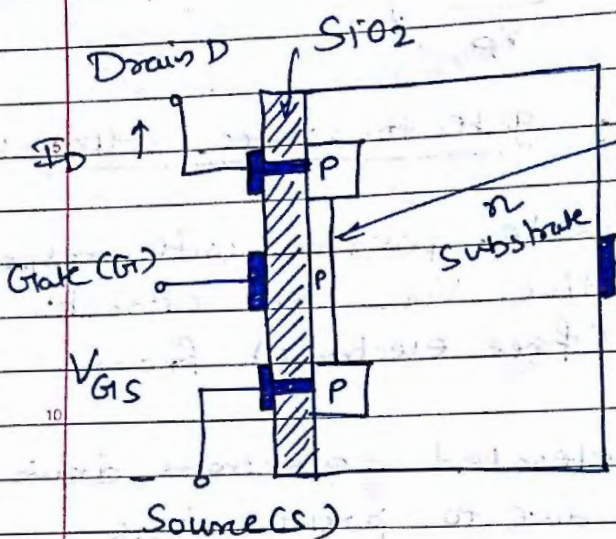
→ We need to check maximum drain current rating, I_D should not exceed above it.

Q. Drain characteristics of n-channel DMOSFET



Drain characteristic is same as MOSFET, only positive V_{GS} part is added.

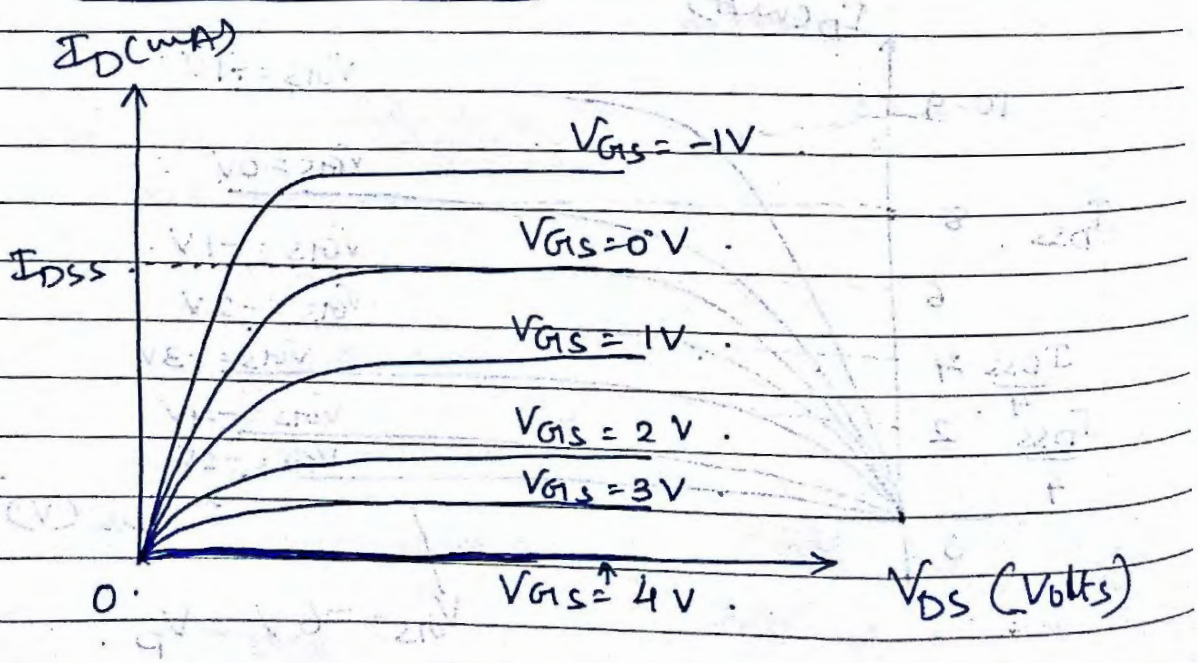
p-channel Depletion type MOSFET.



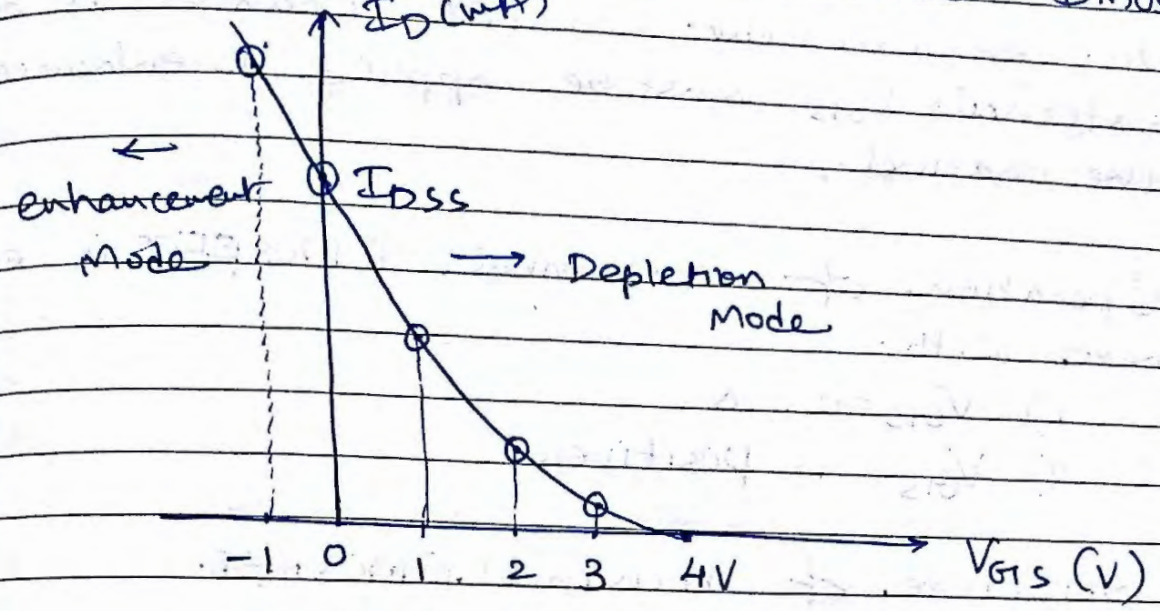
Construction of p-channel DMOSFET.

→ All voltage polarities & current directions are reversed as compared to n-channel MOSFET.

Drain Characteristics: (Drain curves)



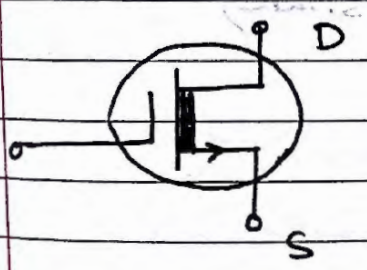
As V_{GS} is reversed, transfer characteristics of p-channel D MOSFET is mirror image of transfer characteristics of n-channel DMOSFET.



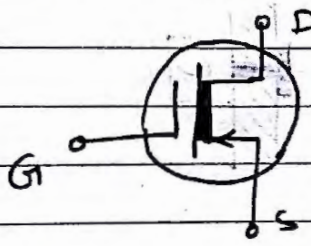
Transfer characteristics of p-channel JFET.

Symbol of n- & p-type Depletion MOSFET.

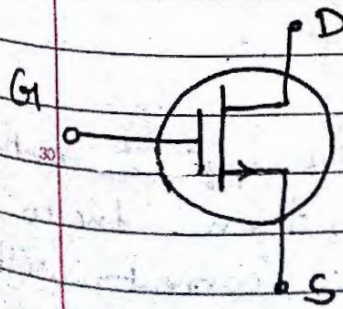
n-channel DMOSFET.



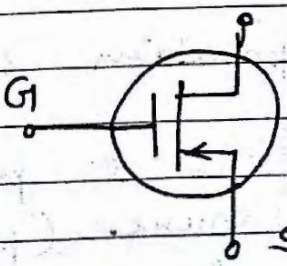
p-channel DMOSFET.



n-channel EMOSFET.



p-channel EMOSFET



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n-channel

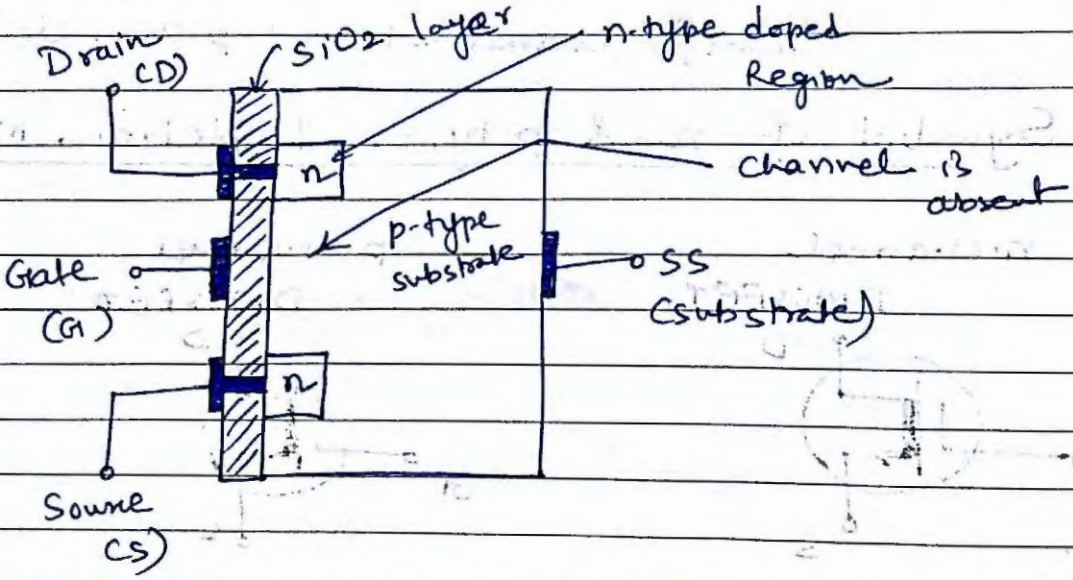
Q Draw & explain operation of enhancement mode MOSFET.

→ In enhancement MOSFET channel is absent. external V_{GS} must be applied to enhance the channel.

Operation of n-channel EMOSFET is explained here with

1) $V_{GS}=0$ &
2) V_{GS} is positive.

Structure of n-channel EMOSFET.



→ Construction of EMOSFET (n-channel) is similar to DMOSFET (n-channel) only channel is absent.

Case 1 Operation with $V_{GS}=0$

→ if $V_{GS}=0$ & positive voltage is applied between drain & source (positive V_{DS}), then due to absence of channel zero drain current will result.

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Case II Operation when V_{GS} is positive:

→ Due to positive V_{GS}, holes in p-type substrate repel in the substrate downward and minority carriers in substrate, attracted towards positive gate terminal & gather near the surface of SiO_2.

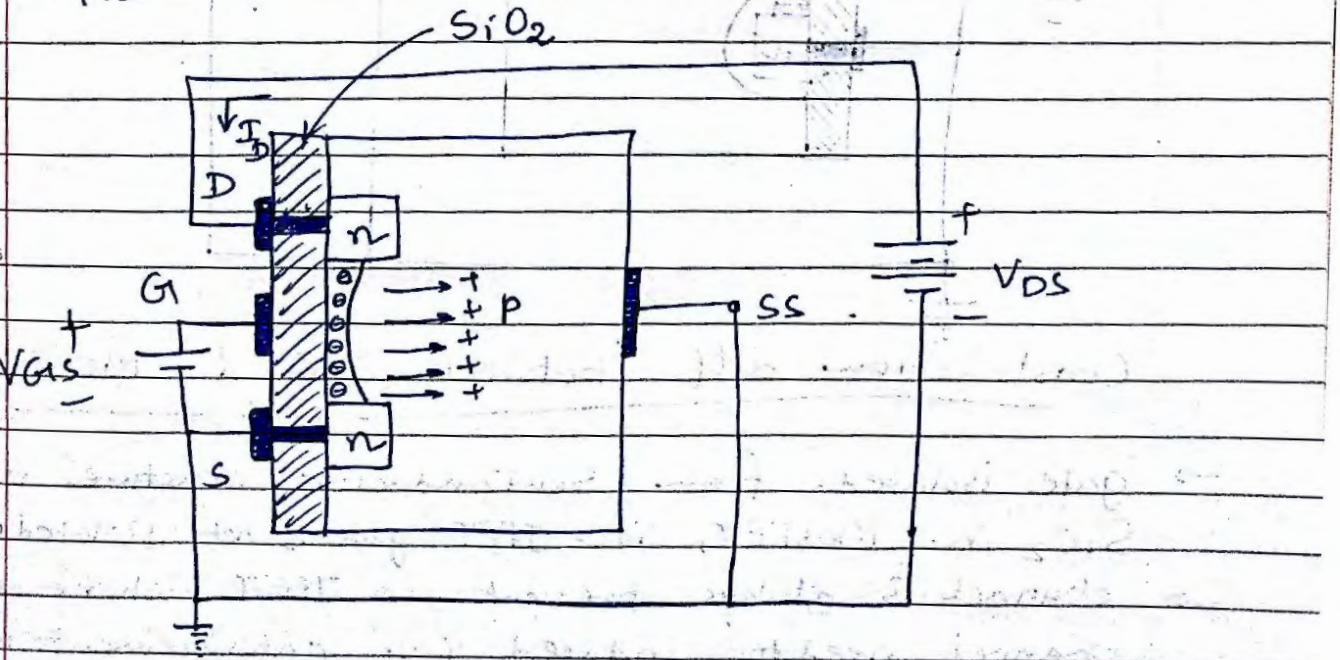
→ Due to applied voltage depletion region created at pn junction.

→ As V_{GS} ↑, electrons gathering near SiO_2 layer will increase, electron concentration at SiO_2 layer increased so, it creates an induced n-channel.

→ Then drain current starts flowing through induced channel.

→ Value of V_{GS} at which the conduction (of current) begins is called the Threshold voltage and it is indicated by V_t.

→ V_{tn} → for n-channel EMOSFET.



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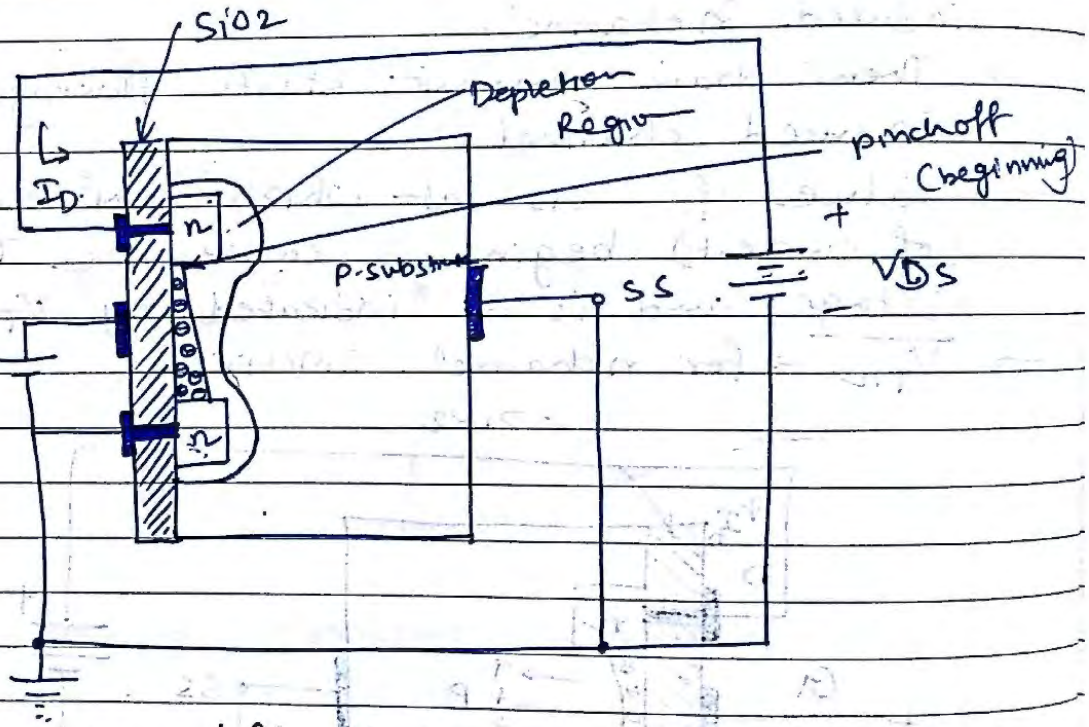
case. III Effect of increase in the drain to source voltage:

→ positive V_{GS} is kept constant & V_{DS} is increased gradually.

→ Due to this Gate terminal becomes less & less positive with respect to drain, so less number of electrons are attracted towards gate terminal & induced channel becomes narrow

→ channel width reduced near drain junction, at pinch off point channel width at drain becomes zero.



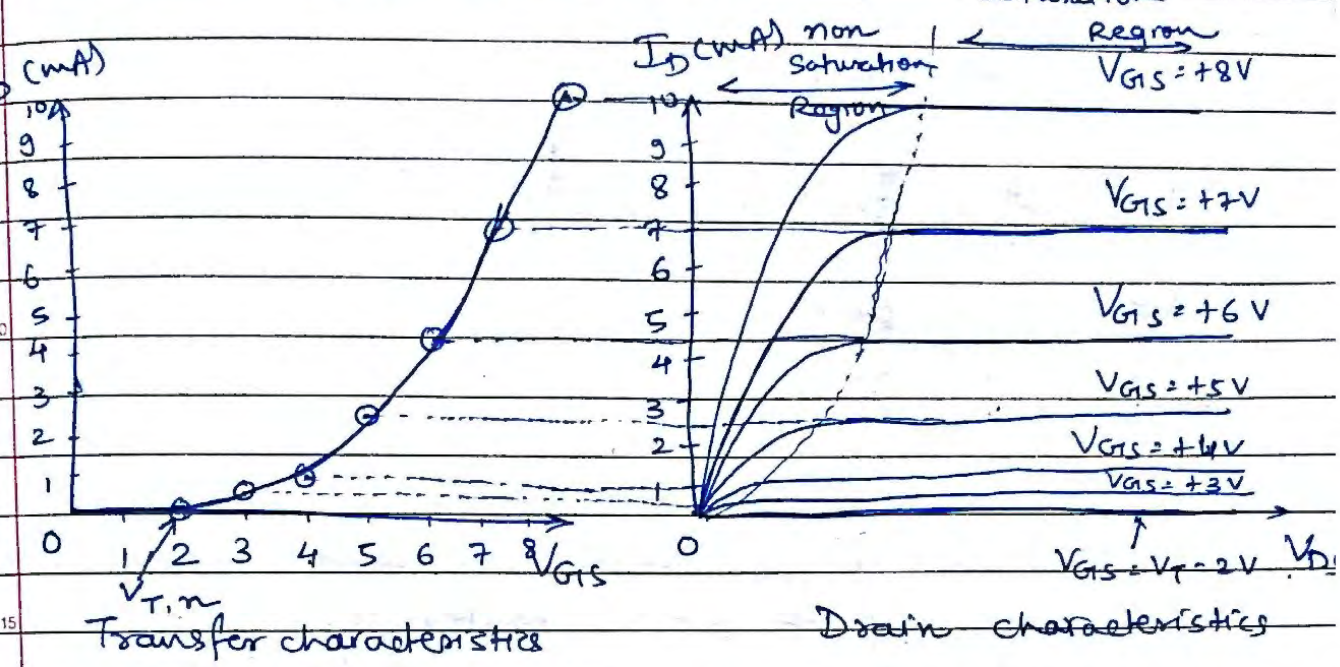
Construction diff. between JFET & MOSFET.

→ gate isolated from Semiconductor structure using SiO_2 in MOSFET, in JFET gate is not isolated in JFET

→ channel is always present in JFET, whereas channel need to induced in enhancement MOSFET.

Q. Draw & Explain characteristics of n-channel EMOSFET.

→ Drain characteristics & transfer characteristics of EMOSFET are as follows.



→ Drain current is 0 for $V_{GS} \leq V_{T,n}$ here $V_{T,n}$ is threshold voltage for n-channel EMOSFET.

→ In saturation region relation between I_D & V_{GS} is given by

$$I_D = K (V_{GS} - V_{T,n})^2$$

$$K = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)$$

$$K = \frac{K_n'}{2} \left(\frac{W}{L}\right) \quad \left(\text{here } K_n' = \mu_n C_{ox}\right)$$

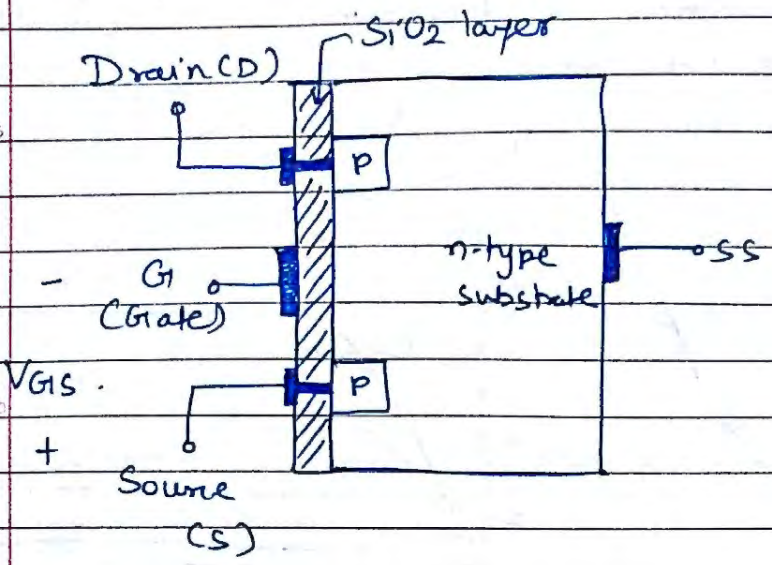
W = channel width

L = channel length

μ_n = mobility of electrons

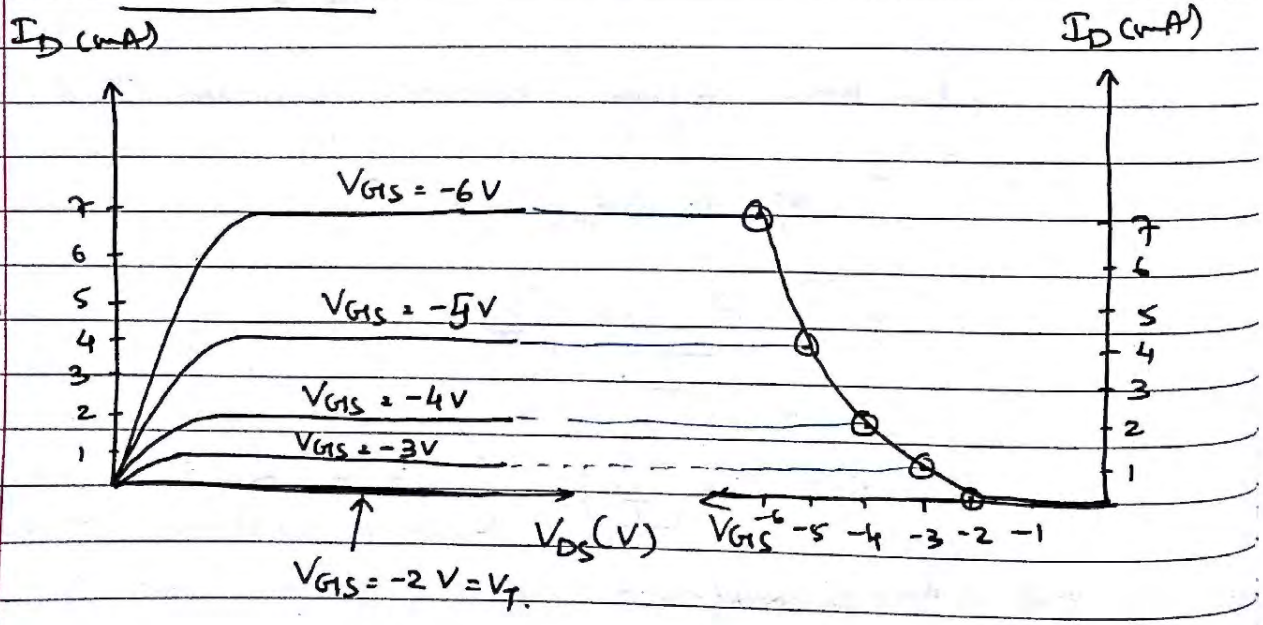
C_{ox} = oxide capacitance (metal oxide capacitance)

Q. Draw & explain construction & characteristics of p-channel EMOSFET.



→ here n-type substrate is used, drain & source is made up of p-type materials.
→ All voltage polarities & current directions are reversed.

Characteristics:



→ Threshold voltage i.e. V_{GS} at which channel forms & current starts flowing from Drain & Source terminals, is negative here, it is denoted with $V_{T,p}$ and value is $-2V$.

→ So drain current is zero upto $-2V$, if V_{GS} is more negative than $-2V$, the current starts, its shown in transfer characteristics.

→ current voltage relationship for non-saturation region is given by.

$$I_D = k_p\left(2(V_{GS} - V_{T,p})V_{DS} - V_{DS}^2\right)$$

here $k_p = \frac{k_p'}{2}\left(\frac{W}{L}\right) = \frac{\mu_p \cdot C_{ox}}{2}\left(\frac{W}{L}\right)$

→ current voltage Relation for saturation region is

$$I_D = k_p\left(V_{GS} - V_{T,p}\right)^2$$

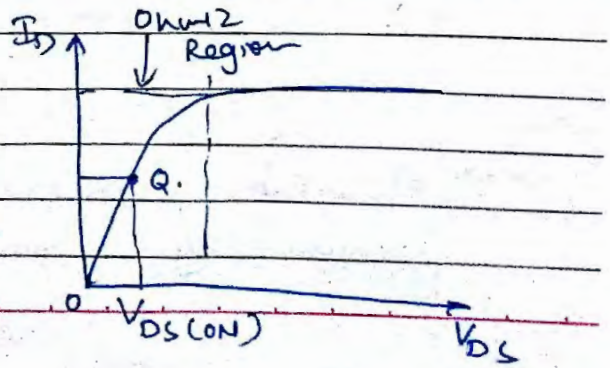
$$k_p = \frac{k_p'}{2}\left(\frac{W}{L}\right) = \frac{\mu_p \cdot C_{ox}}{2}\left(\frac{W}{L}\right)$$

→ Ohmic Region:

In ohmic Region, drain to source on state resistance is $R_{DS(ON)}$.

$$R_{DS(ON)} = \frac{V_{DS(ON)}}{I_{D(ON)}}$$

→ EMOSFET is equivalent to close switch.



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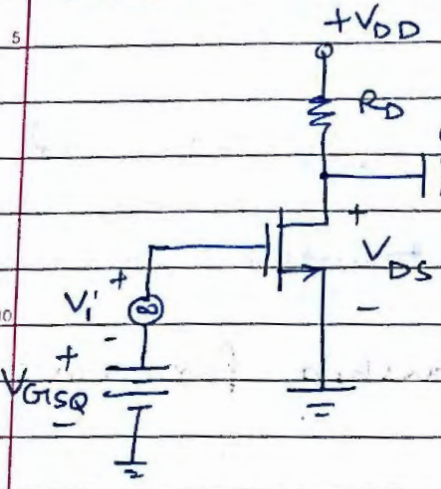
Q. Draw & explain EMOSFET Amplifier.

EMOSFET amplifier circuit diagram is given below.



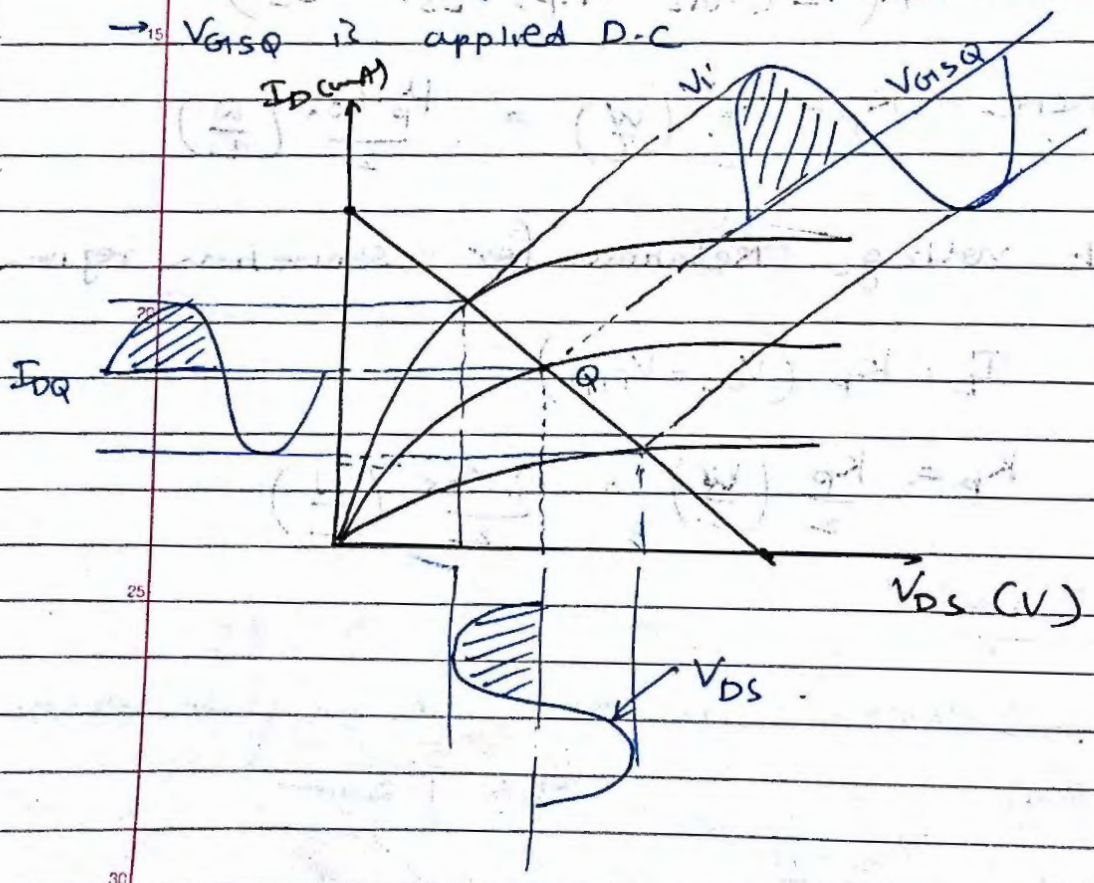
→ fig. shows common source amplifier using n-type EMOSFET.

n-type enhancement MOSFET.

→ here $V_{GS(th)}$ i.e. $V_{t,n}$ is +ve.

→ V_i is i/p signal to be amplified.

→ V_{GSQ} is applied D.C



→ During positive half cycle, V_{gs} changes sinusoidally above V_{GSQ}.

→ hence I_D changes sinusoidally above I_{DQ}.

$V_{DS} = V_{DD} - I_D R_D$

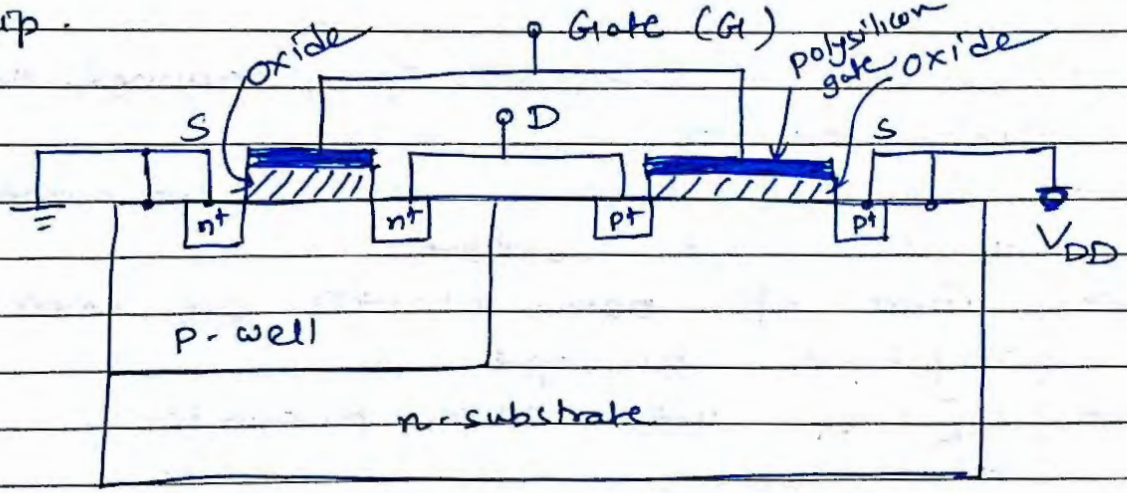
→ As I_D ↑, drop across R_D ↑ & so V_{DS} ↓

→ so, output V_{DS} is inverted. phase shift between i/p & o/p is 180°.

Q. Draw a schematic of CMOS digital switching circuit & explain its operation.

→ CMOS (complementary MOS) technology uses both n-channel & p-channel device in the same circuit.

→ Fig shows cross section diagram of n-channel & p-channel devices fabricated on the same chip.



→ n^+ is highly doped than n-substrate.

→ p^+ is having high doping than p-well.

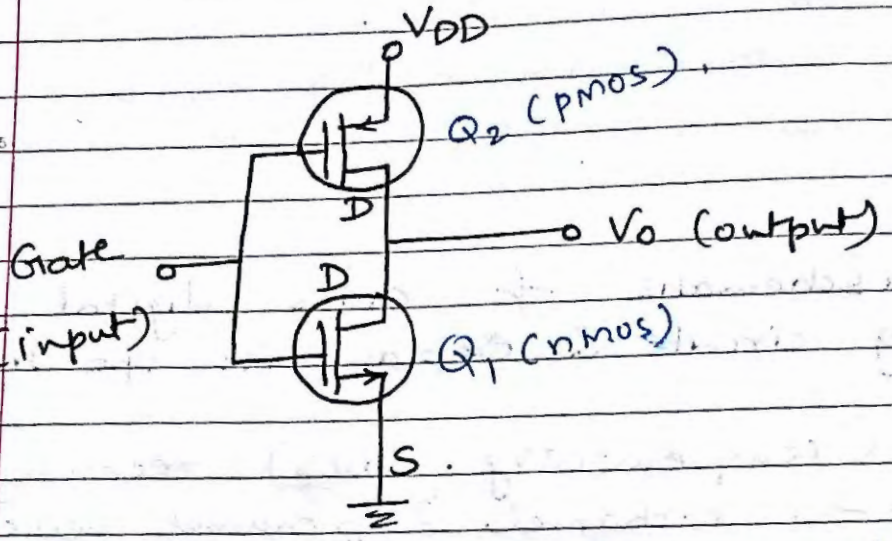
→ gate is made up of polysilicon material

→ Gate oxide is SiO_2.

→ Contacts are made up of metal.

→ CMOS has many advantages over only nMOS devices & pMOS devices.

CMOS Inverter Circuit (CMOS NOT) gate



→ Source & substrate of n-channel device is connected to ground., n-channel MOSFET is fabricated in p-well.

→ Source & substrate of p-channel device is connected to V_{DD}.

→ Drain of Both MOSFETs are connected together. i.e. output

→ Gate of both MOSFETs are connected together i.e. input.

→ k_n & V_{tn} are nMOS parameter

$V_{Tn} > 0$.

→ k_p & V_{tp} are pmos parameters

$V_{Tp} < 0$.

→ When $V_i = 0$, (log2. 0)

Q_1 · OFF , Q_2 · ON.

$V_{out} = V_{DD}$

i/p. log2. 0 & o/p. log2. 1.

→ when $V_i = V_{DD}$ (logic 1)

Q_1 - ON, Q_2 - OFF, $V_o = 0V$ (logic 0)

$V_i = V_{DD}$ (logic 1) → then V_o = (logic 0)

Waveforms.