CHAPTER - 6 - DIGITAL CIRCUITS.

→ Digital Electronics used in many applications such as

1. Television
2. Communication system
3. Radar, navigation
4. Military systems.
5. Medical
6. Industrial process control
7. consumer electronics.

→ Signals :

→ Analog signals : Analog signal is defined as signal having continuous values. They can have infinite number of different value.

Most of the quantities observed in nature are analog.

Ex. Temperature, Brightness, Sound.

Analog signals are continuous in time & value.

→ Digital Signals : Digital signal is defined as signal which has only finite number of distinct values.

Digital signals are discrete signal. (not continuous)

Digital signals are discrete in time & value

Ex. Binary signal can take 0 & 1 value.

Binary logic in Digital Circuit :

→ In Binary logic there are only two levels. 0 & 1.

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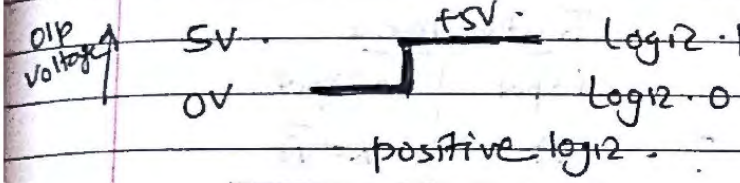
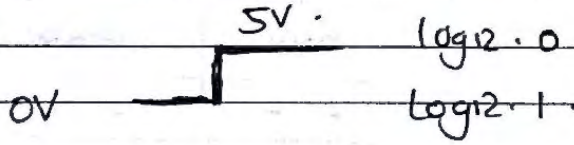
Positive logic:

Logic 0 (Low) = 0V
Logic 1 (High) = 5V



Negative logic:

Logic 0 (low) = +5V
logic 1 (High) = 0 V



Negative logic.

Logic Operators:

1) AND operator. A.B
2) OR operator A+B
3) NOT operator. $\bar{A}$ = NOT - A.

Logic Gates:

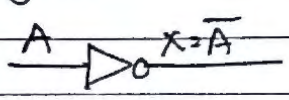
Logic Gates

- Basic Gates.
  - NOT
  - OR
  - AND
- Universal Gate
  - NAND
  - NOR
- Derived Gate
  - Ex-OR
  - Ex-NOR

Q. Draw symbol, truthtable & equation for NOT, AND, NAND, OR, NOR, EXOR & EXNOR Gates.

1) NOT.

Symbol.

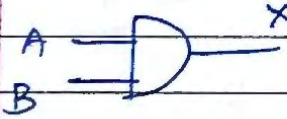


$X = \bar{A}$

Truth table

input	output
A	$X = \bar{A}$
0	1
1	0

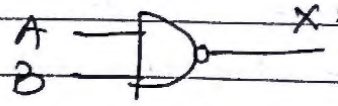
2) AND



Truth table

inputs		output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

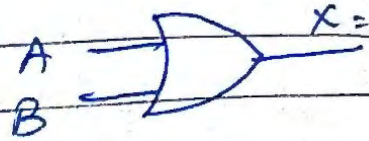
3) NAND



Truth table

inputs		output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

4) OR

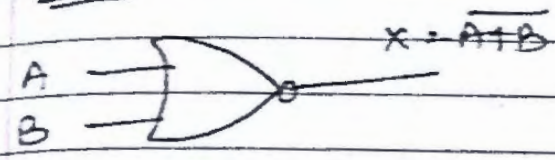


Truth table

inputs		output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

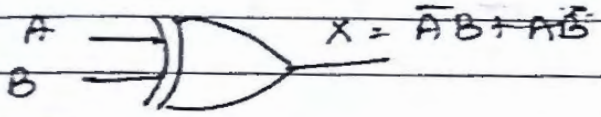
Truth table

5) NOR



inputs	output
A B	X
0 0	1
0 1	0
1 0	0
1 1	0

6) EXOR



Truth table

inputs	output
AB	X
0 0	0
0 1	1
1 0	1
1 1	0

7) EXNOR

$X = \bar{A}B + A\bar{B}$

OR

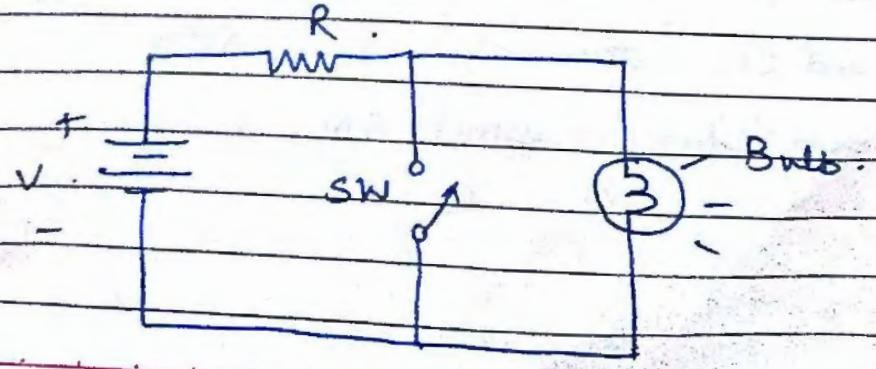
$X = AB + \bar{A}\bar{B}$

Truth table

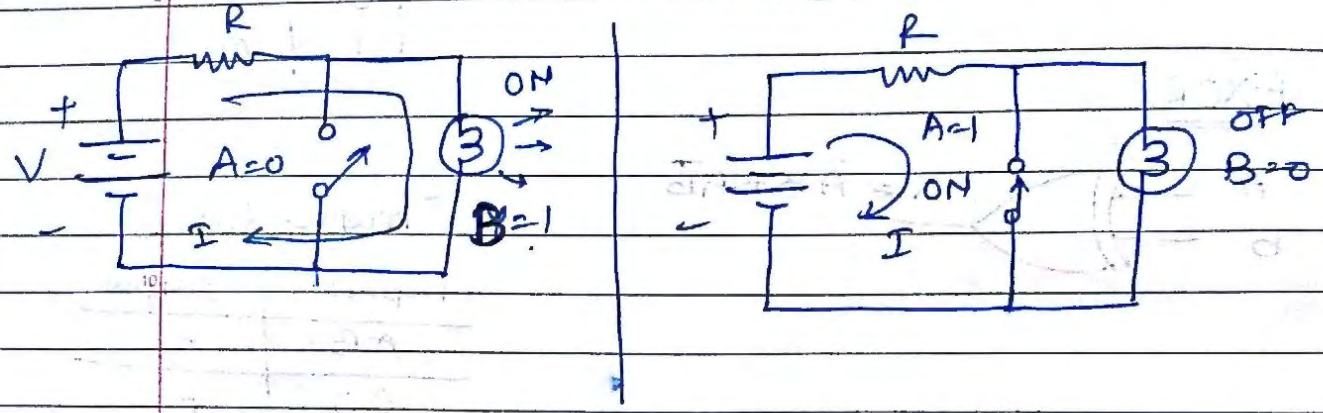
inputs	output
AB	X
0 0	1
0 1	0
1 0	0
1 1	1

Q. Implement NOT, AND & OR gates using switches.

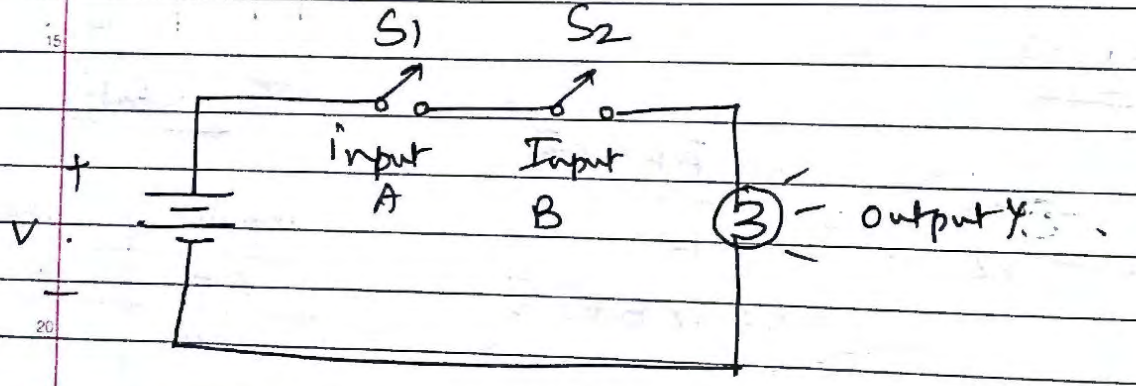
1) NOT.



Input Switch (A)	output Bulb (B)
open (0)	ON (1)
closed (1)	OFF (0)

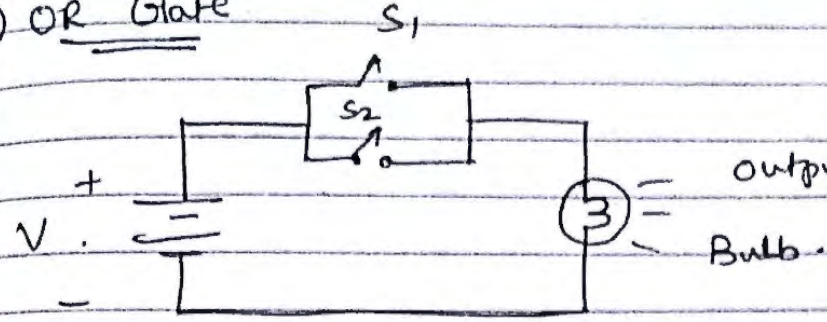


2) AND Gate:



Input A (S1)	Input B (S2)	output (Bulb) Y
open (0)	open (0)	OFF (0)
open (0)	closed (1)	OFF (0)
Closed (1)	open (0)	OFF (0)
Closed (1)	closed (1)	ON (1)

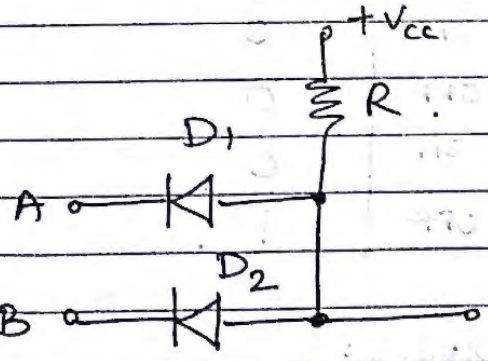
3) OR Gate



Input A S_1	Input B S_2	output Bulb (Y)
open (0)	open (0)	OFF (0)
open (0)	closed (1)	ON (1)
closed (1)	open (0)	ON (1)
closed (1)	closed (1)	ON (1)

Q. Implement AND & OR Gate using Diodes.

1) AND Gate Using diode:



Operation of Circuit :

1) When A = B = 0, D_1 & D_2 forward bias, so ON. (Here we consider ideal diode, drop across diode is 0) then Y = 0.

2) When A=0, B=1

→ D_1 is forward Bias (A=0)
→ D_2 is reversed Bias (B=1)

So, D_1=ON, D_2=OFF, Y=0.

3) When A=0, B=1.

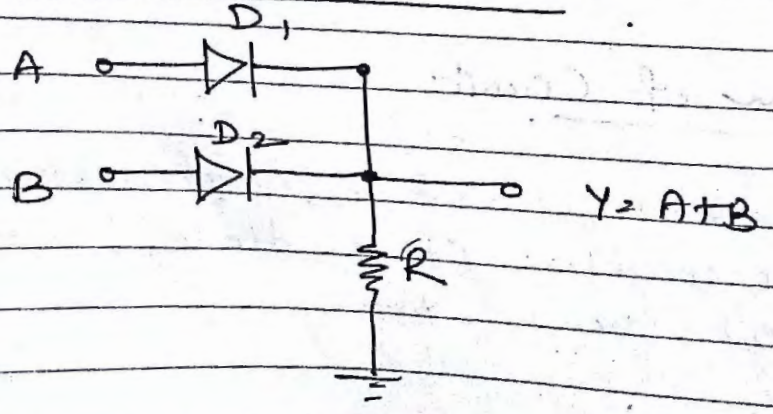
→ D_1→ON, D_2→OFF, Y=0.

4) When A=1, B=1.

→ Both diode OFF., so Y is connected to V_{cc} through R so, Y=1

Inputs		Diodes		Output (Y)
A	B	D_1	D_2	
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1

OR Gate Using Diodes:



→ When A = B = 0 :

→ Both diodes are reversed biased

→ So Y = 0 .

→ When A = 0 , B = 1 :

→ D_1 reversed Biased

→ D_2 Forward Biased .

So. Y = 1 (Here we consider ideal diodes).

→ When A = 1 , B = 0 .

→ D_1 . ON .

→ D_2 . OFF

& output Y = 1 .

→ When A = 1 , B = 1

→ Both diodes are forward Biased & Y = 1 .

Inputs		Diodes		Output
A	B	D_1	D_2	(Y)
0	0	OFF	OFF	0
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	1

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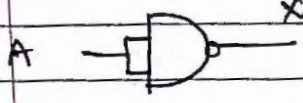
Q. Justify NAND & NOR gate as Universal gate.
OR
Why NAND & NOR gate is called Universal gate?

→ NAND & NOR gate is called universal gate as we can implement all basic gates using only NAND or only NOR gate.

NAND as Universal Gate:

→ NOT using NAND:



$X = \overline{A \cdot A}$

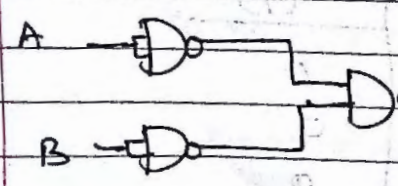
$= \bar{A}$

→ OR using NAND:

$X = A + B$

$= \overline{A+B}$

$X = \overline{\bar{A} \cdot \bar{B}}$ (Using Demorgan's theorem $\overline{A+B} = \bar{A} \cdot \bar{B}$)



$X = \overline{\bar{A} \cdot \bar{B}} = A + B$

→ AND Using NAND:

$X = A \cdot B$

$= \overline{\overline{A \cdot B}}$

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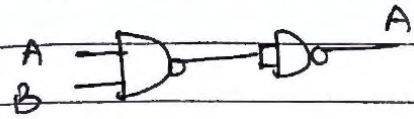
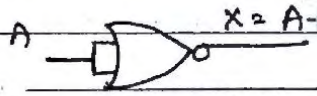
$\overline{\overline{A \cdot B}} = A \cdot B$



NOR as Universal Gate :-

→ NOT using NOR :-



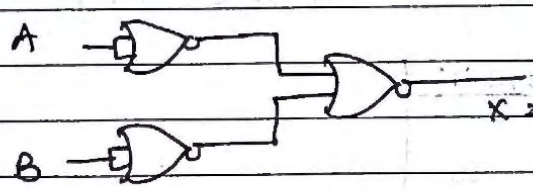
→ AND using NOR :

$X = A \cdot B$

$= \overline{\overline{A \cdot B}}$

$= \bar{A} + \bar{B}$ (using Demorgan's theorem)

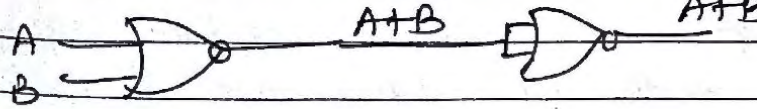
$\overline{A \cdot B} = \bar{A} + \bar{B}$



→ OR using NOR :

$X = A + B$

$= \overline{\overline{A + B}}$



Define:

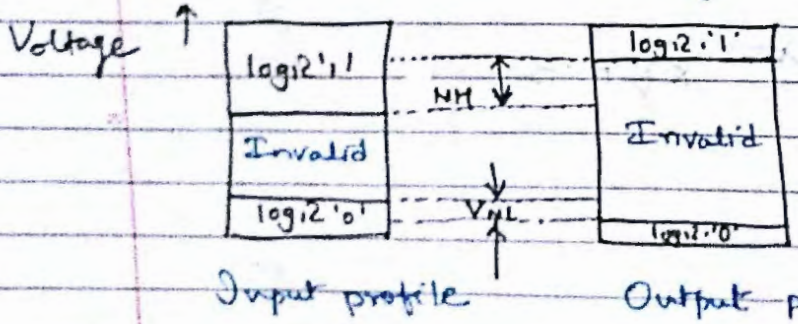
Fan-in: Number of inputs a gate has
Ex. 2 input gate has fan-in equal to 2.

Fan out: Maximum number of inputs of same IC family that gate can drive without falling outside the specified o/p voltage limit.

Ex. fan out is 5 means gate can drive at the most 5 inputs of the same IC family.

Noise Margin:

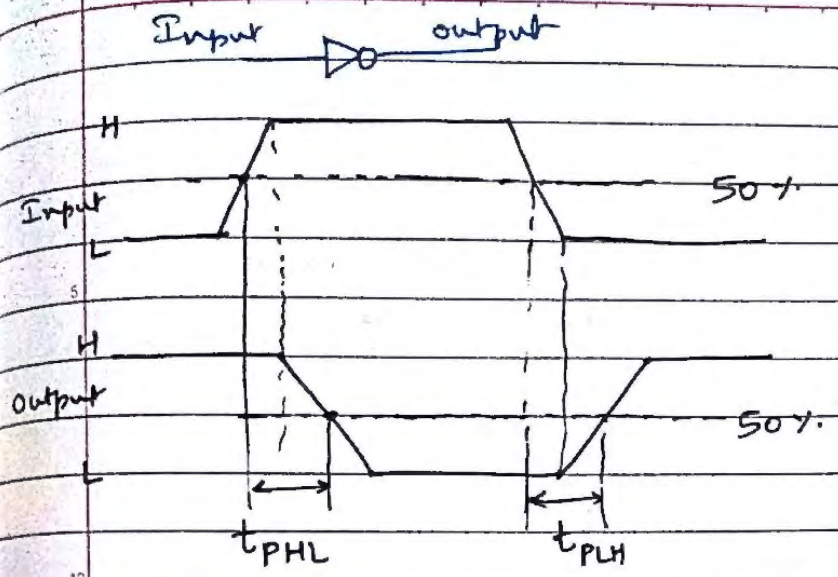
It is defined as ability of logic circuit to tolerate the noise without causing the output to change undesirably.



Propagation Delay:

→ The output of logic gate does not change its state instantaneously when state of its input is changed.

→ Time delay between the instant of application of an input pulse & instant of occurrence of the corresponding output pulse.



Power Dissipation:

→ Due to applied voltage & currents flowing through the logic ICs, some power will be dissipated in it in form of heat.

power drawn by IC from power supply.

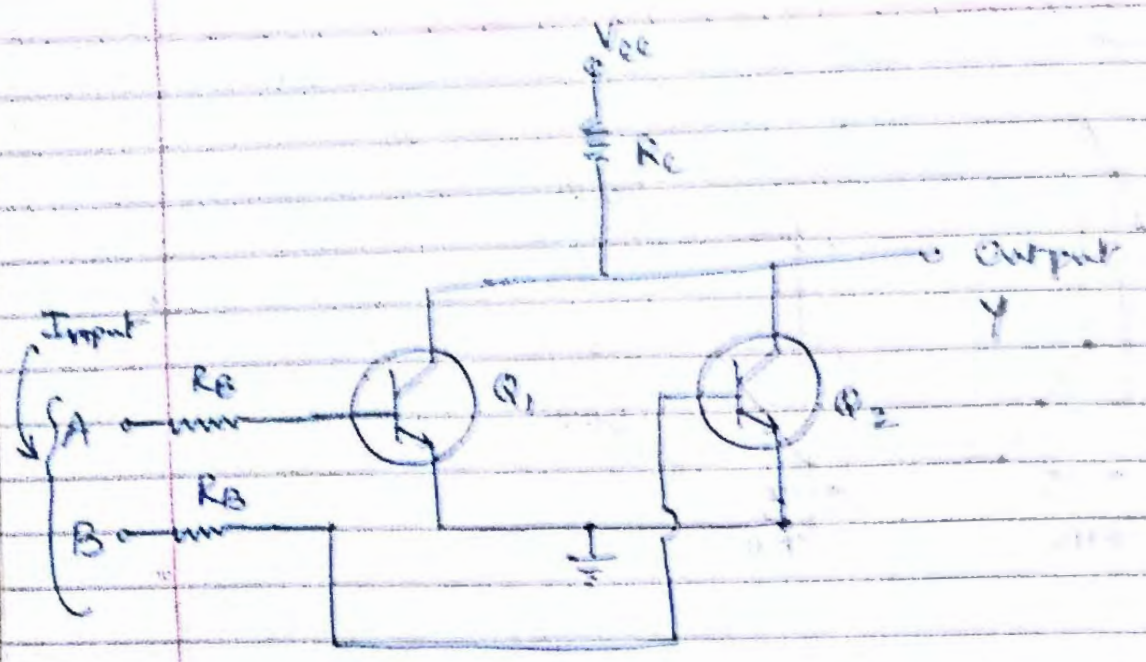
$$P = V_{CC} \times I_{CC}$$

Q. Implement NOR & NAND using Resistor transistor logic (RTL)

→ RTL is the earliest logic family but it has become obsolete now.

→ Full form of RTL is resistor, transistor logic which suggests that it uses resistors & transistors.

→ RTL circuits were first constructed using discrete components.



Truth table.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Operation:

Case: 1

→ A=B=0

→ Both transistor remain OFF

→ current through R_C is zero.

→ So drop across it is 0.

→ output voltage is equal to V_{CC}

Case. 2 A=0, B=1.

→ With A=0 & B=1 Q_1 is OFF & Q_2 ON.

So output voltage $V_{out} = V_{CE_2(sat)}$ i.e. 0

So. When A=0, B=1

Y=0

3. A=1, B=0

with A=1 & B=0, Q_1 is saturated & Q_2 OFF

So, Y=0 $Y = V_{CE(sat)}$.

4. A=1 & B=1

Both transistors saturated & Y=0.

Advantage: This uses minimum number of transistors.

Limitations:

- → High power dissipation
- → Its fan in is only 3
- → Low noises margin (0.4V)
- → Low fan out (only 3)
- → Low speed.

Characteristics of RTL

	Characteristics	Value
1.	Fan in	3
2.	Fan out	3
3.	Power dissipation	30 mW
4.	Propagation delay	12 ns
5.	Noise	0.4V

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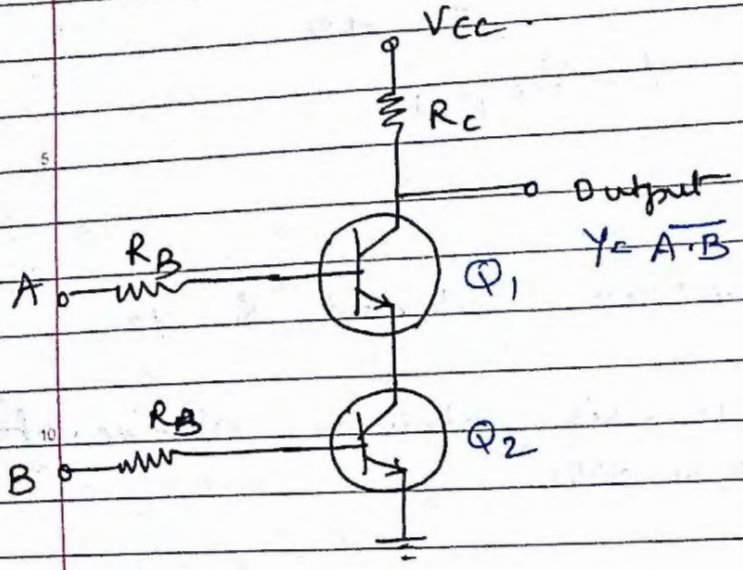
Q. Implement NAND Gate using RTL.



truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Operations:

case.1 A=B=0

→ both transistors Q_1 & Q_2 are in cut off, so output is connected to V_{CC}.

so, $\boxed{Y = 1}$

case.2 A=0, B=1

→ Here transistor Q_1 is in cut off & transistor Q_2, BE junction is forward biased.

→ As Q_1 is in cutoff output is connected to V_{CC}. $\boxed{Y=1}$

case.3 A=1, B=0

→ In transistor Q_1, BE junction forward biased

→ Q_2 is in cutoff

→ Output is connected to V_{CC}.

so, $\boxed{Y = 1}$

case.4 A=1, B=1

→ here transistors Q_1 & Q_2 both saturated

$\boxed{Y=0}$

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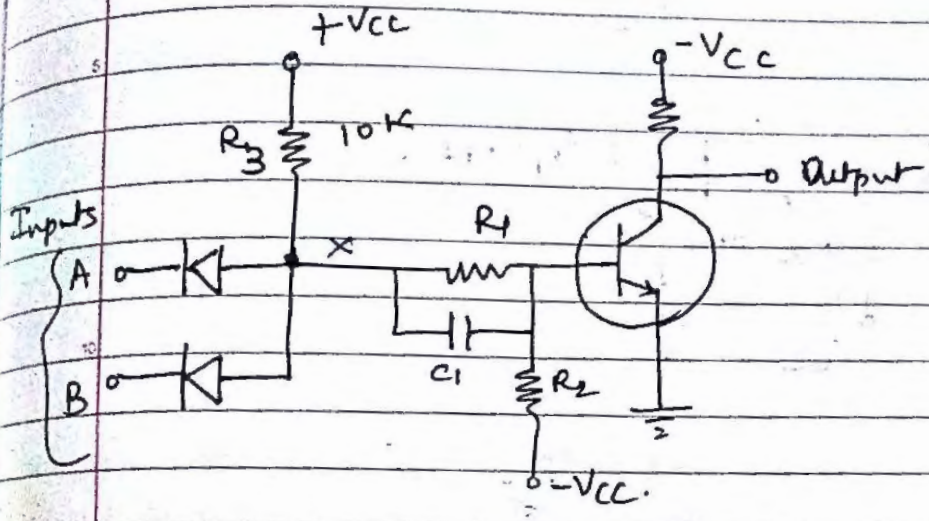
Q. Implement NAND using DTL.

→ DTL Stands for diode transistor Logic

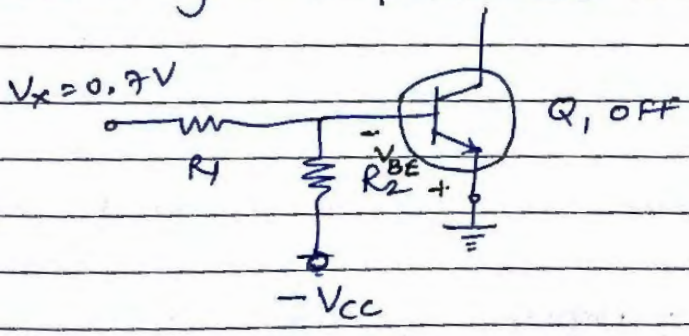


Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

1. Operation with AB=00, 01 or 10

when AB=00, both the diodes D_1 & D_2 are conducting. so potential at X is 0.7V.



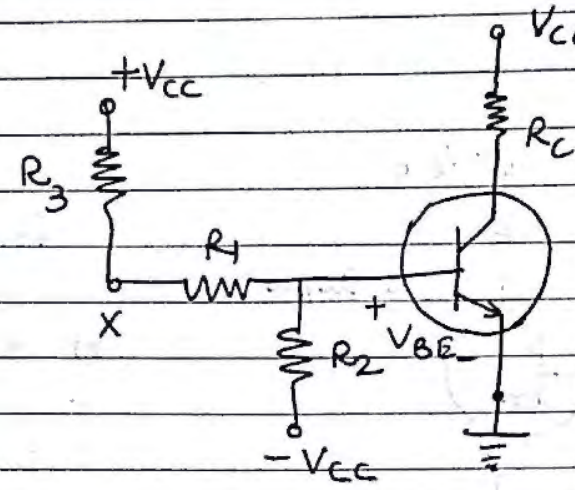
→ when V_x = 0.7V Base of emitter is -ve as shown in circuit above, so, V_{BE} is -ve & transistor BE junction Reverse biased. So output is 1 (High).

Thus when AB=00/01/10, output Y=1

2. Operation with AB=11

→ When AB=11, both D_1 & D_2 are reversed biased and acts as open circuit,

Equivalent Circuit is



→ As both Diodes are off V_x is much higher than $V_x = 0.7V$, so Base of Q_1 transistor will be positive & BE junction will get forward biased in Q_1. So, output Y=0.

Thus when AB=11, Y=0

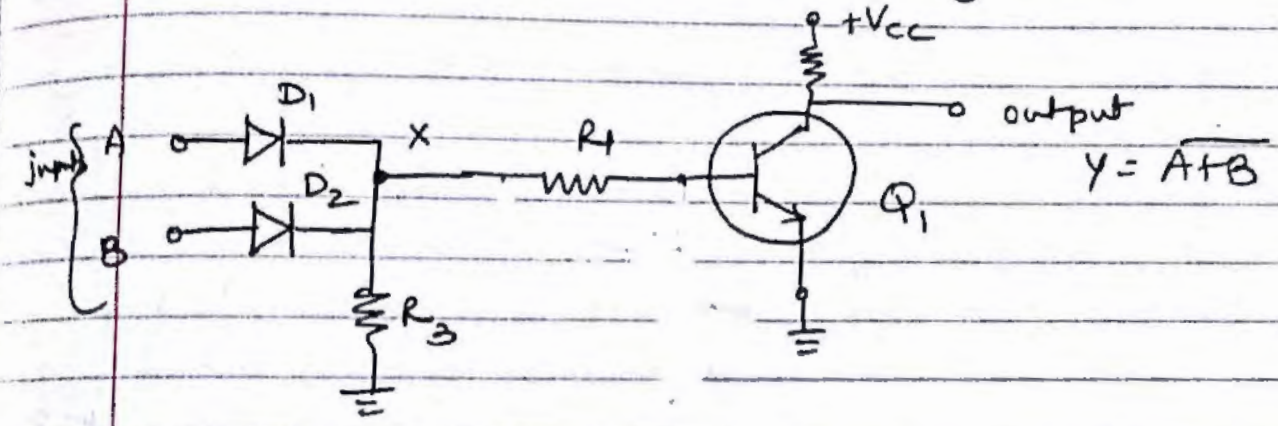
Advantages:

→ Greater fan-out is possible. (due to high input impedance)
→ Higher noise margin than RTL.
→ use of diode than Capacitor & resistors make DTL circuit more economical in IC form.

Sr. No.	Characteristics	Value
1.	Voltage levels	$V_{OH} = 5V$
		$V_{OL} = 0.2V$
		$V_{IH} = 1.5V$
		$V_{IL} = 1.4V$
2.	fanout	45

3.	Power dissipation	10mW
4.	Propagation delay	75ns
5.	Noise margin	0.7V

Q. Implement NOR Gate using DTL.



Truth table

AB	Y
0 0	1
0 1	0
1 0	0
1 1	0

Case:1 operation with A=0=B=0.

→ Voltage at Node X is denoted by V_x.

→ When A=0 & B=0

→ both diodes are reverse biased and $V_x = 0$ as node X is connected to ground through R_3.

→ So voltage at base of transistor is 0 & so, base to emitter junction is reverse biased so in cutoff.

→ So, **Y=1**

Case.2 A=0, B=1
A=1, B=0
A=1, B=1

→ When A=0 & B=1 diode D_2 is ON (forward biased) and V_x = high voltage
→ When A=1, B=0 diode D_1 is ON, & V_x is high voltage
→ When A=1, B=1, both D_1 & D_2 ON & V_x is high voltage.
→ So Base of transistor Q_1 is connected to high voltage, so BE junction is forward biased & current flows through transistor, so Output y=0.

TTL family:

→ Long form of TTL is transistor logic.
→ In TTL only transistors are used as their basic building block.

TTL characteristics

→ Texas Instruments first introduced two TTL series — 54 series & 74 series.

	TTL Series	Supply voltage Rating	Temparature Range
1.	74 series	4.75V to 5.25V	0°C to 70°C
2.	54 series	4.5V to 5.5V	−55°C to 125°C

Important Parameters for TTL

Sr. No	Parameters	Values
1.	Supply voltage	(74 series – 4.75 to 5.25 V 54 series – 4.5 to 5.5 V)
2.	temparatures	(74 series – 0 to 70°C 54 series – −55°C to 125°C)
3.	Voltage levels	$V_{IL(max)} = 0.8V$ $V_{OL(max)} = 0.4V$ $V_{IH(min)} = 2V$ $V_{OH(min)} = 2.4V$.
4.	Noise margin	0.4V
5.	Power dissipation	10 mW
6.	Propagation delay	10 n s.
7.	Fan out	10
8.	Fan in	100

Advantages of TTL

→ TTL circuits are fast
→ Low propagation delay
→ Power dissipation is not dependent on frequency.
→ Compatible to all other families
→ High current sourcing & sinking capabilities.

CMOS Logic:

→ CMOS Logic stands for complementary MOSFET.

CMOS characteristics.

Sr. No	Parameters	CMOS
1.	V_{IH} (min.)	3.5V (V_{DD} = 5V)
2.	V_{IL} (max)	1.5V
3.	V_{OH} (min)	4.95V
4.	V_{OL} (max)	0.05V
5.	High level Noise margin	V_{NH} = 1.45V
6.	Low level Noise margin	V_{NL} = 1.45V
7.	Noise immunity	Better than TTL
8.	Propagation delay	105ns (Metal gate CMOS)
9.	Switching speed	less than TTL
10.	Power dissipation	P_D = 0.1mW
11	Fan out - 50.	
12.	Power supply	3V to 15V.