

3. Implement the function F= \(\Sigma(13.7.11.15)\) with don't care conditions of \(\Sigma(0.2.15)\). Discuss the effect of don't caxe conditions.

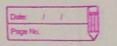
 $\Rightarrow F = \sum (1317.11.15)$ d= E(0,2,5)

F = A'D + CD

The "Don't care" conditions allows us to replace the empty cell of a k-map to form a grouping of the variables which is larger than that of forming groups without don't care

While toxming groups of cells, we consider a "Don't Caxe" cell as 1 or 0 or we can also ignore that cell.

Therefore, the "On & case" condition can help us to form a larger group of cells.



4. Find the complement of the foollowing Boolean function and reduce to a minimum number of literals.

B'D + A'BC' + ACD + A'BC

=> FB'D + A'BC' + ACD + A'BC

F' = (B'D + A'BC' + ACD + A'BC) = (B'D) (A'BC') (ACD) (A'BC)

= (B+D')(A+B'+c)(A'+C'+D')(A+B'+C')

= (AA' + B+CC'+ D')(A+B'+C+DD')(A'+BB'+C'+D')

(A+B+C+00')

= (A+B+C+D')(A+B+C'+D')(A+B'+C+D)(A+B'+C+D')

(A'+B+('+0') (A'+B'+C'+D') (A+B'+C'+D) (A+B'+C'+D')

= (A+B+C+D')(A+B+C+D')(A+B+C+D)(A+B+C+D') (A'+B'+C'+D)(A+B'+C'+D)

5. Obtain the simplified expressions in sum of

products using k-map:

x'z + w'xy' + w(x'y + xy')

 \Rightarrow F = x'z + w'xy' + w(x'y + xy')

= x'z(w+w')(y+y') + w'xy'(z+z') + wx'y +they wxy'

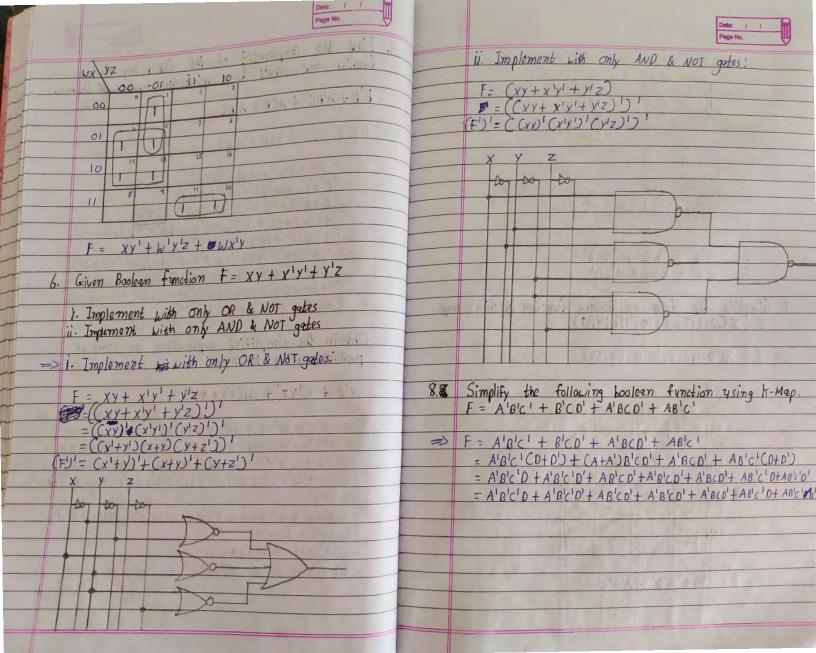
=WX'YZ + W'X'Y'Z + W'XY'Z + W'XY'Z' + WX'Y(Z+Z')+WXY(Z+Z). = Wx'yz + W'x'y'z + W'xy'z + W'xy'z' + Wx'yz + Wx'yz' + 6xx'z+

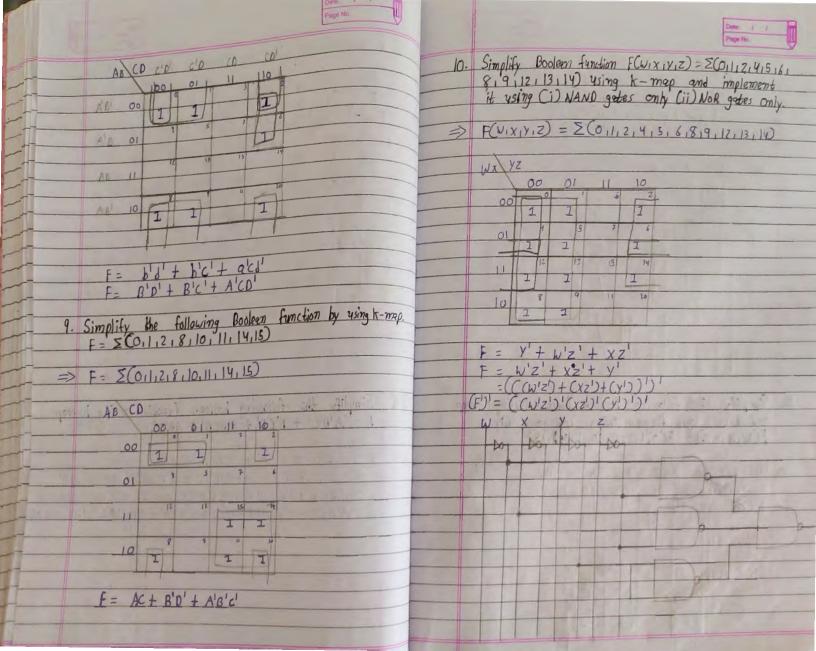
= Wx'yz + Ux'y'z+ W'xy'z+ w'xy'z+ &Wx'yz'+

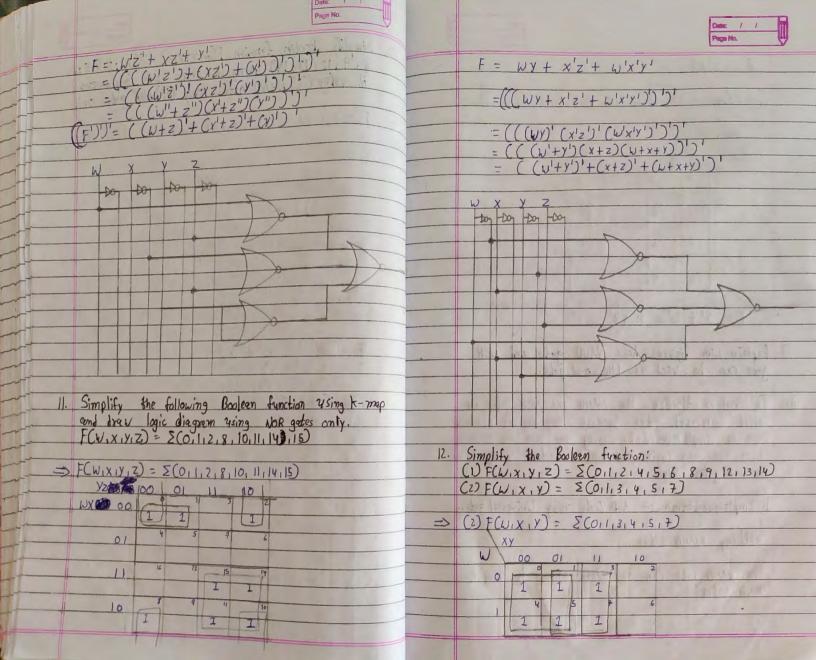
Wxy'z + Wxy'z'

= 5(11,1,5,4,10,13,12)

= S (1,4,5,10,11,12,13)



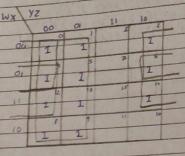






F= x1+x

(1) F(U,X,Y,Z)= E(0,1,Z,4,5,6,8,9,1Z,13,14)



F = y' + w'z' + xz'

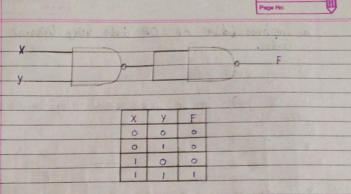
13. Explain hith figures how NAND gate and NOR gate can be used as Universal gate.

Ans In Boolean Algebra, the NAND and NOR gates are called universal gates because any digital circuit can be implemented by using any one of these two i.e. any lagic gate can be exected using NAND or NOR gates only.

1. Implementation of AND Gate using Universal gates.

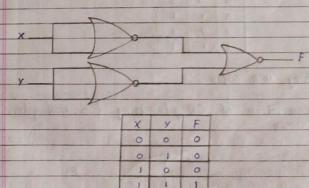
2) Using NAND Gates

The MAND gate can be implemented by using two



b) Using NOR Gates

Implementation of AND gate using only NOR gates.



| iii. Implementation | of | NOT | Gate | using | Universal |
|---------------------|----|-----|------|-------|-----------|
| gates. | | | - | - | - |

a) Using NAND artes

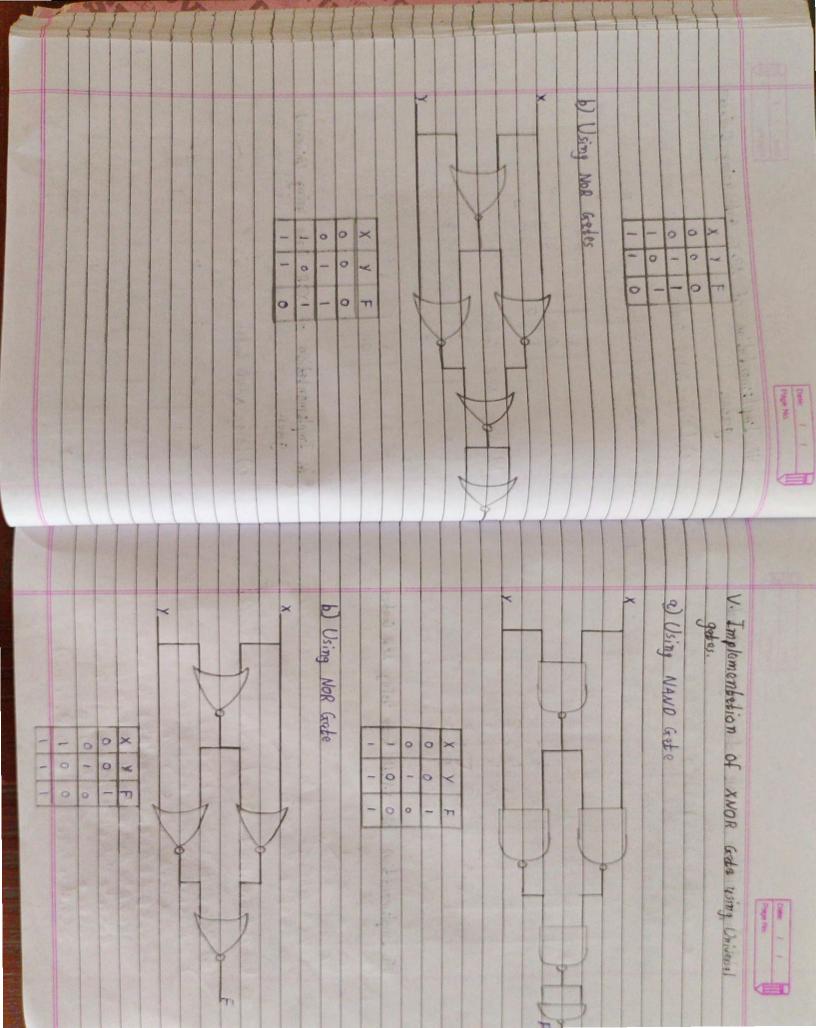
| Ī | X | F | 1 |
|---|---|---|---|
| - | 0 | 1 | |
| | 1 | 0 | |

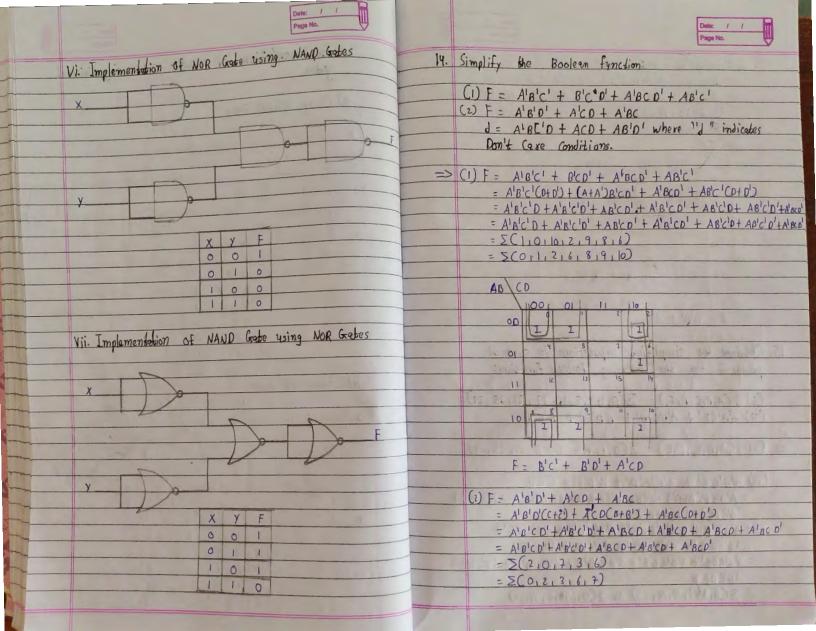
b) Using NOR Gates

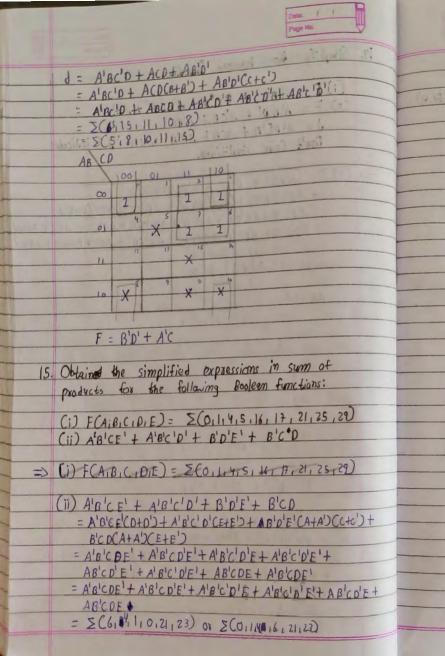
| - | | |
|---|---|--|
| X | F | |
| 0 | 1 | |

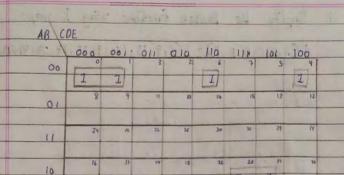
iv. Implementation of XOR Gate using Universal gates.

a) Using NAND Gates

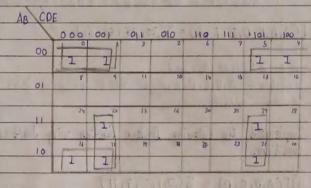








F = A'B'C'D' + A'B'CE' + AB'CE



F = B'C'D' + A'B'D' + A'D'E .

000A4 2/8 4 0/8 4.1.0 10/2/A/ 200 A 2/1

