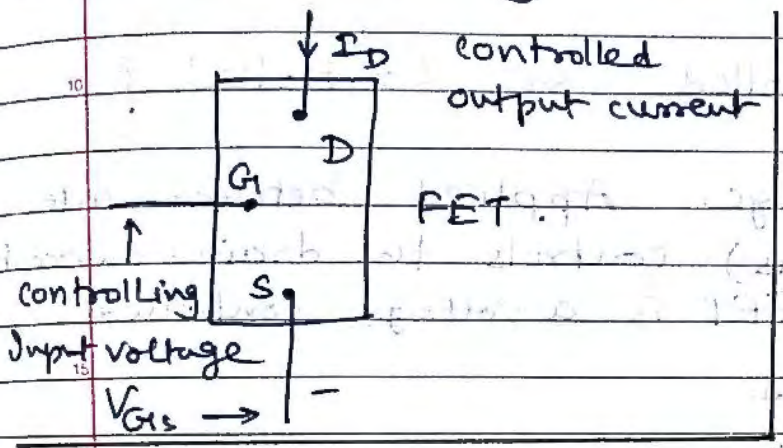
CHAPTER - 5

FET and Jt's Biasing.

→ Field Effect transistor (FET) is a three terminal Device.

→ Three terminals are a drain (D), source (S) and the Gate (G.) out of these Gate as a controlling terminals.



→ Input Impedance of FET is very high.

→ FET is voltage controlled device.

→ FET is unipolar device, that means the current flowing through it is only due to one type of charge particles, holes or electrons.

→ If conduction takes place due to electrons then it is called n-channel FET.

→ If conduction takes place due to holes then it is called p-channel FET.

→ FET are more temperature stable as compaire to BJT.

FET are classified as follows:

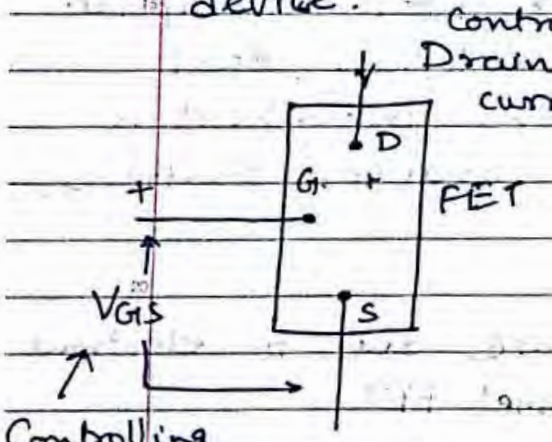
1. Junction field effect transistor (JFET)
2. Metal oxide semiconductor field Effect transistor. (MOSFET)

Field Effect Transistors (FETs)

- Junction FET (JFET)
  - n-channel JFET
  - p-channel JFET.
- MOSFETs
  - Depletion MOSFET
  - Enhancement MOSFET.

Voltage Controlled or Controlled ?

→ In FET voltage Applied between gate and source (V_{GS}) controls the drain current I_D. Therefore FET is a voltage controlled device.

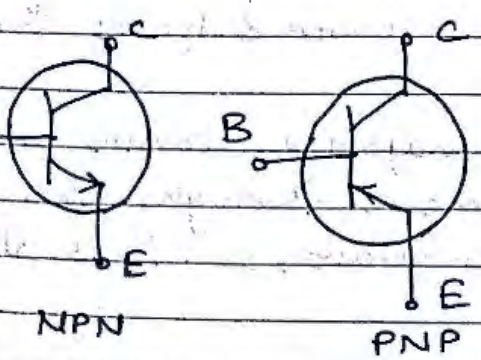
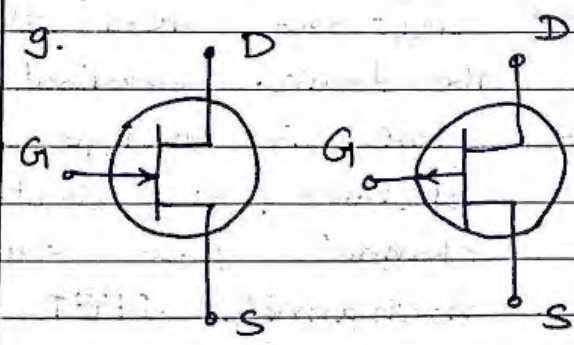


→ In transistor (BJT) output current I_c is controlled by varing the base current I_B.

Field Effect:

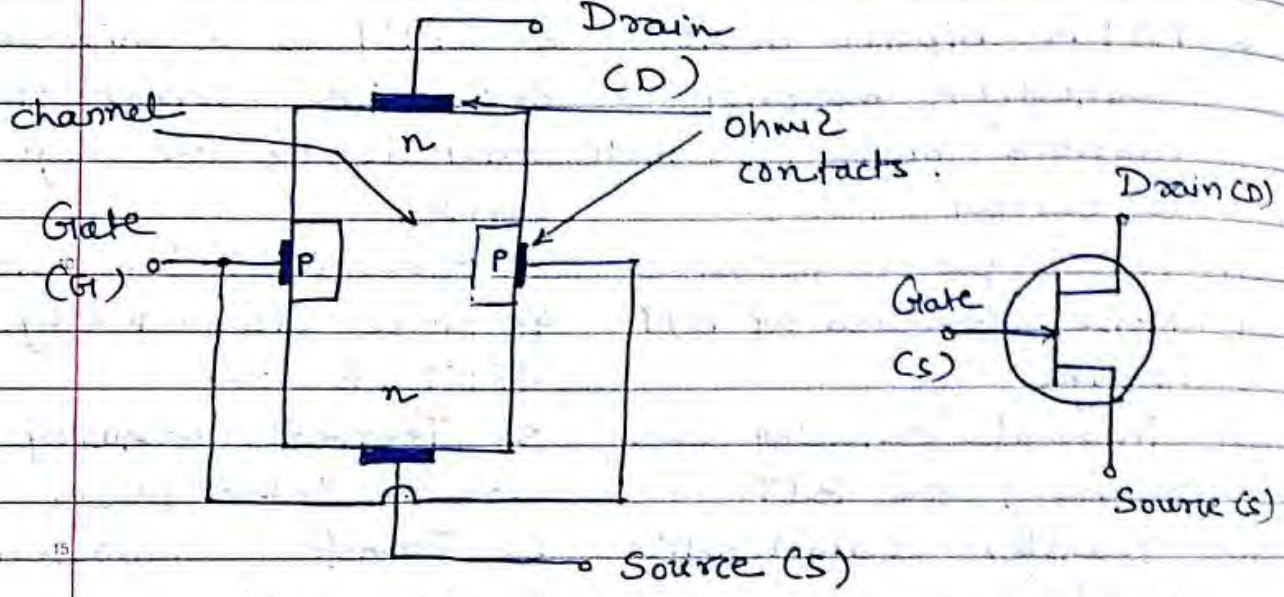
→ current flow in FET is controlled by an electric field created by an external voltage. Depletion regions set around the p. regions are controlled by negative gate voltage to control the drain current. This is called as the field Effect.

Q. Give Difference between BJT & JFET.

	BJT.	JFET.
1.	BJT is current controlled device.	It is a voltage controlled device.
2.	BJT is bipolar device (minority & majority carriers both contribute to current flow).	JFET is a unipolar device i.e. current flows only due to the majority carriers.
3.	Low Input Impedance.	High input Impedance.
4.	Noise Generated by BJT is high.	Noise Generated by JFET is low.
5.	Thermal runaway can damage the BJT.	Thermal runaway doesn't take place.
6.	Transfer characteristics is linear.	Transfer characteristics is nonlinear.
7.	Voltage gain of transistor amplifiers is much higher than that of JFET amplifiers.	Voltage Gain of JFET amplifier is less than that of BJT amplifier.
8.	BJT is bigger in size JFET.	JFET is smaller in size than BJT.
9.		
10.	Useful regions of operation: Saturation & cutoff for switching applications, active region for amplification.	Useful regions of operation: ohmic & cutoff for the switching applications & Sat. for amplification.

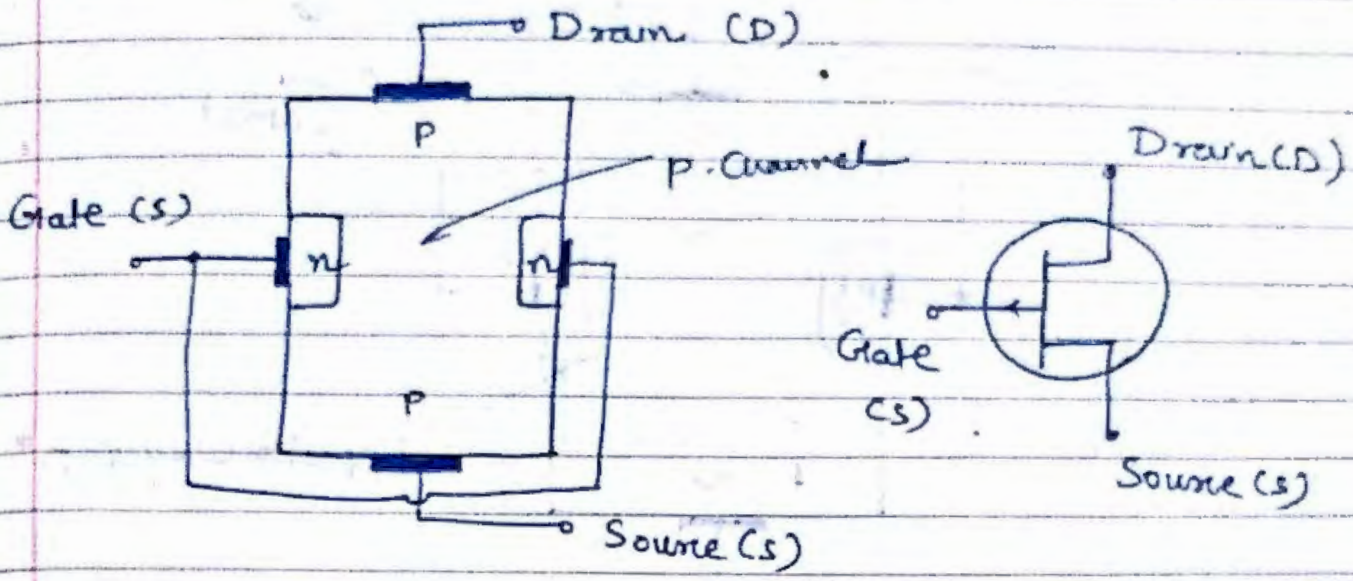
Q. Give structure (construction) of n-channel JFET & p-channel JFET.

Structure of n-channel JFET:



→ p type regions are heavily doped. (Gate)
→ between two gate regions n-type material is channel.
→ Supply voltage is connected between drain & source terminals, so current flows along length of n-type bar.
→ electron enters through source & leaves through the drain terminal.
→ Here in n-type bar majority carries are electrons, so electron move through this channel from source to drain, so it is called n-channel JFET.

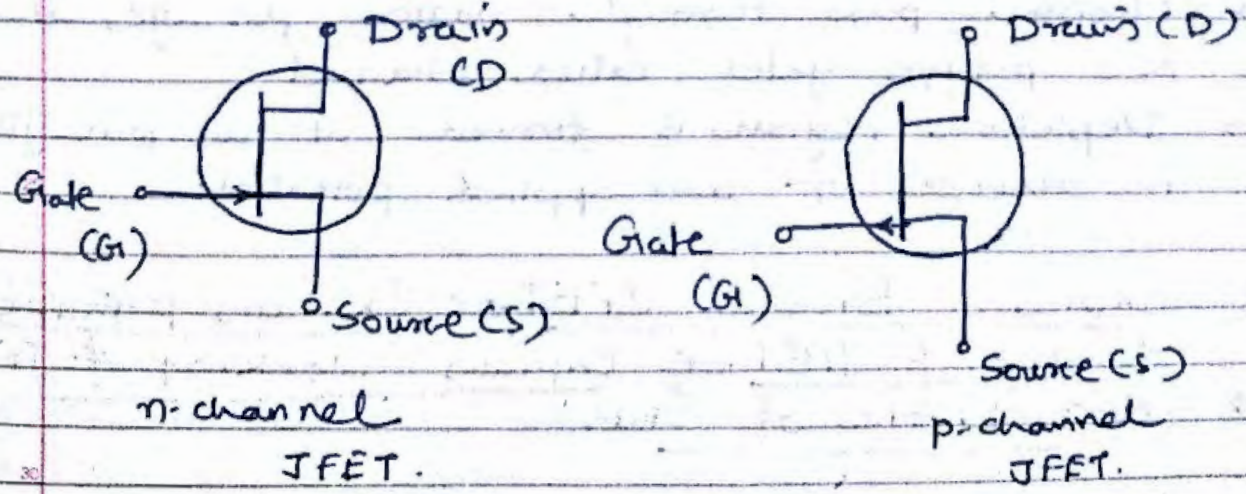
Structure of p-channel JFET.



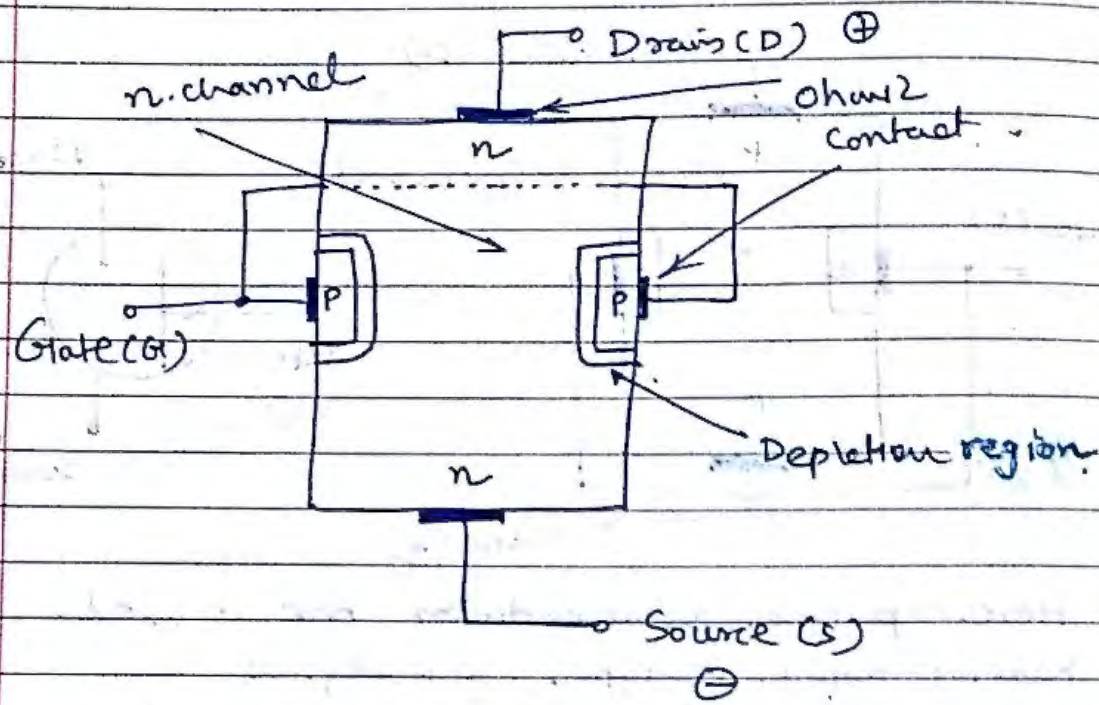
→ Here p-type semiconductor bar is used.
→ heavily doped n-type gate regions.
→ Here current flows due to holes, as holes are majority charge carries in p-type material.

OFFSET Gate Symbol.

→ offset Gate symbol points to source terminal of device in symbol itself.



Q. Explain Unbiased JFET.



→ When control terminal gate B open, how FET will operated?

→ positive supply V_{DS} is connected between drain & source.

→ Electron starts movement from source to drain.

→ This constitute I_D.

→ Electron pass through narrow passage between two p-type gates, called channel.

→ Depletion region is formed at two p-n junction in absence of any applied potential.

Q Explain Biased JFET or Explain principle of operation of JFET or explain working of JFET.

→ Reverse bias of Gate:

→ Gate to source junction is always reverse biased for operation of JFET.

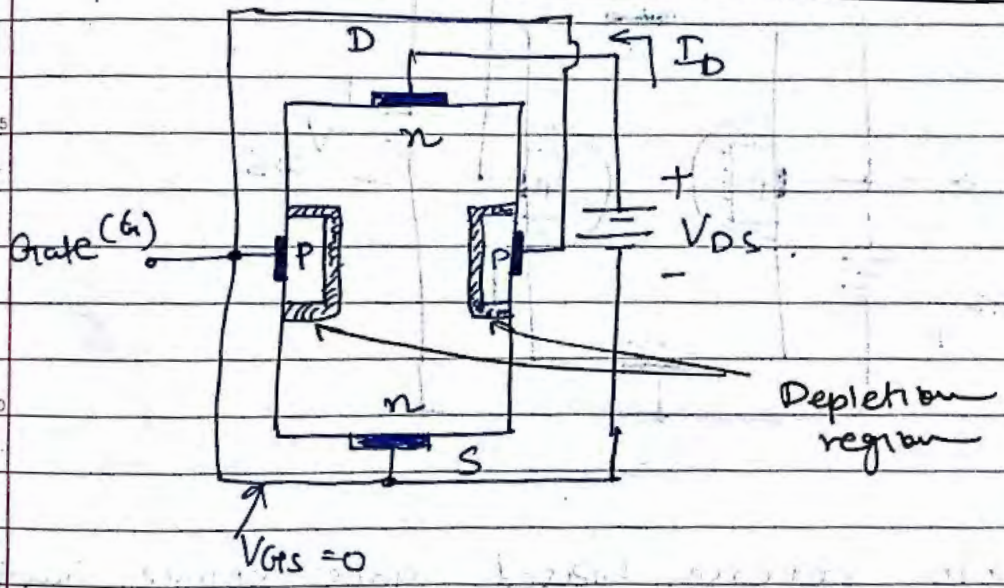
→ Due to this V_{GS} negative (Reverse biased) I_G is approximately zero.

→ Zero input current I_G gives almost infinite input resistance. so Input resistance of FET is very high.

→ practical value of input resistance is hundreds of MΩ.

→ Voltage applied between drain & source terminals of JFET is positive. (i.e. V_{DS} is +ve & V_{GS} is -ve).

1) Operation of n-channel JFET with $V_{GS}=0$.



→ As $V_{GS}=0$.

→ Due to supply voltage V_{DS}, current starts flowing through the channel. I_D is controlled by the resistance of semiconductor material between drain & source.

→ n-type material has finite resistance, so there is a voltage drop along the channel.

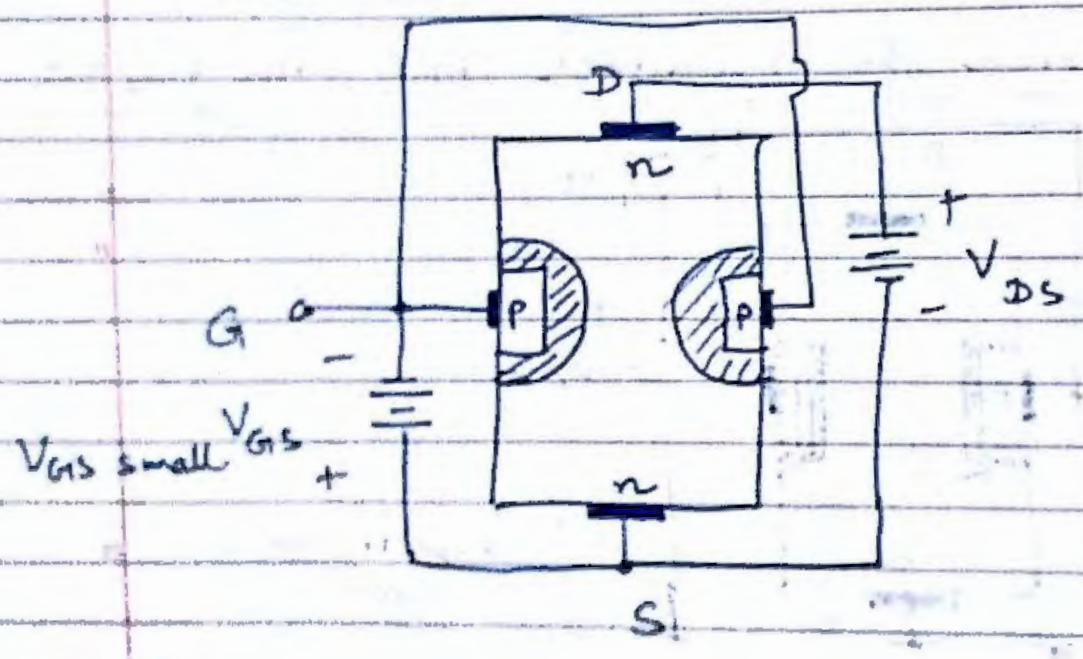
→ This voltage drop reverse bias gate to source pn junction. Depletion region of reverse biased pn junction more penetrated in n type material

as p-type material is heavily doped.

→ Due to depletion region width of channel is reduced.

→ when $V_{GS} = 0$, value of drain current is maximum because channel is widest. This drain current is refered as source saturation current I_{DSS}.

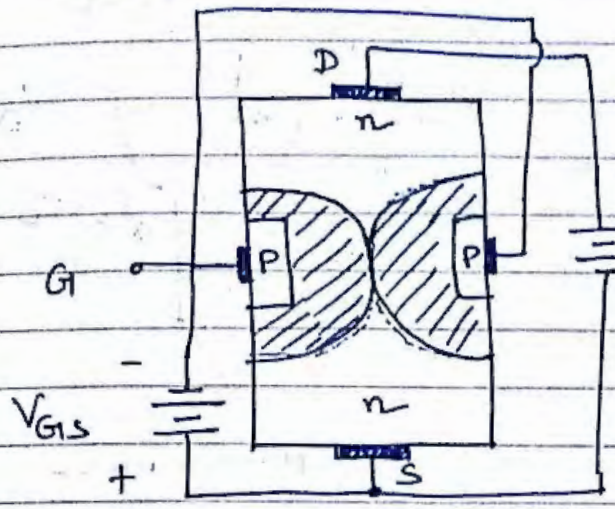
2. Operation of n-channel JFET with small negative V_{GS}



→ Due to reverse biased gate source junction depletion region width increases, and it penetrate more in n-type region.

→ This will reduce channel width, so less number of electrons can pass from source to drain, I_D reduces.

3. Operation of n-channel JFET for large value of negative V_{GS}:



→ As V_{GS} is further increased (negative), depletion region spread more into n-type region.

→ At certain V_{GS}, depletion regions of both p.n. junction touches each other as shown in figure.

→ At this point channel width is zero, and therefore $I_D = 0$, V_{GS} at which I_D is cutoff is called $V_{GS(off)}$

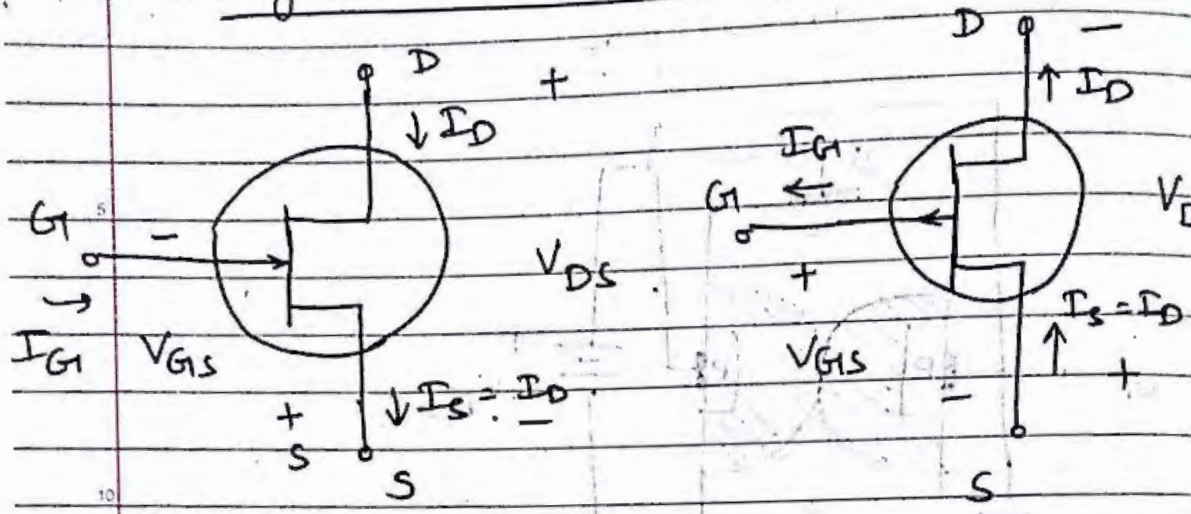
→ When $V_{GS} = 0$, drain current is I_{DSS} (maximum saturation)

→ when $V_{GS(off)}$ (maximum negative voltage), $I_D = 0$.

$V_{GS(off)}$ - cutoff voltage

I_{DSS} - Source Saturation current or maximum drain current.

Voltage & Current polarities.



Q Write short note on JFET characteristics.

OR

Write short note on Drain curves of n-channel JFET.

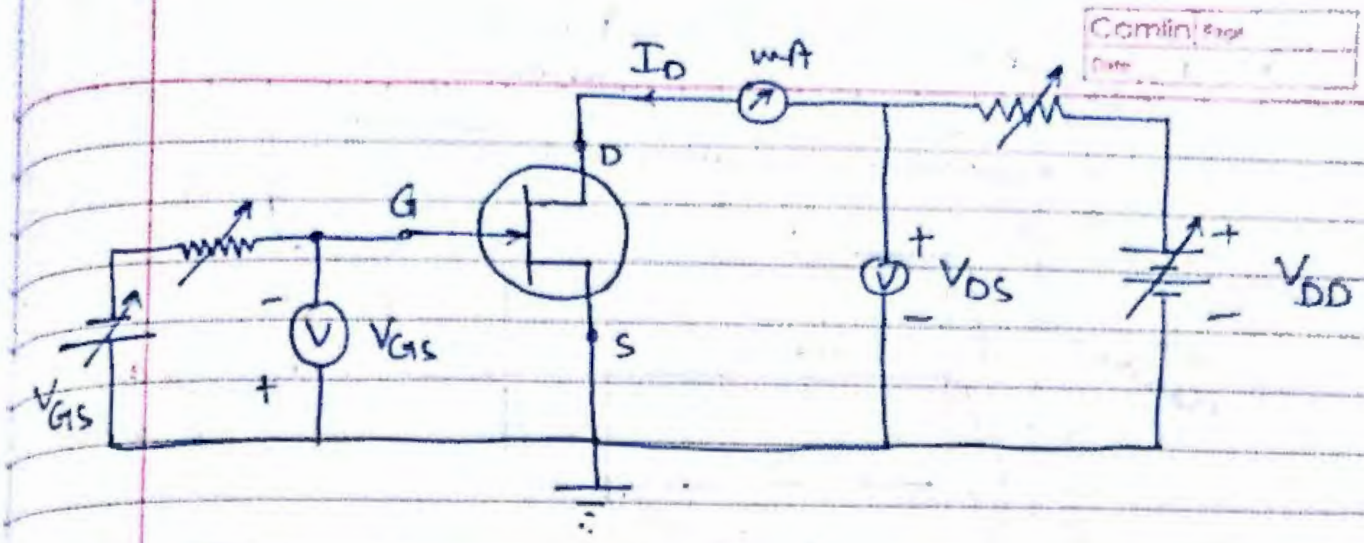
A Important V-I characteristics of JFET are.

1) Drain characteristics or drain curves.
2) Transfer characteristics or transconductance

Drain characteristics or Output characteristics or Drain curves

→ Figure shows experimental set up to plote the drain characteristics.

→ Drain characteristic is plot of I_D versus V_{DS}.



→ Above fig. shows experimental setup to plot drain characteristics.

→ drain characteristic is I_D versus V_{DS} for different values of V_{GS}.

→ Drain curves can be divided into three regions cutoff, saturation & ohmic region.

1) Cut-off Region:

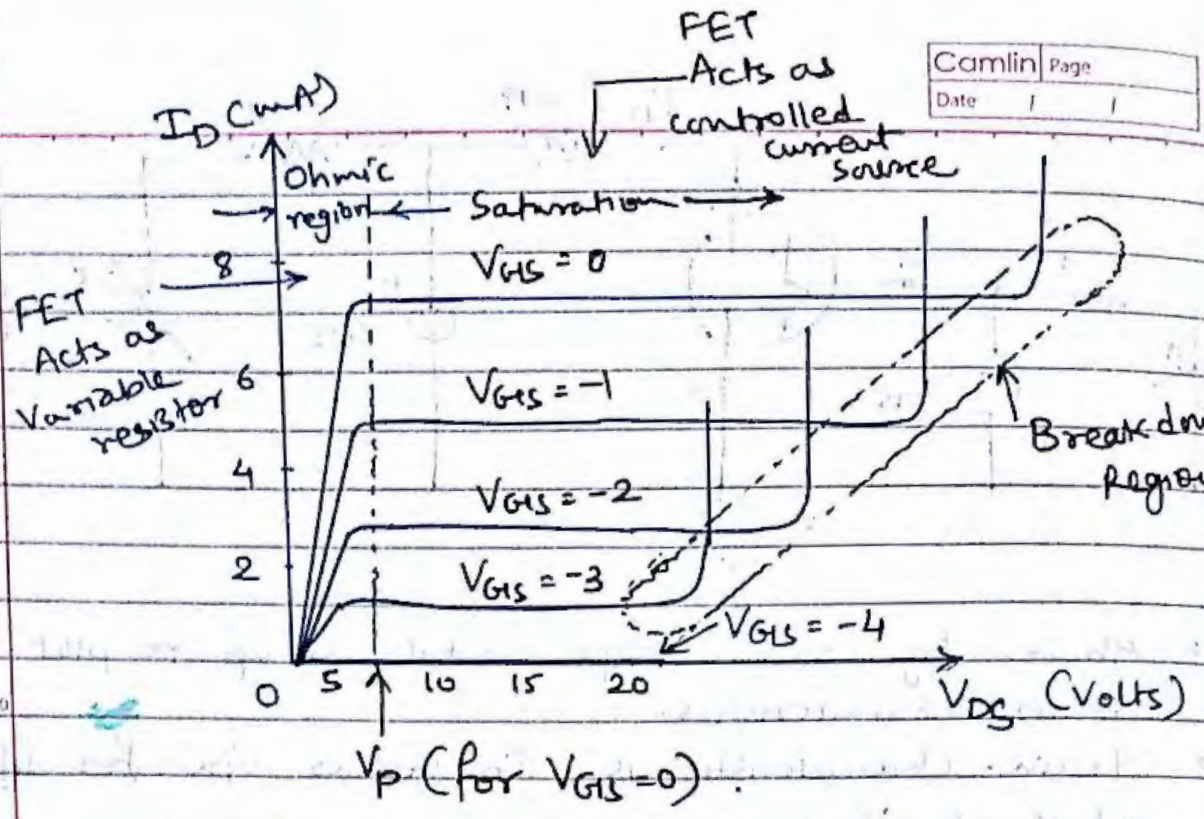
→ with increase in negative V_{GS}, channel width available for conduction decreases.

→ At $V_{GS(off)}$, both depletion region touches each other & close the channel completely.

→ So cutoff region means $I_D = 0$ and $V_{GS} > V_{GS(off)}$

→ In cutoff $I_D = 0$ & no effect on I_D even if we change the V_{DS}.

→ It operates as switch open.



2. Saturation Region (Active Region).

→ Saturation Region is portion of the characteristics where I_D remains fairly constant & doesn't change with V_{DS}.

→ Here 'saturation' is entirely different from BJT.

→ To operate JFET as an amplifier it is operated in saturation called active region of JFET.

Maximum Drain current I_{DSS}:

→ for $V_{GS}=0$; maximum Drain current flowing is denoted with I_{DSS} as channel width is maximum.

Pinch off voltage: (V_p)

Pinch off voltage is value of V_{DS}, at which the drain current reaches its

constant Saturation value.

→ Any further increase in V_{DS} does not have any effect on value of I_D.

→ As V_{GS} becomes more negative, pinchoff voltage V_P decrease.

→ If V_{GS} more negative, then small positive voltage V_{DS} will be sufficient to force pinchoff situation to take place.

Current Source:

In saturation Region, I_D remains constant irrespective of change of V_{DS}, it is used as current source.

→ With increase in negative V_{GS} channel width decreases & I_D reduces, so V_{GS} controlles I_D.

3. Ohmic Region:

→ Acts as closed switch.

→ I_D varies with variation in V_{DS} with constant V_{GS} in ohmic region.

→ The JFET is operating as a voltage variable resistor (VVR) in ohmic region.

→ Resistance offered by the JFET decreases with decrease in the value of negative gate to source bias.

FET resistance in the ohmic region is given by

$$R_{DS} = V_P / I_{DSS}$$

V_P = Pinch off voltage

I_{DSS} = maximum drain current

R_{DS} = ohmic resistance of FET.

Breakdown Region:

When a JFET is operating in saturation region, I_D does not change with change in V_{DS} up to certain V_{DS}.

→ If V_{DS} is increased further beyond this value the gate channel junction breakdown due to avalanche effect & the drain current shoots up suddenly. This can damage the device.

→ Value of breakdown voltage not remain const. It decreases with increase of -ve V_{GS}.

Q Explain Transfer characteristics of JFET.

OR

Write short note on The transconductance curve.

→ Transfer characteristics is the plot of output current I_D versus the input controlling quantity which is V_{GS} in this case.

→ So transfer characteristic is curve of I_C versus V_{GS}.

→ In BJT transfer characteristic is I_C versus I_B.

→ In BJT it is a linear line as

$$I_C = \beta_{dc} I_B$$

→ β_{dc} is considered to be constant.

→ Relation between I_D & V_{DS} is nonlinear. It is defined by shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

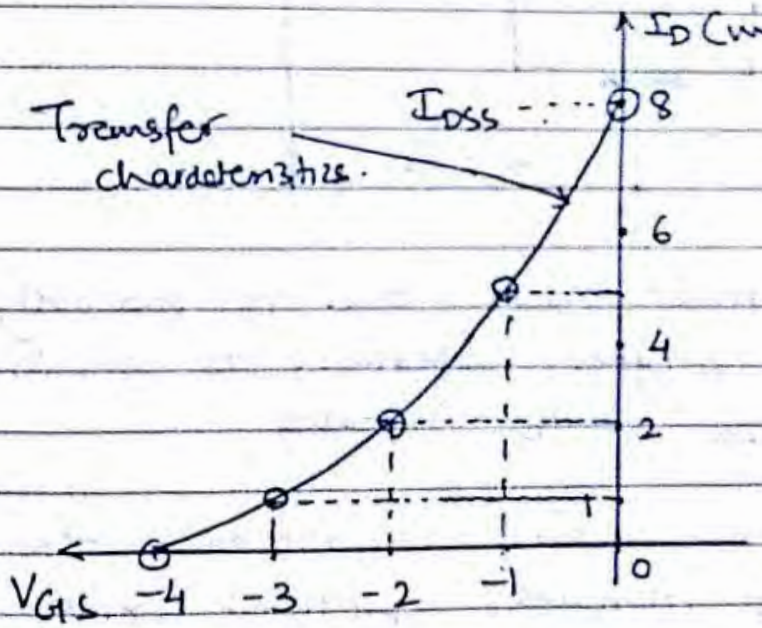
I_{DSS} = maximum drain current or source saturation current.

V_P = Pinch off voltage.

→ Here, I_{DSS} & V_P are considered constant quantity.

→ Relation between I_D & V_{GS} is therefore a squared relationship, which produces a curve which is growing exponentially.

→ When $V_{GS} = 0$, $I_D = I_{DSS}$ & when $V_{GS} = V_P = -4$, the drain current $I_D = 0$.



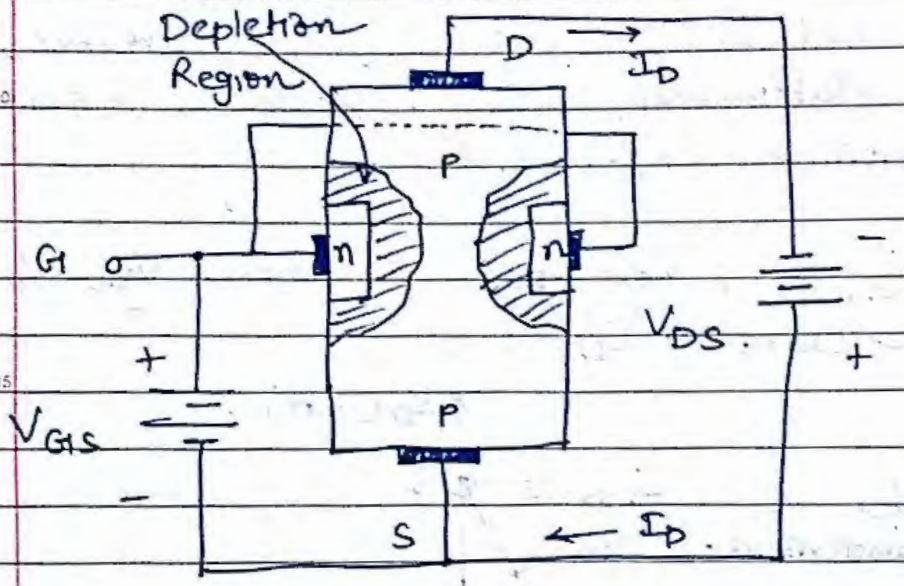
→ Transfer characteristics grow exponentially with reduction in negative V_{GS}.

→ for transfer characteristics, half cut-off point corresponds to $V_{GS} = \frac{1}{2} V_{GS(off)}$ i.e. $V_{GS} = -2V$ & $I_D = 2mA = \frac{I_{DSS}}{4}$

The p-channel JFET:

→ Explain construction & working operation of p-channel JFET with neat diagram.

↪ polarities of V_{GS}, V_{DS} are exactly opposite to those for n-channel JFET.

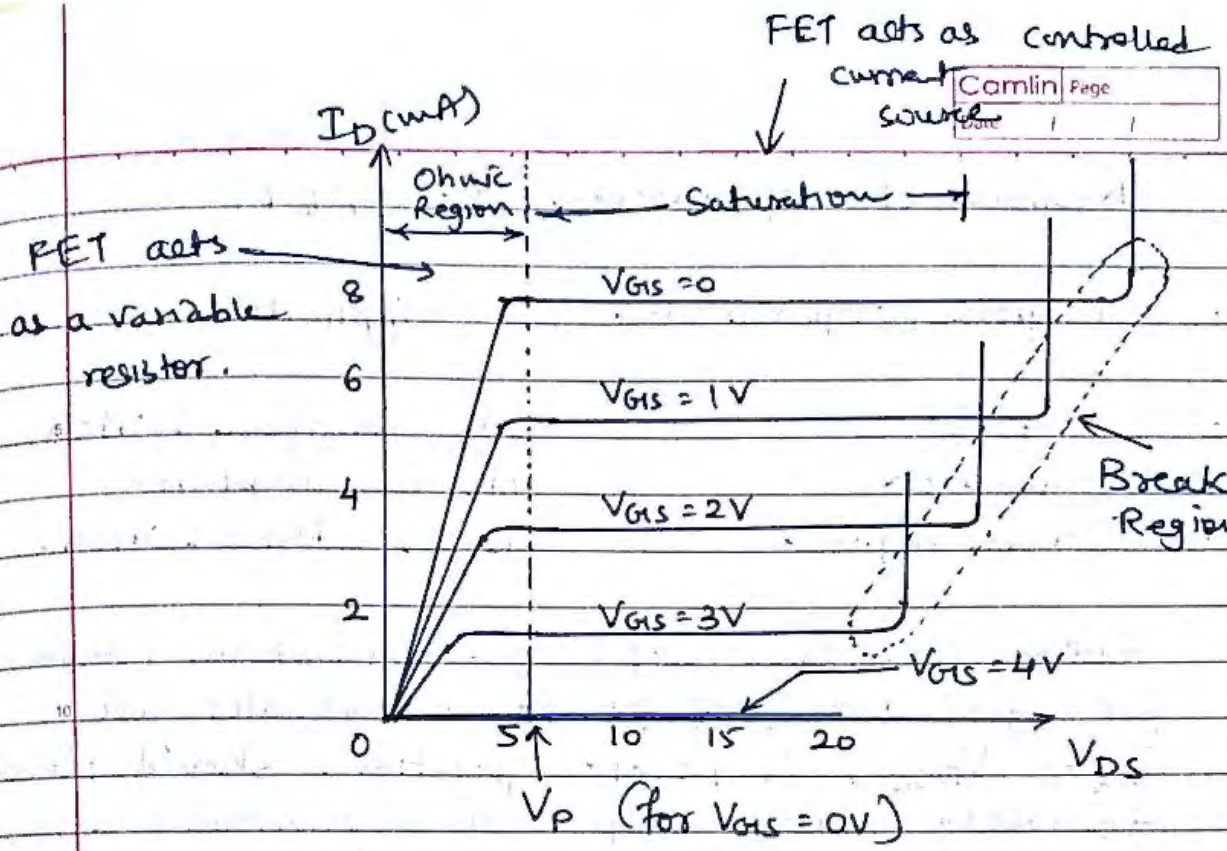


→ Drain current flows due to majority charge carrier of p-type material, as we increase negative V_{DS}, I_D increases.

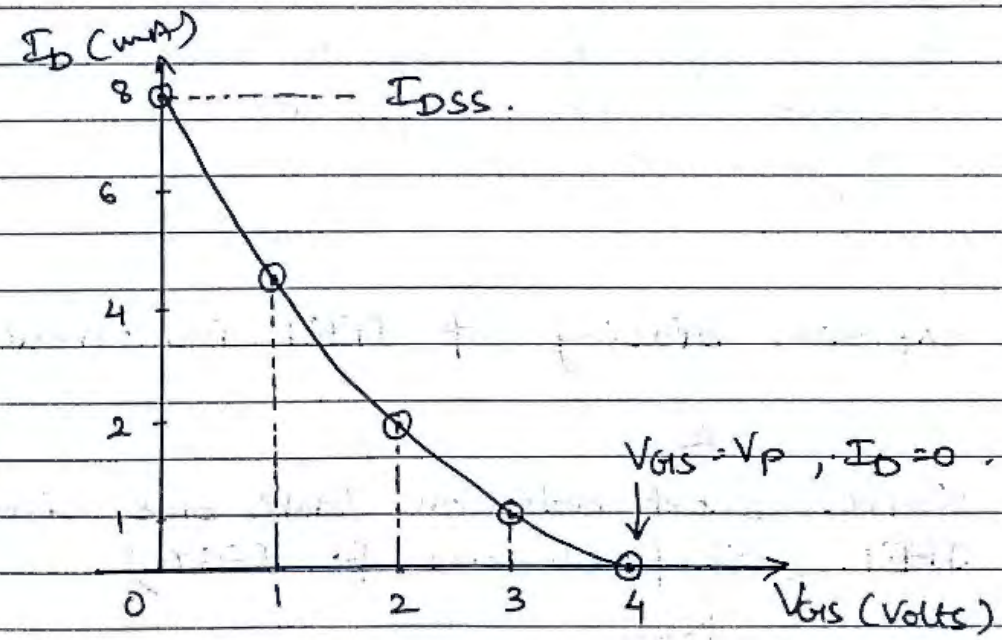
→ V_{GS} is +ve, which reverse bias the pn-junction so, as V_{GS} increases depletion region width increases and due to this I_D, drain current decreases.

Drain Curves of p-channel JFET:

→ Shape of the characteristics is same as that of n-channel JFET, only polarities of voltages reverses.



Drain characteristics of p-channel JFET.



Transfer characteristics of p-channel JFET.

→ mathematically expressed as.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

→ V_{GS} & V_P are positive here.

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Region of operation of JFET.

	Region of operation	: Application
1.	Cutoff	As an open switch
2.	Saturation	As an amplifier
3.	Ohmic region	As a closed switch.

→ When we bias JFET in saturation region for amplification, Q-point co-ordinates are I_{DQ} & V_{DSQ}, Q-point position should remain absolutely stable inspite of any variation in temperature.

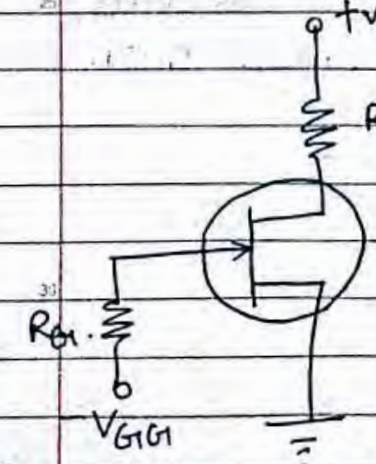
→ FET is voltage controlled device. As V_{GS} reversed bias the gate to source junction its gate current is very small.

so, $I_G \approx 0$, $I_D = I_S$.

Q. Explain biasing of JFET in ohmic region.

OR

Write short note on Gate bias circuit for JFET. (or fixed bias for JFET.)



→ fig. shows gate bias ckt.
→ V_{GG} is -ve (Applied to gate)
→ This sets up drain current less than I_{DSS}.
→ When drain current flows through R_D it sets up the drain voltage of V_{DS}

Apply KVL to drain loop

$V_{DD} - I_D R_D - V_{DS} = 0$

$V_{DS} = V_D$ = drain voltage

$V_{DS} = V_D = V_{DD} - I_D \cdot R_D$

→ Gate bias is not use for biasing JFET in saturation (active) region because Q-point is this scheme is extremely unstable

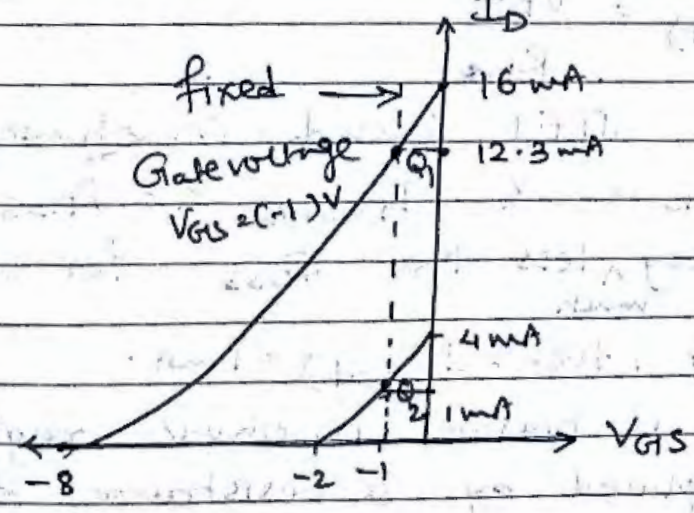
→ For example, a 2N5459 has following spreads between maximum & minimum.

I_{DSS} varies from 4mA to 16mA

$V_{GS(off)}$ varies from −2V to −8V

Optional

Fig. below shows maximum & minimum transconductance curve

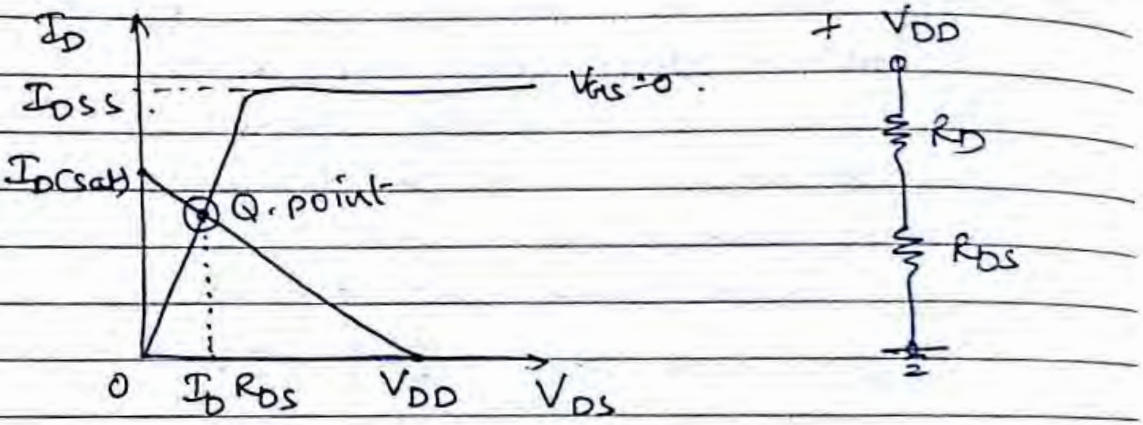


→ If $V_{GS} = -1V$ is used then we get max & min Q-points, Q_1 & Q_2

Q_1 has $I_D = 12.3$ mA, Q_2 has I_D 1mA.

Hard Saturation:

Gate bias is perfect for ohmic region biasing because stability of Q. point doesn't matter here. Following fig. shows how to bias a JFET in the ohmic region.



$$I_{D(sat)} = \frac{V_{DD}}{R_D}$$

→ To ensure JFET biased in ohmic region we keep $V_{GS}=0$ & $I_{D(sat)} << I_{DSS}$.

$I_{D(sat)}$ is very (much) less than I_{DSS}. for example if $I_{DSS} = 10\,mA$, then $I_{D(sat)} = 1\,mA$.

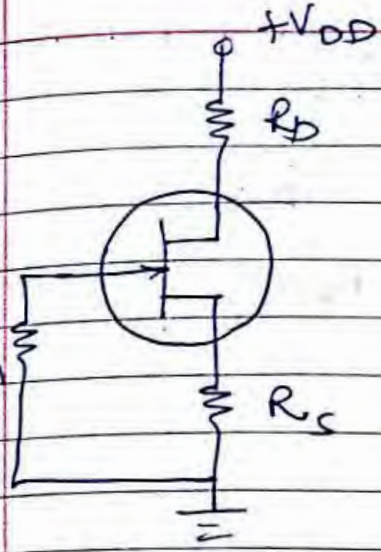
→ When JFET is biased in ohmic region it can be replaced by a resistance R_{DS}.

Q. Draw & explain self bias circuit of JFET.

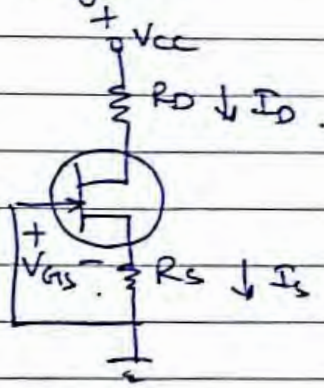
OR

Draw & explain biasing of JFET in saturation (Active) Region.

→ Self bias circuit is shown in the figure



As, $I_G = 0$, due to reversed biase gate to source junction, no drop across R_G (As current 0) so, R_G Replaced by short circuit for DC Analysis.



DC equivalent ckt for self bias.

Self Bias circuit

$I_D = I_S$.

Apply KVL in gate loop.

$V_{GS} + I_S \cdot R_S = 0$

$V_{GS} = -I_S R_S$

$\boxed{V_{GS} = -I_D R_S}$

→ To obtain I_D use shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

→ To obtain V_{DS}.

Apply KVL in Drain loop.

$V_{DD} = I_D R_D + V_{DS} + I_S R_S$.

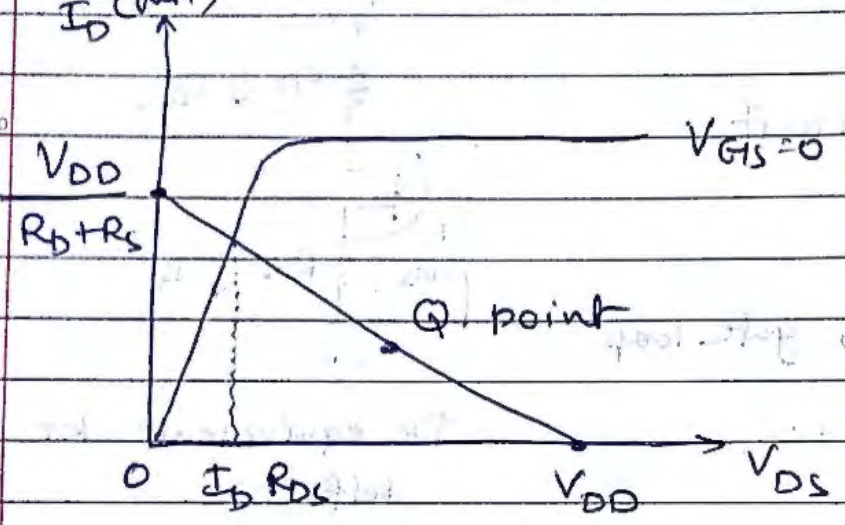
$V_{DD} = I_D R_D + V_{DS} + I_D R_S$.

$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

$$V_{DD} = I_{DQ} (R_D + R_S) + V_{DSQ}$$

$$\boxed{V_{DSQ} = V_{DD} - I_{DQ} (R_D + R_S)}$$

DC load line:



Apply KVL in drain loop.

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

$$V_{DD} = I_D (R_D + R_S) + V_{DS}$$

when $I_D = 0$, $V_{DS} = V_{DD}$

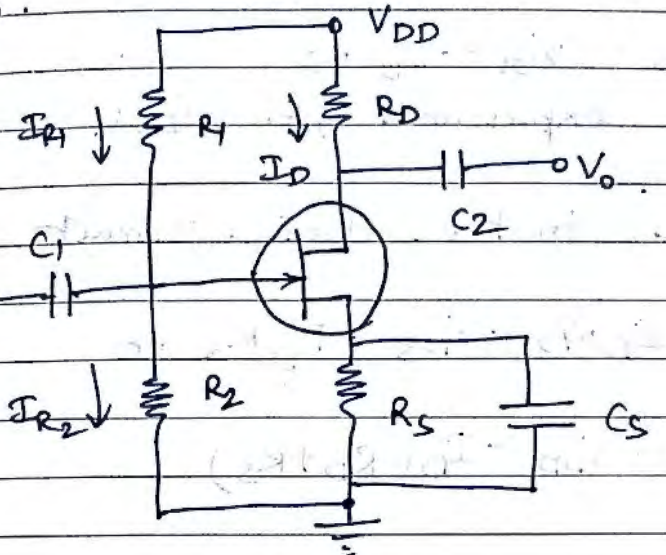
when $V_{DS} = 0$, $I_D = \frac{V_{DD}}{R_D + R_S}$

→ In Saturation Region $V_{DS} > I_D R_{DS}$.

Q. Draw & explain voltage divider bias for FET.

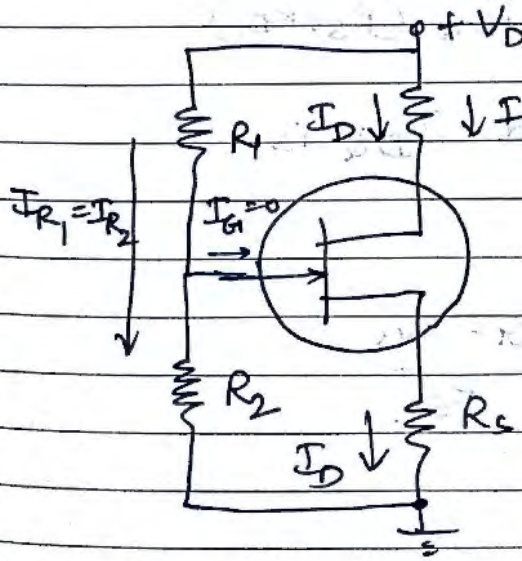
OR

Explain FET biasing in active region using VDB.



→ When we do DC Analysis of the circuit, C_1, C_2 & C_S are assumed to be open circuit.

DC equivalent Circuit



$I_{R_1} = I_{R_2}$, because $I_{G_1} = 0$.

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

DC Analysis:

Step 1 →

Obtain expression for V_{G_1}:

V_{G_1} = voltage across R_2.

$$V_{G1} = \frac{R_2}{R_1+R_2} \times V_{DD}.$$

Step 2 obtain expression for V_{GS}:

$$V_{GS} = V_G - I_D R_S.$$

Step 3 obtain expression for V_{DS}:

→ Apply KVL to the drain circuit.

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0.$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

Value of drain current I_D can be obtained by using the shockley's equation.

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{DSQ} = V_{DD} - I_{DQ}(R_S + R_D)$$

→ Another way to find I_{DQ} is

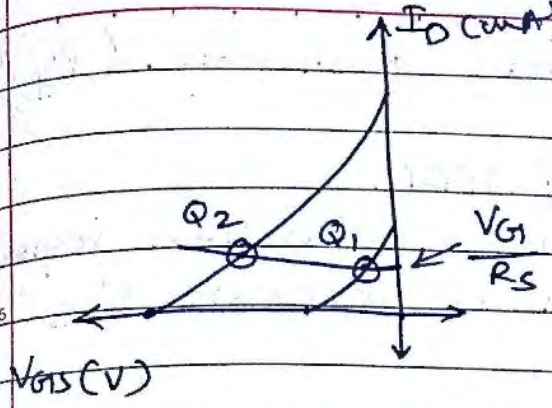
$$V_S = V_G - V_{GS}$$

$$I_{DQ} = \frac{V_S}{R_S} = \frac{V_G - V_{GS}}{R_S}.$$

$$V_G \gg V_{GS}$$

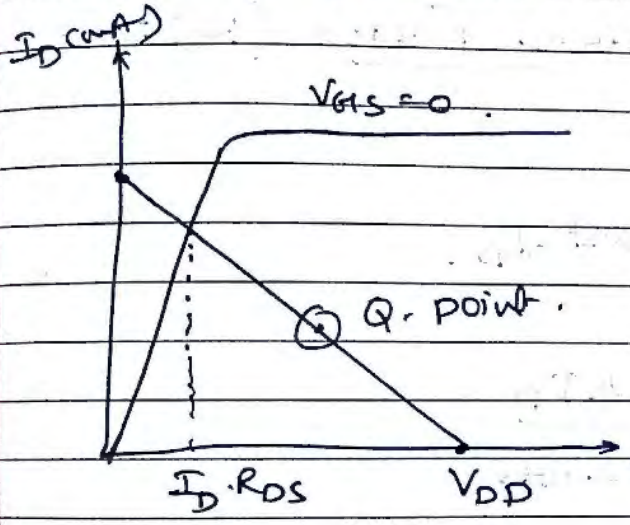
So, $I_{DQ} \approx \frac{V_G}{R_S}$.

→ So, I_{DQ} doesn't depends on V_{GS}, I_{DQ} is almost const. for JFET.



I_D is almost constant.

Load line for VDB.



for DC load line:

→ Apply KVL in drain loop

$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$

$I_D (R_D + R_S) = V_{DD} - V_{DS}$

$I_D = \frac{V_{DS}}{(R_D+R_S)} + \frac{V_{DD}}{(R_D+R_S)}$

→ extreme points are

put $I_D = 0$, $V_{DS} = V_{DD}$.

$V_{DS} = 0$; $I_D = \frac{V_{DD}}{R_D+R_S}$.

Q. Define transconductance:

denoted by g_m

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$ | constant V_{DS}.

→ It is calculated at a particular operating point.

Q. Define Dynamic Drain Resistance (r_d)

→ It is ac resistance of JFET.

→ It is calculated in the saturation region of the FET output characteristics at const. V_{GS}.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{\text{const. } V_{GS}}$$

Q. Define Amplification Factor (μ):

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{\text{const } I_D}.$$

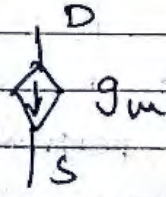
$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = r_d \times g_m}$$

Q. AC equivalent Circuit of JFET (small signal ckt of JFET):

→ In JFET, $I_G = 0$, input resistance is very high so, it is represented as open ckt.

→ I_d is controlled by V_{GS}, so it is represented by controlled current source.

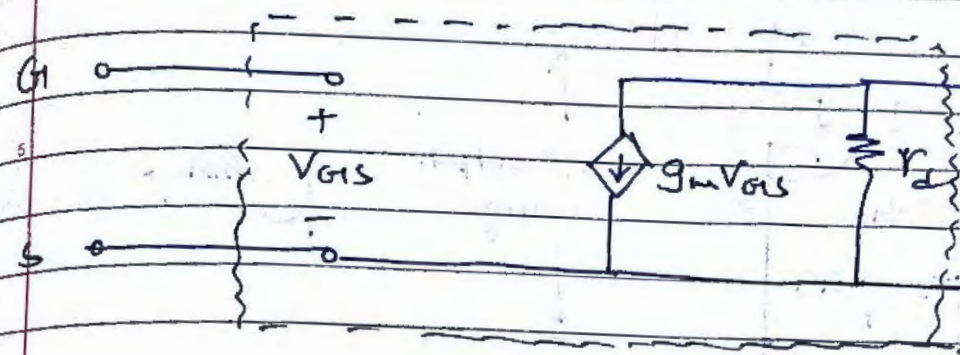


$g_m V_{GS}$.

$$V_{GS} g_m = \frac{I_D}{V_{GS}} \cdot V_{GS}$$

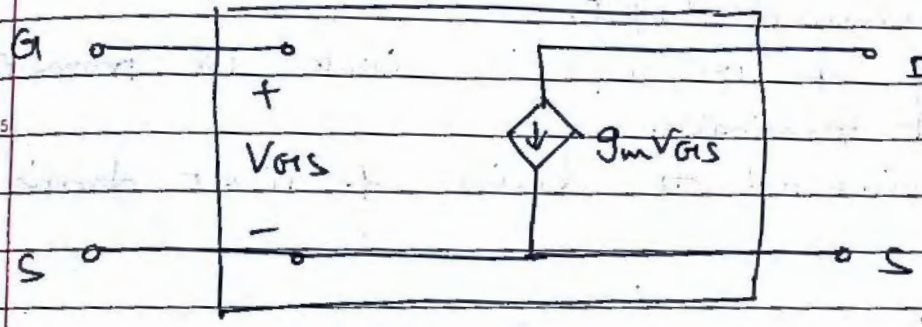
$$V_{GS} g_m = I_D.$$

→ o/p resistance is r_d represented is parallel to current source.



AC equivalent ckt of JFET.

→ here r_d is very large compare to other component, so in approximate analysis r_d is replaced by open ckt.



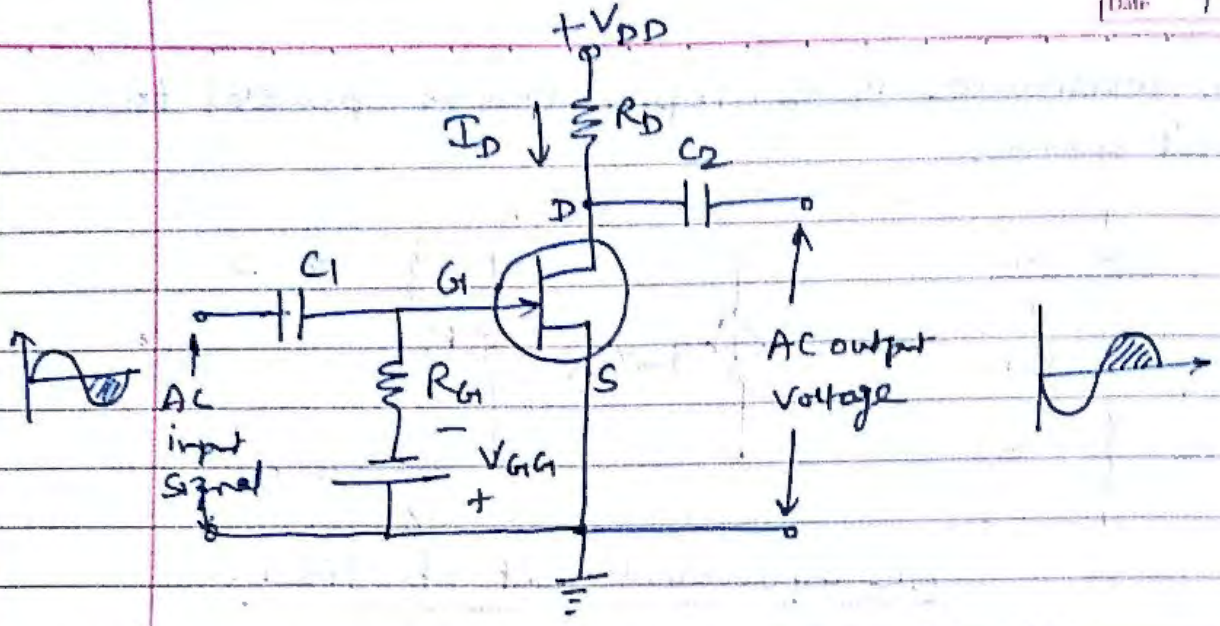
Approximate AC equivalent circuit of JFET.

Q. Draw & explain JFET as an amplifier.

Types of JFET amplifier (amplifier configurations)

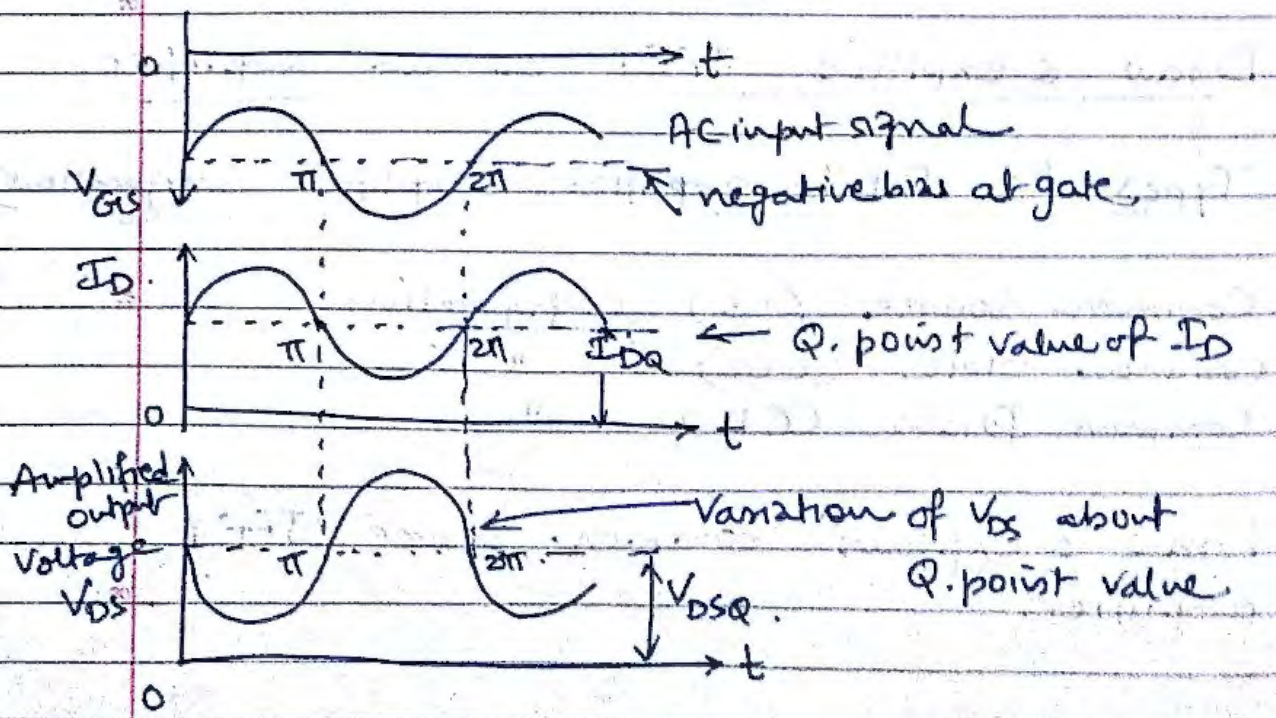
→ Common Source (CS) configuration
→ Common Gate (CG) "
→ Common Drain (CD) "

Q. Draw & explain common source JFET amplifier.



→ here C_1 & C_2 are coupling capacitor.
→ here common source amplifier circuit is shown using n-channel JFET.
→ Coupling capacitor C_1 & C_2 block DC from input & output terminals.
→ R_D is connected to drain to limit drain current.

Operation as an amplifier:



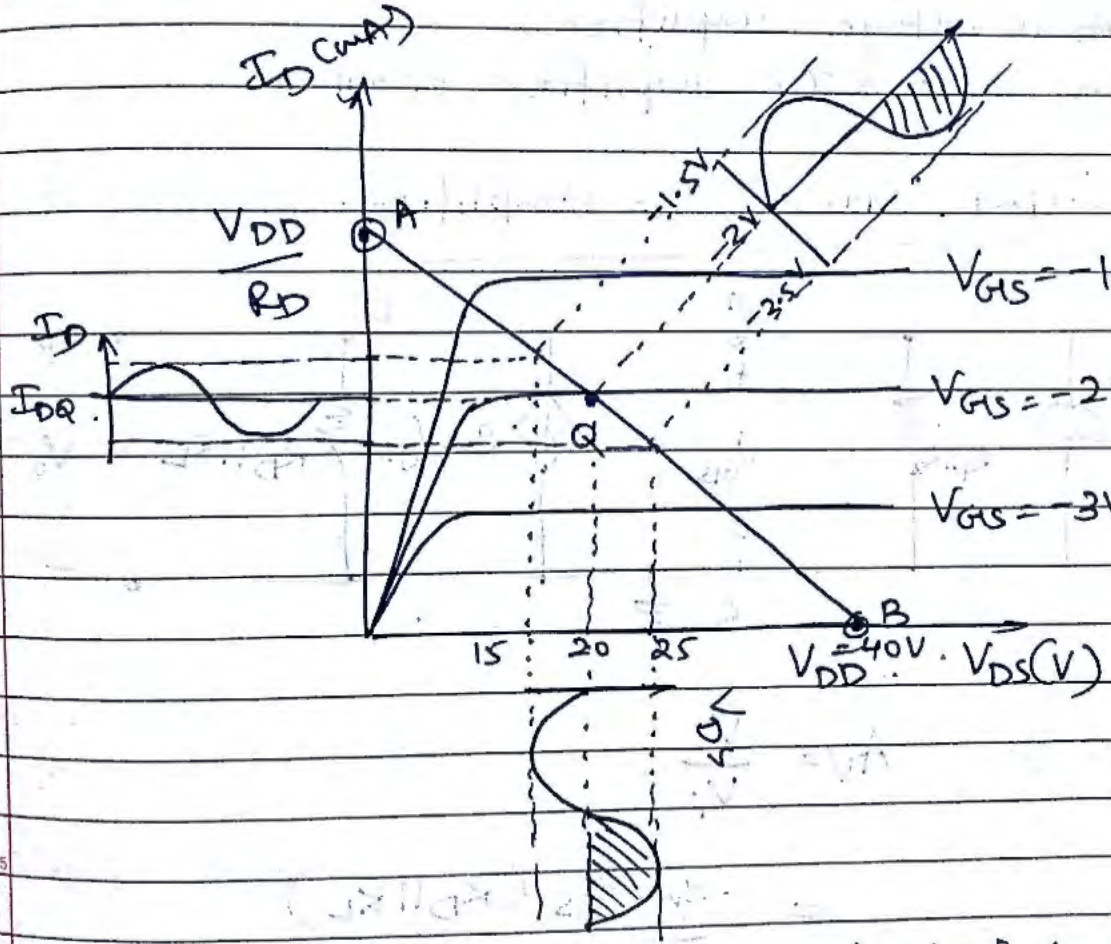
→ During positive half cycle of input signal, gate to source voltage becomes less negative so, channel width increases, so I_D increases.

As $V_{DS} = V_{DD} - I_D R_D$.

→ As $I_D \uparrow$, $I_D R_D \uparrow$ & so, $V_{DS} \downarrow$.

→ So, during positive half cycle of input V_{DS} decreases from its Q-point value (V_{DSQ}).

→ So, there is a phase difference of 180° between input & output.



for DC load line: Apply KVL in drain loop.

$$V_{DD} - I_D R_D - V_{DS} = 0$$

put $V_{DS} = 0$, $I_D = \frac{V_{DD}}{R_D}$ point (A) on y-axis.

put $I_D = 0$, $V_{DS} = V_{DD}$ point (B) on x-axis.

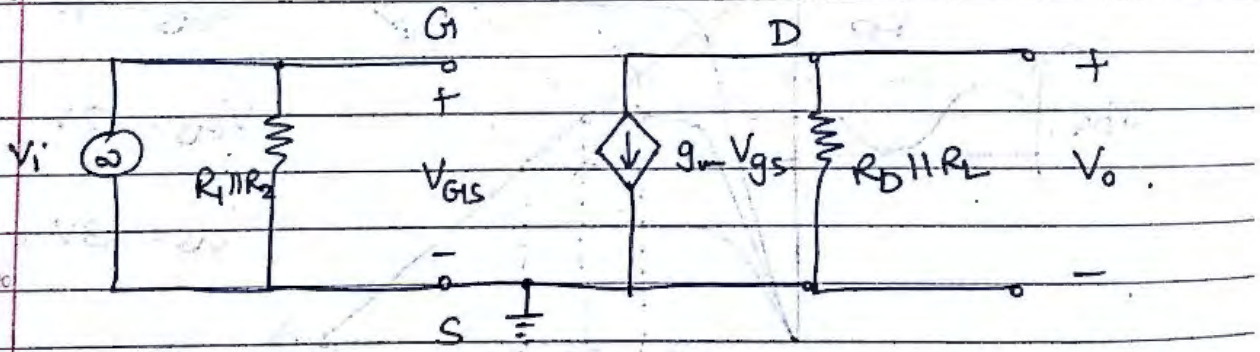
Features of CS Amplifier:

- High input Resistance.
- Low output Resistance
- High voltage Gain
- 180° phase shift between i/p & o/p.

Applications:

- As preamplifier in audio circuit
- As a voltage amplifier.
- In radio & TV amplifier circuit.

Voltage Gain of CS Amplifier.



$$A_V = \frac{V_o}{V_i}$$

$$= \frac{-g_m V_{gs} (R_D \| R_L)}{V_{gs}}$$

$$A_V = -g_m (R_D \| R_L)$$

→ Negative sign indicates 180° phase shift between i/p & o/p.

Q. Explain JFET as a switch.

→ To operate JFET as a switch it has to biased in cutoff or ohmic region.

cutoff Region → switch open
ohmic " → switch closed.

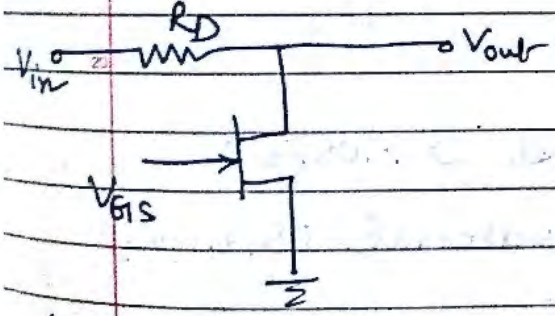
JFET as an open switch:

When $V_{GS} < V_{GS(off)}$, then $I_D = 0$, so Resistance offered is very high.
(for n-channel JFET V_{GS} is negative)

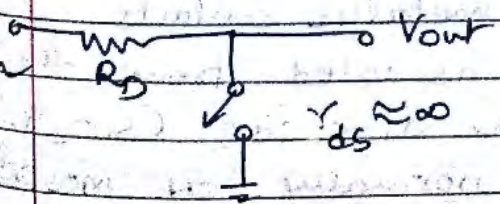
JFET as a closed switch:

When $V_{GS} = 0$, JFET operates in the ohmic region.

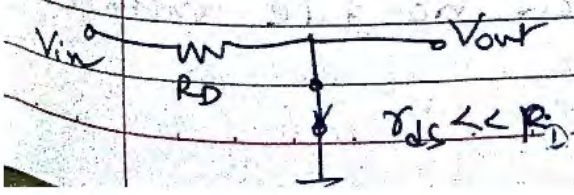
JFET Shunt Switch



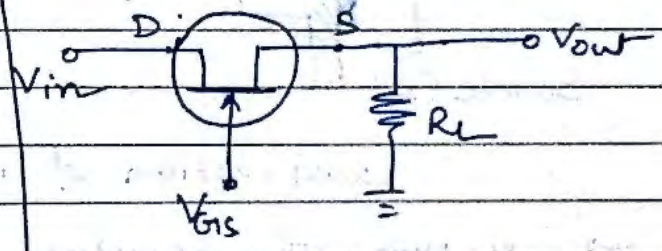
for $V_{GS} \leq V_{GS(off)}$



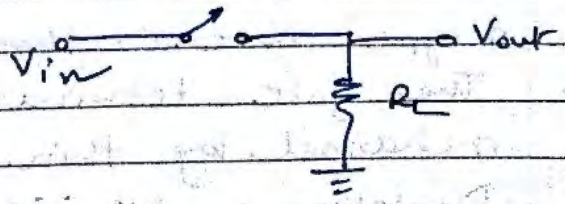
for $V_{GS} = 0$



JFET Series switch



for $V_{GS} \leq V_{GS(off)}$



for $V_{GS} = 0$.