DMA Register Specification Document

1. Overview

This document describes the complete register-level specification of the **Enhanced DMA Design**. It includes register addresses, access permissions, bit-field descriptions, and functional explanations. The DMA provides configurable data transfer control, status monitoring, interrupt support, error reporting, and descriptor-based operation.

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2. Register Map Summary

Offset (Hex)	Register Name	Access	Description
0x400	INTR	RO/RW	Interrupt status and mask register
0x404	CTRL	RW	DMA control register
0x408	IO_ADDR	RW	IO/source address
0x40C	MEM_ADDR	RW	Memory/destination address
0x410	EXTRA_INFO	RW	User-defined extra information
0x414	STATUS	RO	DMA runtime status
0x418	TRANSFER_COUNT	RO	Transfer progress counter
0x41C	DESCRIPTOR_ADDR	RW	Descriptor base address
0x420	ERROR_STATUS	RW1C/RO	Error flags and debug info
0x424	CONFIG	RW	DMA configuration register

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3. Register Descriptions

3.1 INTR Register (0x400)

Purpose: Provides interrupt status and interrupt masking capability.

Bits	Field	Access	Description
[15:0]	intr_status	RO	Interrupt status bits. Bit[0] indicates DMA transfer completion.
[31:16]	intr_mask	RW	Interrupt mask. 1 = interrupt enabled.

3.2 CTRL Register (0x404)

Purpose: Controls DMA start and basic transfer behavior.

Bits	Field	Access	Description
[0]	start_dma	RW (Self-clear)	Writing 1 starts DMA. Auto-clears after 1 cycle.
[15:1]	w_count	RW	Number of transfer beats.
[16]	io_mem	RW	0 = IO to MEM, 1 = MEM to IO.
[31:17]	Reserved	RO	Reserved, read as 0.

3.3 IO_ADDR Register (0x408)

Purpose: Holds the IO/source address for DMA transfer.

Bits	Field	Access	Description
[31:0]	io_addr	RW	IO or peripheral address.

3.4 MEM_ADDR Register (0x40C)

Purpose: Holds the memory destination/source address.

Bits	Field	Access	Description
[31:0]	mem_addr	RW	Memory base address for DMA.

3.5 EXTRA_INFO Register (0x410)

Purpose: Software-defined register for passing auxiliary information.

Bits	Field	Access	Description
[31:0]	extra_info	RW	User-defined metadata.

3.6 STATUS Register (0x414)

Purpose: Provides real-time DMA engine status.

Bits	Field	Access	Description
[0]	busy	RO	DMA is currently active.
[1]	done	RO	DMA transfer completed.
[2]	error	RO	Error detected during transfer.
[3]	paused	RO	DMA paused state.
[7:4]	current_state	RO	DMA FSM state encoding.
[15:8]	fifo_level	RO	Current FIFO fill level.
[31:16]	Reserved	RO	Reserved, read as 0.

3.7 TRANSFER_COUNT Register (0x418)

Purpose: Indicates number of completed transfer beats.

Bits	Field	Access	Description
[31:0]	transfer_count	RO	Incremented each successful transfer.

3.8 DESCRIPTOR_ADDR Register (0x41C)

Purpose: Base address of DMA descriptor list.

Bits	Field	Access	Description
[31:0]	descriptor_addr	RW	Descriptor table base address.

3.9 ERROR_STATUS Register (0x420)

Purpose: Reports DMA error conditions. Error bits are **Write-1-to-Clear (W1C)**.

Bits	Field	Access	Description
[0]	bus_error	RW1C	Bus access failure.

Bits	Field	Access	Description
[1]	timeout_error	RW1C	Transfer timeout occurred.
[2]	alignment_error	RW1C	Address alignment error.
[3]	overflow_error	RW1C	FIFO overflow detected.
[4]	underflow_error	RW1C	FIFO underflow detected.
[7:5]	Reserved	RO	Reserved.
[15:8]	error_code	RO	Encoded error reason.
[31:16]	error_addr_offset	RO	Address offset where error occurred.

3.10 CONFIG Register (0x424)

Purpose: Configures DMA behavior and performance.

Bits	Field	Access	Description
[1:0]	priority	RW	DMA priority level.
[2]	auto_restart	RW	Automatically restart DMA after completion.
[3]	interrupt_enable	RW	Enables DMA interrupts.
[5:4]	burst_size	RW	Transfer burst size configuration.
[7:6]	data_width	RW	Transfer data width selection.
[8]	descriptor_mode	RW	Enables descriptor-based DMA mode.
[31:9]	Reserved	RO	Reserved, read as 0.

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4. DMA Operation Summary

1. Program IO_ADDR, MEM_ADDR, CTRL, and CONFIG registers.
2. Write `start_dma = 1` in CTRL register.
3. STATUS.busy asserts while DMA is active.
4. TRANSFER_COUNT increments per transfer.
5. On completion:
6. STATUS.done asserted
7. INTR.status[0] set
8. Errors are reported via ERROR_STATUS and STATUS.error.

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5. Notes

- CTRL.start_dma is a pulse and self-clears.
- ERROR_STATUS bits must be cleared by writing 1.
- STATUS and TRANSFER_COUNT are read-only.
- Reserved bits must be written as 0.

End of DMA Register Specification