EC200A&EC2x Series

Compatible Design

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
-	2022-07-11	Shiye ZHU/ Brant WAN/ Dylan LIU	Creation of the document
1.0	2022-09-28	Shiye ZHU/ Handor QIN/ Dylan LIU/ Frank WANG	First official release

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1 Introduction

Quectel LTE Standard EC200A series modules are compatible with EC2x family modules (EC25 series, EC21 series, EC20-CE). This document outlines the compatible design among EC200A series and EC2x family modules, which can help you easily migrate from one design to either of the others.

NOTE

For conciseness purposes, EC200A, EC25, EC21 and EC20-CE modules will hereinafter be referred to collectively as "the module/modules" in parts hereof applicable to all said modules, and individually as “EC200A” and “EC2x” in parts hereof referring to the differences between them.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 General Descriptions

2.1. Product Description

The general information and frequency bands of EC200A and EC2x modules are presented in the tables below.

2.1.1. General Information

Table 2: General Information

Module Name	Appearance	Packaging	Dimensions (mm)
EC200A Series		80 LCC pins + 64 LGA pins	29.0 × 32.0 × 2.4
EC25 Series		80 LCC pins + 64 LGA pins	29.0 × 32.0 × 2.4
EC21 Series		80 LCC pins + 64 LGA pins	29.0 × 32.0 × 2.4
EC20-CE		80 LCC pins + 64 LGA pins	29.0 × 32.0 × 2.4

2.2. Feature Overview

The general features of EC200A and EC2x modules are compared in the table below.

Table 3: Feature Overview

Feature	EC200A Series	EC25 Series/EC21 Series/EC20-CE
Power Supply	Supply voltage: 3.4–4.5 V, Typ. 3.8 V	Supply voltage: 3.3–4.3 V, Typ. 3.8 V
Sleep Current (USB Suspend)	< 3 mA. For more information, see ***document [1]***.	< 4 mA. For more information, see ***document [2]*** & ***[3]*** & ***[4]***.
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS 1-4 ● Max. 85.6 kbps (DL)/ Max. 85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 12 ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1-9 ● Uplink coding schemes: MCS 1-9 ● Max. 236.8 kbps (DL)/Max. 236.8 kbps (UL)	**GPRS:** ● Supports GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1-4 ● Max. 107 kbps (DL)/Max. 85.6 kbps (UL) **EDGE:** ● Supports EDGE multi-slot class 33 (33 by default) ● Supports GMSK and 8-PSK for different MCS (Modulation and Coding Scheme) ● Downlink coding schemes: MCS 1-9 ● Uplink coding schemes: MCS 1-9 ● Max. 296 kbps (DL)/Max. 236.8 kbps (UL)
UMTS Features	● Supports 3GPP Rel-7 HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK,16-QAM and 64QA modulations ● HSPA+: Max. 21 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/Max. 384 kbps (UL)	● Supports 3GPP Rel-8 DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Supports QPSK, 16QAM and 64QAM modulations ● DC-HSDPA: Max 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/Max. 384 kbps (UL)
LTE Features	Non-CA LTE Cat 4: FDD: Max. 150 Mbps (DL), Max. 50 Mbps (UL) TDD: Max. 130 Mbps (DL), Max. 30 Mbps (UL)	**EC25 Series/EC20-CE:** Non-CA LTE Cat 4: FDD: Max. 150 Mbps (DL), Max. 50 Mbps (UL) TDD: Max. 130 Mbps (DL), Max. 30 Mbps (UL) **EC21 Series:** Non-CA LTE Cat 1: FDD: Max. 10 Mbps (DL), Max. 5 Mbps (UL) TDD: Max. 8.96 Mbps (DL), Max. 3.1 Mbps (UL)

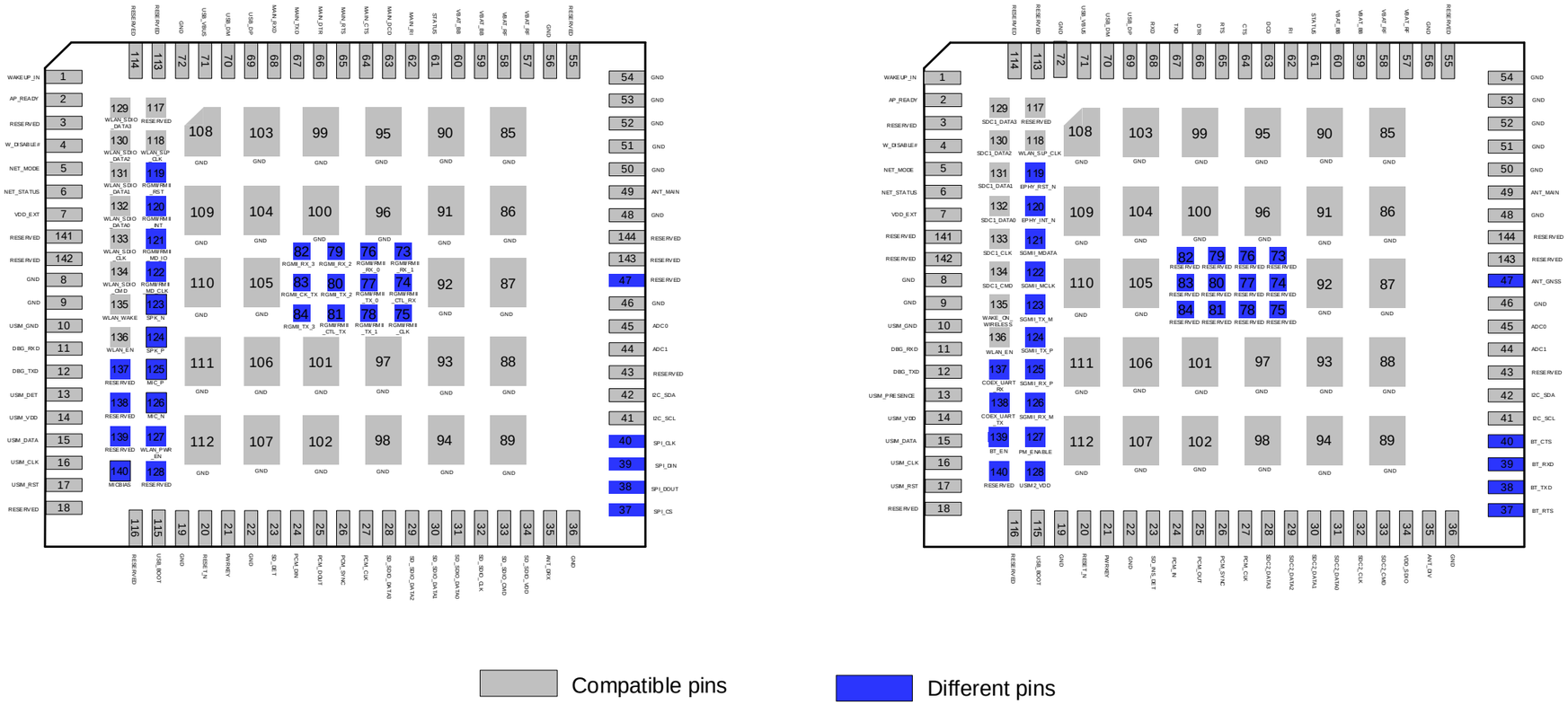
Temperature Ranges	Operating temperature range: -35 to +75 °C [1] Extended temperature range: -40 to +85 °C [2] Storage temperature range: -40 to +90 °C	Operating temperature range: -35 to +75 °C [3] Extended temperature range: -40 to +85 °C [4] Storage temperature range: -40 to +90 °C
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rates: up to 921600 bps, 115200 bps by default ● RTS and CTS hardware flow control **Debug UART:** ● Used for the output of partial logs ● 115200 bps baud rate	**Main UART:** ● Used for AT command communication and data transmission ● Baud rates: up to 921600 bps, 115200 bps by default ● RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● 115200 bps baud rate
USB Interface	Compliant with USB 2.0 High-speed and full-speed modes (slave only)	Compliant with USB 2.0 High-speed and full-speed modes (slave only)
Digital Audio	PCM interface	PCM interface
I2C Interfaces	Supported	Supported
SD Card Interface	SD 3.0 protocol	SD 3.0 protocol
WLAN/Bluetooth Interface	Supported SDIO interface for WLAN	Low-power SDIO 3.0 interface for WLAN; UART & PCM interfaces for Bluetooth
SGMII Interface	-	10 Mbps/100 Mbps/1000 Mbps Ethernet work modes **EC25 Series/EC20-CE:** Max. 150 Mbps (DL)/50 Mbps (UL) for 4G network **EC21 Series:** Max. 10 Mbps (DL)/Max. 5 Mbps (UL) for 4G network
RGMII/RMII	RMII: 1.8/ 3.3 V; default: 3.3 V RGMII: 1.8 V	-
(U)SIM Card Detection	Supported	Supported
GNSS	-	GPS, GLONASS, BDS, Galileo, QZSS [5]
Firmware Upgrade	USB interface or DFOTA	USB interface or DFOTA

[1] Within the operating temperature range, the module meets 3GPP specifications.
[2] Within the extended temperature range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[3] Within the operating temperature range, the module meets 3GPP specifications.
[4] Within the extended temperature range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.
[5] GNSS function is optional.

2.3. Pin Assignment

Pin assignments of EC200A and EC2x modules are presented in the figure below.

EC200A Series



EC25 Series/EC21 Series/EC20-CE

Compatible pins

Different pins

Figure 1: EC200A & EC2x Pin Assignments

NOTE

1. The USB_BOOT and RGMII/RMII_RST_N pin of EC200A series cannot be pulled to high level before module startup. There are no restrictions on other pins.
2. WAKEUP_IN, NET_MODE, WLAN_EN, COEX_UART_RX, COEX_UART_TX, USB_BOOT, BT_CTS pins of EC2x family cannot be pulled to high level before module startup.

3 Pin Description

The pins on the modules are described below.

Table 4: I/O Parameter Definition

Symbol	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

3.1. Pin Description

Pin definitions of EC200x and EC2x modules are presented in the following table.

Table 5: Pin Definition

EC200A Series				EC25 Series/EC21 Series/EC20-CE			
Pin No.	**Pin Name**	**I/O**	**Power Domain**	**Pin No.**	**Pin Name**	**I/O**	**Power Domain**
1	WAKEUP_IN*	DI	1.8 V	1	WAKEUP_IN	DI	1.8 V
2	AP_READY*	DI	1.8 V	2	AP_READY	DI	1.8 V
3	RESERVED	-	-	3	RESERVED	-	-
4	W_DISABLE#	DI	1.8 V	4	W_DISABLE#	DI	1.8 V
5	NET_MODE	DO	1.8 V	5	NET_MODE	DO	1.8 V
6	NET_STATUS	DO	1.8 V	6	NET_STATUS	DO	1.8 V
7	VDD_EXT	PO	1.8 V	7	VDD_EXT	PO	1.8 V
8	GND	-	GND	8	GND	-	GND
9	GND	-	GND	9	GND	-	GND
10	USIM_GND	-	GND	10	USIM_GND	-	GND

11	DBG_RXD	DI	1.8 V	11	DBG_RXD	DI	1.8 V
12	DBG_TXD	DO	1.8 V	12	DBG_TXD	DO	1.8 V
13	USIM_DET	DI	1.8 V	13	USIM_PRESENCE	DI	1.8 V
14	USIM_VDD	PO	1.8/ 3.0 V	14	USIM_VDD	PO	1.8/ 3.0 V
15	USIM_DATA	DIO	1.8/ 3.0 V	15	USIM_DATA	DIO	1.8/ 3.0 V
16	USIM_CLK	DO	1.8/ 3.0 V	16	USIM_CLK	DO	1.8/ 3.0 V
17	USIM_RST	DO	1.8/ 3.0 V	17	USIM_RST	DO	1.8/ 3.0 V
18	RESERVED	-	-	18	RESERVED	-	-
19	GND	-	GND	19	GND	-	GND
20	RESET_N	DI	1.8 V	20	RESET_N	DI	1.8 V
21	PWRKEY	DI	VBAT	21	PWRKEY	DI	The output voltage is 0.8 V when the module is powered on.
22	GND	-	GND	22	GND	-	GND
23	SD_DET*	DI	1.8 V	23	SD_INS_DET	DI	1.8 V
24	PCM_DIN	DI	1.8 V	24	PCM_IN	DI	1.8 V
25	PCM_DOUT	DO	1.8 V	25	PCM_OUT	DO	1.8 V
26	PCM_SYNC	DIO	1.8 V	26	PCM_SYNC	DIO	1.8 V
27	PCM_CLK	DIO	1.8 V	27	PCM_CLK	DIO	1.8 V

28	SD_SDIO_DATA3	DIO	1.8/ 2.8 V	28	SDC2_DATA3	DIO	1.8/ 2.85 V
29	SD_SDIO_DATA2	DIO	1.8/ 2.8 V	29	SDC2_DATA2	DIO	1.8/ 2.85 V
30	SD_SDIO_DATA1	DIO	1.8/ 2.8 V	30	SDC2_DATA1	DIO	1.8/ 2.85 V
31	SD_SDIO_DATA0	DIO	1.8/ 2.8 V	31	SDC2_DATA0	DIO	1.8/ 2.85 V
32	SD_SDIO_CLK	DO	1.8/ 2.8 V	32	SDC2_CLK	DO	1.8/ 2.85 V
33	SD_SDIO_CMD	DIO	1.8/ 2.8 V	33	SDC2_CMD	DIO	1.8/ 2.85 V
34	SD_SDIO_VDD	PO	1.8/ 2.8 V	34	VDD_SDIO	PO	1.8/ 2.85 V
35	ANT_DRX	AI	-	35	ANT_DIV	AI	-
36	GND	-	GND	36	GND	-	GND
37	SPI_CS	DO	1.8 V	37	BT_RTS	DI	1.8 V
38	SPI_DOUT	DO	1.8 V	38	BT_TXD	DO	1.8 V
39	SPI_DIN	DI	1.8 V	39	BT_RXD	DI	1.8 V
40	SPI_CLK	DO	1.8 V	40	BT_CTS	DO	1.8 V
41	I2C_SCL	OD	An external 1.8 V pull-up resistor is required.	41	I2C_SCL	OD	An external 1.8 V pull-up resistor is required.
42	I2C_SDA	OD	An external 1.8 V pull-up resistor is required.	42	I2C_SDA	OD	An external 1.8 V pull-up resistor is required.
43	RESERVED	-	-	43	RESERVED	-	-

44	ADC1	AI	0–VBAT_BB	44	ADC1	AI	0.3 V–VBAT_BB
45	ADC0	AI	0–VBAT_BB	45	ADC0	AI	0.3 V–VBAT_BB
46	GND	-	GND	46	GND	-	GND
47	RESERVED	-	-	47	ANT_GNSS	AI	-
48	GND	-	GND	48	GND	-	GND
49	ANT_MAIN	AIO	-	49	ANT_MAIN	AIO	-
50–54	GND	-	GND	50–54	GND	-	GND
55	RESERVED	-	-	55	RESERVED	-	-
56	GND	-	GND	56	GND	-	GND
57	VBAT_RF	PI	3.4–4.5 V	57	VBAT_RF	PI	3.3–4.3 V
58	VBAT_RF	PI	3.4–4.5 V	58	VBAT_RF	PI	3.3–4.3 V
59	VBAT_BB	PI	3.4–4.5 V	59	VBAT_BB	PI	3.3–4.3 V
60	VBAT_BB	PI	3.4–4.5 V	60	VBAT_BB	PI	3.3–4.3 V
61	STATUS	OD	-	61	STATUS	OD	-
62	MAIN_RI	DO	1.8 V	62	RI	DO	1.8 V
63	MAIN_DCD	DO	1.8 V	63	DCD	DO	1.8 V
64	MAIN_CTS	DO	1.8 V	64	CTS	DO	1.8 V
65	MAIN_RTS	DI	1.8 V	65	RTS	DI	1.8 V

66	MAIN_DTR	DI	1.8 V	66	DTR	DI	1.8 V
67	MAIN_TXD	DO	1.8 V	67	TXD	DO	1.8 V
68	MAIN_RXD	DI	1.8 V	68	RXD	DI	1.8 V
69	USB_DP	AIO	-	69	USB_DP	AIO	-
70	USB_DM	AIO	-	70	USB_DM	AIO	-
71	USB_VBUS	AI	3.0–5.25 V	71	USB_VBUS	PI	3.0–5.25 V
72	GND	-	GND	72	GND	-	GND
73	RGMII/RMII_RX_1	DI	1.8/ 3.3 V	73	RESERVED	-	-
74	RGMII/RMII_CTL_RX	DI	1.8/ 3.3 V	74	RESERVED	-	-
75	RGMII/RMII_CLK	DI	1.8/ 3.3 V	75	RESERVED	-	-
76	RGMII/RMII_RX_0	DI	1.8/ 3.3 V	76	RESERVED	-	-
77	RGMII/RMII_TX_0	DO	1.8/ 3.3 V	77	RESERVED	-	-
78	RGMII/RMII_TX_1	DO	1.8/ 3.3 V	78	RESERVED	-	-
79	RGMII_RX_2	DI	1.8 V	79	RESERVED	-	-
80	RGMII_TX_2	DO	1.8 V	80	RESERVED	-	-
81	RGMII/RMII_CTL_TX	DO	1.8/ 3.3 V	81	RESERVED	-	-
82	RGMII_RX_3	DI	1.8 V	82	RESERVED	-	-
83	RGMII_CK_TX	DO	1.8 V	83	RESERVED	-	-

84	RGMII_TX_3	DO	1.8 V	84	RESERVED	-	-
85–112	GND	-	GND	85–112	GND	-	GND
113	RESERVED	-	-	113	RESERVED	-	-
114	RESERVED	-	-	114	RESERVED	-	-
115	USB_BOOT	DI	1.8 V	115	USB_BOOT	DI	1.8 V
116	RESERVED	-	-	116	RESERVED	-	-
117	RESERVED	-	-	117	RESERVED	-	-
118	RESERVED	-		118	WLAN_SLP_CLK	DO	1.8 V
119	RGMII/RMII_RST_N	DO	1.8 V	119	EPHY_RST_N	DO	1.8/ 2.85 V
120	RGMII/RMII_INT	DI	1.8/ 3.3 V	120	EPHY_INT_N	DI	1.8 V
121	RGMII/RMII_MD_IO	DIO	1.8/ 3.3 V	121	SGMII_MDATA	DIO	1.8/ 2.85 V
122	RGMII/RMII_MD_CLK	DO	1.8/ 3.3 V	122	SGMII_MCLK	DO	1.8/ 2.85 V
123	SPK_N	AO	-	123	SGMII_TX_M	AO	-
124	SPK_P	AO	-	124	SGMII_TX_P	AO	-
125	MIC_P	AI	-	125	SGMII_RX_P	AI	-
126	MIC_N	AI	-	126	SGMII_RX_M	AI	-
127	WLAN_PWR_EN	DO	1.8 V	127	PM_ENABLE	DO	1.8 V
128	RESERVED	-	-	128	USIM2_VDD	PO	1.8/ 2.85 V

129	WLAN_SDIO_DATA3	DIO	1.8 V	129	SDC1_DATA3	DIO	1.8 V
130	WLAN_SDIO_DATA2	DIO	1.8 V	130	SDC1_DATA2	DIO	1.8 V
131	WLAN_SDIO_DATA1	DIO	1.8 V	131	SDC1_DATA1	DIO	1.8 V
132	WLAN_SDIO_DATA0	DIO	1.8 V	132	SDC1_DATA0	DIO	1.8 V
133	WLAN_SDIO_CLK	DO	1.8 V	133	SDC1_CLK	DO	1.8 V
134	WLAN_SDIO_CMD	DIO	1.8 V	134	SDC1_CMD	DIO	1.8 V
135	WLAN_WAKE	DI	1.8 V	135	WAKE_ON_ WIRELESS	DI	1.8 V
136	WLAN_EN	DO	1.8 V	136	WLAN_EN	DO	1.8 V
137	RESERVED	-	-	137	COEX_UART_RX	DI	1.8 V
138	RESERVED	-	-	138	COEX_UART_TX	DO	1.8 V
139	RESERVED	-	-	139	BT_EN	DO	1.8 V
140	MICBIAS	PO	-	140	RESERVED	-	-
141	RESERVED	-	-	141	RESERVED	-	-
142	RESERVED	-	-	142	RESERVED	-	-
143	RESERVED	-	-	143	RESERVED	-	-
144	RESERVED	-	-	144	RESERVED	-	-

NOTE

1. Keep all reserved and unused pins unconnected.
2. All GND pins should be connected to ground.
3. For more details about Wi-Fi & Bluetooth, SGMII and RGMII/RMII functions, see ***document [1]*** & ***[2]*** & ***[3]*** & ***[4]***.
4. Pins in blue have different functions or voltage domain, but the module footprints are compatible.

4 Hardware Reference Design

The following sub-chapters outline the main functionalities of the compatible design among EC200A and EC2x modules.

4.1. Power Supply

Use a TVS diode with low reverse stand-off voltage V_{RWM}, low clamping voltage V_C and high reverse peak pulse current I_{PP} to ensure the power source stability. A reference design for +5.0 V input power source and the power supply in a star configuration routing are presented in the figure below.

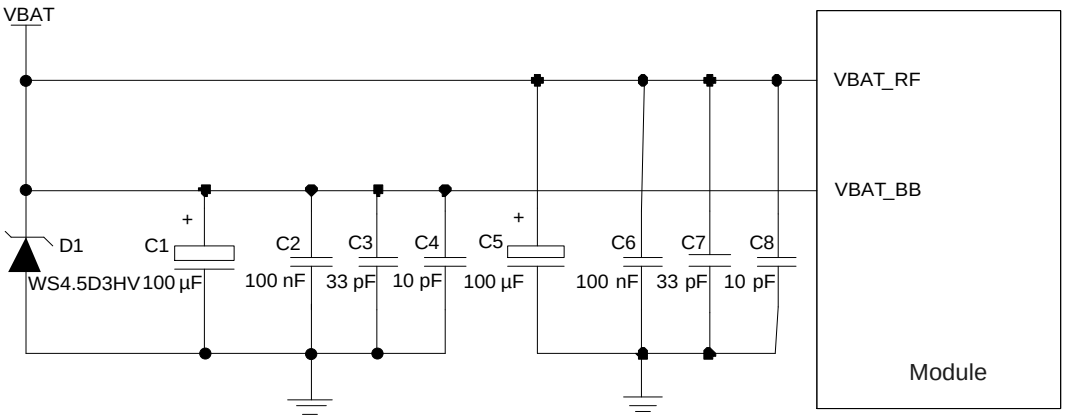


Figure 2: Power Supply in Star Configuration Routing

The power supply for EC2x family should be able to provide the current up to 2.0 A. For EC200A series, the power supply should be able to provide up to 3.0 A as it supports the GSM network.

A reference design for + 5.0 V input power source is presented in the figure below. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

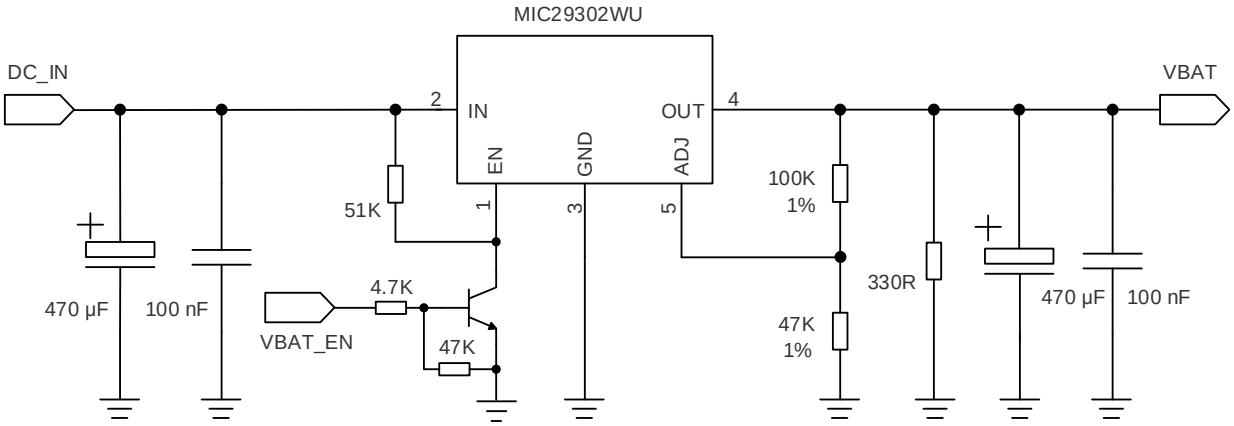


Figure 3: Power Supply Reference Design

4.2. Turn-on/-off

4.2.1. Turn-on

A reference design for the turn-on circuit of the modules is presented in the figure below.

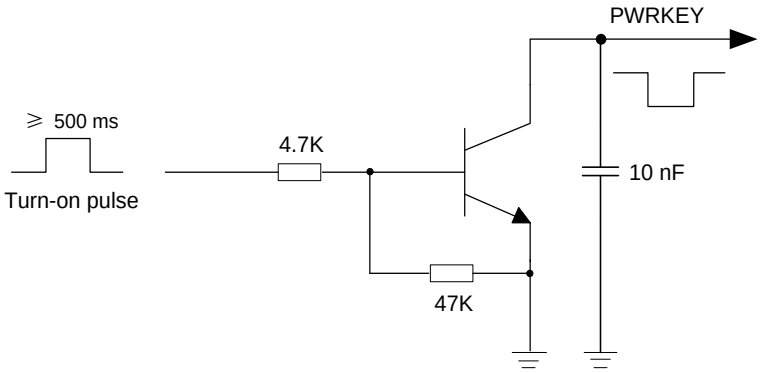


Figure 4: Turn-on Circuit

The power-up scenario of EC200A series is illustrated in the figure below.

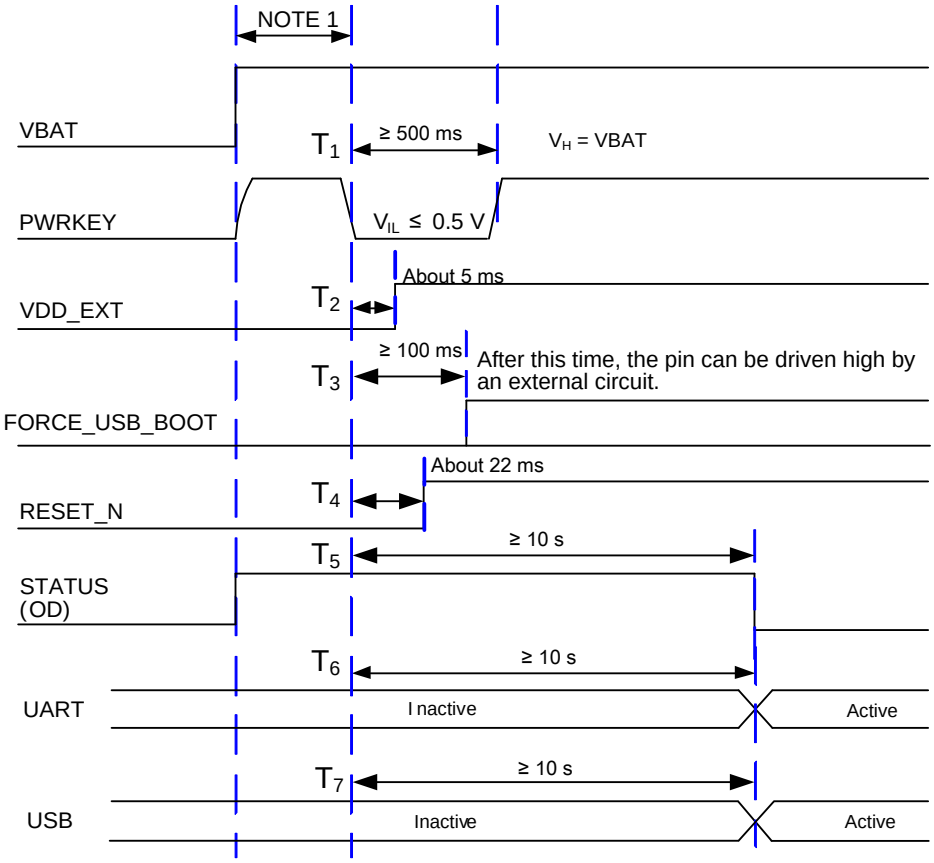


Figure 5: Power-up Timing (EC200A Series)

The power-up scenario of EC2x family is illustrated in the figure below.

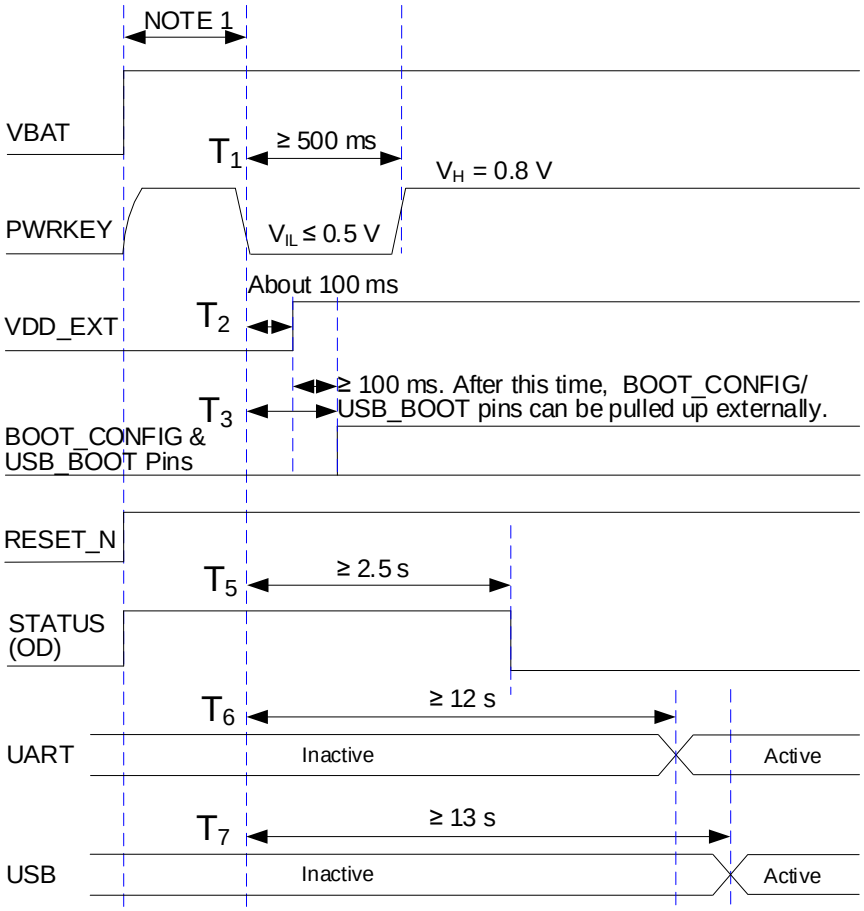


Figure 6: Power-up Timing (EC2x Family)

The power-up timing for EC200A and EC2x modules is illustrated in the table below.

Table 6: Power-up Timing of EC200A and EC2x

Module	T_1	T_2	T_3	T_4	T_5	T_6	T_7
EC200A Series	≥ 500 ms	Typ. 5 ms	≥ 100 ms	Typ. 22 ms	≥ 10 s	≥ 10 s	≥ 10 s
EC25 Series/ EC21 Series/ EC20-CE	≥ 500 ms	Typ. 100 ms	≥ 200 ms	-	≥ 2.5 s	≥ 12 s	≥ 13 s

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. The interval between powering up VBAT and pulling down PWRKEY pin should be at least 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended resistor if the module needs to be powered on automatically and shutdown is not needed. The pull-down resistors of EC200A series should be 4.7 kΩ each, and the pull-down resistor of EC2x family should be 10 kΩ.
3. RESET_N pin of EC200A series should be pulled up after pulling down the PWRKEY pin, and RESET_N pin of EC2x family should be pulled up after the VBAT pin is powered on.

4.2.2. Turn-off

The following is a reference design of the turn-off circuit for The modules.

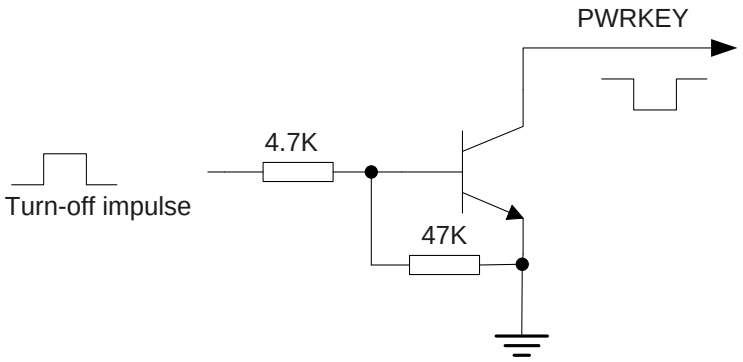


Figure 7: Turn-off Circuit

4.2.2.1.Turn-off with PWRKEY

The turn-off scenario for EC200A and EC2x modules is illustrated in the figure below.

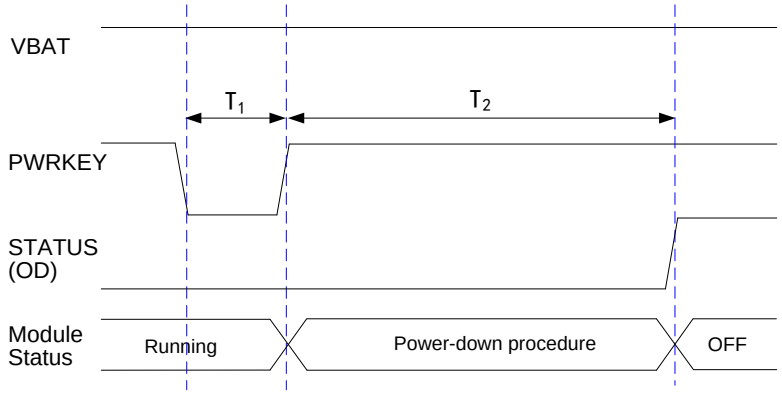


Figure 8: Turn-off with PWRKEY Timing

The turn-off with PWRKEY timing for EC200A and EC2x modules is illustrated in the table below.

Table 7: Turn-off with PWRKEY Timing for EC200A and EC2x

Module	T_1	T_2
EC200A Series	≥ 650 ms	4~12 s
EC25 Series/EC21 Series/EC20-CE	≥ 650 ms	≥ 29.5 s

4.2.2.2.Turn-off with AT Command

The modules can also be safely turned off with **AT+QPOWD**, which is similar to turning off the module via PWRKEY pin. See ***document [5]*** & ***[6]*** or more information about **AT+QPOWD**.

NOTE

1. To avoid damaging the internal flash, do not switch off the power supply when the modules are working normally. The power supply can be cut off only after the modules are shut down with PWRKEY or AT command.
2. When turning off the modules with the AT command, keep PWRKEY at high level after executing the command. Otherwise, the modules will turn on again after being turned off.

4.3. Reset

Use RESET_N only in case of failure to turn off the modules with **AT+QPOWD** or PWRKEY pin. A reference design for the module reset signal circuit is presented in the figures below.

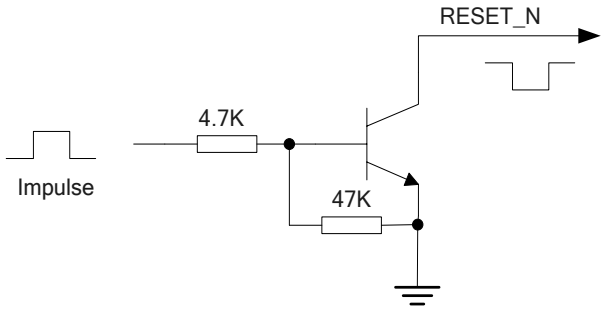


Figure 9: RESET_N Reference Circuit

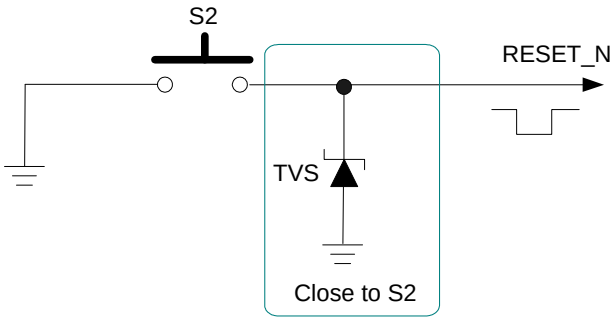


Figure 10: Reference Circuit of RESET_N by Using a Button

The reset scenarios of EC200A and EC2x modules are illustrated in the figures below.

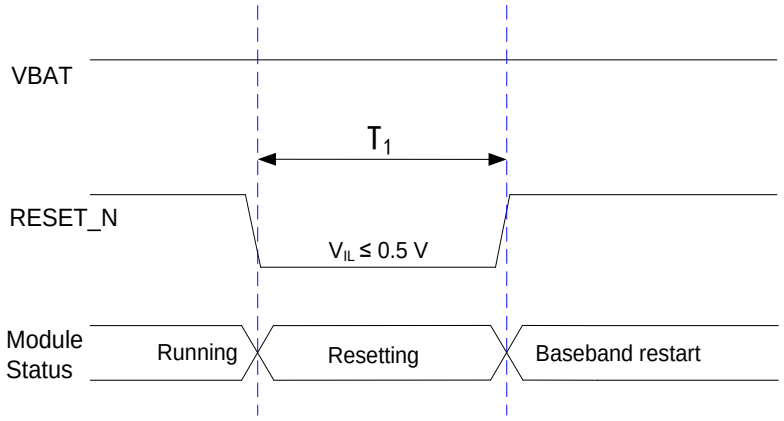


Figure 11: Reset Timing (EC200A Series)

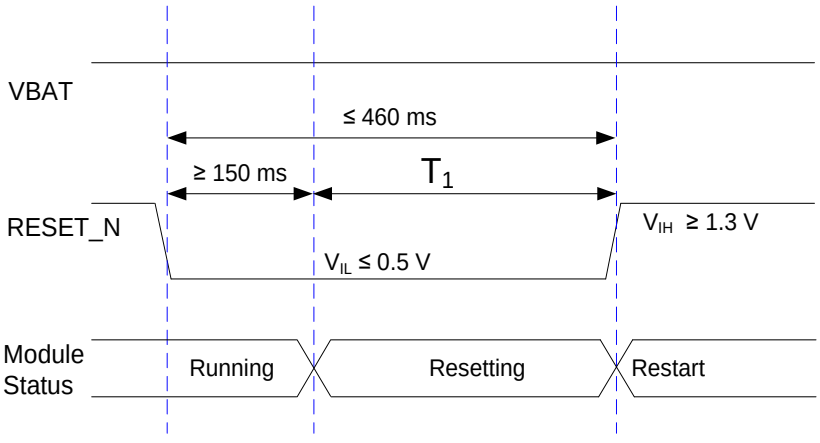


Figure 12: Reset Timing (EC2x Family)

The reset timing of EC200A and EC2x modules is presented in the table below.

Table 8: Reset Timing of EC200A and EC2x

Module	T_1
EC200A Series	≥ 300 ms
EC25 Series/EC21 Series/EC20-CE	150 ms ≤ T_1 ≤ 460 ms

NOTE

1. The RESET_N pin of EC200A series only resets the baseband chip inside the module, not the power management chip, whereas EC20-CE's RESET_N can reset the power management chip.
2. When the RESET_N pin of EC200A series is pulled down, the baseband chip is in the reset state, and the chip system restarts after the pin is released.
3. Ensure that the load capacitance does not exceed 10 nF on PWRKEY and RESET_N pins.

4.4. (U)SIM Interface

(U)SIM interface of the modules meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported. The reference design of the (U)SIM interface with an 8-pin (U)SIM card connector is presented in the figure below.

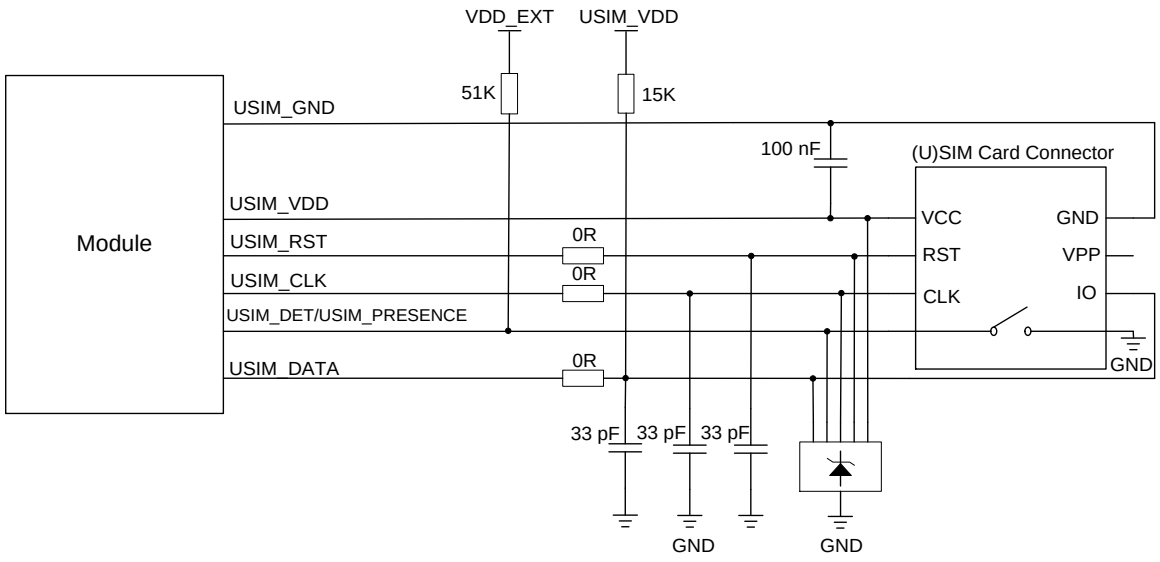


Figure 13: Reference Design of (U)SIM Interface with 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET/USIM_PRESENCE unconnected. The reference design of (U)SIM interface with a 6-pin (U)SIM card connector is presented in the figure below.

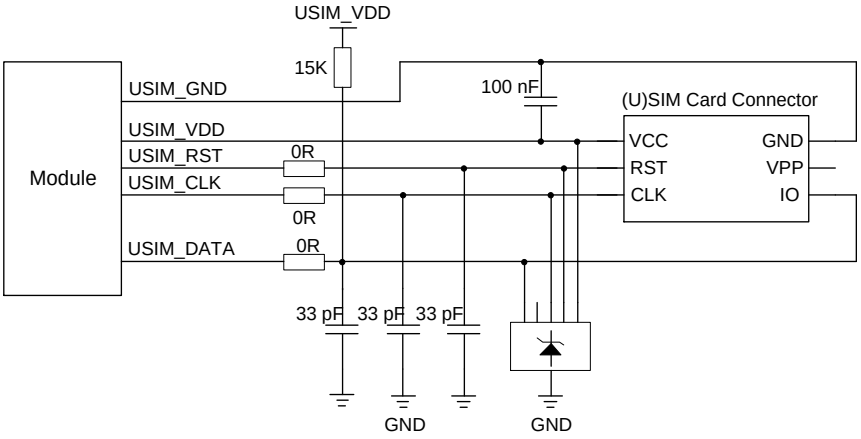


Figure 14: Reference Design of (U)SIM Interface with 6-Pin (U)SIM Card Connector

4.5. USB Interface

EC200A and EC2x contain one integrated Universal Serial Bus (USB) interface complying with USB 2.0 specification, with high-speed (480 Mbps) and full-speed (12 Mbps) modes supported.

The USB interface of the modules can only be a slave device and is used for AT command communication, data transmission, GNSS NMEA sentence outputting [6], software debugging and firmware upgrading.

The USB interface should be reserved for firmware upgrading in your design. USB interface reference design is presented in the figure below.

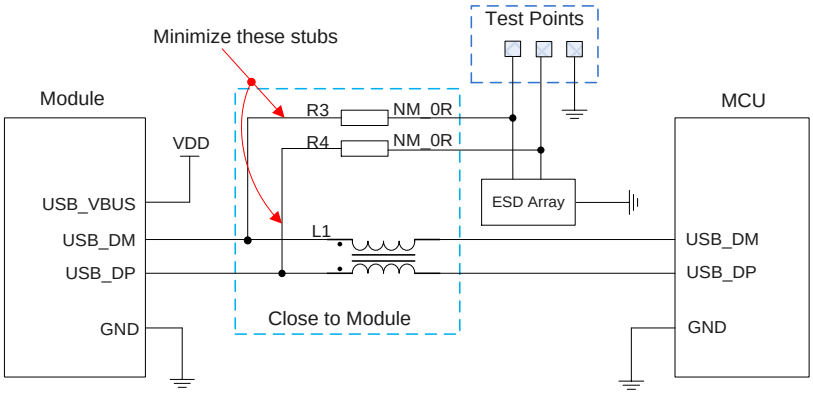


Figure 15: USB Interface Reference Design

[6] The USB interface on EC200A series modules does not support GNSS NMEA sentence outputting.

To suppress EMI spurious transmission, it is recommended to add an L1 common mode choke in series between the module and your MCU. In addition, the 0 Ω resistors (R1 and R2) should be added in series between the module and the test points to facilitate debugging, since they are not mounted by default. To ensure the integrity of USB data line signal, components L1, R1 and R2 must be placed close to the module, and R1 and R2 resistors should be placed close to each other. Extra trace stubs must be as short as possible.

4.6. PCM and I2C Interfaces

EC200A and EC2x support one PCM interface for audio applications and one I2C interface.

Reference design of module PCM and I2C interfaces with external codec IC is presented below.

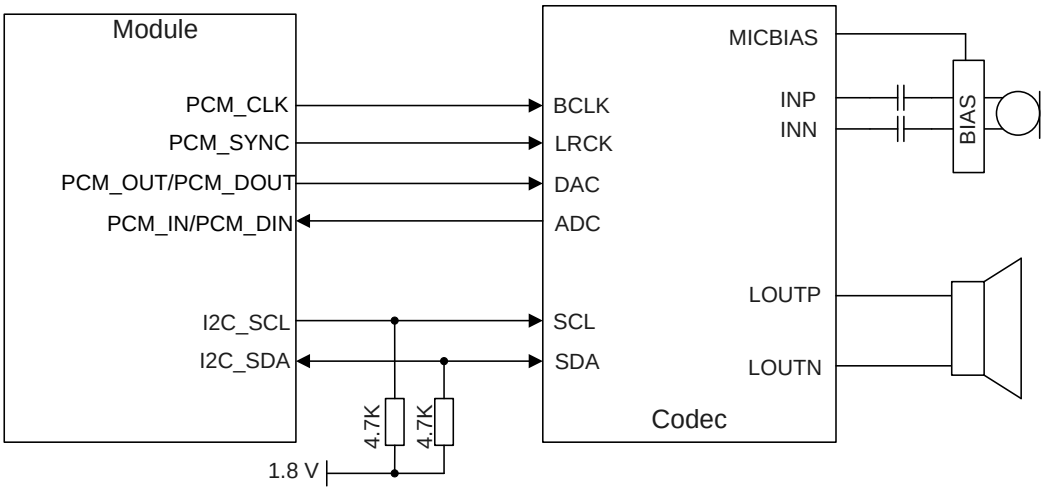


Figure 16: Reference Design of PCM and I2C Interface with Audio Codec

NOTE

1. Reserve RC (R = 22 Ω, C = 22 pF) circuits on PCM traces, especially for PCM_CLK, and close to codec.
2. EC200A and EC2x modules are master devices.

4.7. UART Interfaces

EC200A and EC2x support one main UART and one debug UART interface.

The main UART interface can be used for data transmission and AT command communication. In addition, it supports RTS and CTS hardware flow control.

EC200A series' debug UART interface supports 115200 bps baud rate, and is used for partial log outputting. EC2x family's debug UART interface can be used as a Linux console and a log output.

EC200A and EC2x modules have a 1.8 V UART interface. A level translator should be used if the application has a 3.3 V UART interface. TXS0108EPWR level translator by *Texas Instruments* is recommended. And you can visit http://www.ti.com for more information. A reference design is illustrated in the following figure.

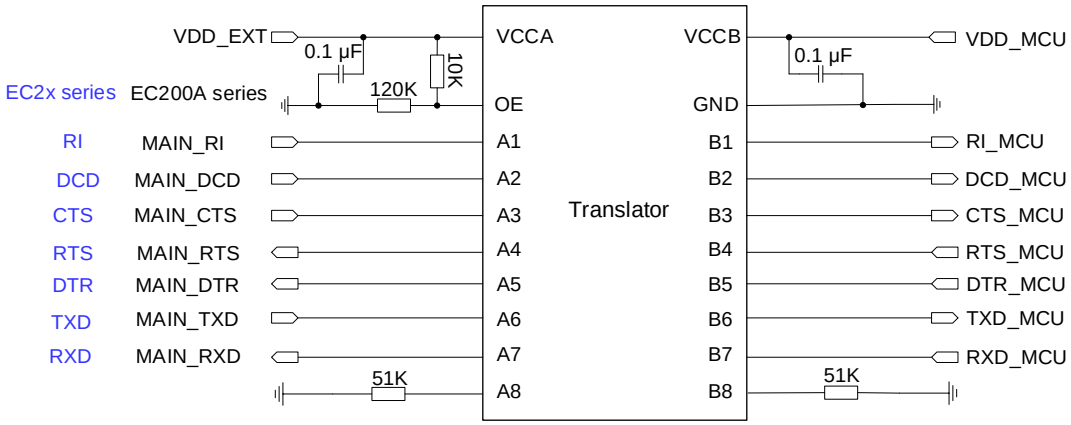


Figure 17: Reference Design of Voltage-Level Translation Using IC

Another example of a voltage-level translator with transistor reference design is shown below. For the design of circuits shown in dotted lines, please refer to that shown in solid lines, but pay attention to the direction of connection.

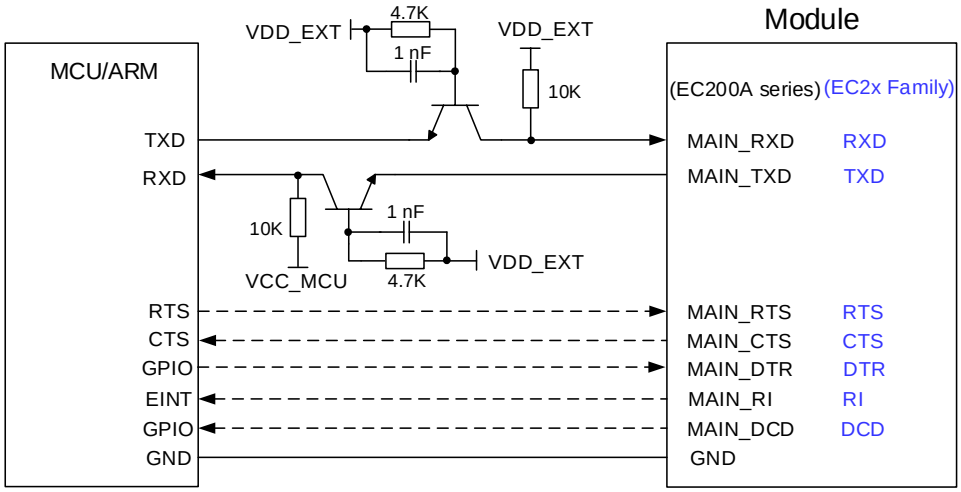


Figure 18: Reference Design of Voltage-level Translation Using Transistors

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.8. Antenna Interfaces

4.8.1. RF Antenna Interface

The ANT_MAIN pins on the modules are compatible. The impedance of RF antenna interface is 50 Ω. For better RF performance, a π-type matching circuit should be reserved, and the π-type matching components should be placed as close to the antenna as possible.

EC200A and EC2x support Rx-diversity function via ANT_DIV/ANT_DRX interface. ANT_DIV/ANT_DRX antenna interface reference design of the modules is shown below.

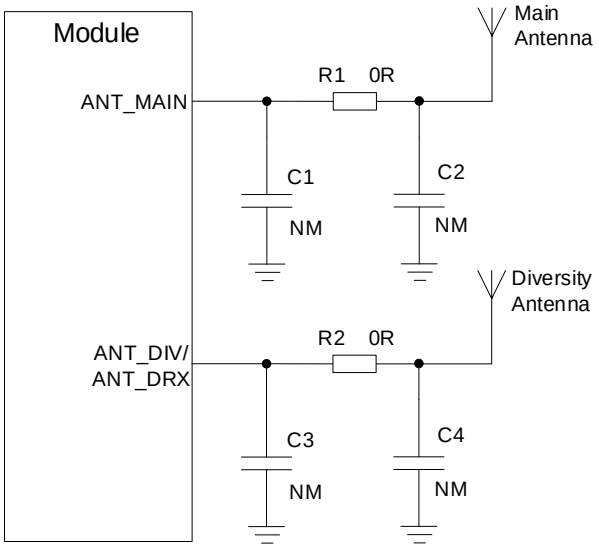


Figure 19: RF Antenna Interface Reference Design

NOTE

1. To improve receiver sensitivity, ensure the proper distance between the main antenna and the Rx-diversity antenna.
2. Place the π-type matching components (R1 & C1 & C2 and R2 & C3 & C4) as close to the antenna as possible.

4.8.2. GNSS Antenna Interface

EC25 series, EC21 series, and EC20-CE modules support a GNSS antenna with ANT_GNSS pin. A reference design of ANT_GNSS antenna interface of EC2x family is shown below.

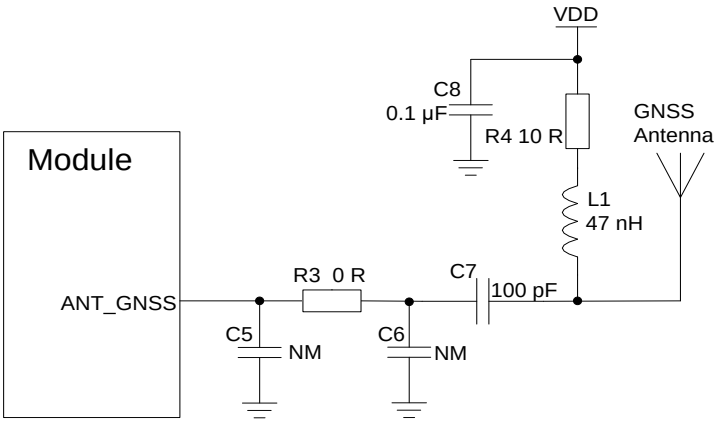


Figure 20: Reference Design of GNSS Antenna Interface (EC2x Family)

It is recommended to reserve C5, R3 and C6 for adjusting antenna impedance. C5 and C6 are not mounted by default, and R3 is only mounted with a 0 Ω resistor. The impedance of the RF trace should be controlled at about 50 Ω, and the trace should be as short as possible.

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5 Recommended Footprints

The recommended compatible footprint of the modules is shown in the following figure. All dimensions are in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

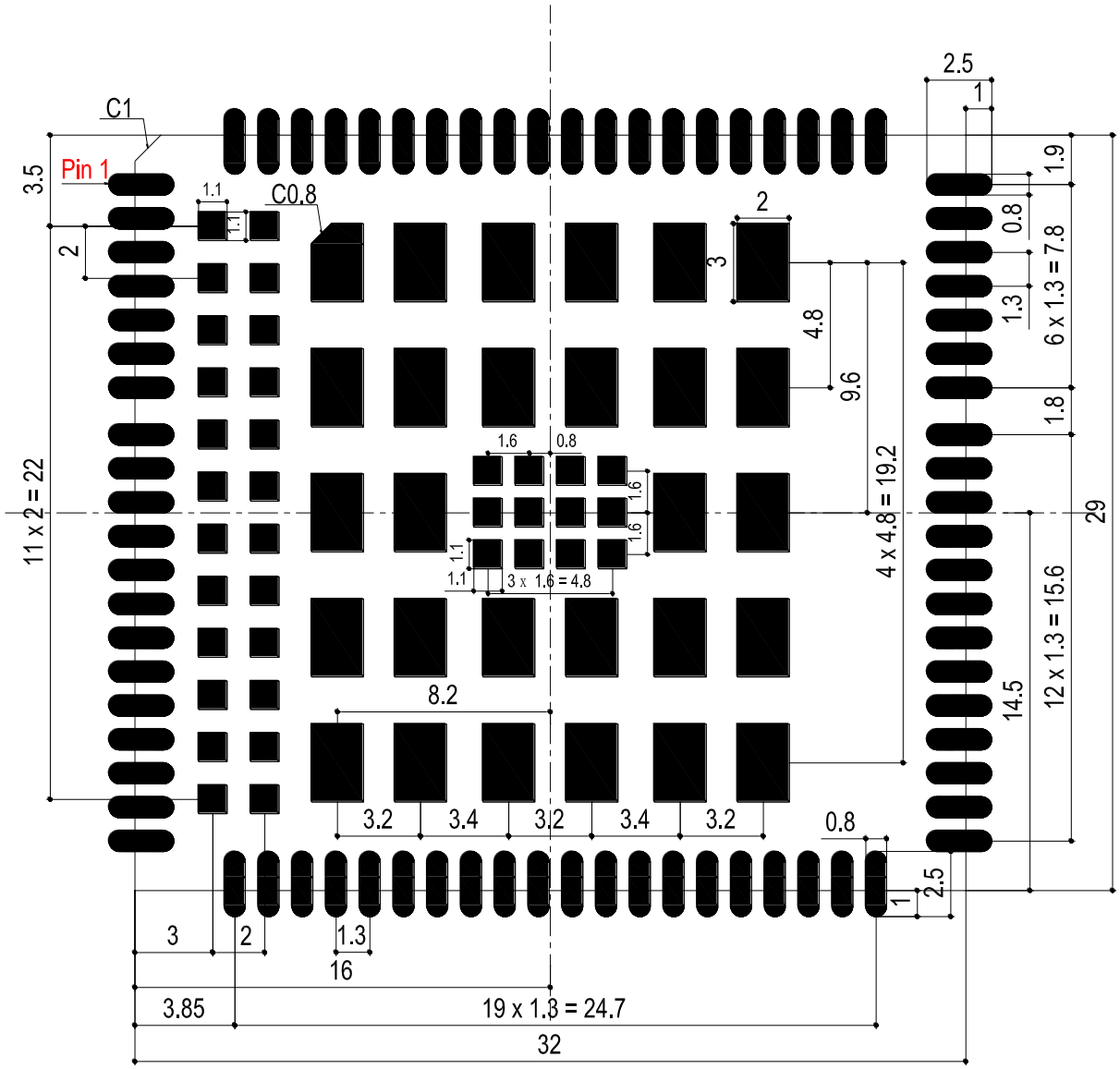


Figure 21: Recommended Compatible Footprint (EC200A & EC2x)

If SGMII, RGMII/RMII, audio, or Wi-Fi function is not needed, clear the keepout area for pins 73-84 and 117–140 in the compatible design. The recommended compatible footprint without SGMII, RGMII/RMII, audio, or Wi-Fi function is presented in the figure below.

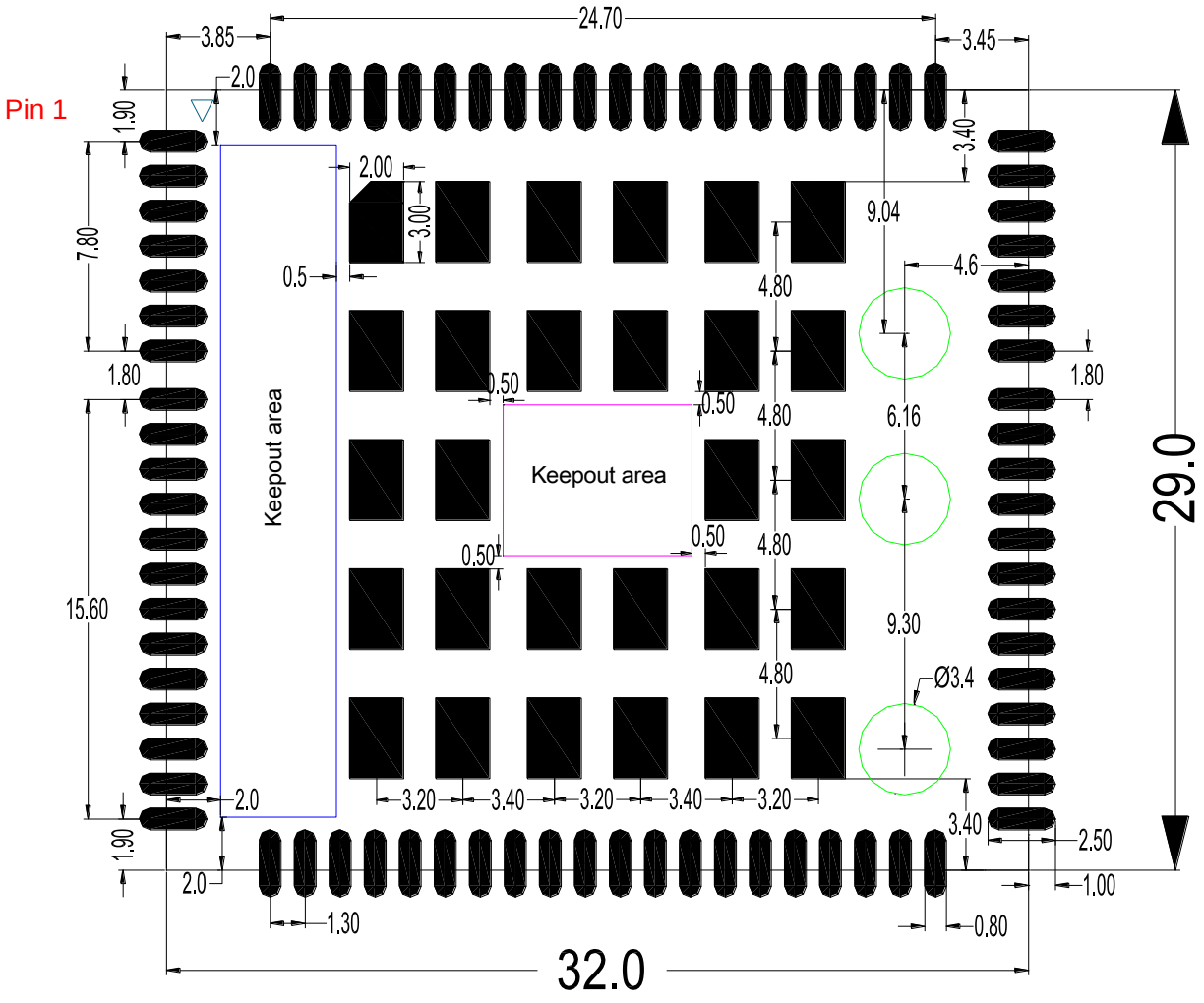


Figure 22: Recommended Compatible Footprint Without SGMII, RGMII/RMII, Audio or Wi-Fi Function

NOTE

1. If SGMII, RGMII/RMII, audio or Wi-Fi function is not needed, do not design the keepout area marked in purple and clear the keepout area marked in blue for pins 117–140.
2. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6 Appendix References

Table 9: Related Documents

Document Name
[1] Quectel_EC200A_Series_Hardware_Design
[2] Quectel_EC25_Series_Hardware_Design
[3] Quectel_EC21_Series_Hardware_Design
[4] Quectel_EC20_R2.1_Hardware_Design
[5] Quectel_EC200x&EG912Y&EC600S_Series_AT_Commands_Manual
[6] Quectel_EC2x&EG9x&EG2x-G&EM05_Series_AT_Commands_Manual
[7] Quectel_EC200A_Series_Reference_Design
[8] Quectel_EC2x&EG2x-G_Reference_Design

Table 10: Terms and Abbreviations

Abbreviation	Description
bps	Bits Per Second
CDMA	Code-Division Multiple Access
CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTR	Data Terminal Ready
EMI	Electromagnetic Interference
FDD	Frequency Division Duplex

Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Russian Global Navigation Satellite System
GND	Ground
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
I2C	Inter-Integrated Circuit
I/O	Input/Output
LCC	Leadless Chip Carrier
LCD	Liquid Crystal Display
LDO	Low-dropout Regulator
LGA	Land Grid Array
LTE	Long Term Evolution
MCU	Microcontroller Unit/Microprogrammed Control Unit
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RTS	Real-Time Clock
SDIO	Secure Digital Input/Output
SGMII	Serial Gigabit Media Independent Interface
SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter

UL	Uplink
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VDD	Drain Voltage
V_{rwm}	Reverse Working Maximum Voltage
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network