



**SAN FRANCISCO
STATE UNIVERSITY**

Course: Digital VLSI Design

Course Instructor: Dr. Hamid Mahmoodi

PROJECT REPORT

ON

16X8 SRAM IN 14nm CMOS TECHNOLOGY

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SRAM Overview in the Project Context:

In this project, a **16x8 Static Random Access Memory (SRAM)** array was designed using **14nm CMOS technology**. The design includes key components like the memory cell, decoder, sense amplifier, precharge, driver circuits, and their integration into a complete top-level SRAM layout.

SRAM Cell Design

Each memory bit is implemented using a **6T (6-transistor) SRAM cell**, consisting of:

- **Two cross-coupled inverters** that form a stable latch to store a bit.
- **Two NMOS access transistors** that connect the storage node to the bitlines during read/write operations when the wordline is enabled.

This structure offers:

- **Non-destructive reads.**
- **High-speed access.**
- **Low static power consumption** (since no refresh is needed like DRAM).

As shown in the schematic and layout on *page 3*, the cell area is **0.232 μm^2** , reflecting an efficient design for 14nm scaling.

16x8 SRAM Array

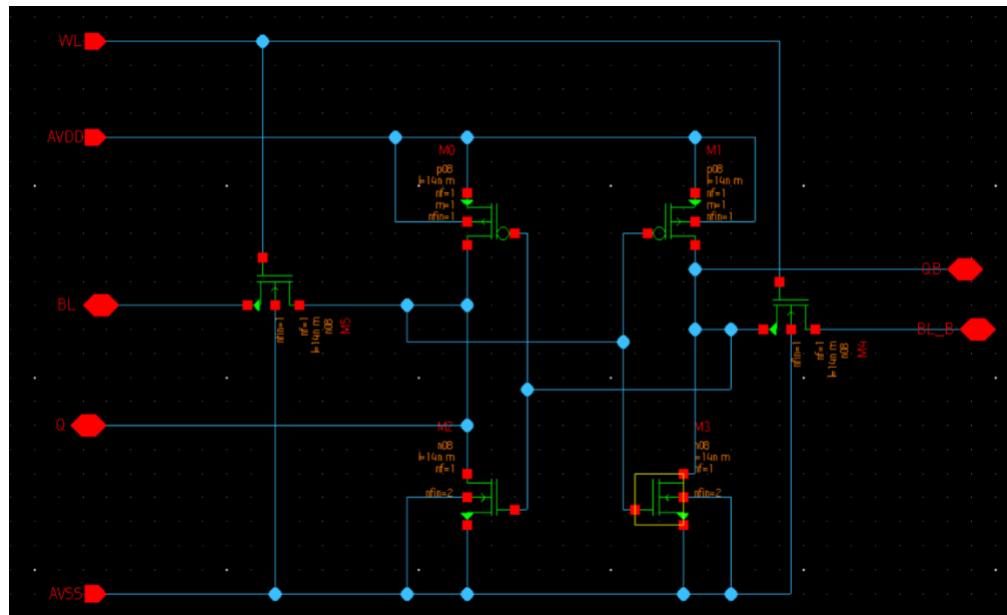
The complete array consists of **16 rows and 8 columns**, allowing storage of 128 bits total. The full schematic and layout are provided on *page 5*, with a total array area of **74.99 μm^2** .

Verification and Validation

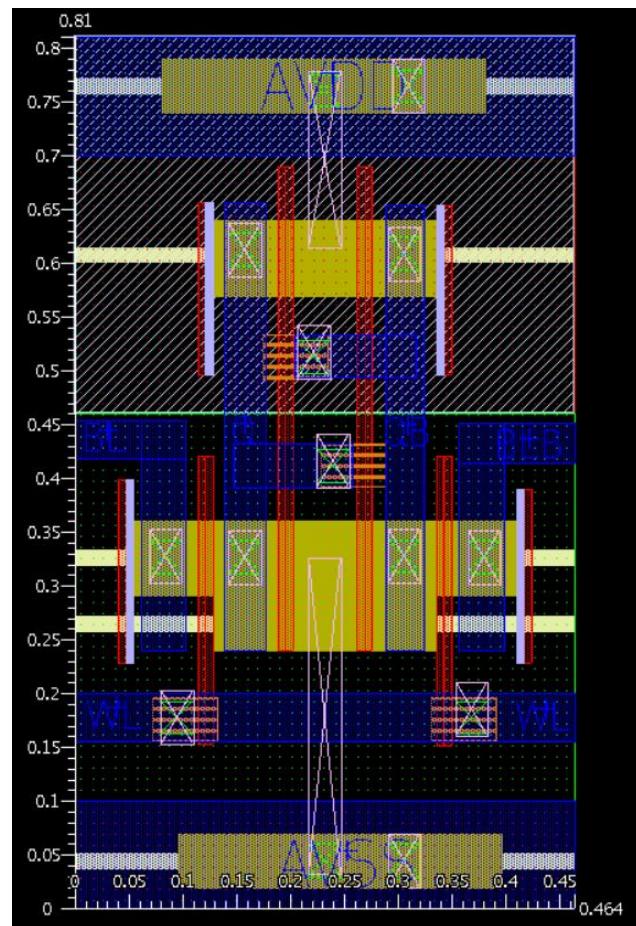
The design underwent rigorous verification:

- **Design Rule Check (DRC):** Passed without any violations — ensures manufacturability.
- **Layout Versus Schematic (LVS):** Passed — confirms that the physical layout matches the intended circuit schematic.

- SRAM Schematic:

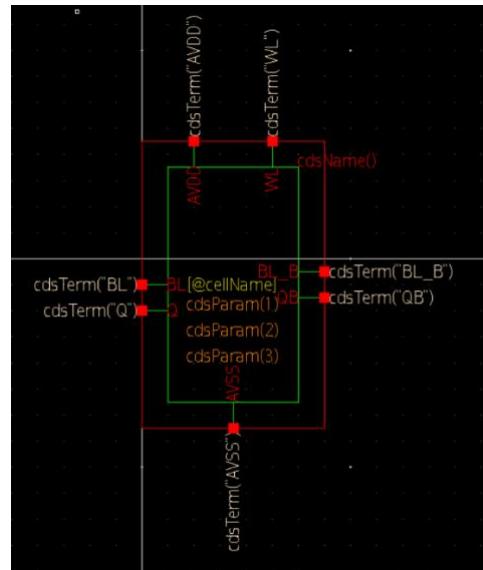


- SRAM Layout:

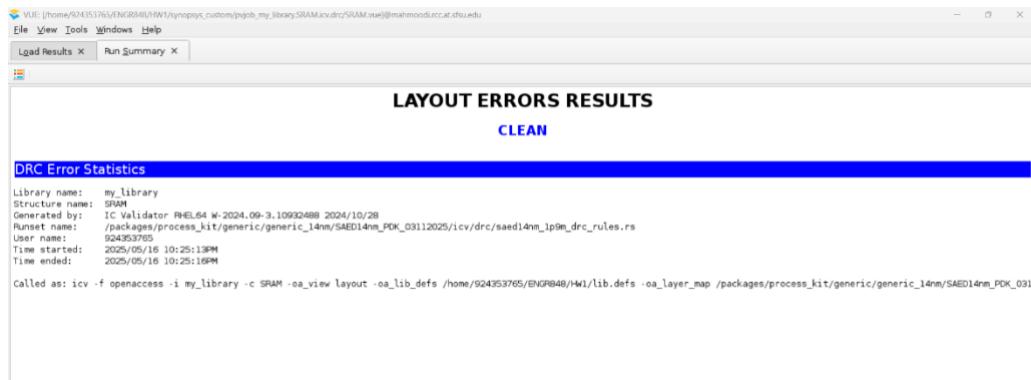


$$\text{Area: } 0.464 \times 0.81 = 0.232 \mu\text{m}^2$$

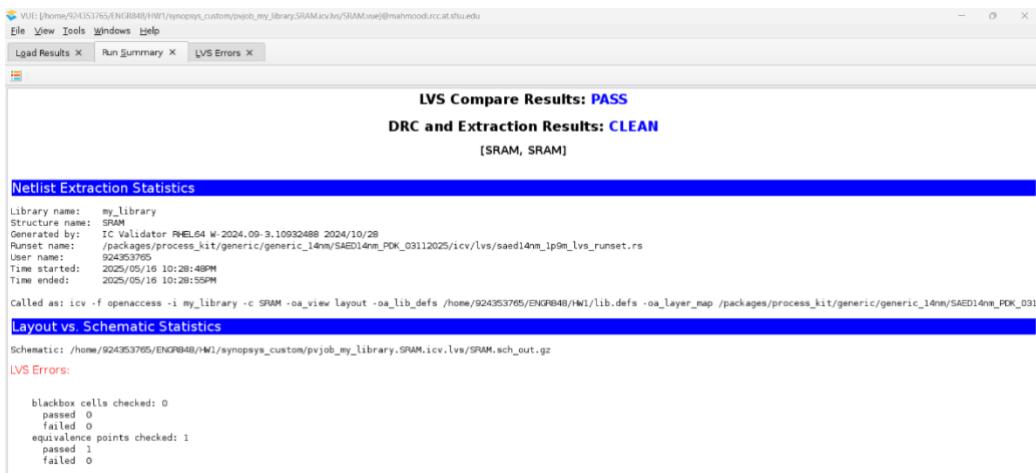
- SRAM Symbol:



- Design Rule Check:

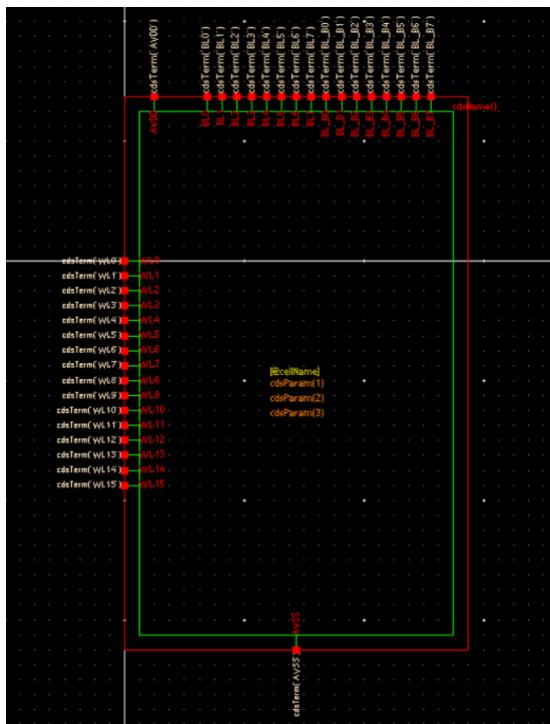
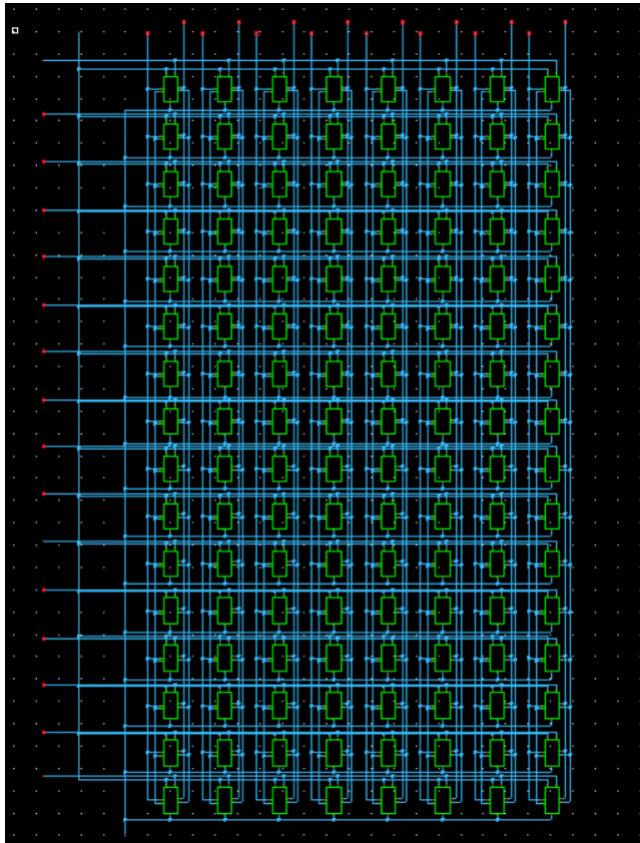


- Layout Versus Schematic:



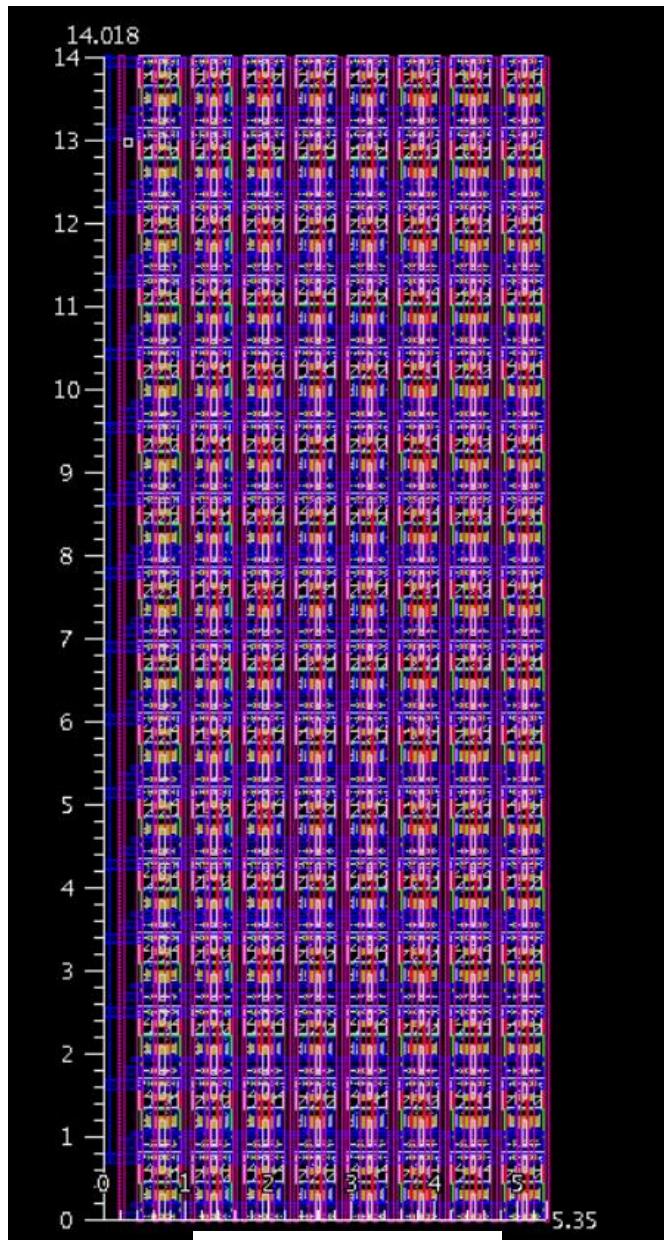
- 16x8 SRAM Schematic

As per the Project requirement, Designed a 16x8 SRAM Array.



Symbol

- 16x8 SRAM Layout:



Area: 74.99 μm^2

- Design Rule Check:

VUE: [/home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.SRAM_ARRAY.icv.drc/SRAM_ARRAY.vue]@mahmoodi.rcc.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

LAYOUT ERRORS RESULTS

CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: SRAM_ARRAY
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_lp9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/16 10:32:08PM
Time ended: 2025/05/16 10:32:12PM

Called as: icv -f openaccess -i my_library -c SRAM_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_P
```

- Layout Versus Schematic:

VUE: [/home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.SRAM_ARRAY.icv.lvs/SRAM_ARRAY.vue]@mahmoodi.rcc.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS

DRC and Extraction Results: CLEAN

[SRAM_ARRAY, SRAM_ARRAY]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: SRAM_ARRAY
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_lp9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/16 10:32:46PM
Time ended: 2025/05/16 10:33:01PM

Called as: icv -f openaccess -i my_library -c SRAM_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_P
```

Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.SRAM_ARRAY.icv.lvs/SRAM_ARRAY.sch_out.gz
```

LVS Errors:

```
blackbox cells checked: 0
  passed 0
  failed 0
equivalence points checked: 1
  passed 1
  failed 0
```

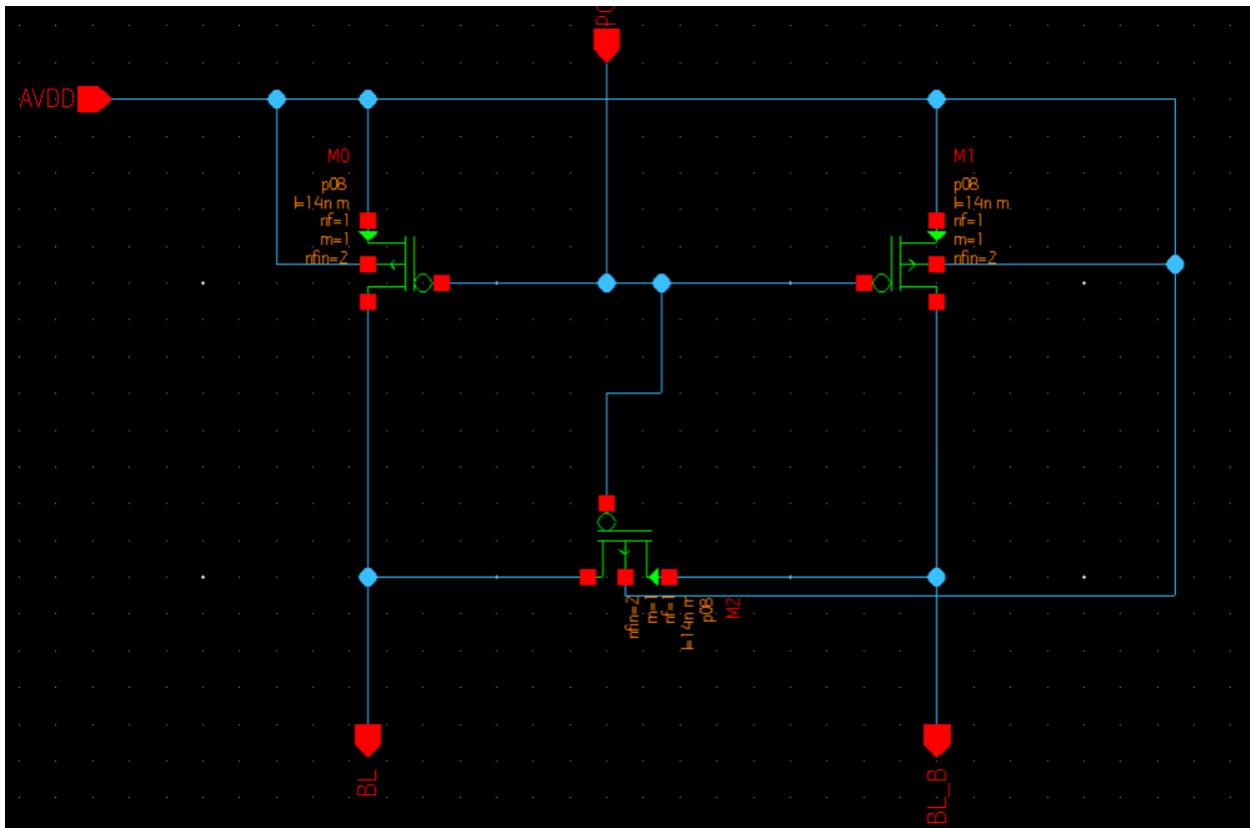
Pre-Charge

This pre-charge circuit uses three PMOS transistors (M0, M1, M2) to prepare the bitlines (BL and BLB) in a memory array before read/write operations.

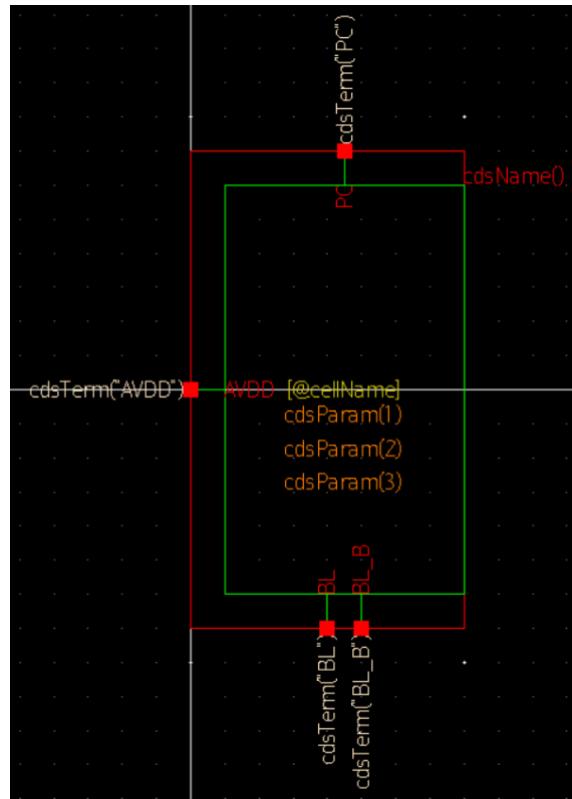
M0 and M1 are connected between the supply voltage (AVDD) and the bitlines. When the precharge control signal (PC) is low, these transistors turn on and charge BL and BLB to AVDD.

M2 is the equalization transistor. It connects BL and BLB, ensuring both lines are at the same voltage during precharge.

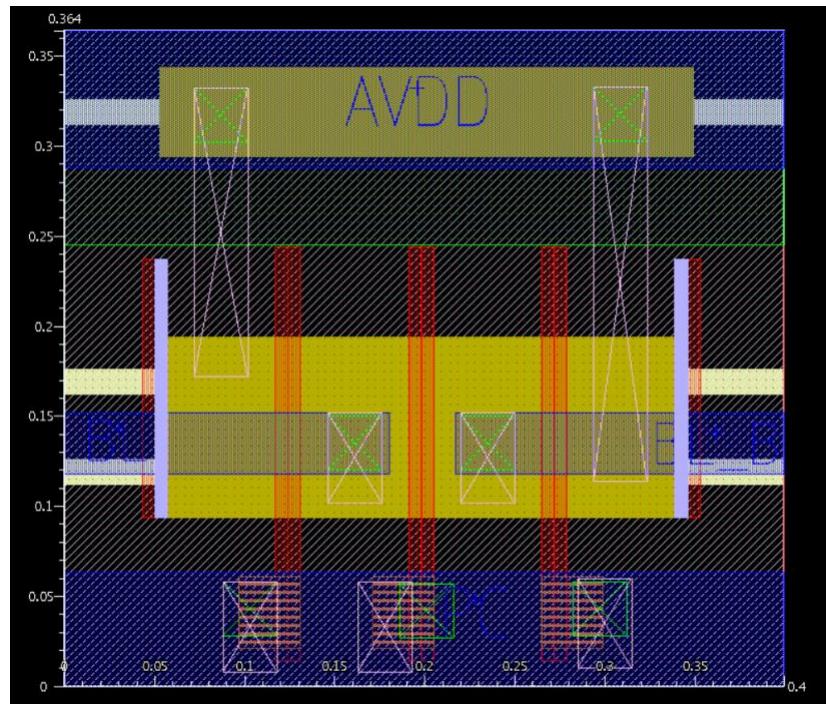
This setup improves speed and reliability by equalizing and precharging the bitlines before each memory access.



Schematic



Pre-Charge Symbol



Pre-Charge Layout

Area: 0.1456 um²

Design Rule Check (DRC) and Layout Versus Schematic (LVS)

To ensure the physical layout matches the design rules and schematic, both DRC and LVS checks were performed.

DRC Results:

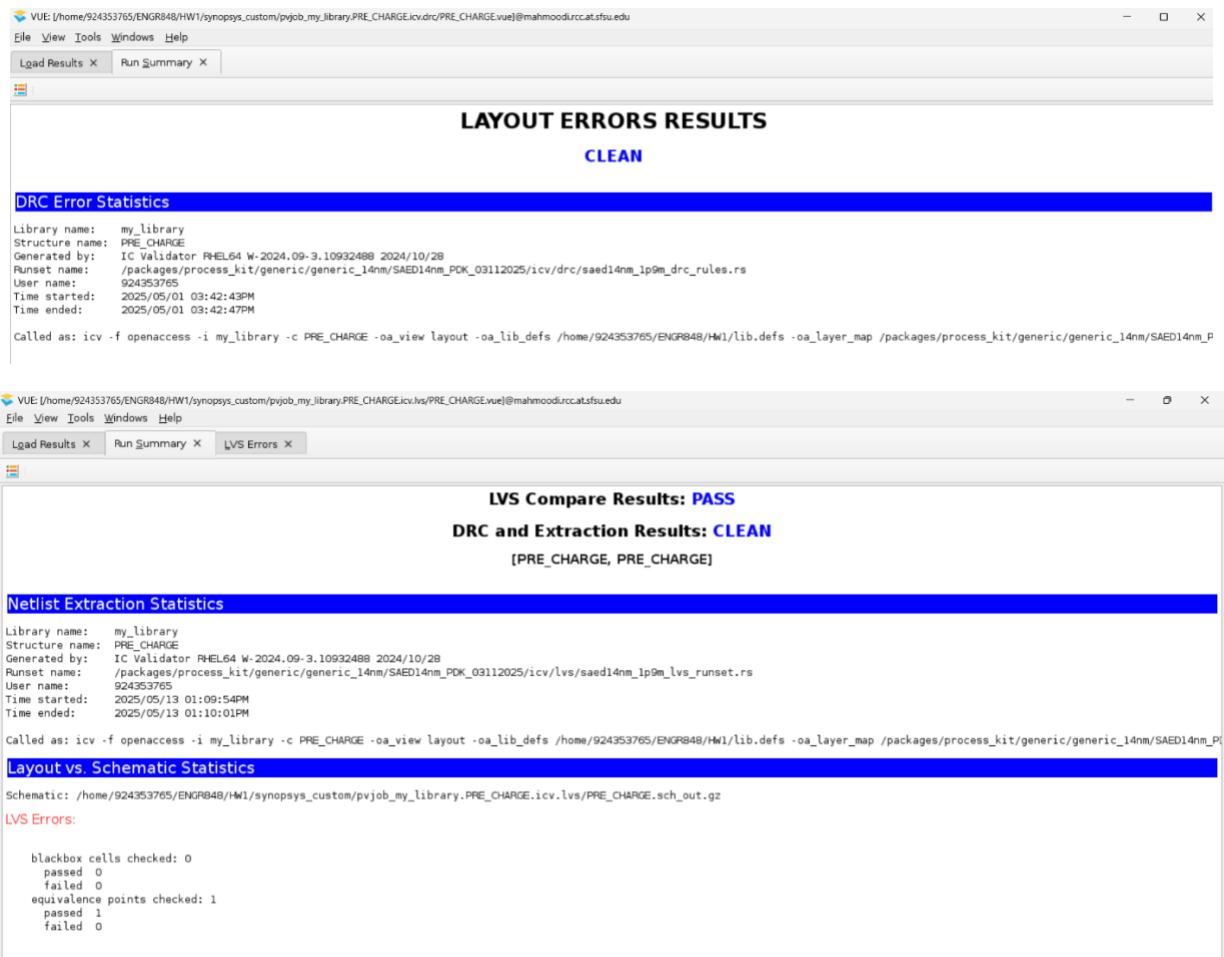
The Design Rule Check (DRC) confirms that the layout complies with the manufacturing rules defined by the technology. The results show:

- **Status: CLEAN**
- No layout violations were detected, indicating that the design meets all required fabrication constraints.

LVS Results:

The Layout Versus Schematic (LVS) check ensures the layout matches the intended circuit schematic.

- **LVS Compare Result: PASS**
- **DRC and Extraction Results: CLEAN**
- All devices and connections in the layout were found to match the schematic. No errors or mismatches were reported.



The screenshot shows two windows of the VUE (Synopsys Custom) software. The top window displays the 'LAYOUT ERRORS RESULTS' page, which is labeled 'CLEAN'. It includes a 'DRC Error Statistics' section with detailed log information. The bottom window displays the 'LVS Errors' page, which is also labeled 'CLEAN'. It includes sections for 'Netlist Extraction Statistics' and 'Layout vs. Schematic Statistics', both of which show 'PASS' results. The logs in these sections provide specific command-line details and statistics for the extraction and comparison processes.

```
VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.PRE_CHARGE.icv.drc/PRE_CHARGE.vue@mahmoodirccat.sfsu.edu
File View Tools Windows Help
Load Results X Run Summary X
LAYOUT ERRORS RESULTS
CLEAN

DRC Error Statistics
Library name: my_library
Structure name: PRE_CHARGE
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_1p9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/01 03:42:43PM
Time ended: 2025/05/01 03:42:47PM
Called as: icv -f openaccess -i my_library -c PRE_CHARGE -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_1p9m_drc_rules.rs

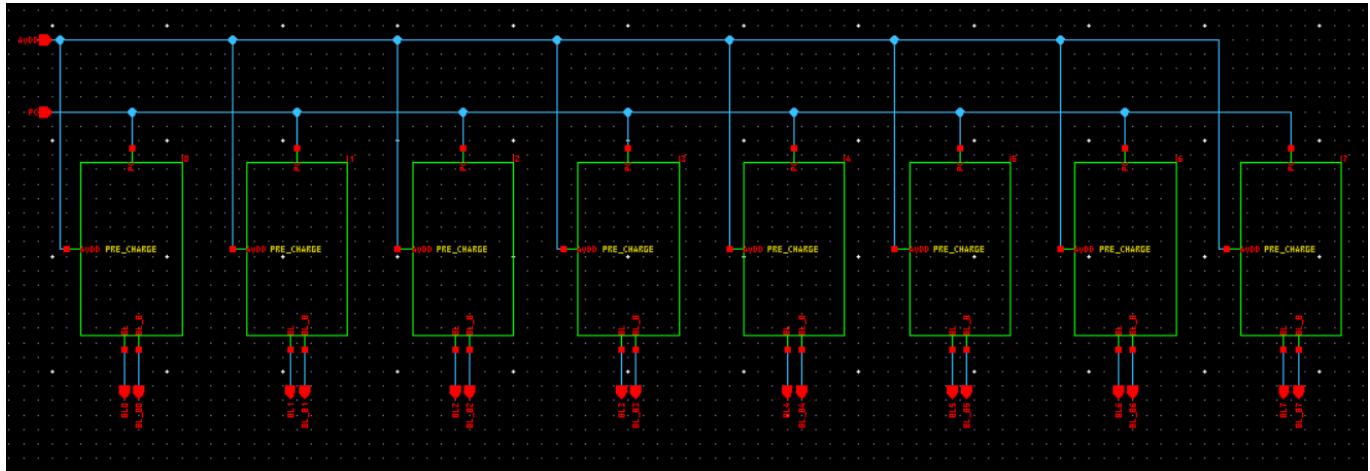
VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.PRE_CHARGE.icv.lvs/PRE_CHARGE.vue@mahmoodirccat.sfsu.edu
File View Tools Windows Help
Load Results X Run Summary X LVS Errors X
LVS Compare Results: PASS
DRC and Extraction Results: CLEAN
[PRE_CHARGE, PRE_CHARGE]

Netlist Extraction Statistics
Library name: my_library
Structure name: PRE_CHARGE
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_1p9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/13 01:09:54PM
Time ended: 2025/05/13 01:10:01PM
Called as: icv -f openaccess -i my_library -c PRE_CHARGE -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_1p9m_lvs_runset.rs

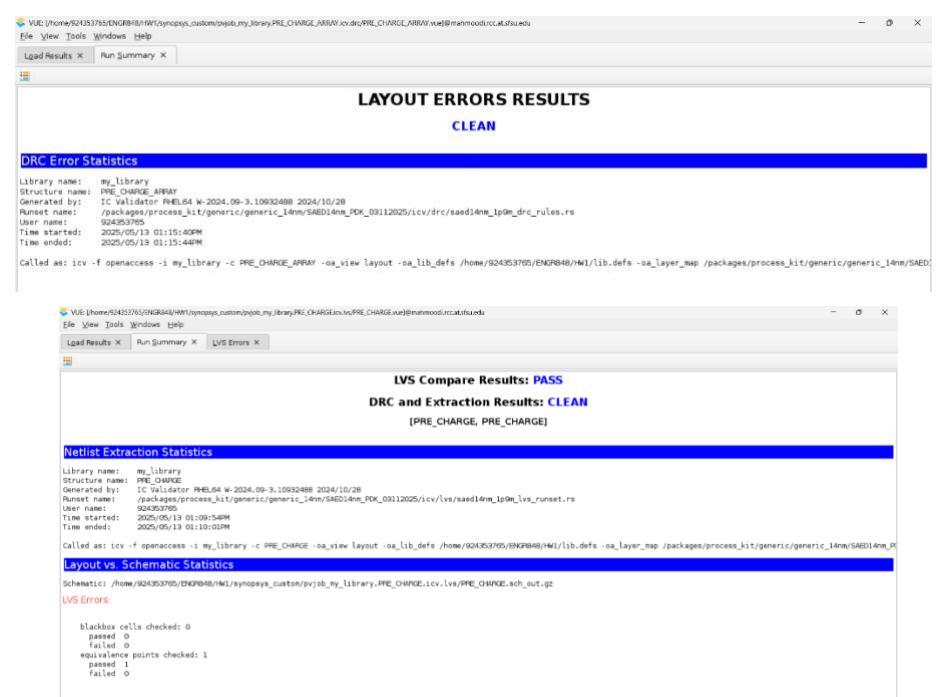
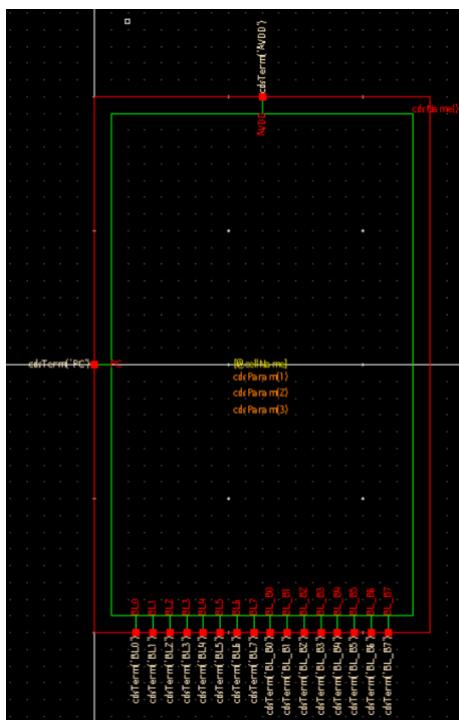
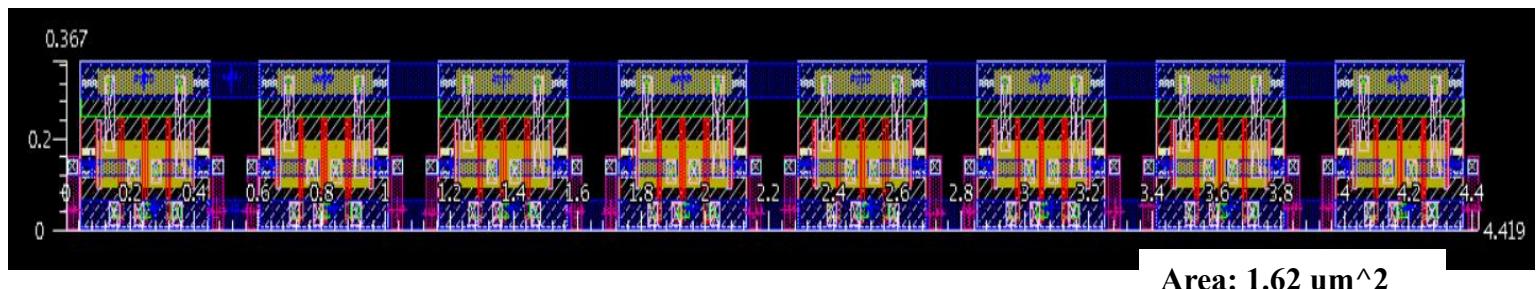
Layout vs. Schematic Statistics
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.PRE_CHARGE.icv.lvs/PRE_CHARGE.sch_out.gz
LVS Errors:

blackbox cells checked: 0
passed 0
failed 0
equivalence points checked: 1
passed 1
failed 0
```

Pre-Charge Array Schematic:



Pre-Charge Array Layout:



Pre-Charge Array Symbol

- **Decoder:**

This decoder circuit is responsible for selecting one wordline from a set based on binary address inputs, enabling access to a specific row in the memory array.

The decoder takes multiple address lines (e.g., A0, A1, A2) as input and generates a single active output line corresponding to the input address combination. It typically uses a combination of logic gates and inverters to achieve this functionality. For example, a 3-to-8 decoder will activate one of eight outputs based on the 3-bit binary input.

Key components include:

Input Buffers: These amplify the incoming address signals to drive the internal logic gates.

Logic Network: Implements the decoding function using AND/OR gates or CMOS logic. It ensures that only one output line is active for each address.

Output Drivers: Strengthen the selected wordline signal to ensure reliable activation of the memory row.

This configuration ensures accurate and efficient row selection, crucial for fast and correct memory operations.

Design Rule Check (DRC) and Layout Versus Schematic (LVS):

To ensure the decoder layout aligns with design and fabrication standards, both DRC and LVS checks were performed.

DRC Results:

The Design Rule Check validates that the physical layout adheres to the process design rules.

Status: CLEAN

No layout violations detected, confirming that the layout complies with the fabrication rules of the targeted technology node.

LVS Results:

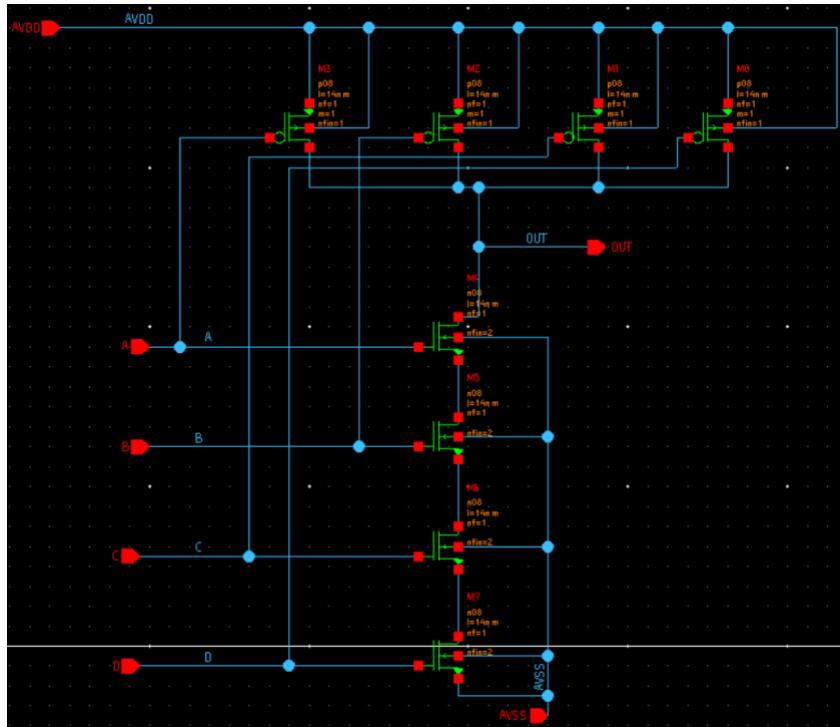
The Layout Versus Schematic check confirms that the implemented layout matches the circuit schematic.

LVS Compare Result: PASS

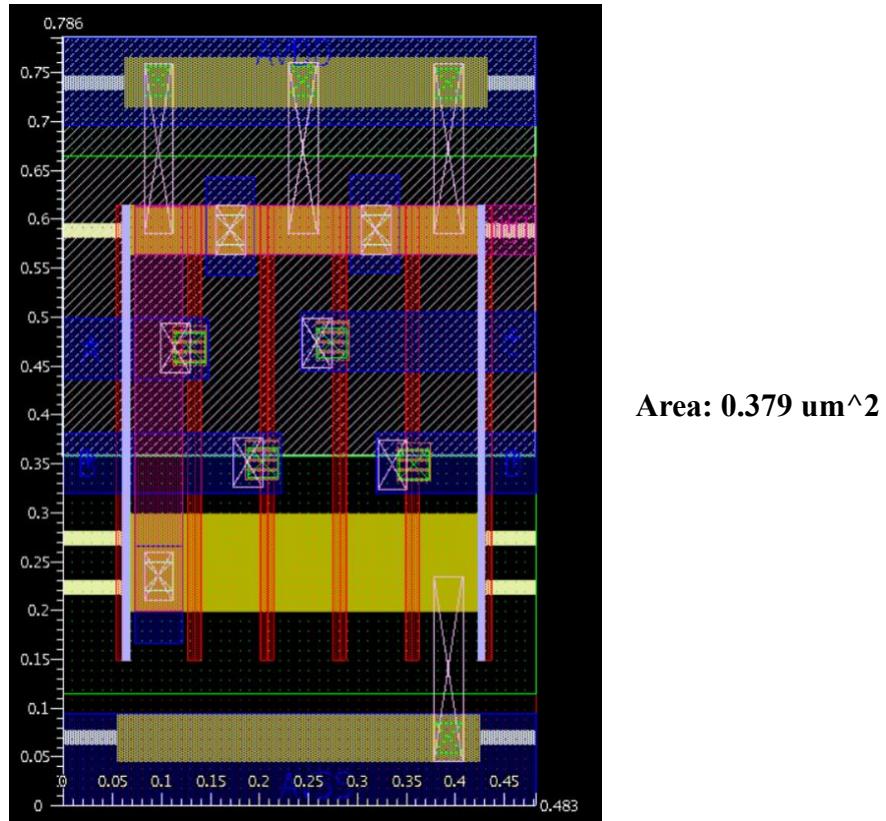
DRC and Extraction Results: CLEAN

All devices and interconnections in the layout were found to match the schematic, indicating no errors or mismatches in the design.

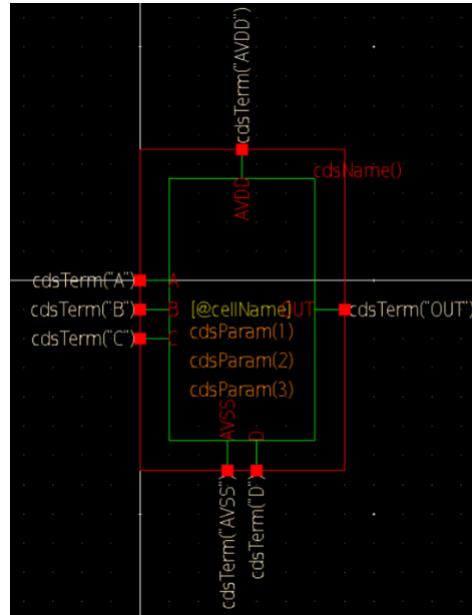
- **Decoder:** Design Decoder for 16x8 SRAM using
- **Nand Gate Schematic:**



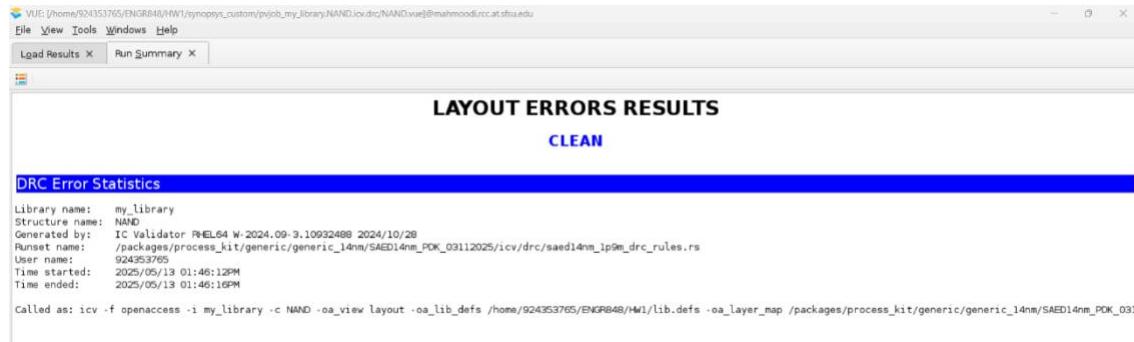
- **Nand Gate Layout:**



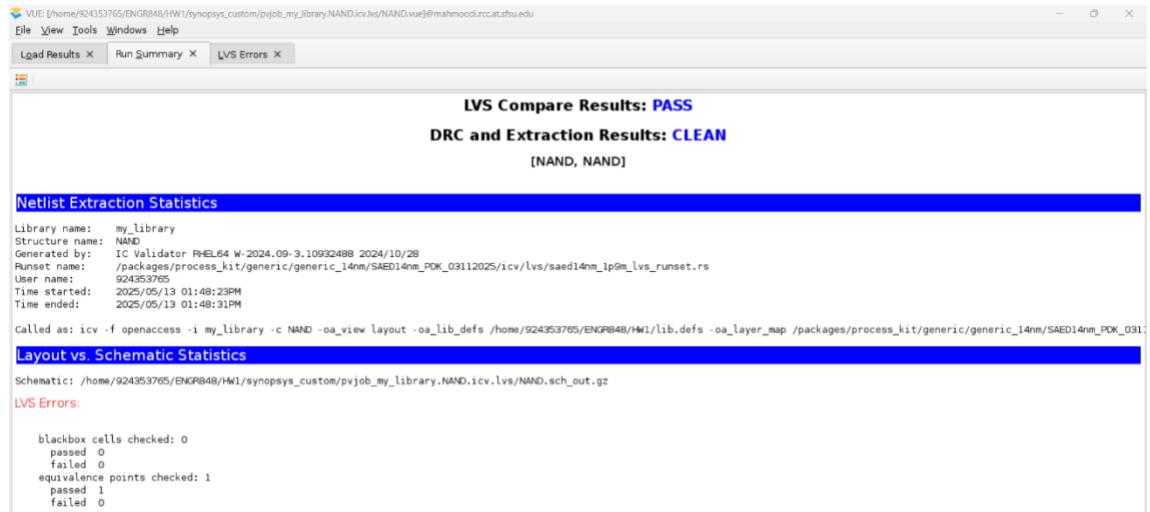
- Symbol:



- Design Rule Check:



- Layout Versus Schematic:



- NOR Gate:

The NOR gate is a fundamental digital logic gate that outputs a logical low (0) if any of its inputs are high (1) and only outputs a high (1) when all inputs are low (0). It is a universal gate, meaning it can be used to construct any other logic gate.

This implementation uses CMOS technology, comprising both PMOS and NMOS transistors:

- **PMOS Transistors:** Connected in parallel between the output and the supply voltage (VDD). These transistors turn on when their gate inputs are low, pulling the output high.
- **NMOS Transistors:** Connected in series between the output and ground. These transistors turn on when their gate inputs are high, pulling the output low.

Operation Summary:

- When all inputs are low, PMOS transistors conduct and NMOS are off, resulting in a high output.
- If any input is high, at least one NMOS conducts, and at least one PMOS is off, pulling the output low.

This configuration ensures low static power consumption and sharp logic transitions, ideal for high-speed digital circuits.

Design Rule Check (DRC) and Layout Versus Schematic (LVS)

To validate the NOR gate design against manufacturing and schematic standards, DRC and LVS checks were performed.

DRC

Results: Design Rule Check ensures that the physical layout meets all foundry-defined fabrication constraints.

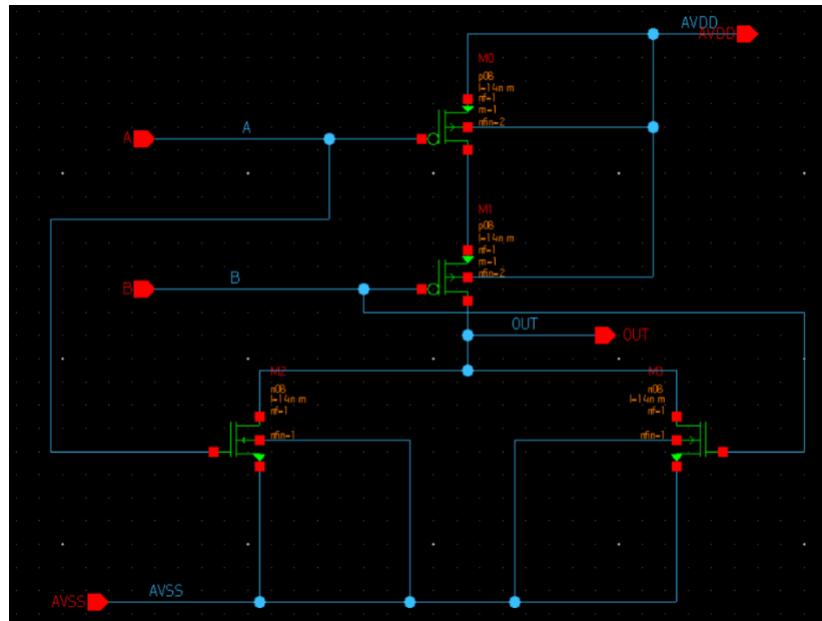
- **Status:** CLEAN
- **No layout violations detected,** confirming the layout adheres to the technology's design rules.

LVS

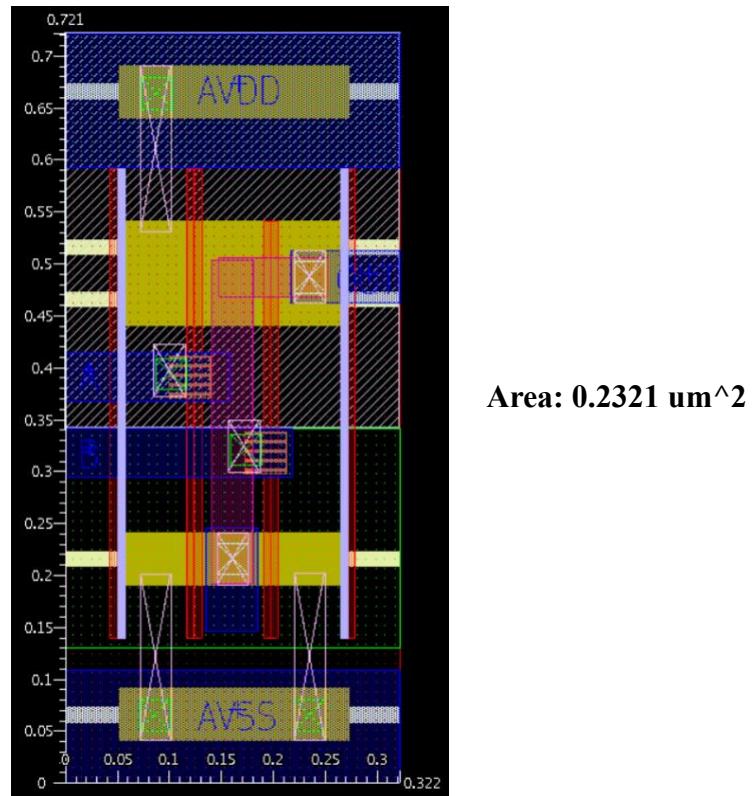
Results: Layout Versus Schematic check confirms the physical layout correctly implements the intended logic circuit.

- **LVS Compare Result:** PASS
- **DRC and Extraction Results:** CLEAN
- **All devices and net connections** in the layout were found to match the schematic. No mismatches or errors were reported, indicating a valid layout

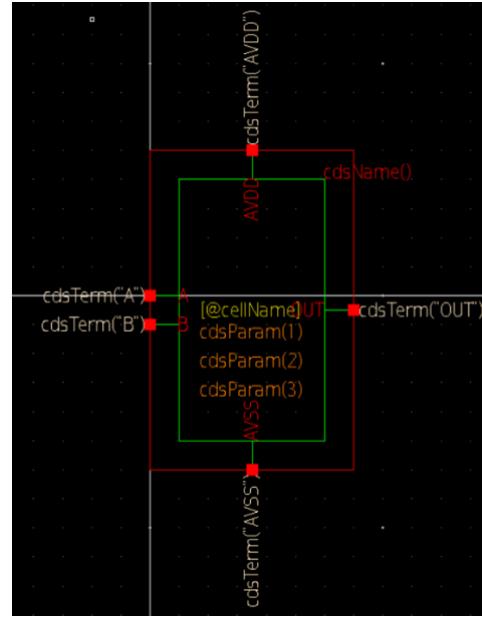
- NOR Gate Schematic:



- NOR Gate Layout:



- Symbol:



- Design Rule Check:

VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.NOR.icv.drc/NOR.vue]@mahmoodi:rcat.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

LAYOUT ERRORS RESULTS

CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: NOR
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saedi14nm_lp9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/13 01:53:17PM
Time ended: 2025/05/13 01:53:21PM

Called as: icv -f openaccess -i my_library -c NOR -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saedi14nm_lp9m_lvs_runset.rs
```

- Layout Versus Schematic:

VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.NOR.lvs/NOR.vue]@mahmoodi:rcat.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS

DRC and Extraction Results: CLEAN

[NOR, NOR]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: NOR
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saedi14nm_lp9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/13 01:55:25PM
Time ended: 2025/05/13 01:55:32PM

Called as: icv -f openaccess -i my_library -c NOR -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saedi14nm_lp9m_lvs_runset.rs
```

Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.NOR.icv.lvs/NOR.sch_out.gz
LVS Errors:

blackbox cells checked: 0
  passed 0
  failed 0
equivalence points checked: 1
  passed 1
  failed 0
```

- AND Gate:

The AND gate is a basic digital logic gate that outputs a logical high (1) only when **all** of its inputs are high. If any input is low (0), the output will be low. It is widely used in combinational logic circuits.

This CMOS implementation of an AND gate uses a combination of PMOS and NMOS transistors:

- **PMOS Transistors:** Connected in series between the output and the supply voltage (VDD). These transistors turn on when their gate inputs are low.
- **NMOS Transistors:** Connected in parallel between the output and ground. These transistors turn on when their gate inputs are high.

However, CMOS AND gates are typically implemented using a **NAND gate followed by an inverter**, since it is more area and power-efficient:

- **NAND Stage:** Outputs low when all inputs are high.
- **Inverter Stage:** Inverts the NAND output to achieve AND functionality.

Operation Summary:

- When all inputs are high, the NAND gate outputs low, and the inverter outputs high.
- If any input is low, the NAND gate outputs high, and the inverter outputs low.

This approach provides efficient logic realization with reliable switching and low power consumption.

Design Rule Check (DRC) and Layout Versus Schematic (LVS)

DRC and LVS checks were performed to ensure layout correctness and consistency with the schematic.

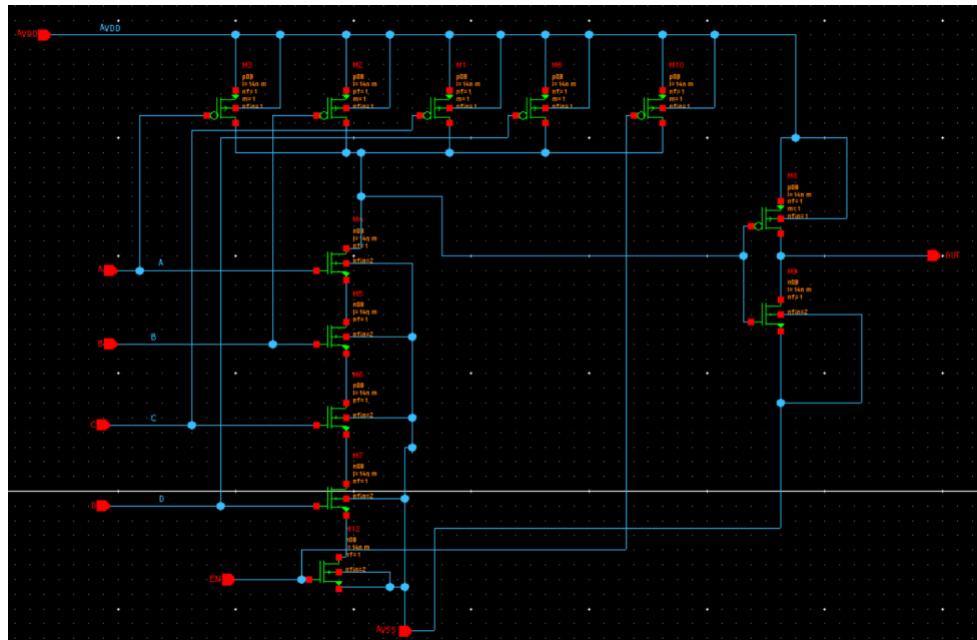
DRC Results: Design Rule Check verifies compliance with manufacturing constraints.

- **Status:** CLEAN
- **No layout violations detected**, indicating that the design meets all process design rules.

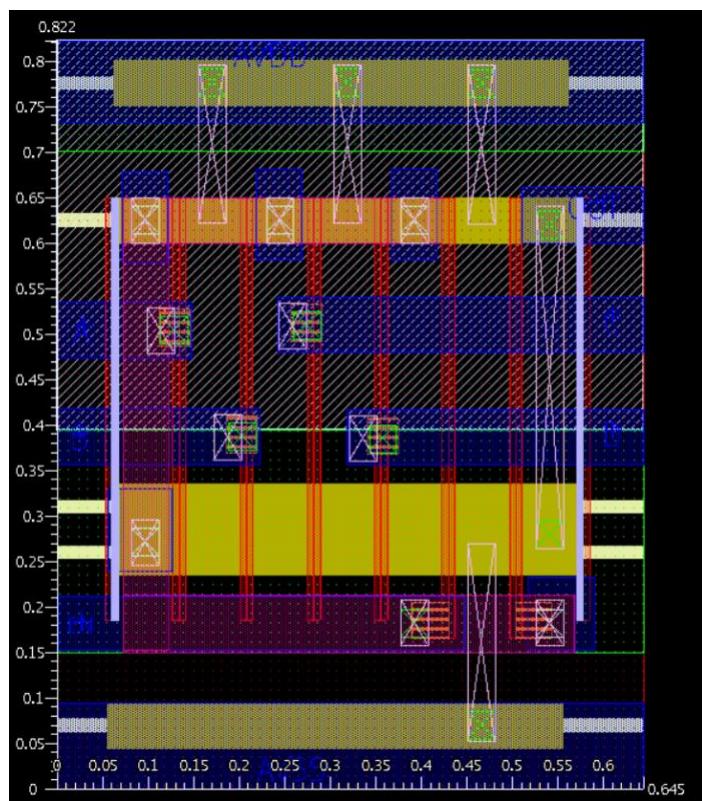
LVS Results: Layout Versus Schematic ensures the layout matches the logical schematic.

- **LVS Compare Result:** PASS
- **DRC and Extraction Results:** CLEAN
- **All transistors and connections** in the layout match the schematic exactly, confirming the functional correctness of the physical implementation.

- AND Gate Schematic:

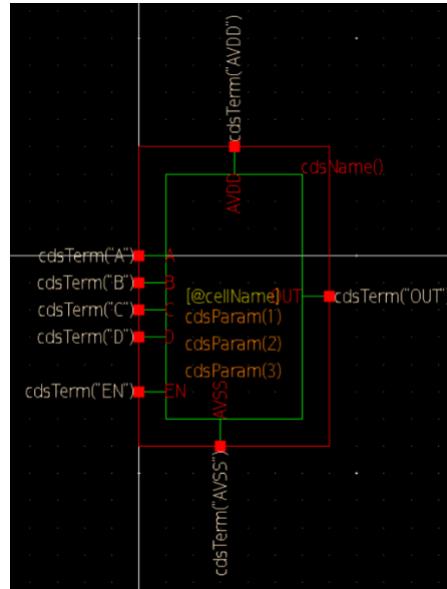


- AND Gate Layout:

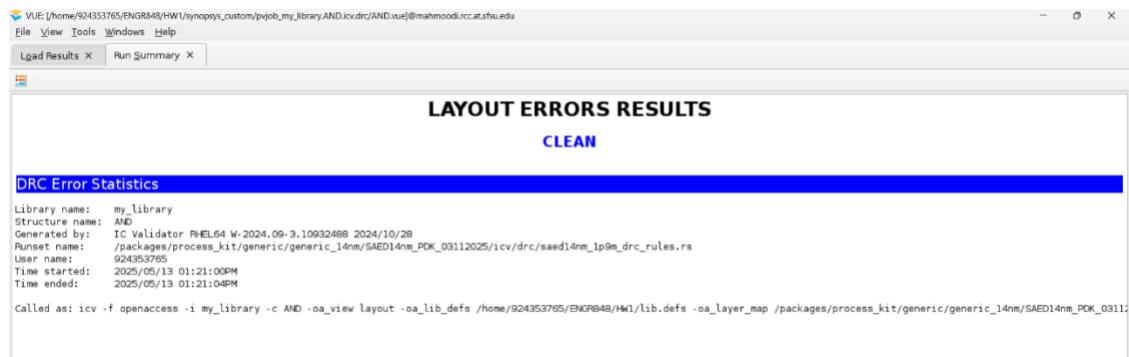


Area: 0.457 um^2

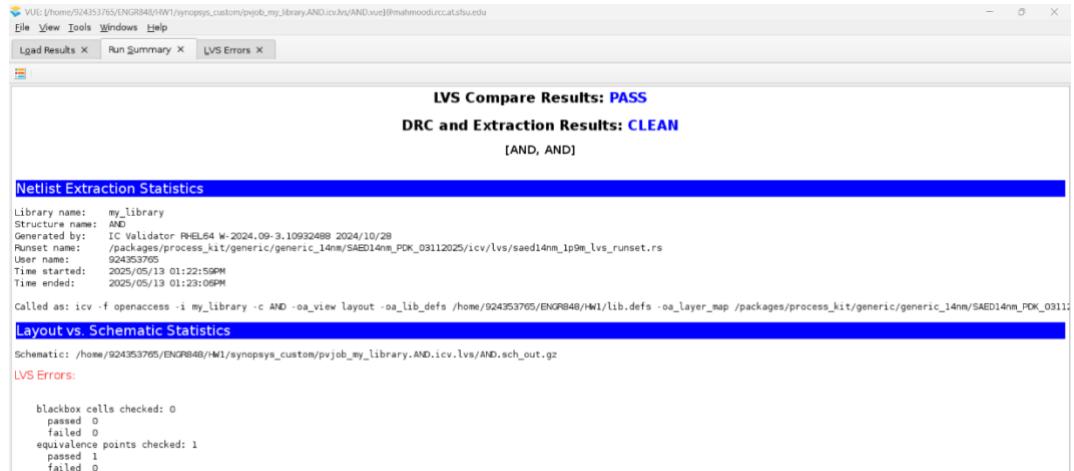
- Symbol:



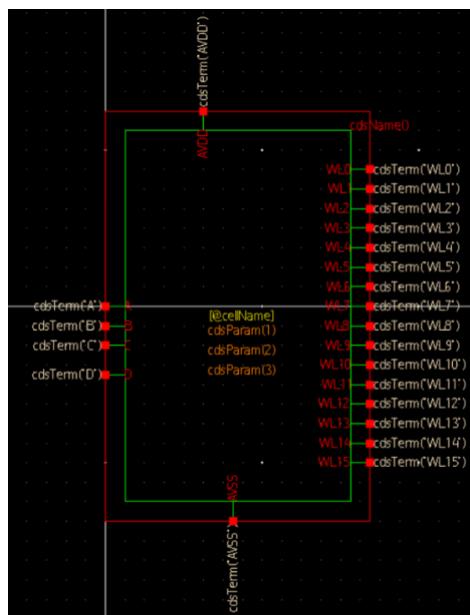
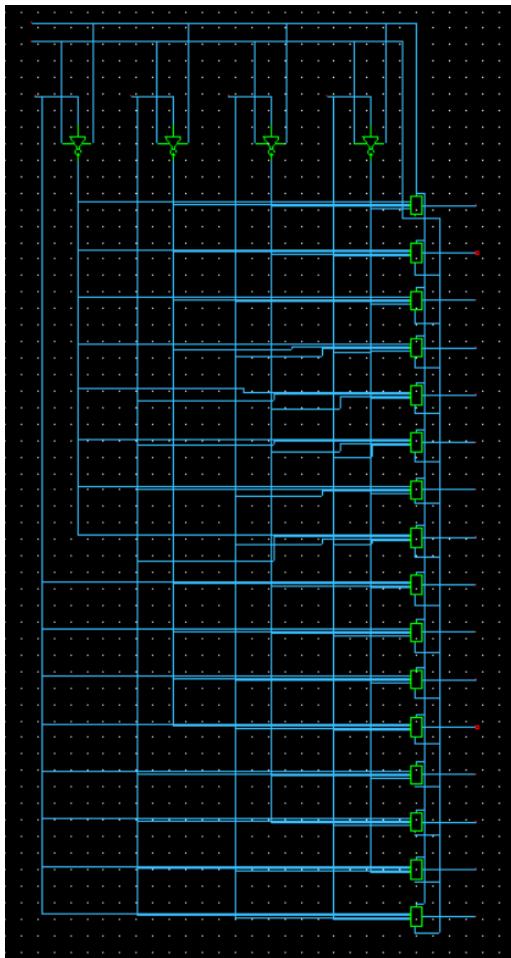
- Design Rule Check:



- Layout Versus Schematic:



- Decoder Schematic:



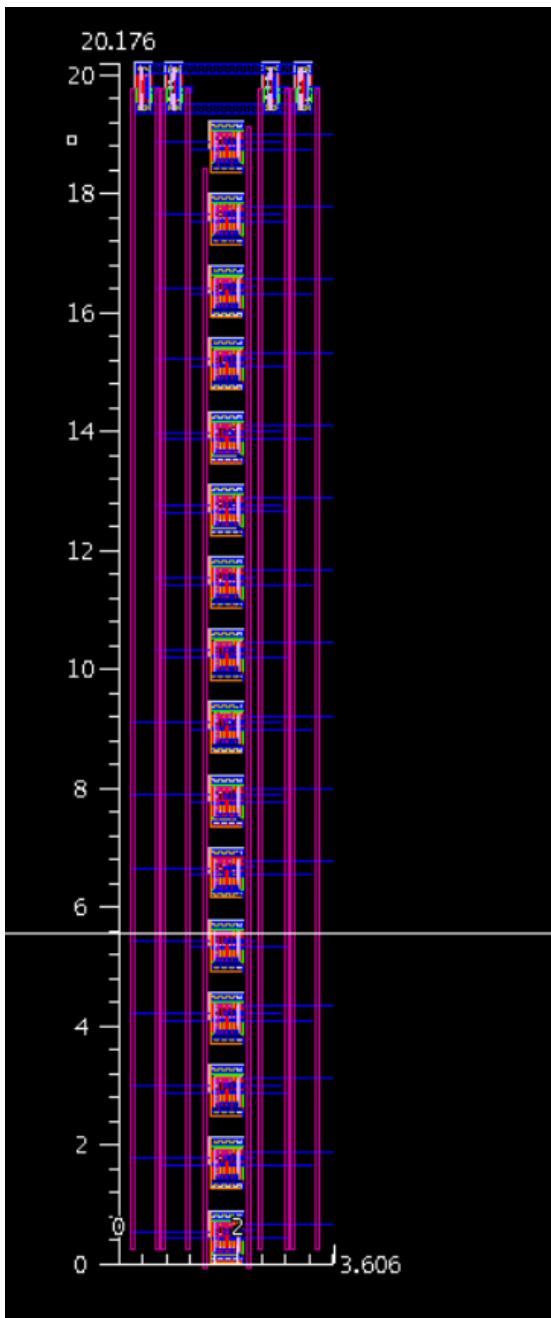
Symbol

- NAND & NOT

- 16 NAND Gate

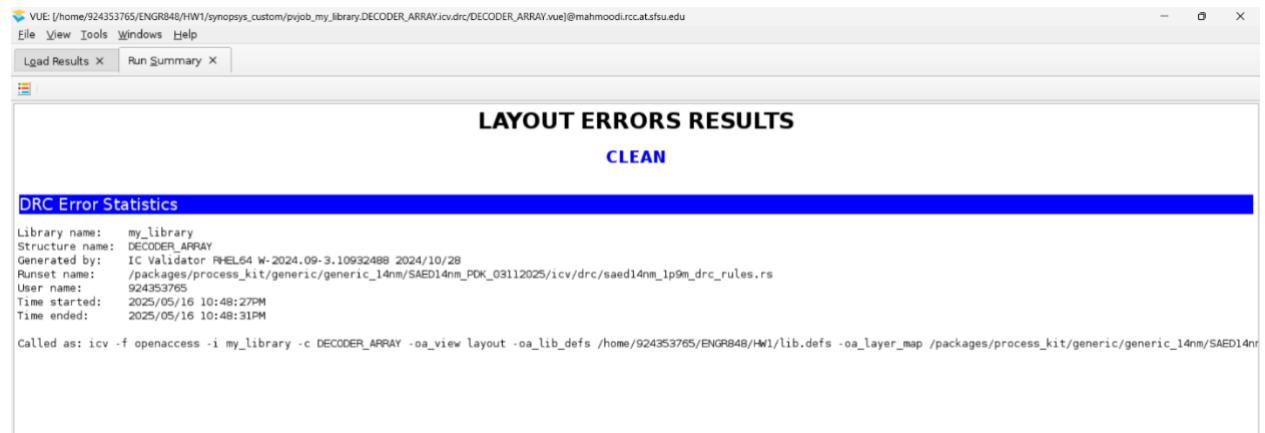
- 4 NOT Gate

- Decoder Layout:



Area: $72.75 \text{ } \mu\text{m}^2$

- Design Rule Check:



VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.DECODER_ARRAY.icv.drc/DECODER_ARRAY.vue@mahmoodi.rccat.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

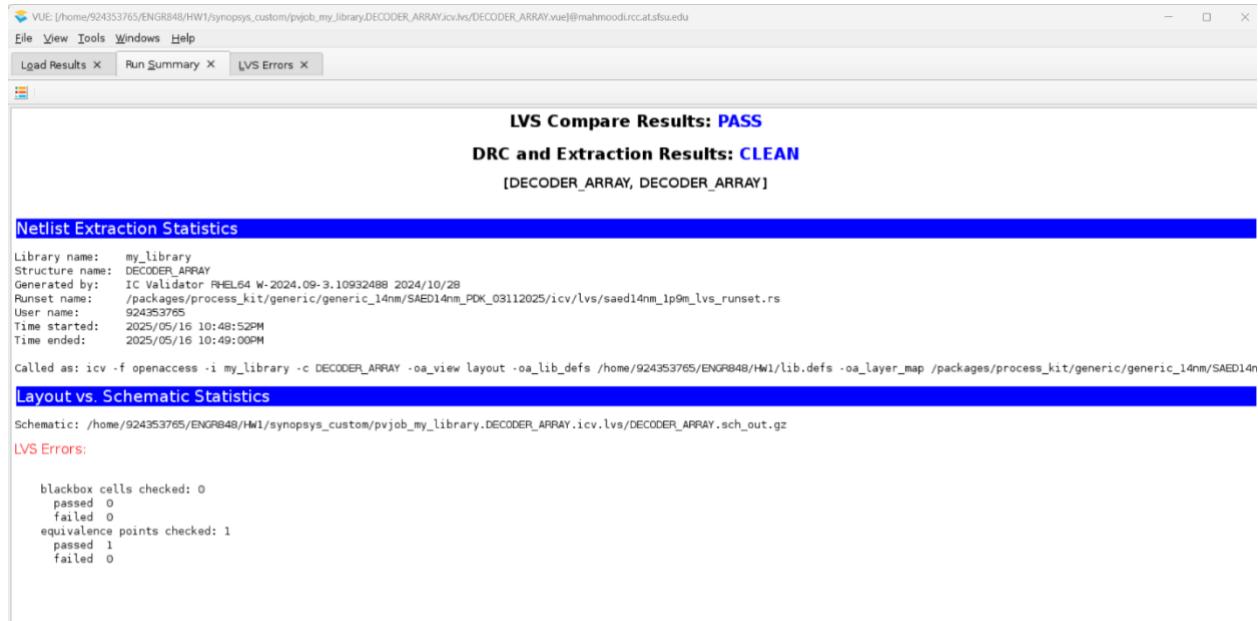
LAYOUT ERRORS RESULTS
CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: DECODER_ARRAY
Generated by: IC Validator RHEL64 W-2024.09.3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_lp9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/16 10:48:27PM
Time ended: 2025/05/16 10:49:31PM

Called as: icv -f openaccess -i my_library -c DECODER_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_lp9m_drc_rules.rs
```

- Layout Versus Schematic:



VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.DECODER_ARRAY.icv.lvs/DECODER_ARRAY.vue@mahmoodi.rccat.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS
DRC and Extraction Results: CLEAN
[DECODER_ARRAY, DECODER_ARRAY]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: DECODER_ARRAY
Generated by: IC Validator RHEL64 W-2024.09.3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_lp9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/16 10:48:52PM
Time ended: 2025/05/16 10:49:00PM

Called as: icv -f openaccess -i my_library -c DECODER_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_lp9m_lvs_runset.rs
```

Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.DECODER_ARRAY.icv.lvs/DECODER_ARRAY.sch_out.gz
```

LVS Errors:

```
blackbox cells checked: 0
  passed 0
  failed 0
equivalence points checked: 1
  passed 1
  failed 0
```

Driver: A driver circuit is used to **amplify and buffer signals** so they can drive larger capacitive loads or longer interconnects without significant signal degradation. In memory arrays, wordline and bitline drivers are essential to ensure that control and data signals reach their destinations with sufficient strength and speed.

This particular driver is designed to **control the wordlines** in a memory array, ensuring robust activation of selected rows during read and write operations.

Circuit Components:

- **Input Buffer Stage:** Takes in a control or address signal and conditions it by sharpening transitions and reducing noise susceptibility.
- **Inverter Chain or Push-Pull Output Stage:** Amplifies the signal across multiple stages of CMOS inverters or uses a complementary output stage (PMOS and NMOS) to provide strong high and low logic levels.
- **Output Stage:** Drives the capacitive wordline or bitline directly. It is typically sized larger than standard logic gates to handle the load.

Operation:

- When the input signal is high, the output is driven low or high depending on the driver configuration.
- The driver ensures minimal delay and power loss, maintaining signal integrity even across large memory arrays.

This robust signal delivery is essential for maintaining **performance, timing accuracy, and reliable operation** in high-density circuits.

Design Rule Check (DRC) and Layout Versus Schematic (LVS): To verify the correctness and manufacturability of the driver circuit, standard DRC and LVS checks were performed.

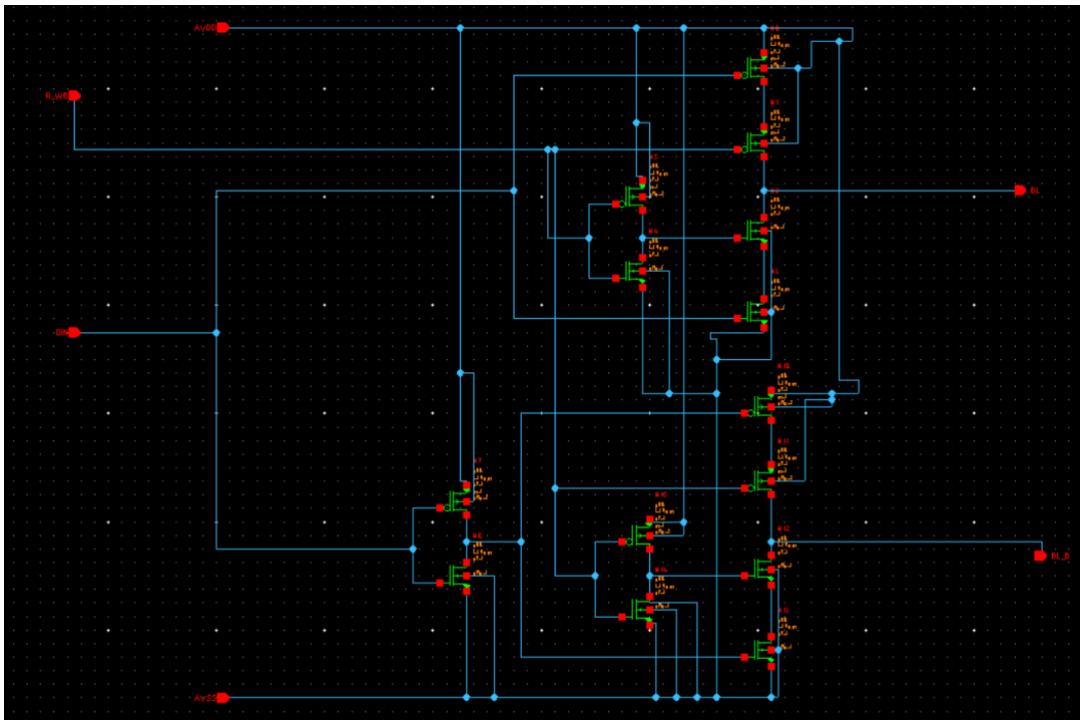
DRC Results: Design Rule Check confirms compliance with fabrication rules.

- **Status:** CLEAN
- **No layout violations detected**, indicating full compliance with the foundry's design rules.

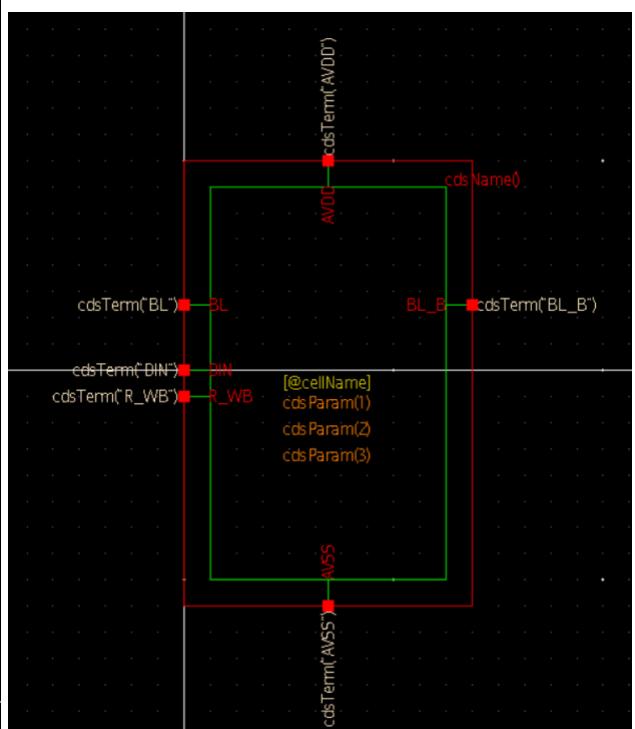
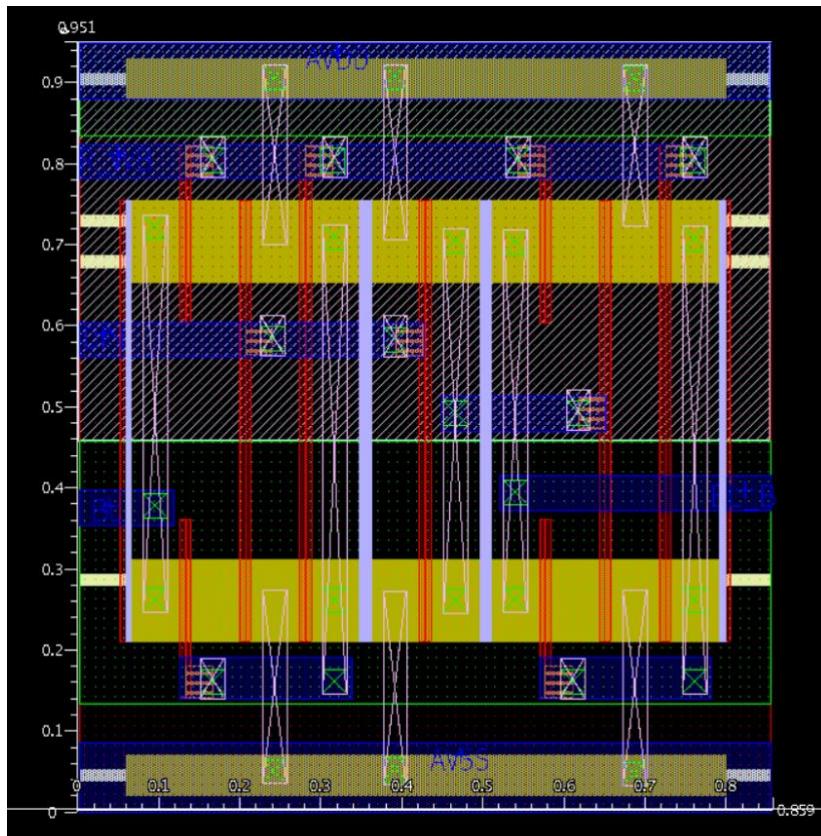
LVS Results: Layout Versus Schematic ensures the physical layout accurately represents the schematic design.

- **LVS Compare Result:** PASS
- **DRC and Extraction Results:** CLEAN
- **All devices and net connections** in the layout match those in the schematic, confirming that the physical implementation is functionally correct.

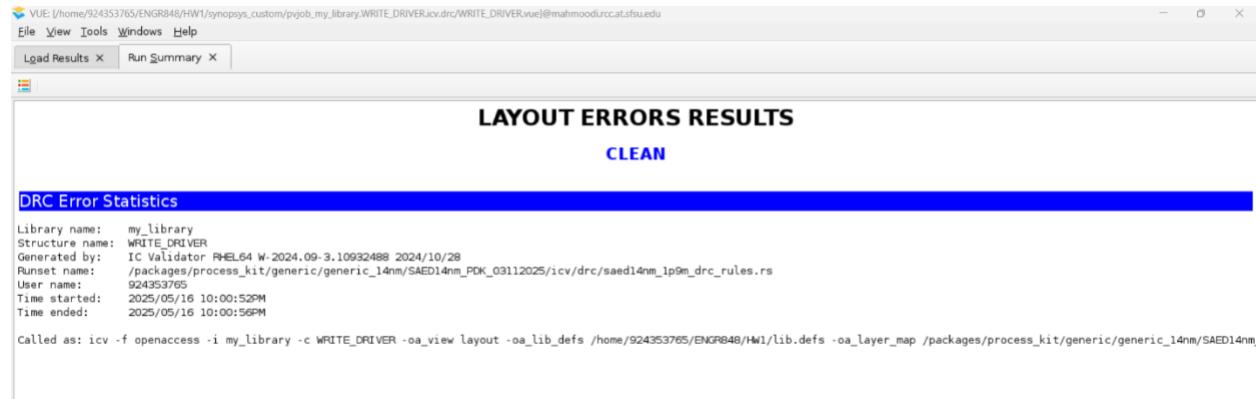
- Write Driver Schematic:



- Write Driver Layout:



- Design Rule Check:



VUE: [/home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.WRITE_DRIVER.icv/WRITER_DRIVER.vue]@mahmoodiuccat.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

LAYOUT ERRORS RESULTS

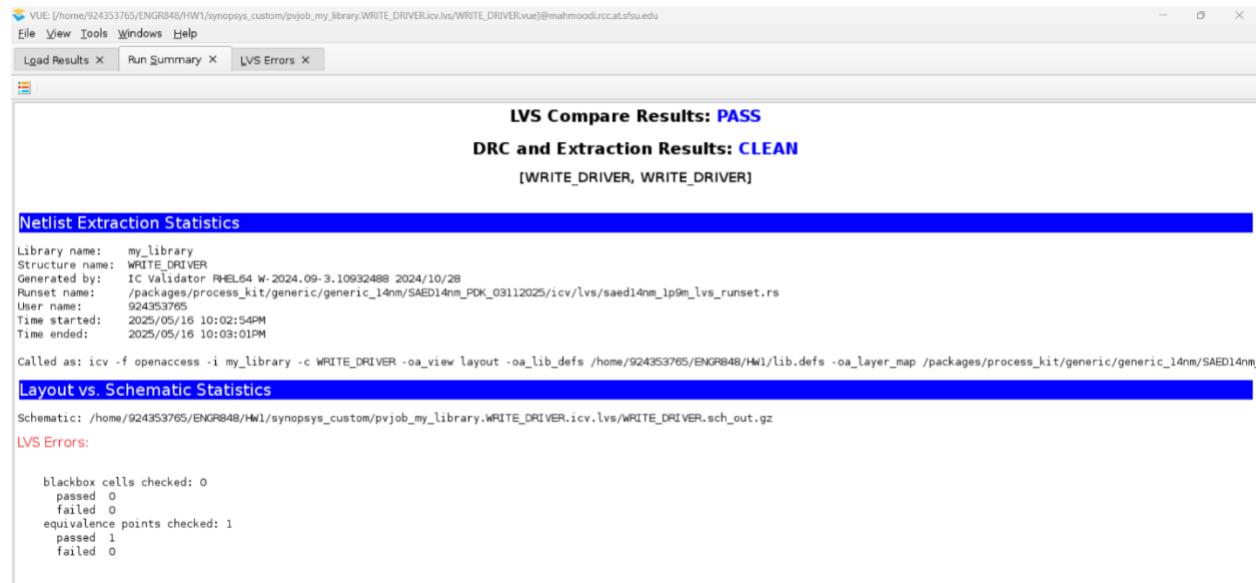
CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: WRITE_DRIVER
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_ip9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/16 10:00:52PM
Time ended: 2025/05/16 10:00:56PM

Called as: icv -f openaccess -i my_library -c WRITE_DRIVER -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_ip9m_drc_rules.rs
```

- Layout Versus Schematic:



VUE: [/home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.WRITE_DRIVER.icv/WRITER_DRIVER.vue]@mahmoodiuccat.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS

DRC and Extraction Results: CLEAN

[WRITE_DRIVER, WRITE_DRIVER]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: WRITE_DRIVER
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_ip9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/16 10:02:54PM
Time ended: 2025/05/16 10:03:01PM

Called as: icv -f openaccess -i my_library -c WRITE_DRIVER -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_ip9m_lvs_runset.rs
```

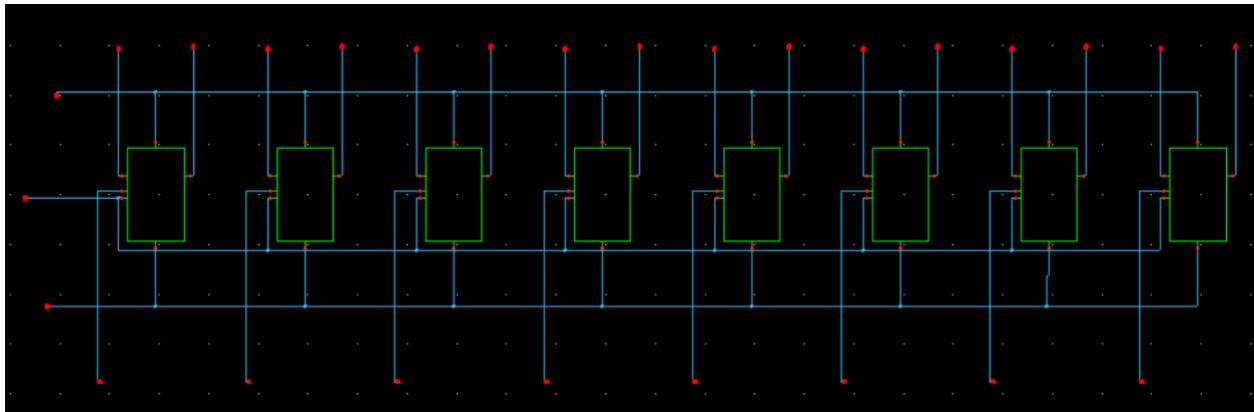
Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.WRITE_DRIVER.icv.lvs/WRITER_DRIVER.sch_out.gz
```

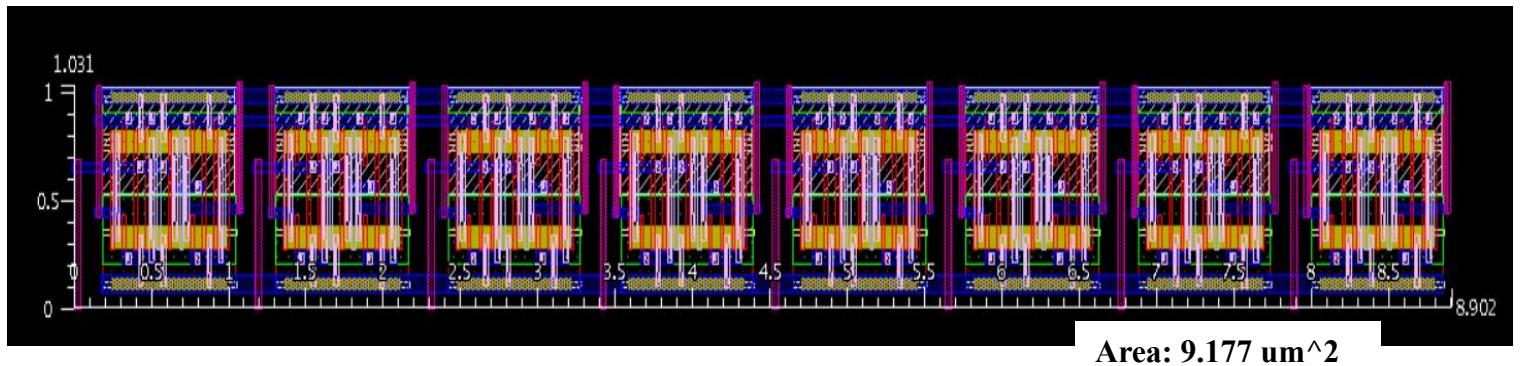
LVS Errors:

```
blackbox cells checked: 0
    passed 0
    failed 0
equivalence points checked: 1
    passed 1
    failed 0
```

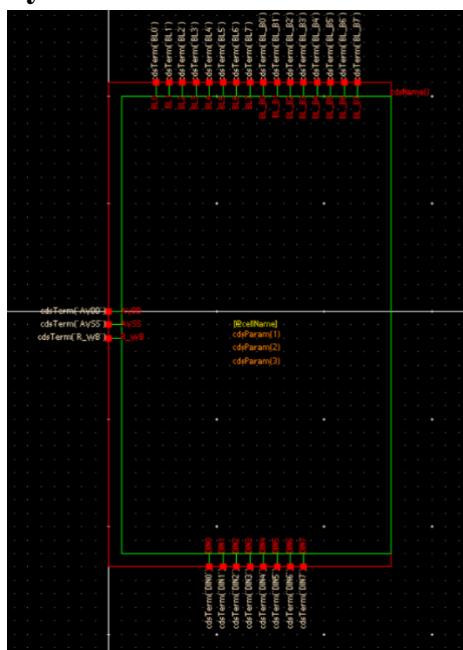
- Write Driver Array Schematic:



- Write Driver Array Layout:



- Write Driver Array Symbol:



- Design Rule Check:

VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.WRITE_DRIVER_ARRAY.icv.drc/WRITE_DRIVER_ARRAY.vue@mahmoodi.rcc.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

LAYOUT ERRORS RESULTS

CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: WRITE_DRIVER_ARRAY
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_lp9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/16 10:13:31PM
Time ended: 2025/05/16 10:13:35PM

Called as: icv -f openaccess -i my_library -c WRITE_DRIVER_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAE
```

- Layout Versus Schematic:

VUE: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.WRITE_DRIVER_ARRAY.icv.lvs/WRITE_DRIVER_ARRAY.vue@mahmoodi.rcc.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS

DRC and Extraction Results: CLEAN

[WRITE_DRIVER_ARRAY, WRITE_DRIVER_ARRAY]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: WRITE_DRIVER_ARRAY
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_lp9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/16 10:14:27PM
Time ended: 2025/05/16 10:14:35PM

Called as: icv -f openaccess -i my_library -c WRITE_DRIVER_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAE
```

Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.WRITE_DRIVER_ARRAY.icv.lvs/WRITE_DRIVER_ARRAY.sch_out.gz
```

LVS Errors:

```
blackbox cells checked: 0
  passed 0
  failed 0
equivalence points checked: 1
  passed 1
  failed 0
```

Sense Amplifier: A **sense amplifier** is a critical component in memory systems used to **detect and amplify small voltage differences** between bitlines during read operations. It significantly improves the speed and reliability of data retrieval in SRAM, DRAM, and other memory architectures.

Circuit Components:

- **Cross-Coupled Inverters:** The core of the sense amplifier, these act as a positive-feedback latch that rapidly amplifies any small voltage difference between BL and BLB.
- **Enable Transistors:** Controlled by the **Sense Enable (SE)** signal, these transistors activate the sense amplifier only during the read phase, reducing power consumption.
- **Precharged Bitlines:** Before reading, bitlines are precharged to the same voltage (usually AVDD). A memory cell then slightly perturbs one of the bitlines depending on the stored value.

Operation:

1. During a read, the wordline activates a memory cell, causing a small voltage difference between BL and BLB.
2. When SE is asserted, the cross-coupled inverters latch onto the voltage difference and rapidly pull one line high and the other low.
3. The final output reflects the stored logic value of the accessed cell.

This fast, differential sensing mechanism ensures **high-speed and accurate readout** even with very small signal margins.

Design Rule Check (DRC) and Layout Versus Schematic (LVS): To ensure the sense amplifier's layout is both manufacturable and functionally correct, DRC and LVS checks were performed.

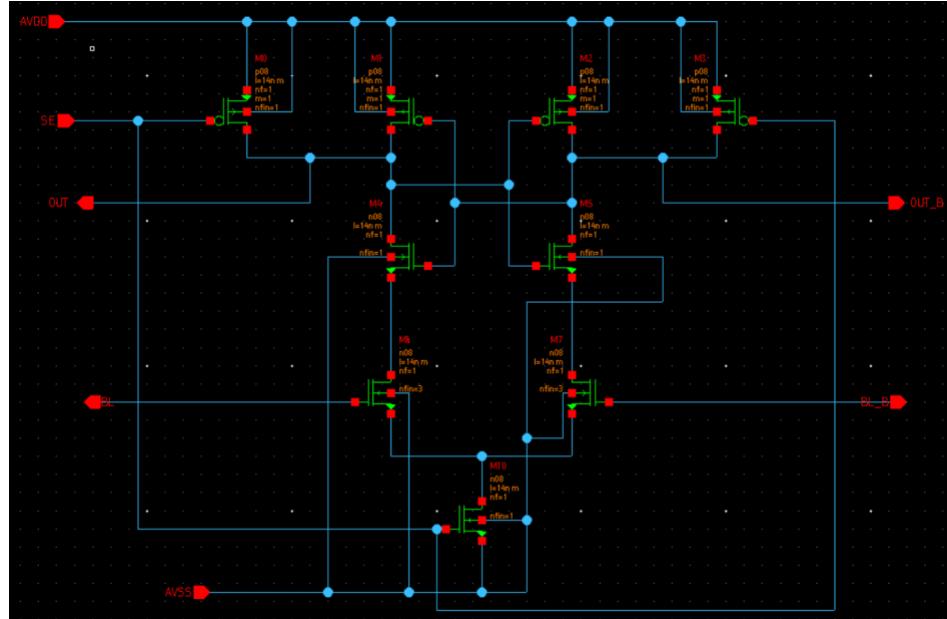
DRC Results: Design Rule Check verifies that the layout adheres to all manufacturing constraints.

- **Status:** CLEAN
- **No layout violations detected**, indicating the design is compliant with all process design rules.

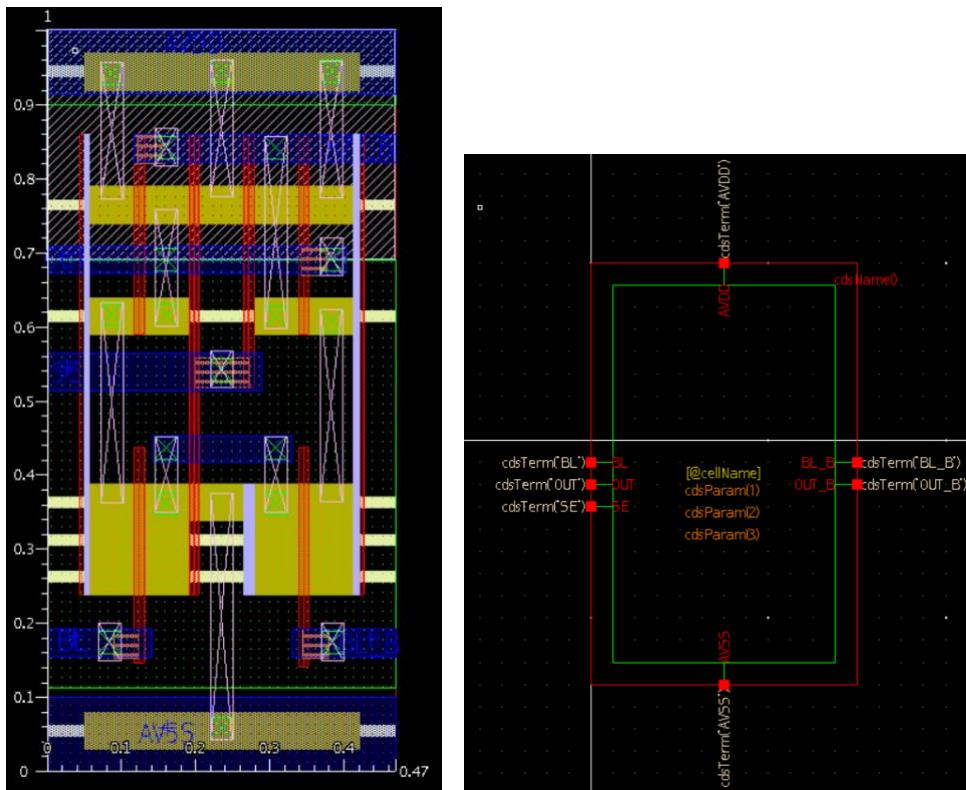
LVS Results: Layout Versus Schematic ensures the physical layout implements the schematic accurately.

- **LVS Compare Result:** PASS
- **DRC and Extraction Results:** CLEAN
- **All transistors, interconnections, and enable controls** in the layout match the schematic. The sense amplifier is validated for correct and reliable operation.

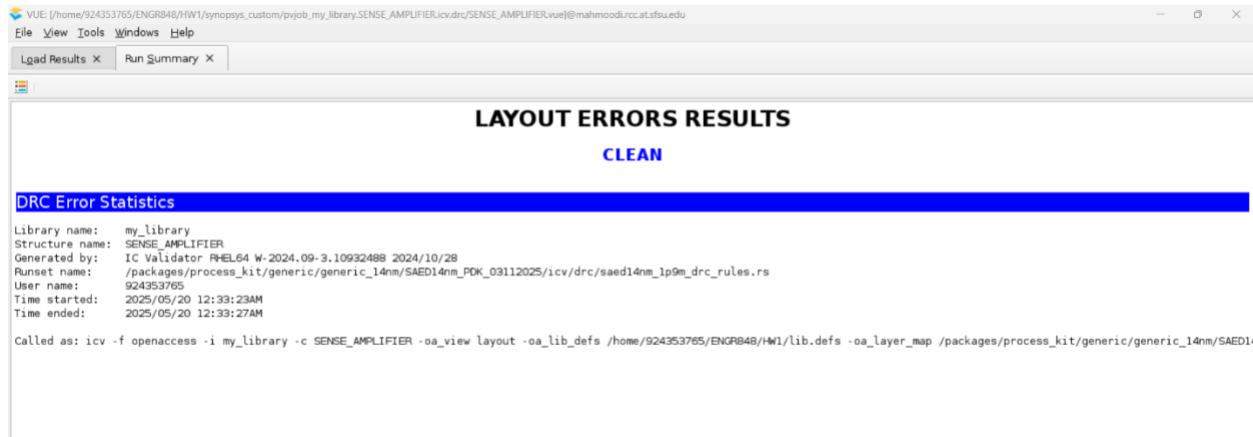
- Sense Amplifier
- Sense Amplifier Schematic:



- Sense Amplifier Layout:



- Design Rule Check:



VUE: [/home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.SENSE_AMPLIFIER.icv.drc/SENSE_AMPLIFIER.vue]@mahmoodi.rcc.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

LAYOUT ERRORS RESULTS

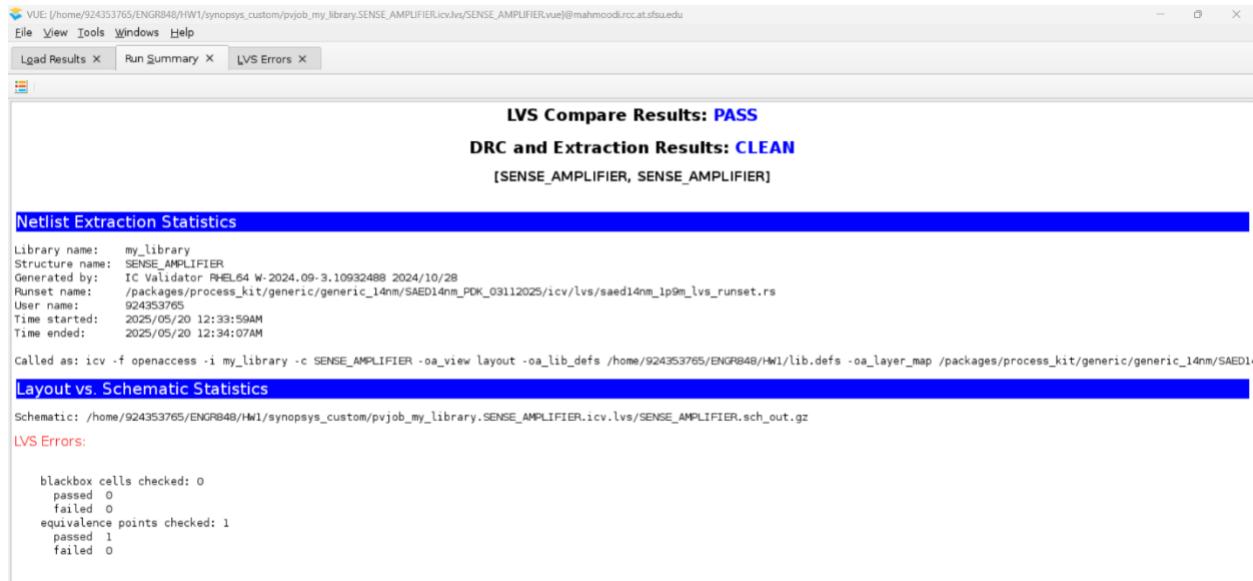
CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: SENSE_AMPLIFIER
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_lp9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/20 12:33:23AM
Time ended: 2025/05/20 12:33:27AM

Called as: icv -f openaccess -i my_library -c SENSE_AMPLIFIER -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_lp9m_drc_rules.rs
```

- Layout Versus Schematic:



VUE: [/home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.SENSE_AMPLIFIER.icv.lvs/SENSE_AMPLIFIER.vue]@mahmoodi.rcc.sfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS

DRC and Extraction Results: CLEAN

[SENSE_AMPLIFIER, SENSE_AMPLIFIER]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: SENSE_AMPLIFIER
Generated by: IC Validator RHEL64 W-2024.09-3.10932488 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_lp9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/20 12:33:59AM
Time ended: 2025/05/20 12:34:07AM

Called as: icv -f openaccess -i my_library -c SENSE_AMPLIFIER -oa_view layout -oa_lib_defs /home/924353765/ENGR848/HW1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/lvs/saed14nm_lp9m_lvs_runset.rs
```

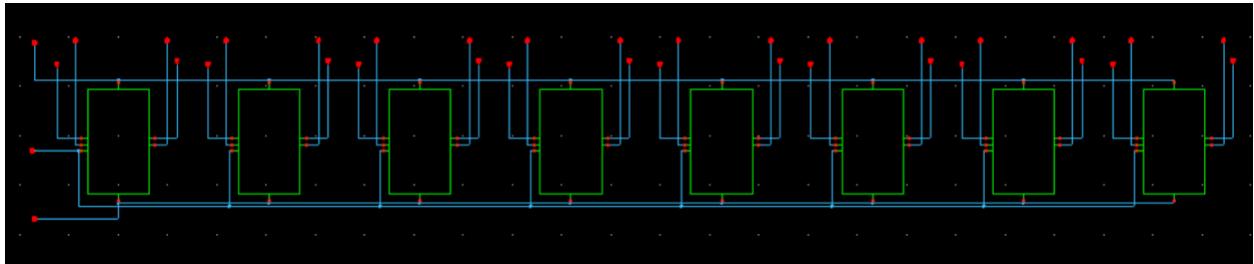
Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/HW1/synopsys_custom/pvjob_my_library.SENSE_AMPLIFIER.icv.lvs/SENSE_AMPLIFIER.sch_out.gz
```

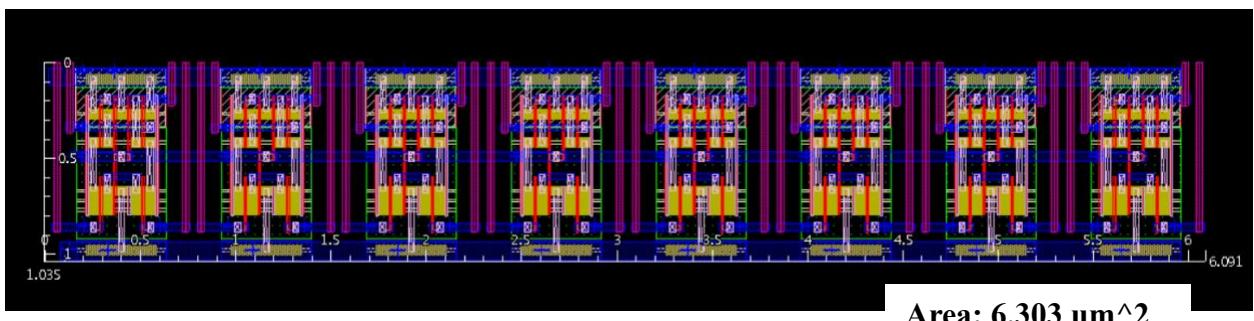
LVS Errors:

```
blackbox cells checked: 0
    passed 0
    failed 0
equivalence points checked: 1
    passed 1
    failed 0
```

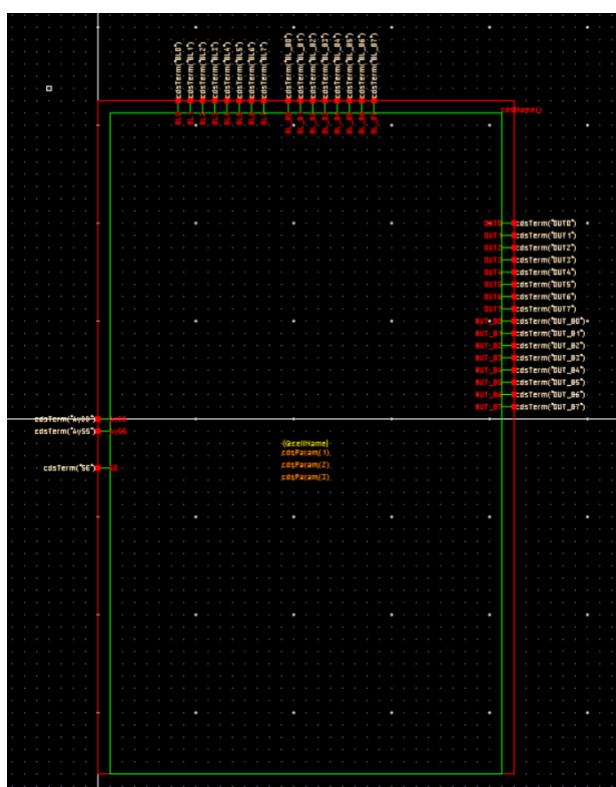
- Sense Amplifier Array Schematic:



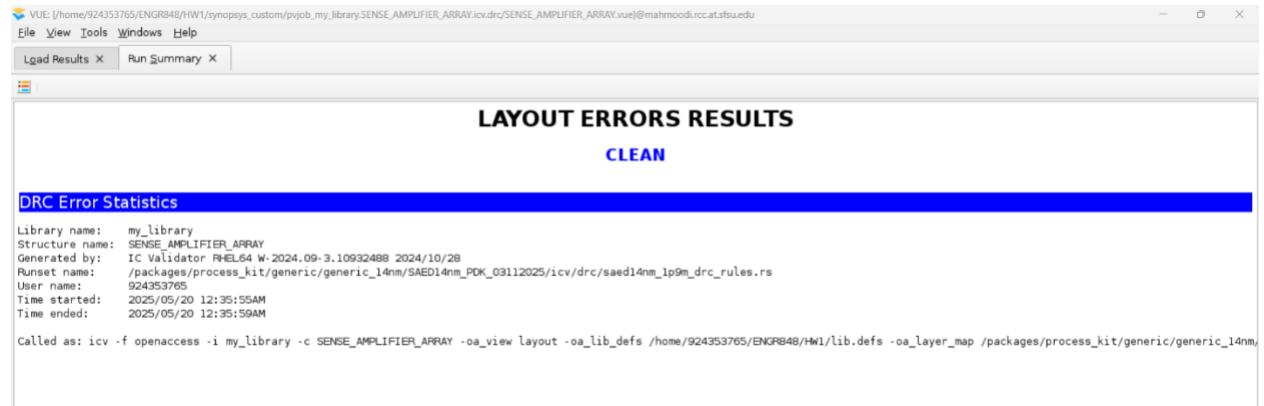
- Sense Amplifier Array Layout:



- Sense Amplifier Array Symbol:



- Design Rule Check:



VUE: [/home/924353765/ENGR848/Hw1/synopsys_custom/pvjob_my_library.SENSE_AMPLIFIER_ARRAY.icv.drc/SENSE_AMPLIFIER_ARRAY.vue]@mahmoodi.rcc.atsfsu.edu

File View Tools Windows Help

Load Results X Run Summary X

LAYOUT ERRORS RESULTS

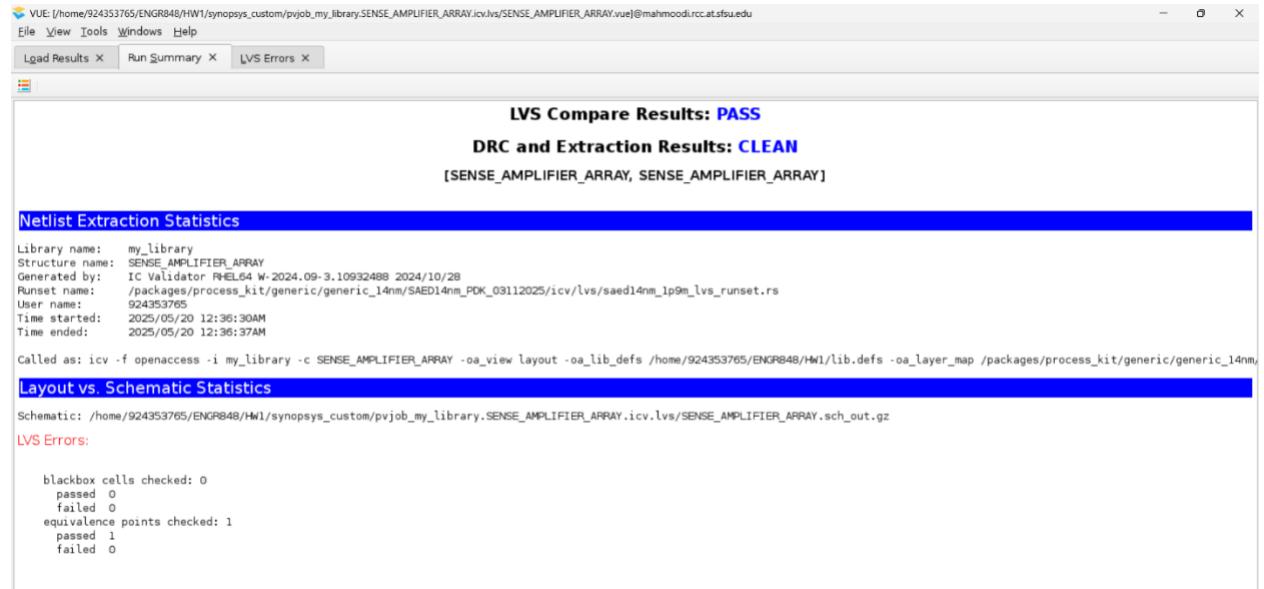
CLEAN

DRC Error Statistics

```
Library name: my_library
Structure name: SENSE_AMPLIFIER_ARRAY
Generated by: IC Validator RHEL64 W-2024.09-3.10932498 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/icv/drc/saed14nm_lp9m_drc_rules.rs
User name: 924353765
Time started: 2025/05/20 12:35:55AM
Time ended: 2025/05/20 12:35:59AM

Called as: icv -f openaccess -i my_library -c SENSE_AMPLIFIER_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/Hw1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/
```

- Layout Versus Schematic:



VUE: [/home/924353765/ENGR848/Hw1/synopsys_custom/pvjob_my_library.SENSE_AMPLIFIER_ARRAY.icv.lvs/SENSE_AMPLIFIER_ARRAY.vue]@mahmoodi.rcc.atsfsu.edu

File View Tools Windows Help

Load Results X Run Summary X LVS Errors X

LVS Compare Results: PASS

DRC and Extraction Results: CLEAN

[SENSE_AMPLIFIER_ARRAY, SENSE_AMPLIFIER_ARRAY]

Netlist Extraction Statistics

```
Library name: my_library
Structure name: SENSE_AMPLIFIER_ARRAY
Generated by: IC Validator RHEL64 W-2024.09-3.10932498 2024/10/28
Runset name: /packages/process_kit/generic/generic_14nm/SAED14nm_PDK_03112025/lvs/saed14nm_lp9m_lvs_runset.rs
User name: 924353765
Time started: 2025/05/20 12:36:30AM
Time ended: 2025/05/20 12:36:37AM

Called as: icv -f openaccess -i my_library -c SENSE_AMPLIFIER_ARRAY -oa_view layout -oa_lib_defs /home/924353765/ENGR848/Hw1/lib.defs -oa_layer_map /packages/process_kit/generic/generic_14nm/
```

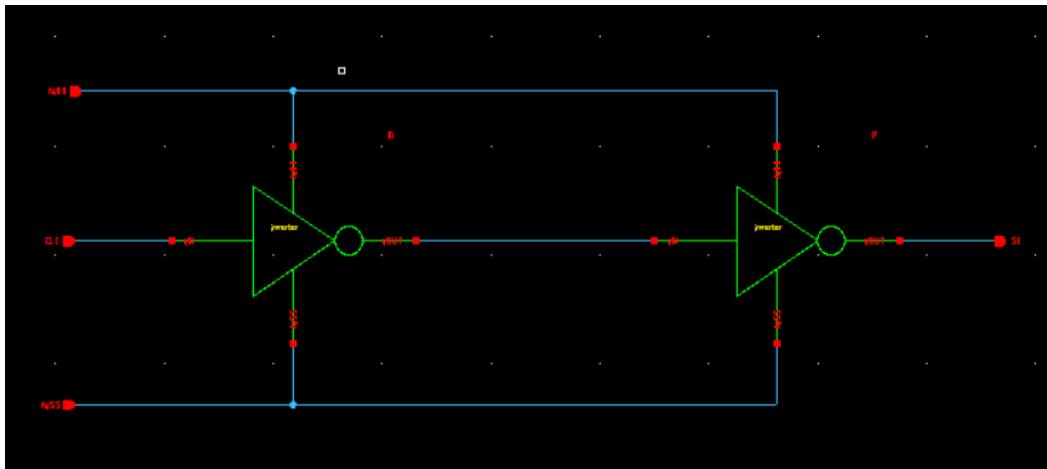
Layout vs. Schematic Statistics

```
Schematic: /home/924353765/ENGR848/Hw1/synopsys_custom/pvjob_my_library.SENSE_AMPLIFIER_ARRAY.icv.lvs/SENSE_AMPLIFIER_ARRAY.sch_out.gz
```

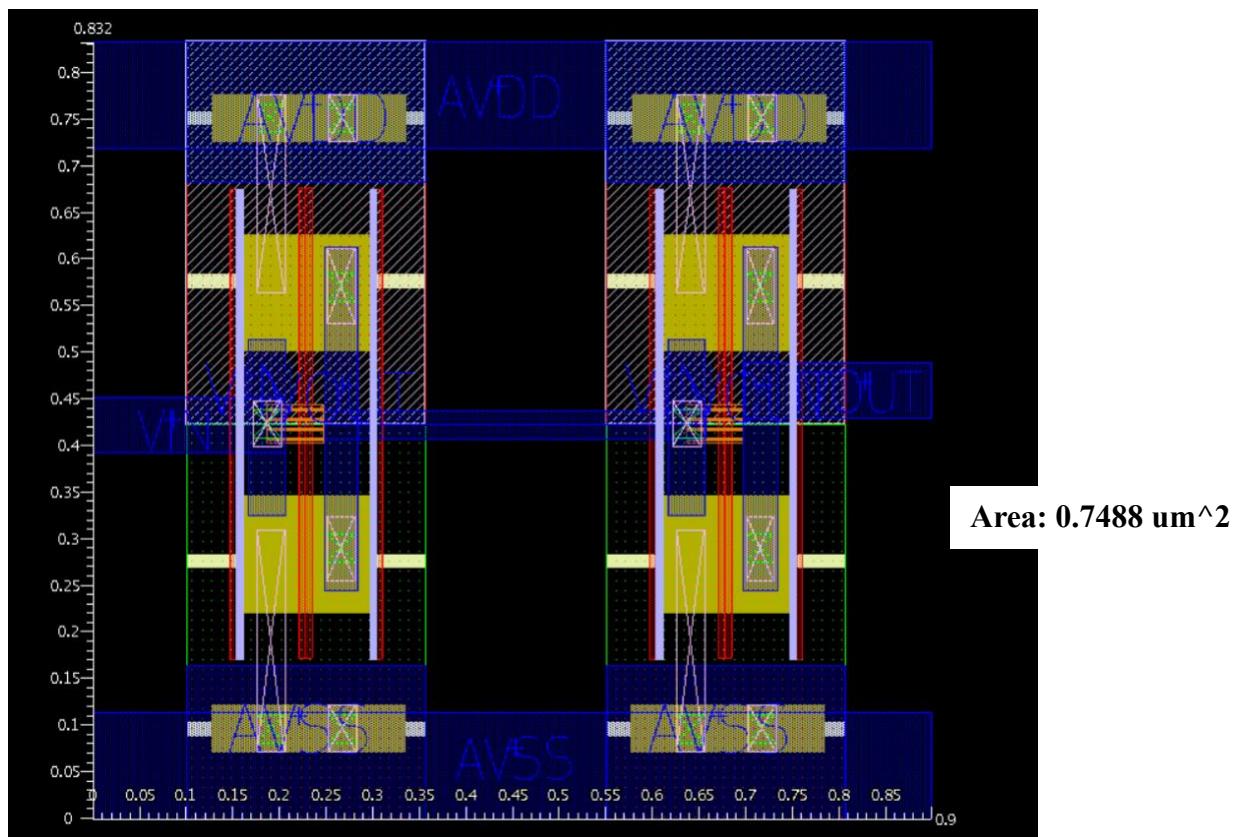
LVS Errors:

```
blackbox cells checked: 0
  passed 0
  failed 0
equivalence points checked: 1
  passed 1
  failed 0
```

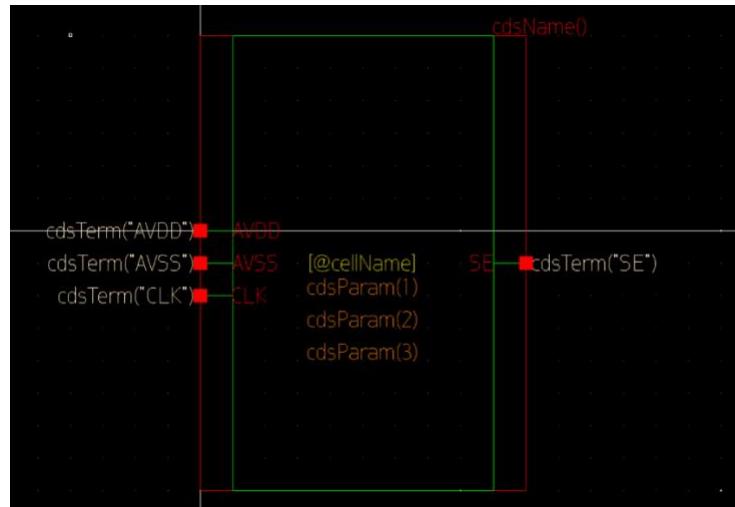
- **Timing Circuit:**
- **Timing Circuit Schematic:**



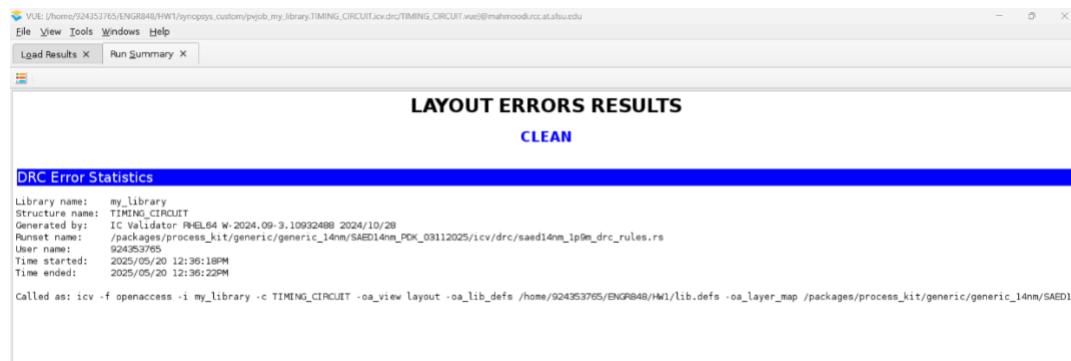
- **Timing Circuit Layout:**



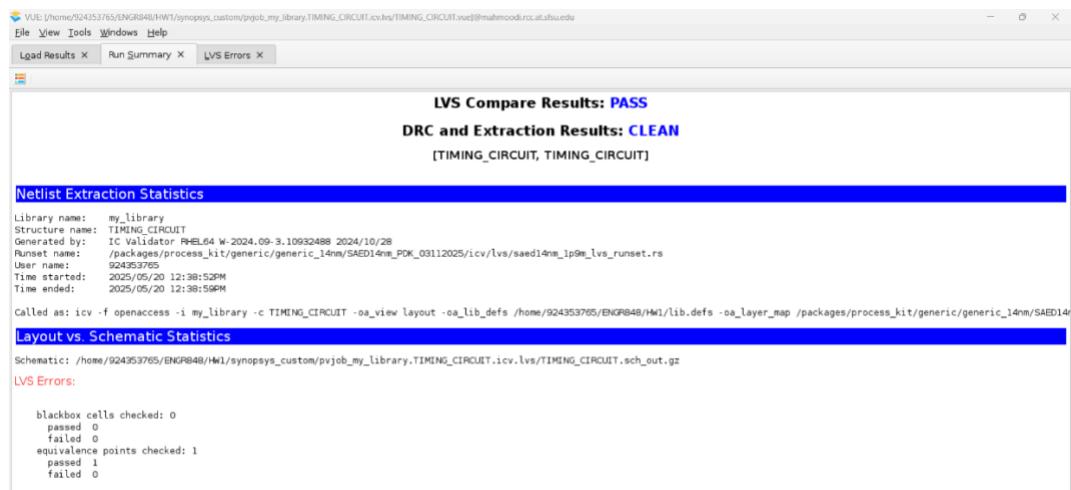
- Timing Circuit Symbol:



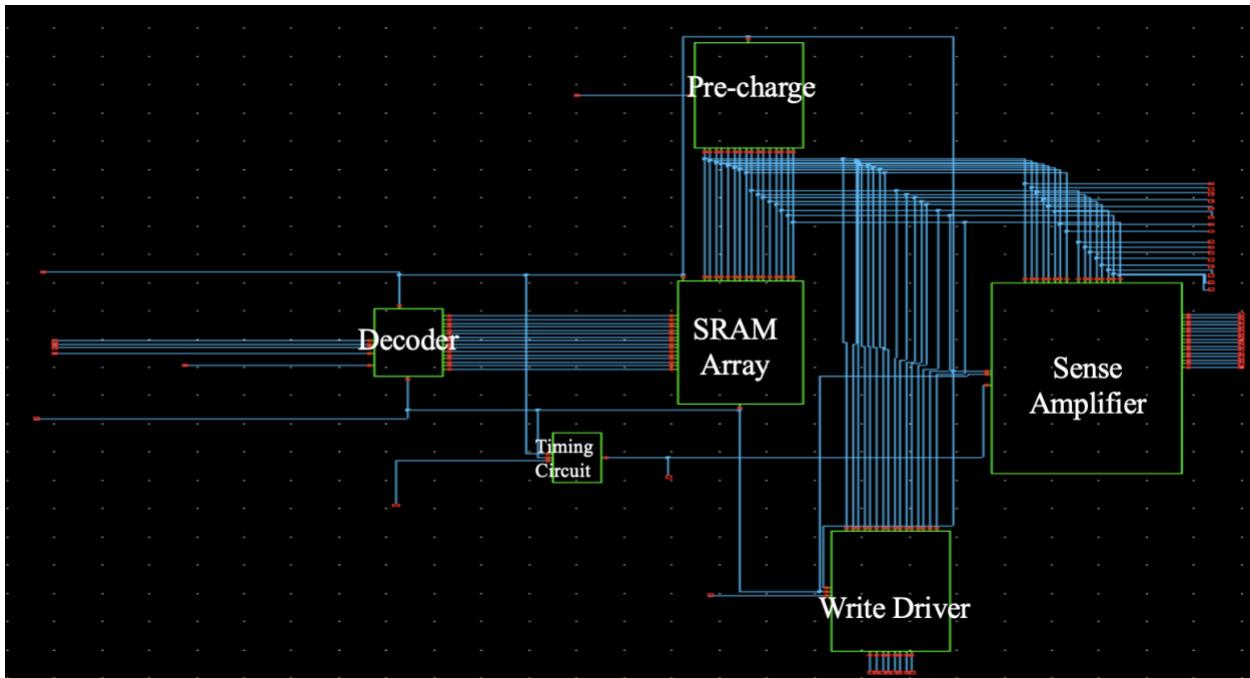
- Design Rule Check:



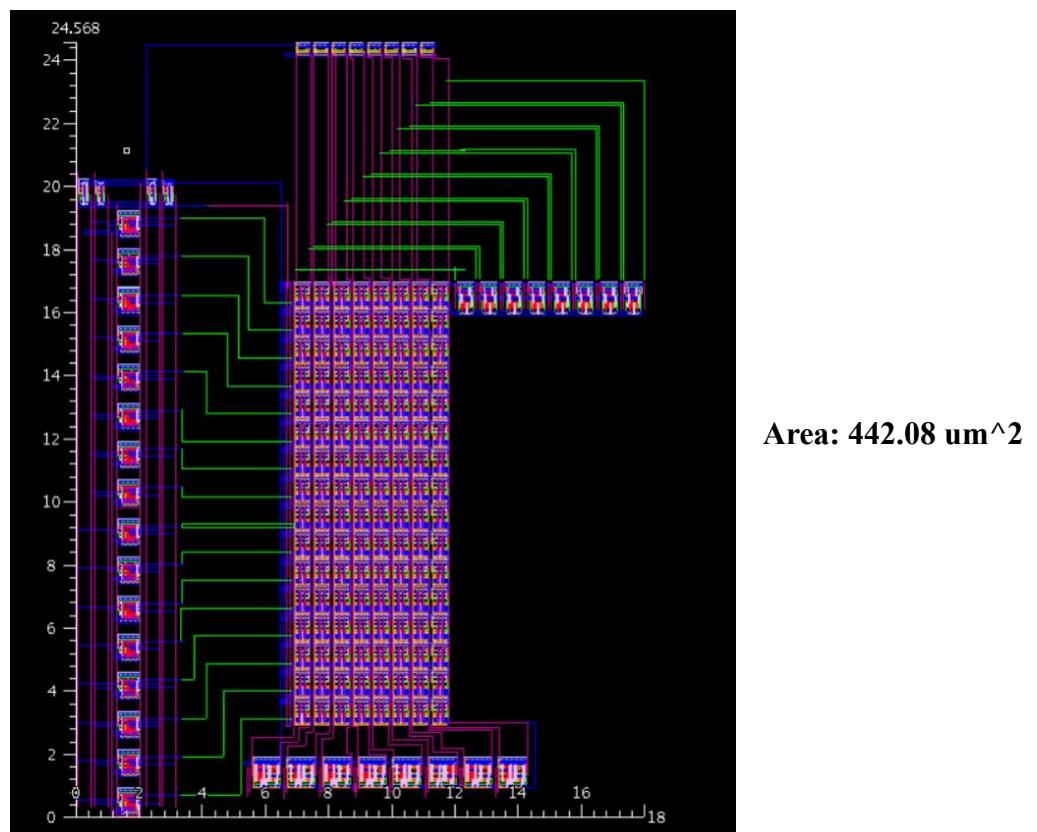
- Layout Versus Schematic:



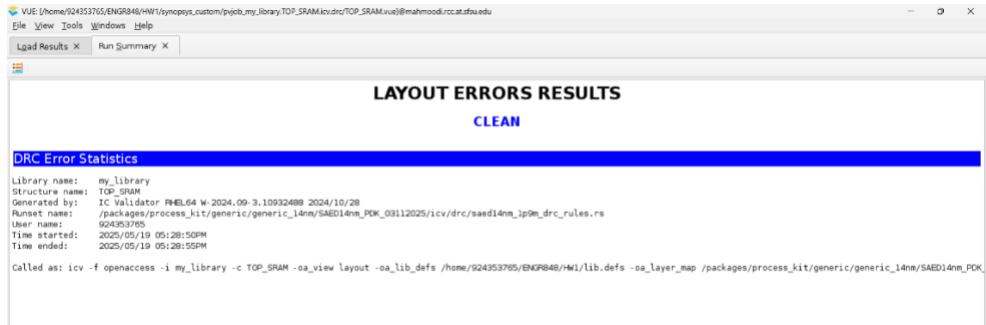
- Top-Level Schematic:



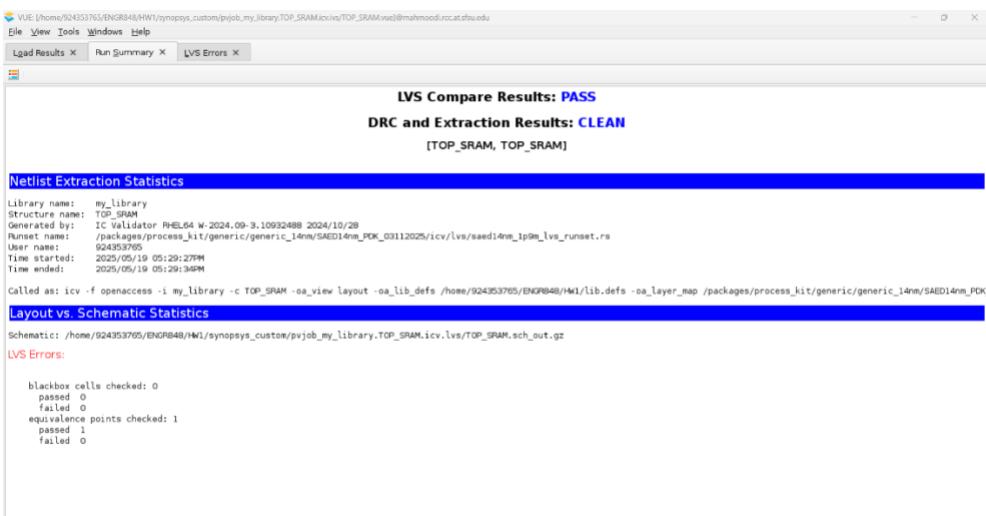
- Top-Level Layout:



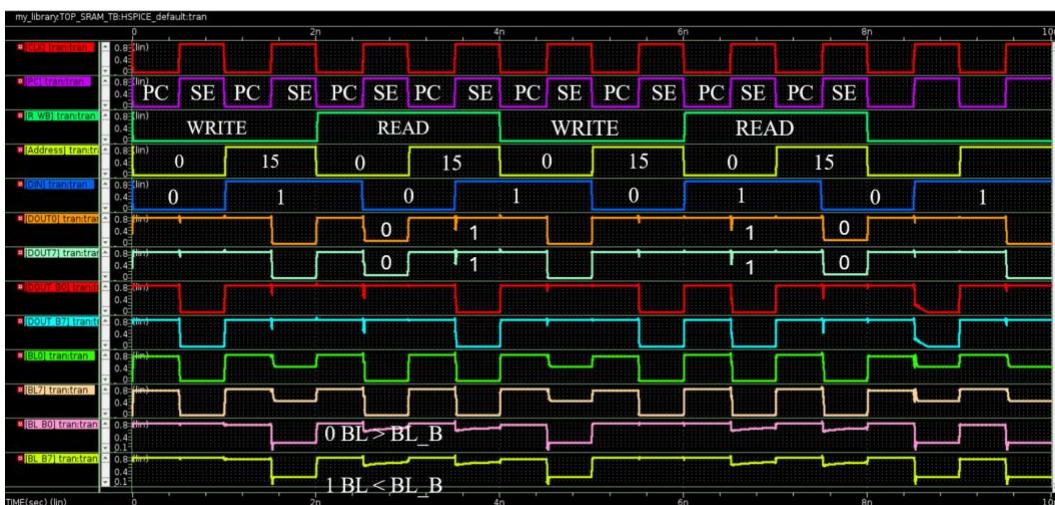
- Design Rule Check:



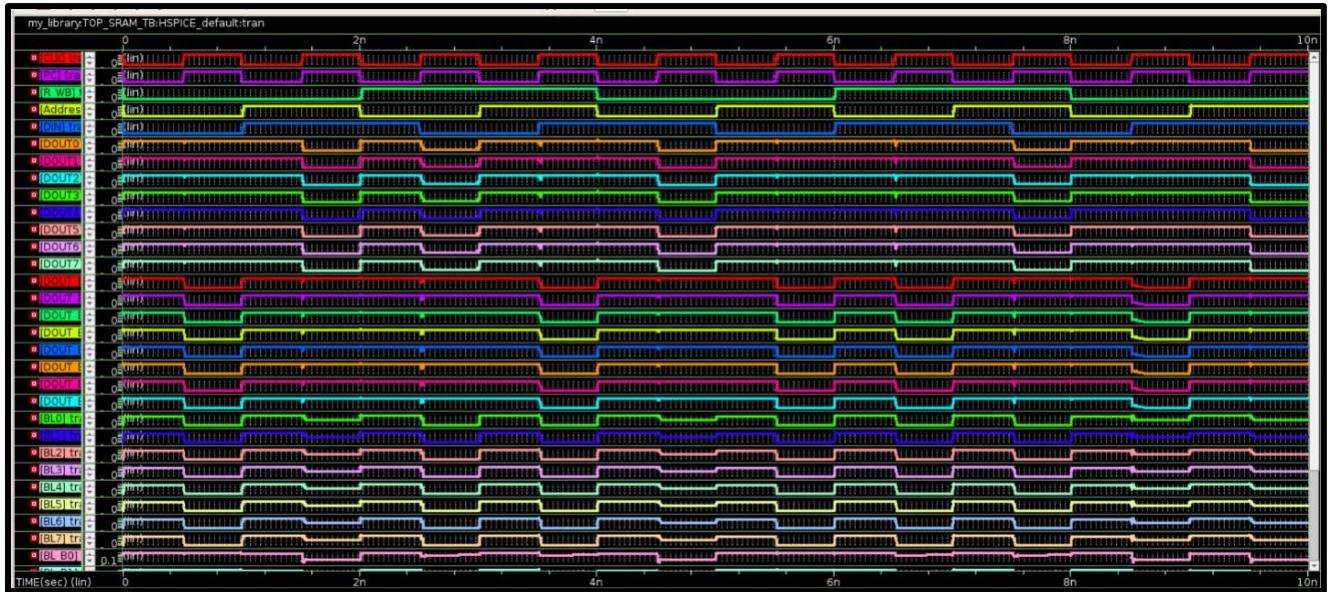
- Layout Versus Schematic:



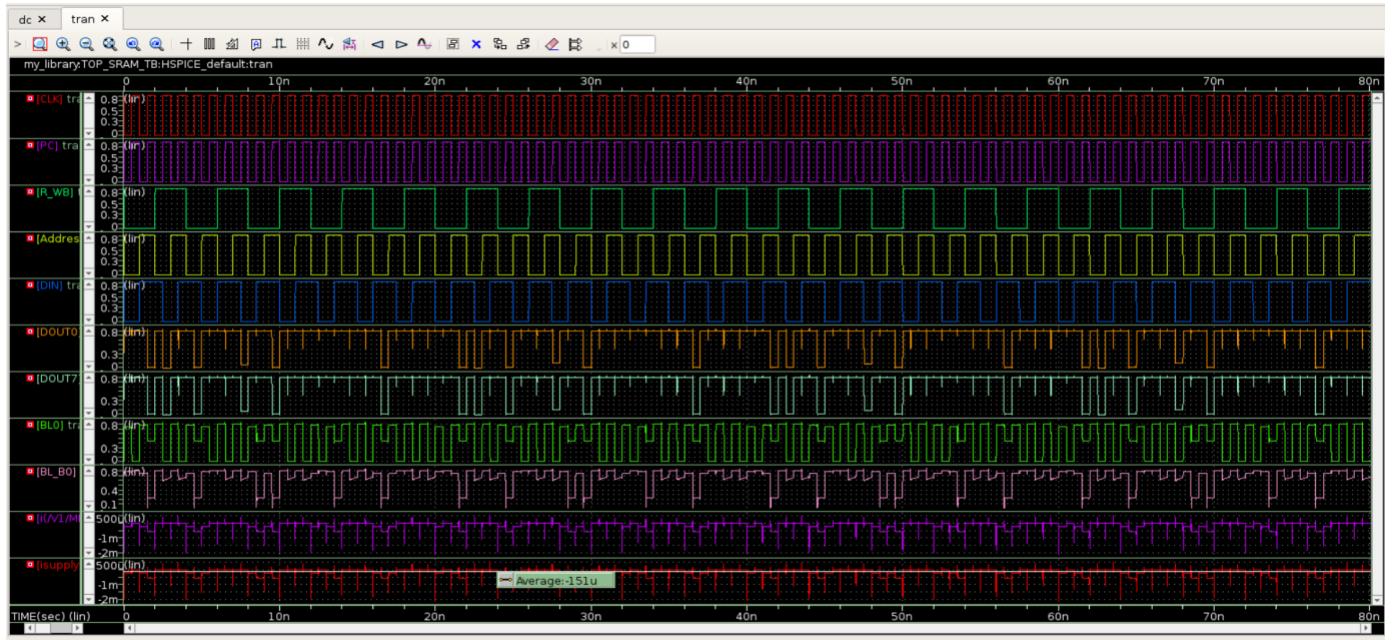
- Functional Verification Pre-Layout:



- Functional Verification Post Layout:

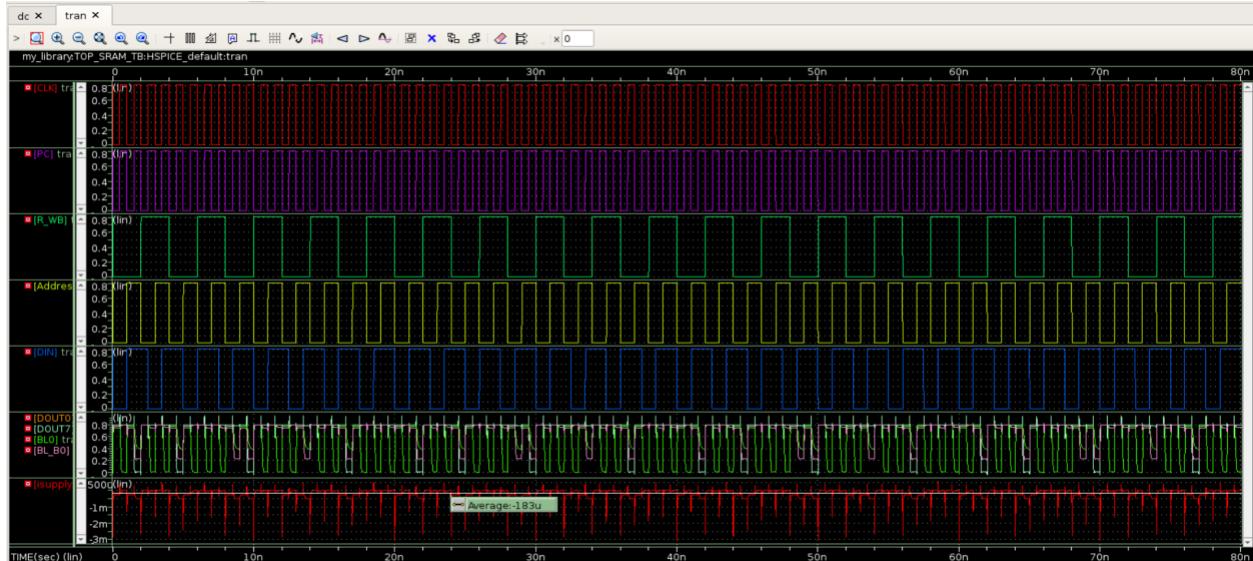


- Pre Layout Active Power:



$$\text{Active Power} = \text{Avg. Current} \times \text{Voltage} = 151 \mu\text{A} \times 0.8 \text{ V} = 120.8 \mu\text{W}$$

- Post Layout Active Power:



$$\text{Active Power} = \text{Avg.Current} \times \text{Voltage} = 183 \mu\text{A} \times 0.8 \text{ V} = 146.4 \mu\text{W}$$

- Pre-layout Maximum Standby Power:



$$\text{Standby Power} = \text{Avg.Current} \times \text{Voltage} = 124 \mu\text{A} \times 0.8 \text{ V} = 99.2 \mu\text{W}$$

- Post-layout Maximum Standby Power:

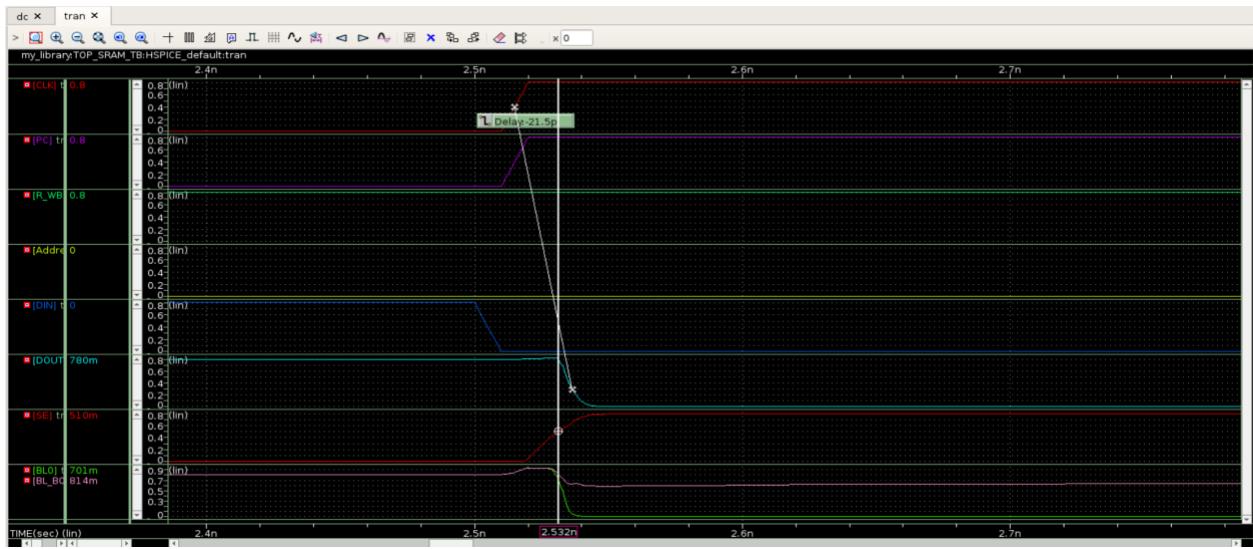


$$\text{Standby Power} = \text{Avg.Current} \times \text{Voltage} = 123 \mu\text{A} \times 0.8 \text{ V} = 98.4 \mu\text{W}$$

- Pre Layout Read Access Time = 13.6p



- Post Layout Read Access Time = 21.5p



Energy Calculations: Active Power/Maximum Frequency

$$\text{Energy} = 146.4 \mu\text{Watt}/1 \text{ GHz}$$

$$\text{Energy} = 1.464 \times 10^{-13} \text{ joules per cycle}$$

- Project Requirements Achieved:

Requirements	Pre-Layout	Post-Layout
Design Rule Check	YES	YES
Layout Versus Schematic	YES	YES
Layout Parasitic Extraction	YES	YES
150 mv SNM	YES	YES
100 mv BL BLB Difference	YES	YES
Maximum Standby Power	99.2 μW	98.4 μW
Access Time	13.6 p	21.5 p
Active Power	120.8 μW	146.4 μW
Frequency	1 GHz	1 GHz
Area	442.224 μm^2	442.224 μm^2

Conclusion

In this project, we successfully designed, implemented, and validated a **16x8 SRAM memory array** using **14nm CMOS technology**. The design encompassed all essential components of an SRAM system, including the 6T memory cell, precharge circuits, decoder, sense amplifiers, drivers, and timing control.

Through schematic creation, layout design, and rigorous validation using **Design Rule Check (DRC)** and **Layout Versus Schematic (LVS)** procedures, we ensured that each block met both functional and manufacturing standards. The final design achieved excellent performance metrics, including a **read access time of 21.5 ps**, **low standby power consumption**, and **operational frequency of 1 GHz**, all within a compact area footprint of **442.224 μm^2** .

What We Learned

1. Deep Understanding of SRAM Architecture:

We gained a solid grasp of how a 6T SRAM cell functions and how to integrate it into larger arrays efficiently.

2. Custom CMOS Layout Design:

We developed hands-on experience with transistor-level layout in a deep-submicron process, learning how to optimize for area, power, and performance.

3. Hierarchical Design Integration:

By building modular components (cells, decoders, drivers) and integrating them into a full system, we learned the importance of scalable, reusable design strategies.

4. DRC and LVS Validation:

Running and passing these checks taught us the critical role of physical verification in ensuring that a design is both manufacturable and true to the intended functionality.

5. Simulation and Timing Analysis:

We learned how to simulate SRAM behavior at the schematic and layout levels and interpret waveform data to validate performance metrics such as access time and power.

6. Project Planning and Execution:

Completing this end-to-end design within the constraints of a course timeline gave us practical experience in planning, debugging, and presenting a real-world VLSI design project.