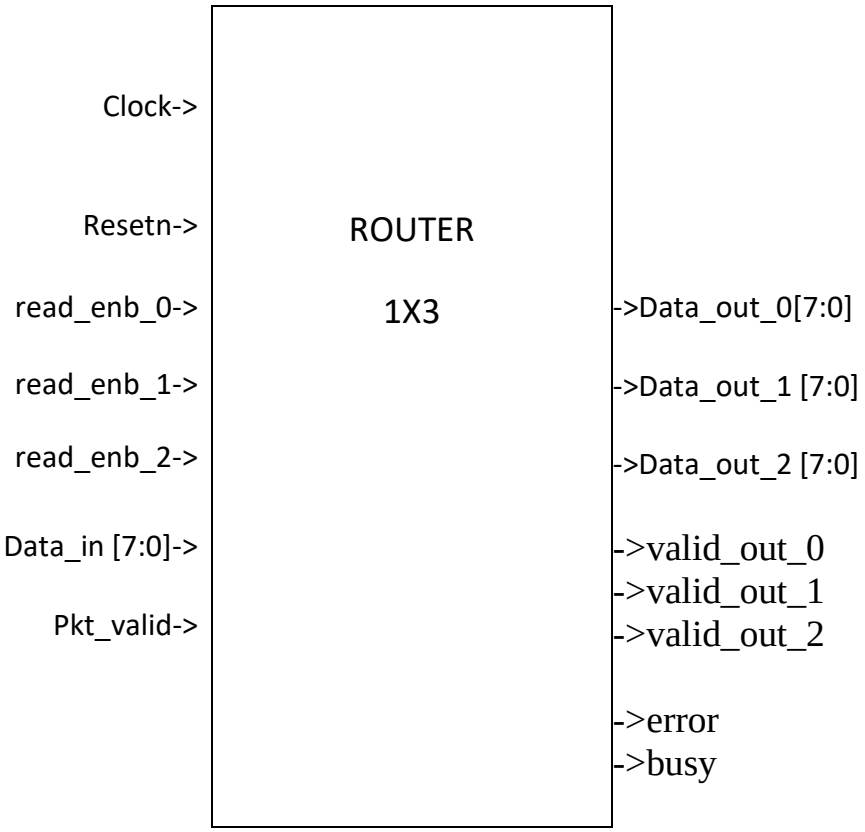
Verification Plan for the ROUTER 1X3

ROUTER 1X3:



Router is a device that forwards data packets between computer networks

- It is an OSI (Open system interconnection) layer 3 routing device
- It drives an incoming packet to the output channel based on the address field contained in the packet header.

  Design architechture contains:

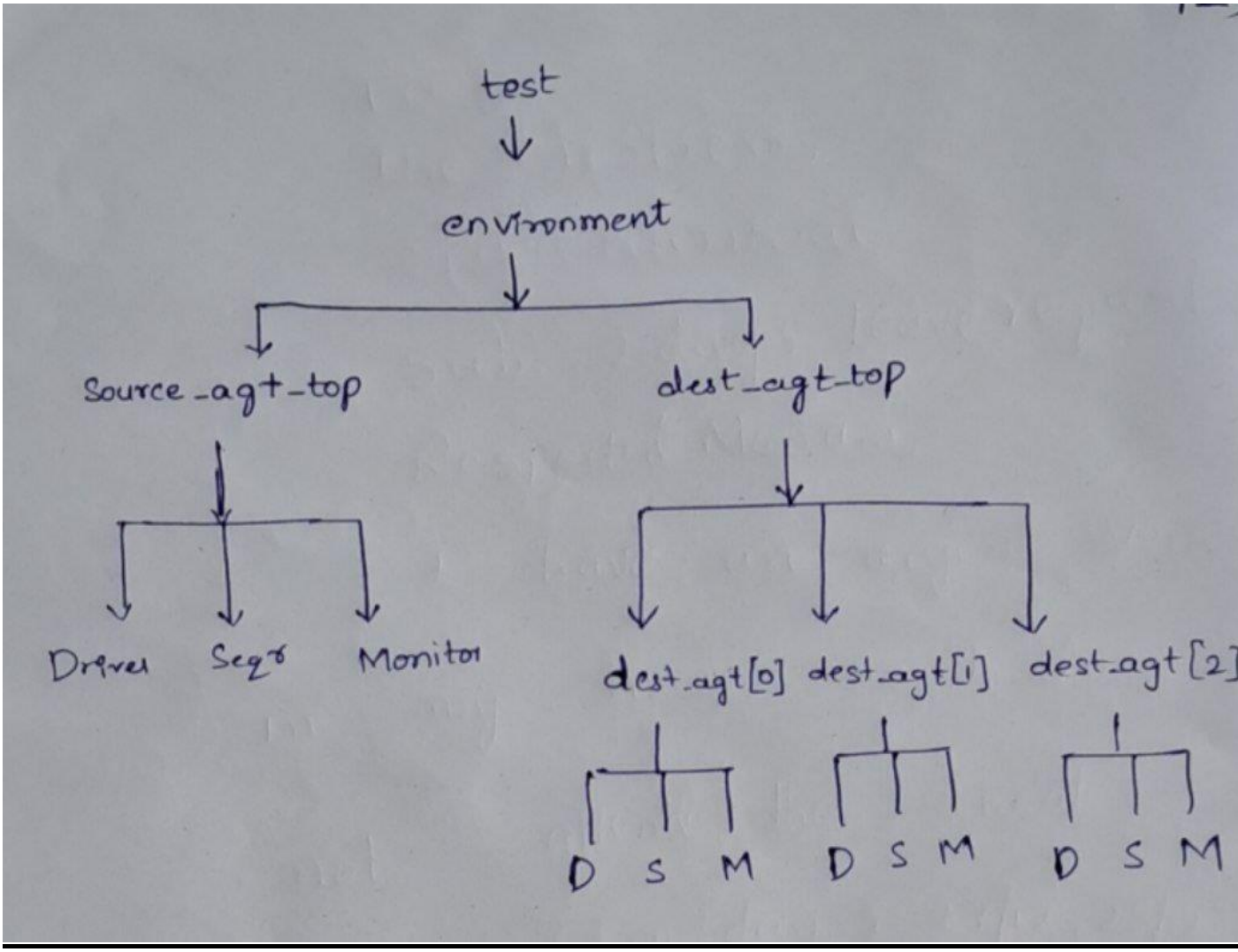
  >> FIFO s =3 of memory size 16X9

  >> FSM (controller circuit)

  >> Synchronizer (for providing faithful communication between input and 3 output ports) &(provides synchronization between FSM and Fifo modules)

  >> Register (4 internal registers logic HB, FFB, IP, PP)

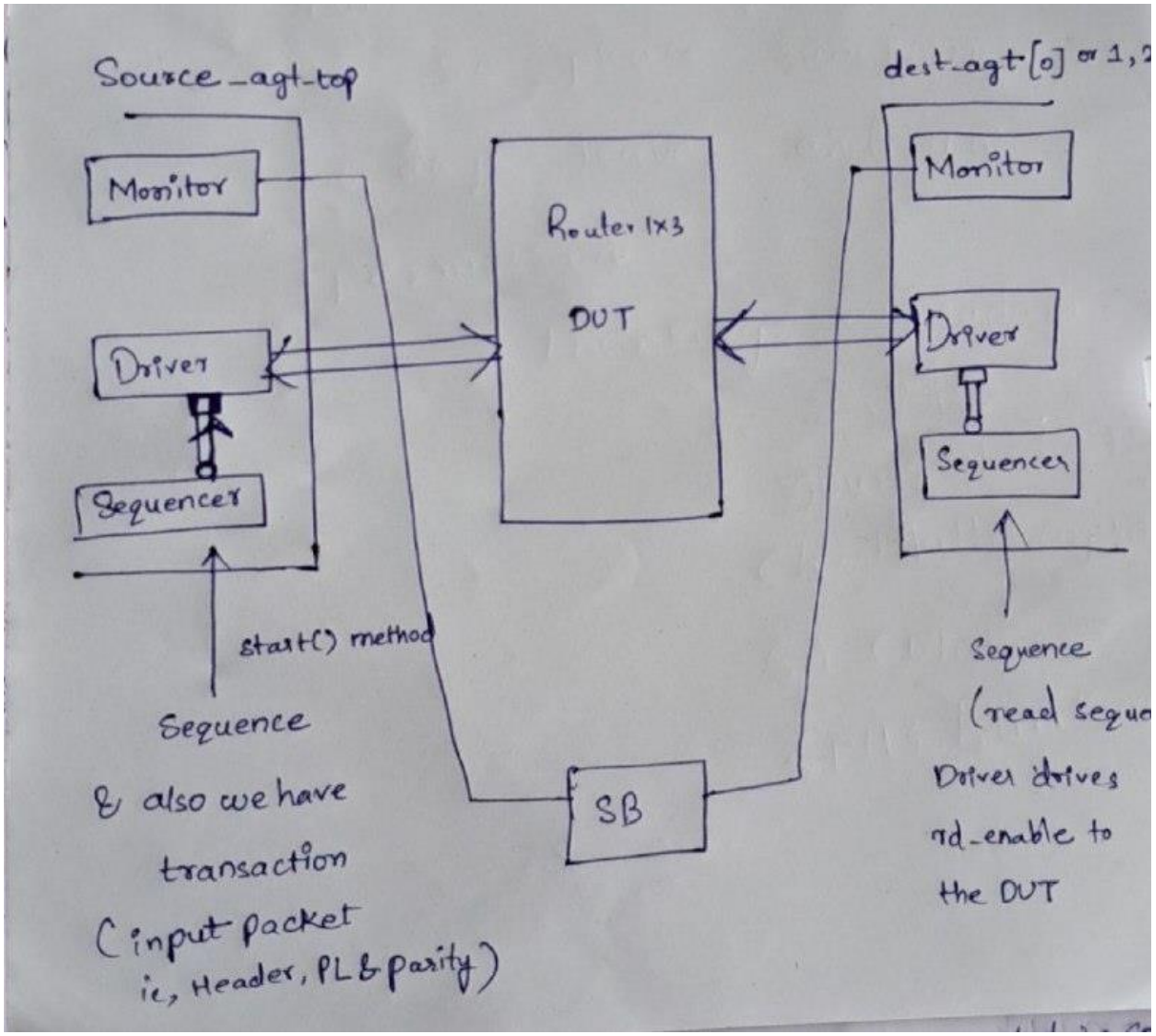
TB Environment:



Create only one dest_agt class

Reason: Anyhow at a time one destination is going to be active (as per Router protocol)

>>Remaining two dest_agt are to be instantiated in top module.


Source_agt_top
Monitor
Driver
Sequencer
start() method
Sequence
& also we have
transaction
(input packet
ie, Header, PL & parity)
Router 1x3
DUT
SB
dest_agt[0] or 1,2
Monitor
Driver
Sequencer
Sequence
(read sequ
Driver drives
rd_enable to
the DUT

Features:

- resetn: active LOW synchronous reset

- read_enb_0, 1,2
  - ❖ reads the packet through output data_out_0,1,2 respectively

- Data_in
  - ❖ 8 bit input data packet (from source_agt[0] to router DUT)

- Pkt_valid: detects arrival of new packet from source network (write seqence

- Data_out
  - ❖ 8 bit output data packet (router DUT to destination dst_agt[0] or 1 or 2.

- busy: detects a busy state for the router that stops accepting any new byte (=1 if fifo_full=1 of destination fifo)

- error : detects mismatch between packet parity and internal parity

- valid_out_0,1,2:
  detects weather valid byte is available for destination network dest_agt[0]/1/2