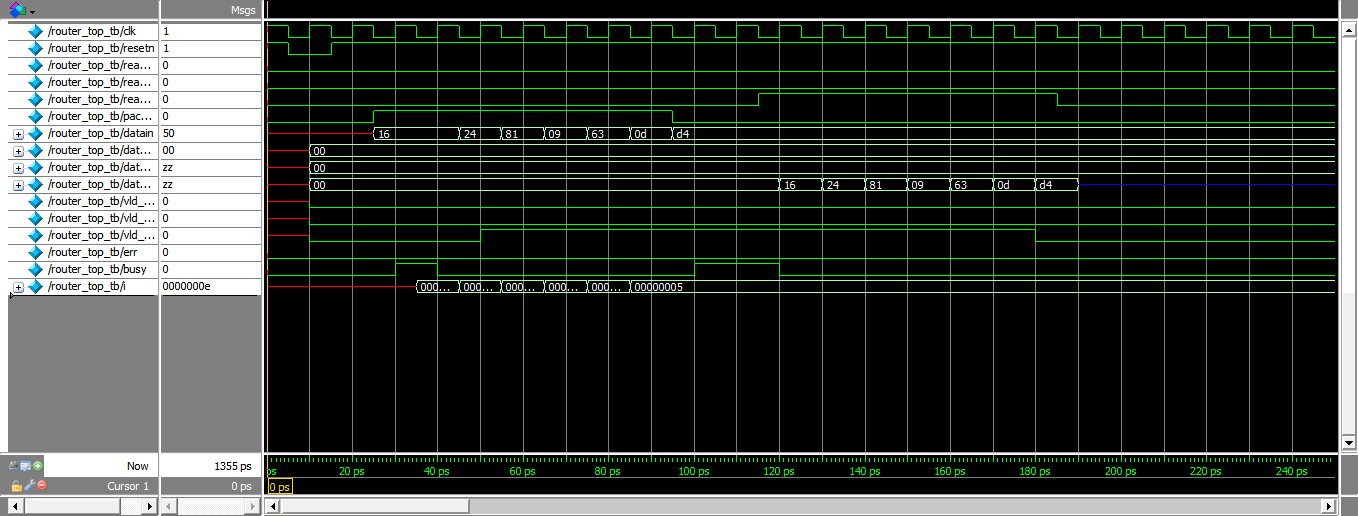
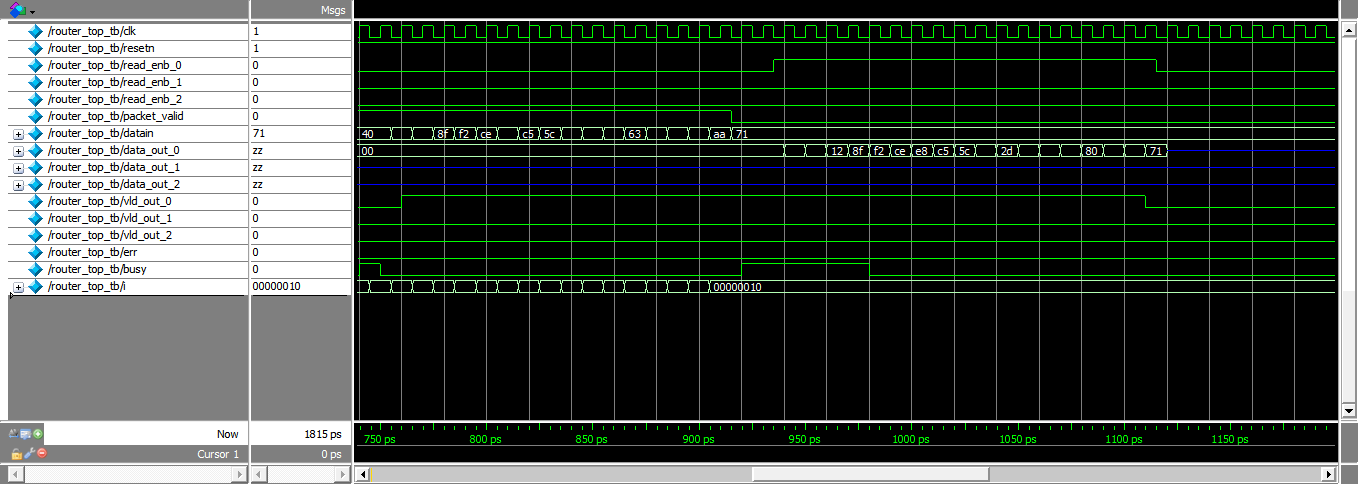
Simulation and Synthesis results:

1)Router Top module

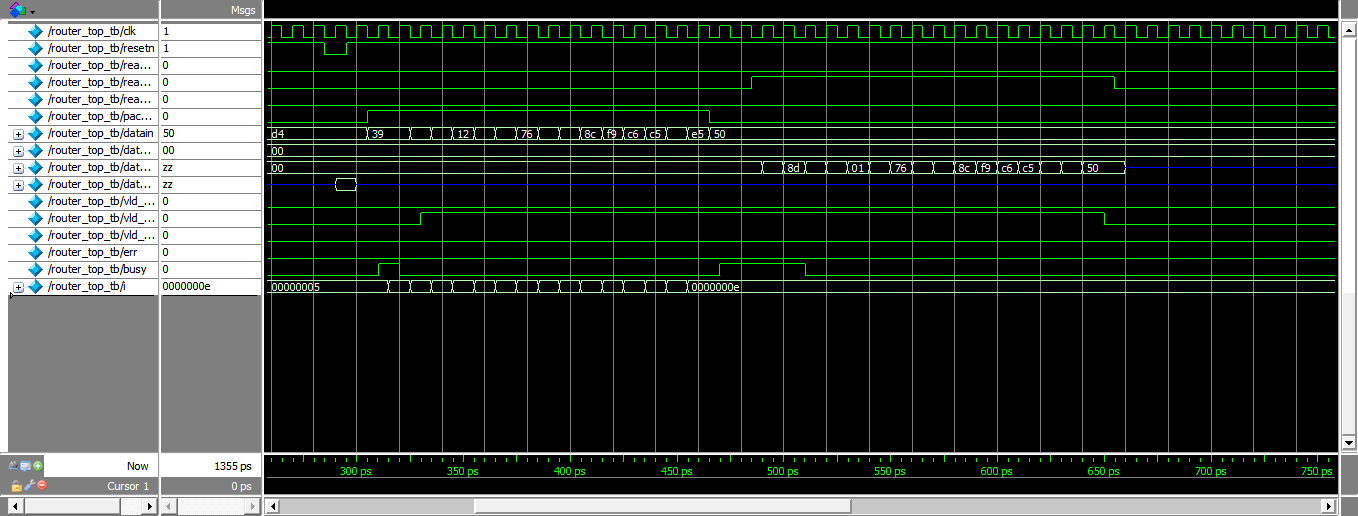
pktm\_gen\_5;

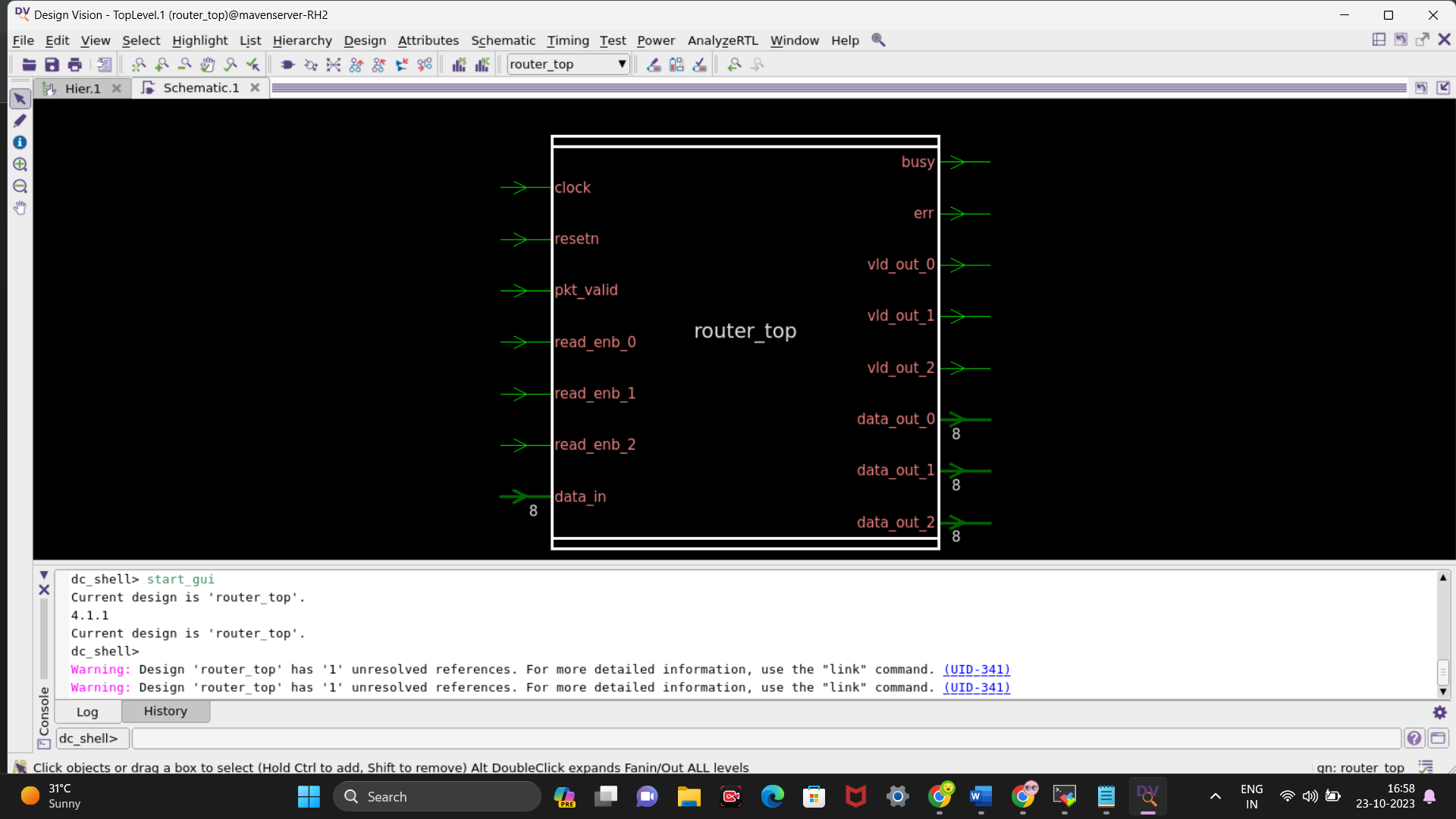


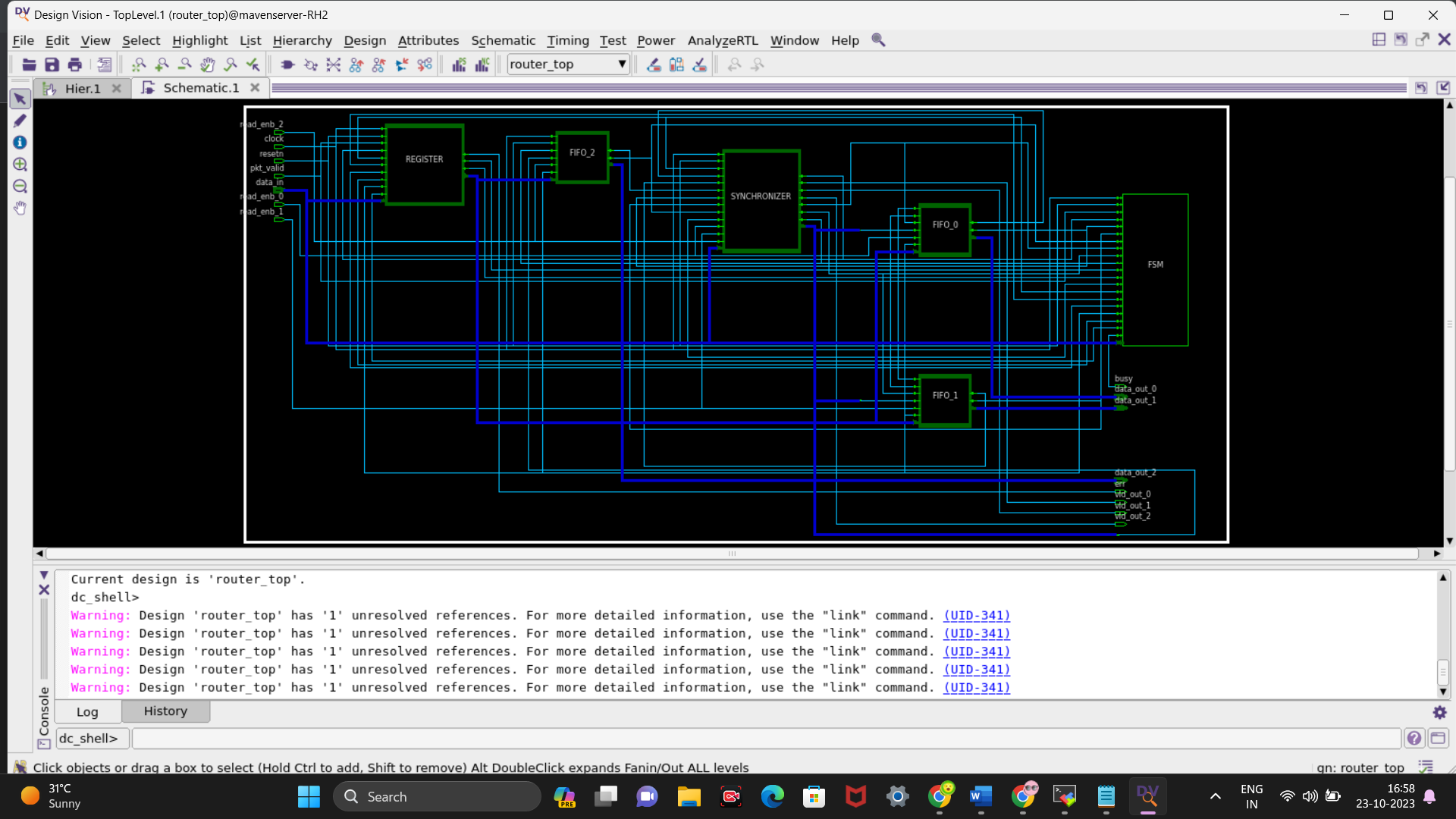
pktm\_gen\_16;



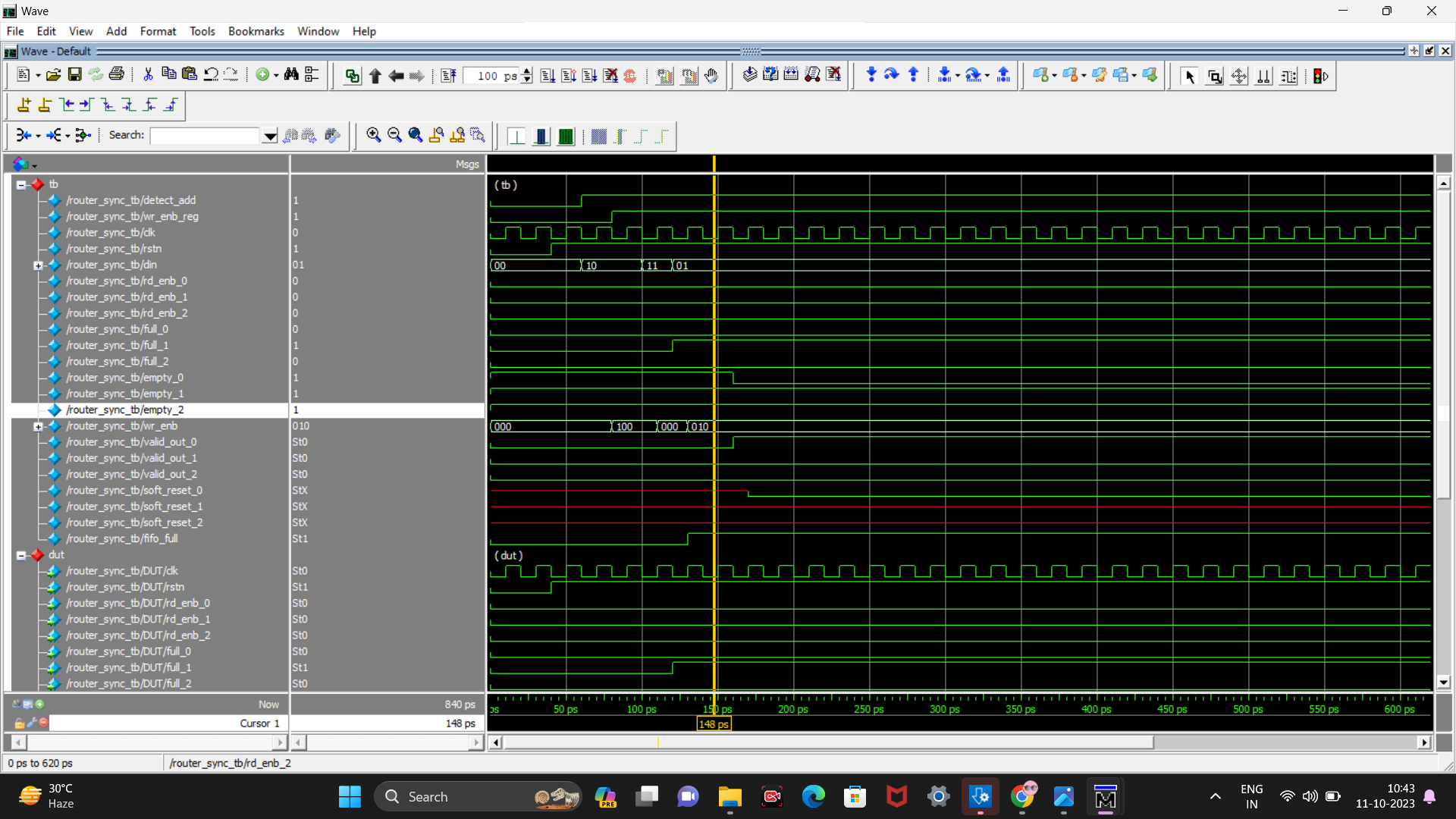
pktm\_gen\_14;



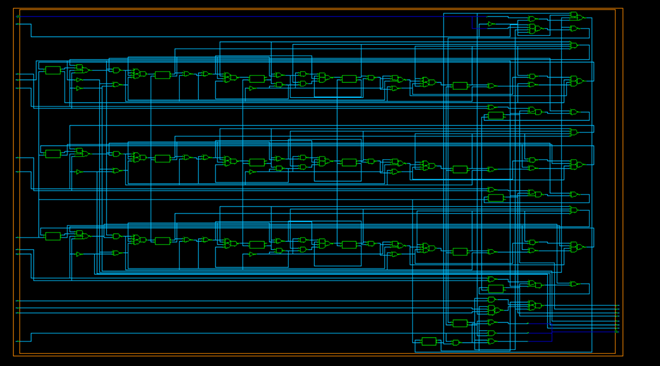




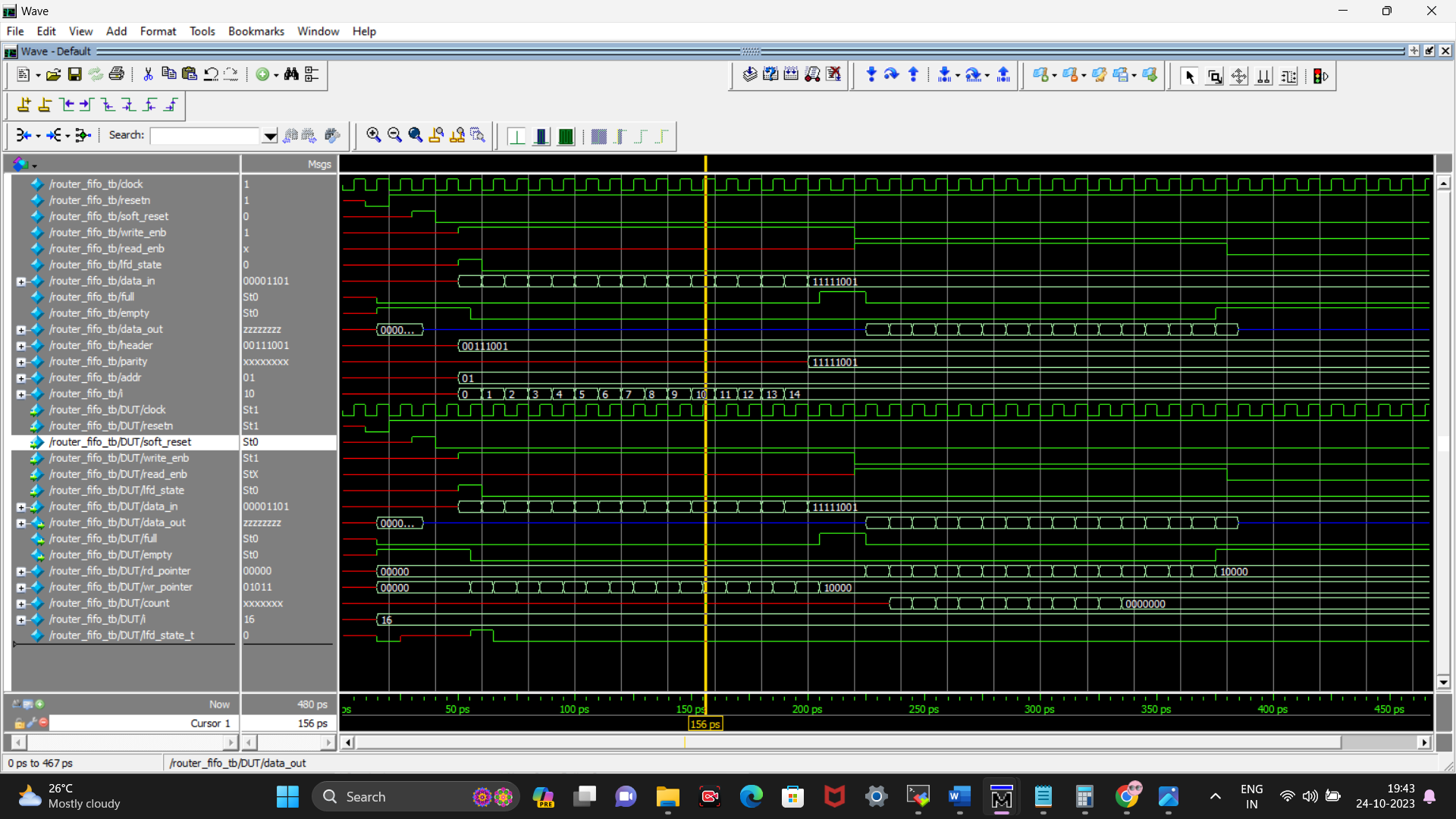
2)Synchroniser module

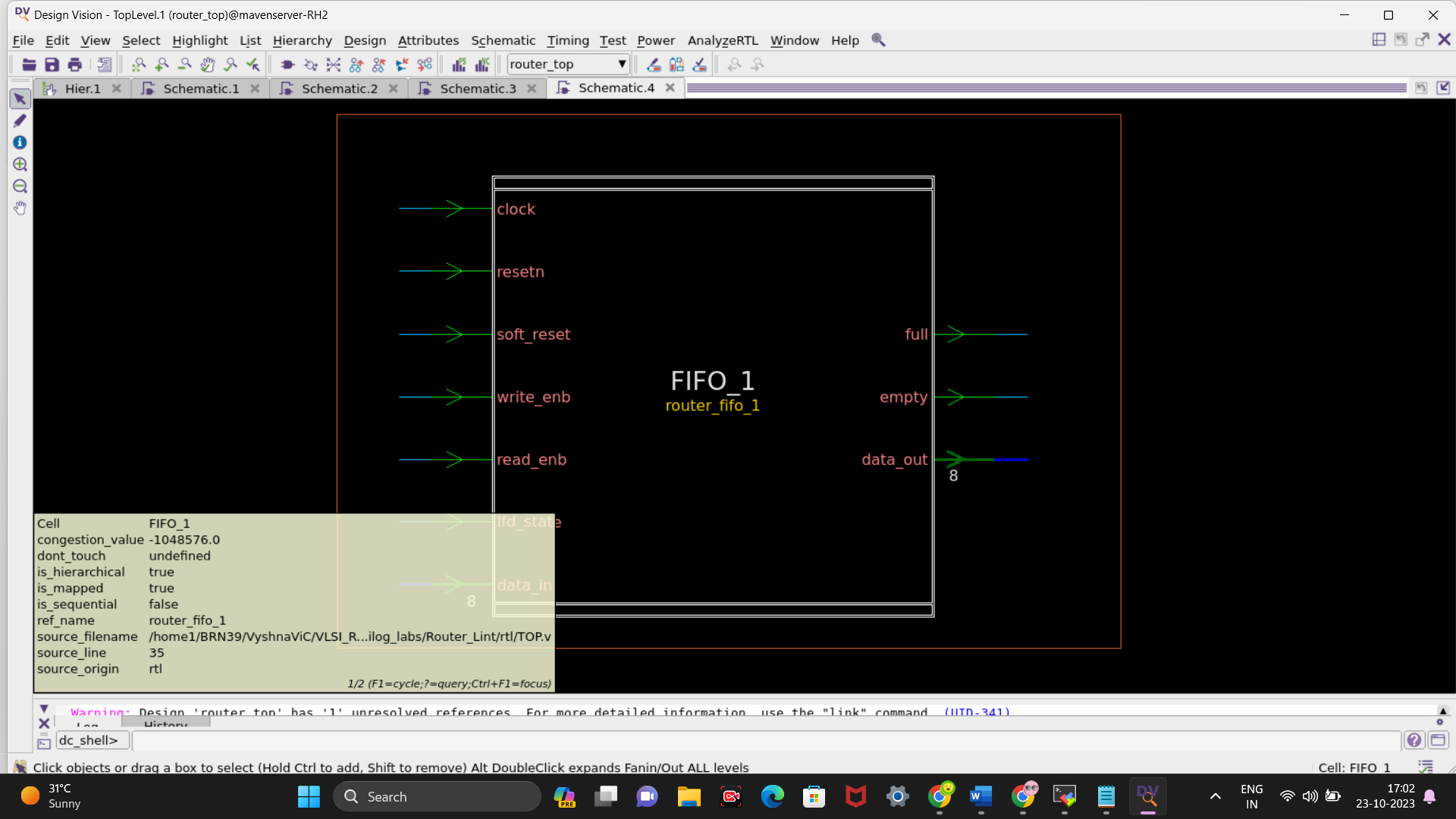


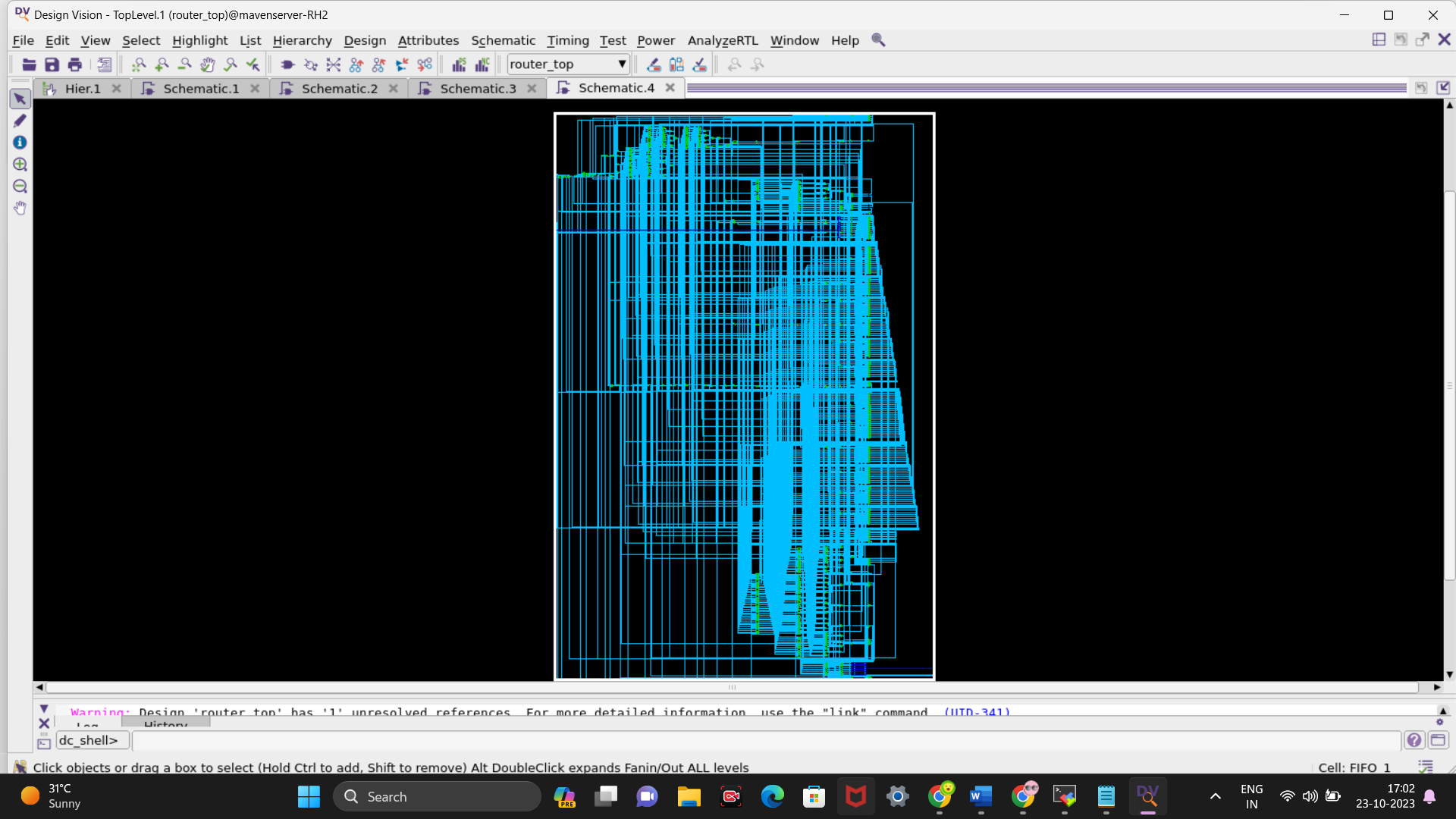




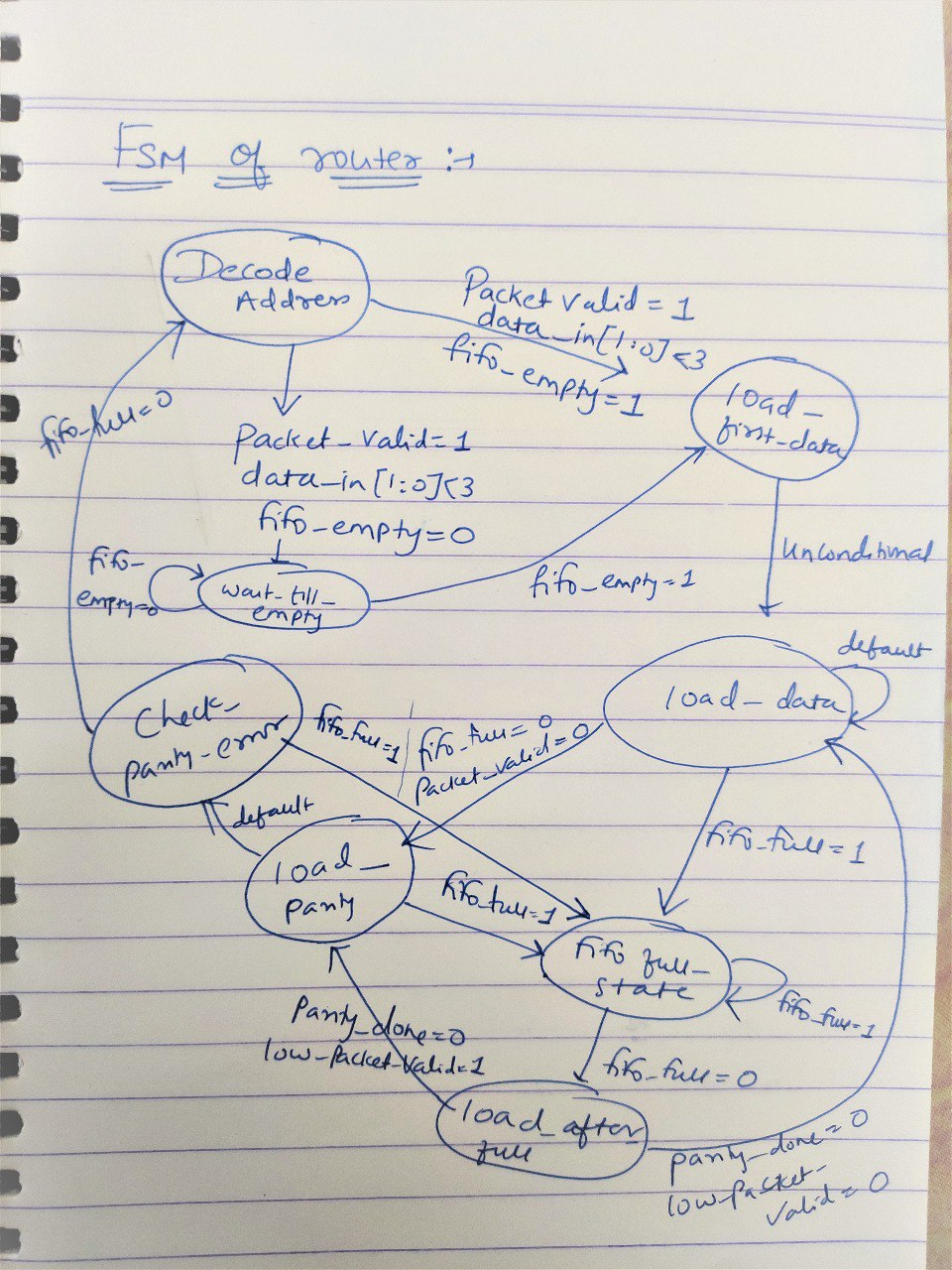
3)fifo module

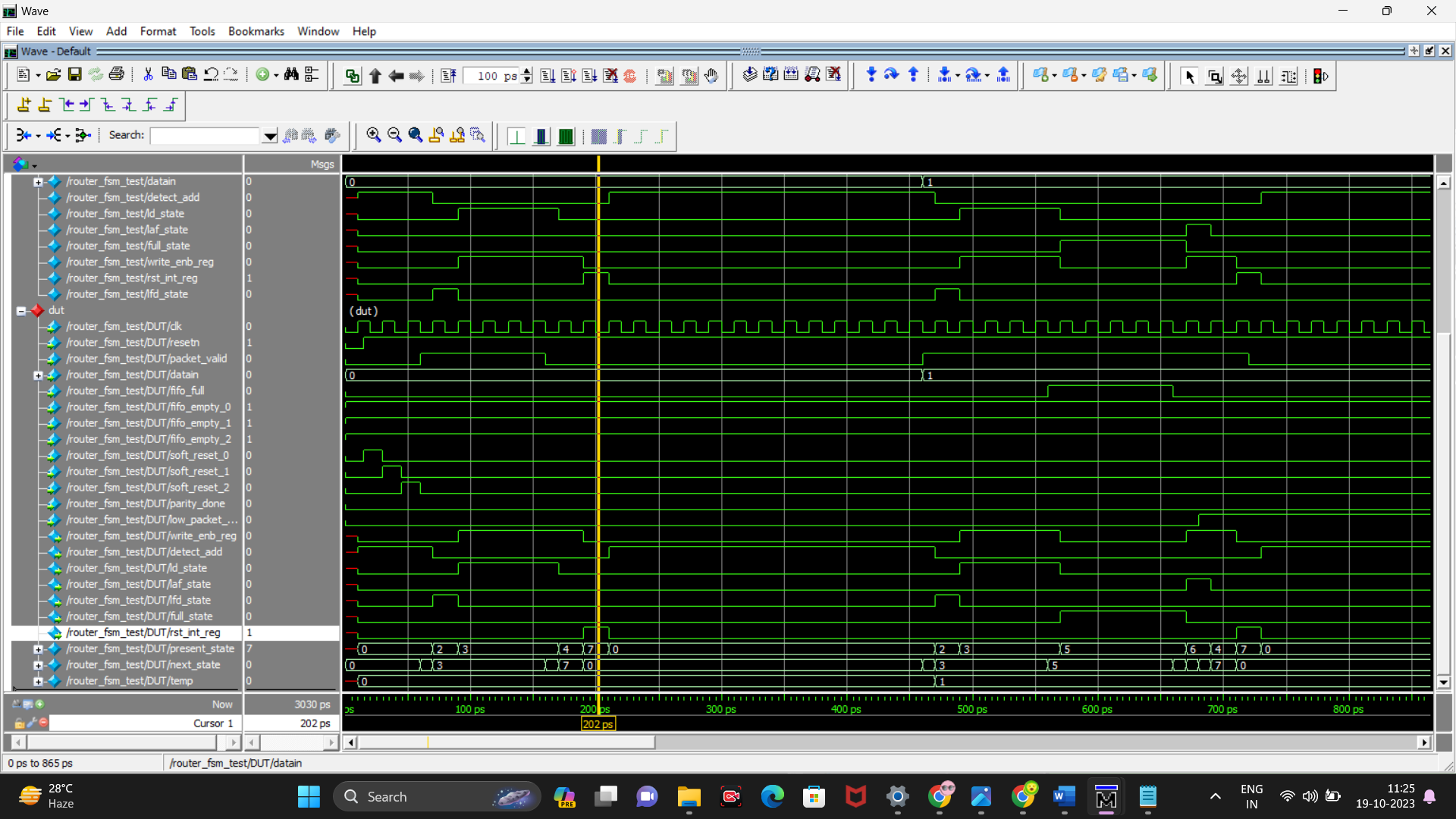




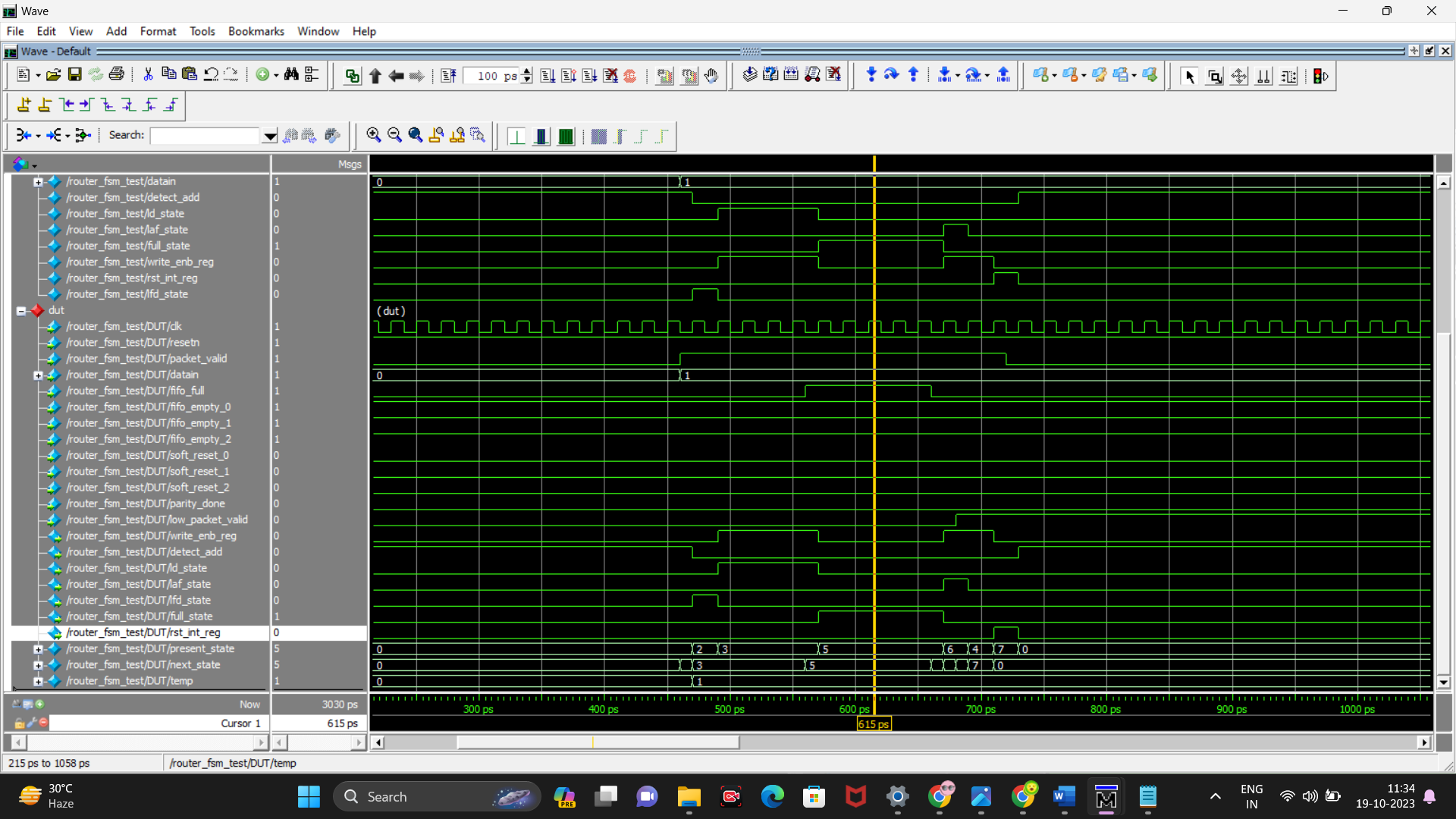


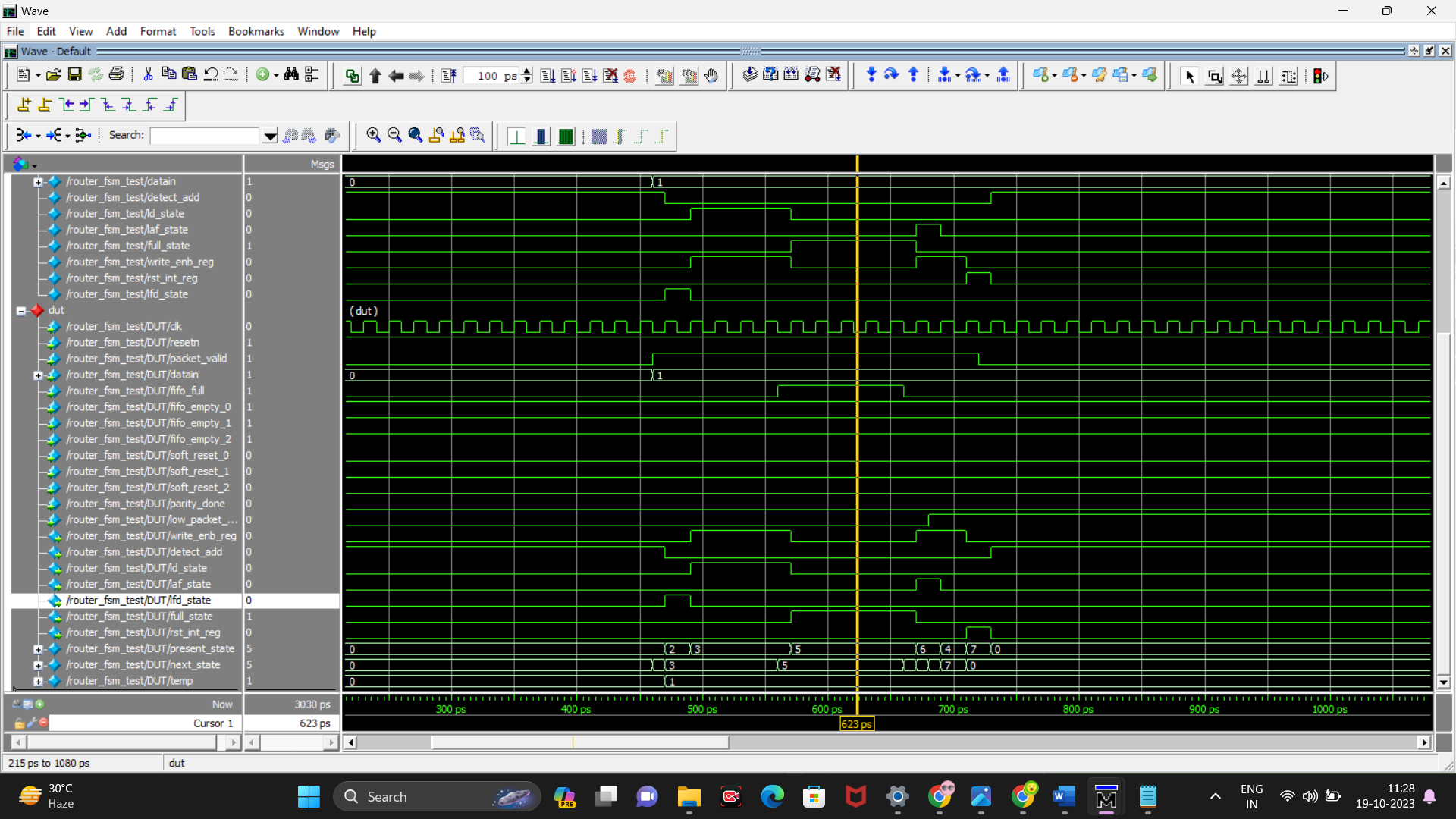
4)FSM module

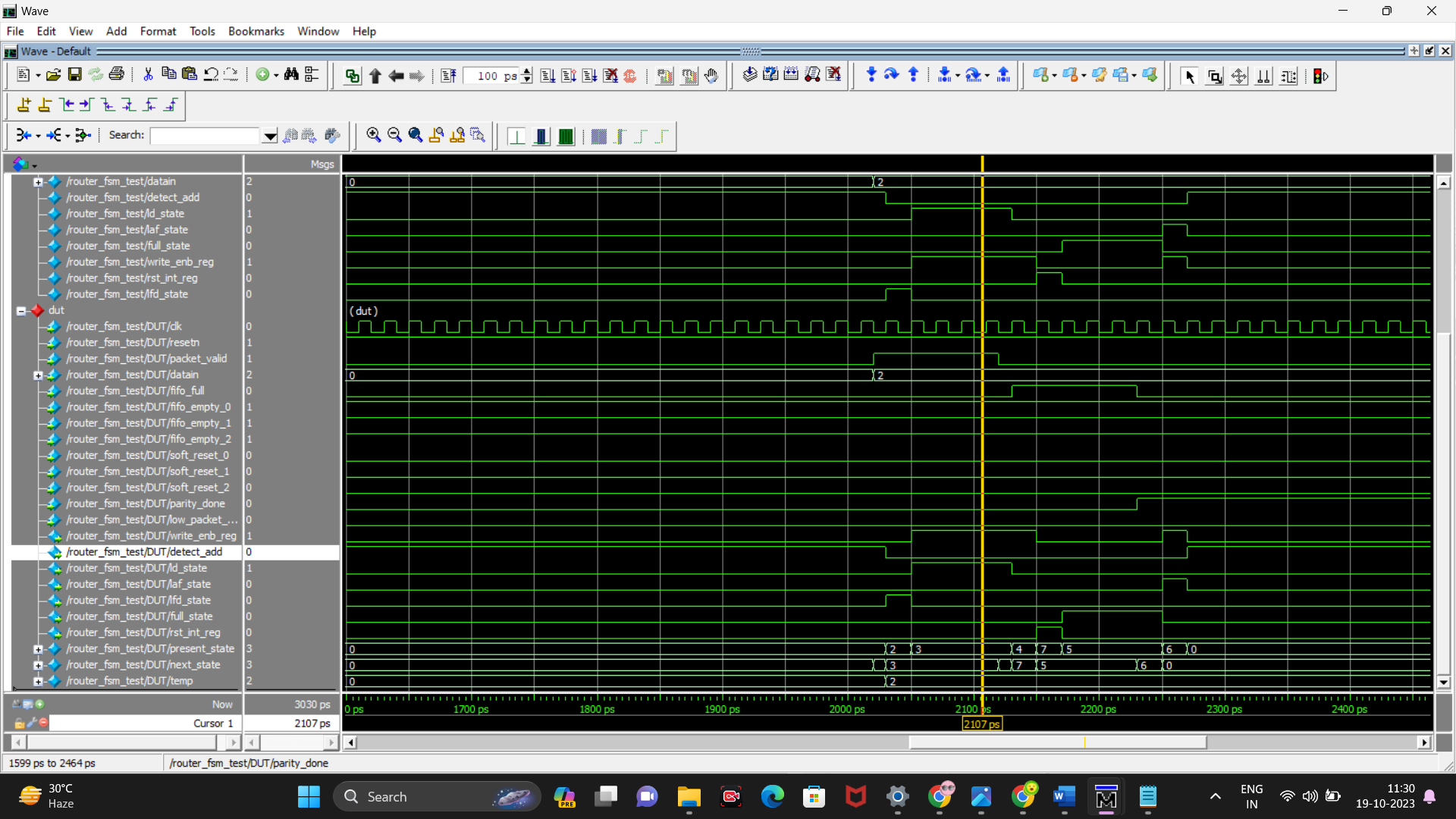


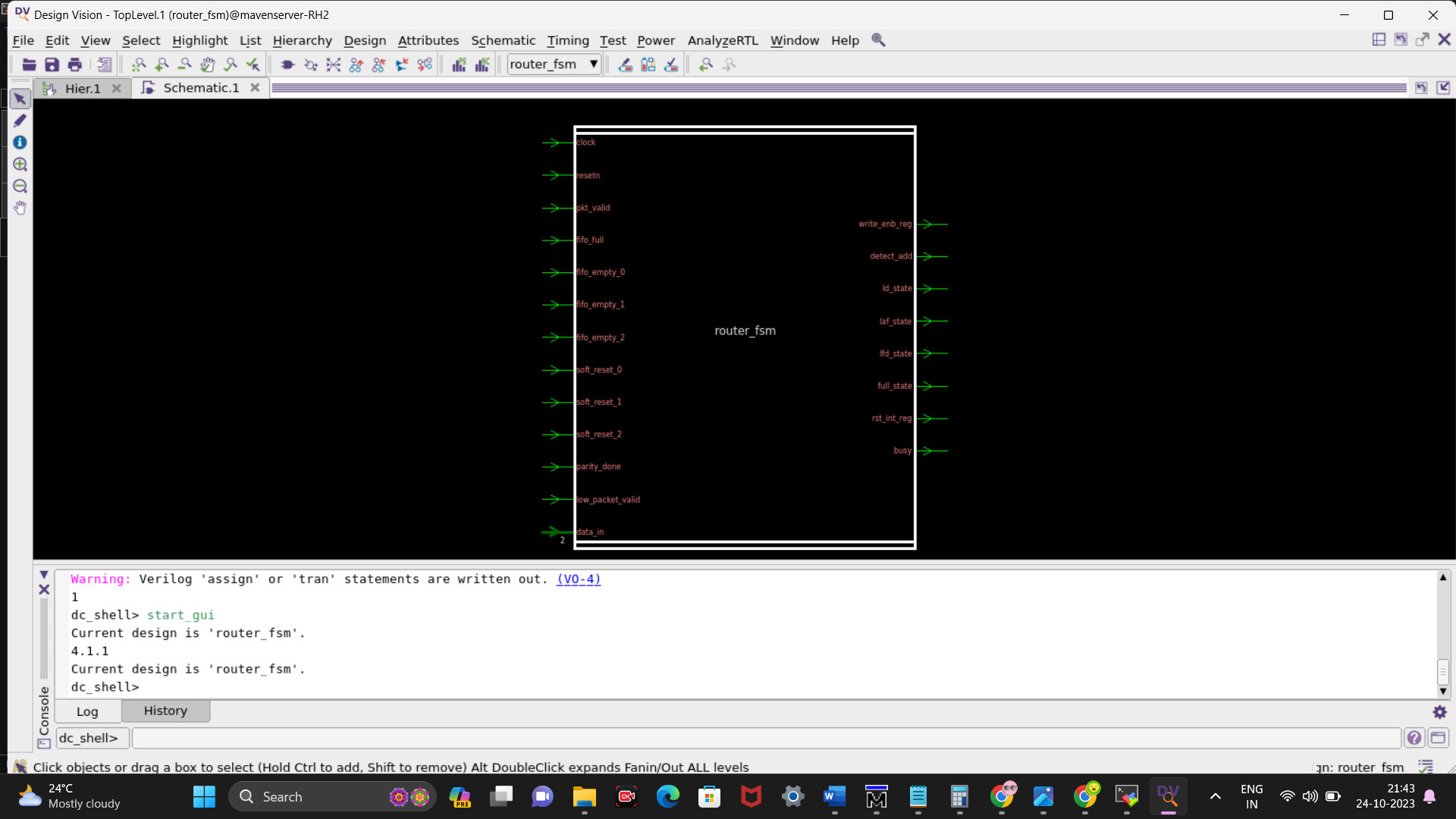
DA\_LFD\_LD\_LP\_CPE\_DA; //000, 010, 011, 100, 111, 000 (0,2,3,4,7,0)

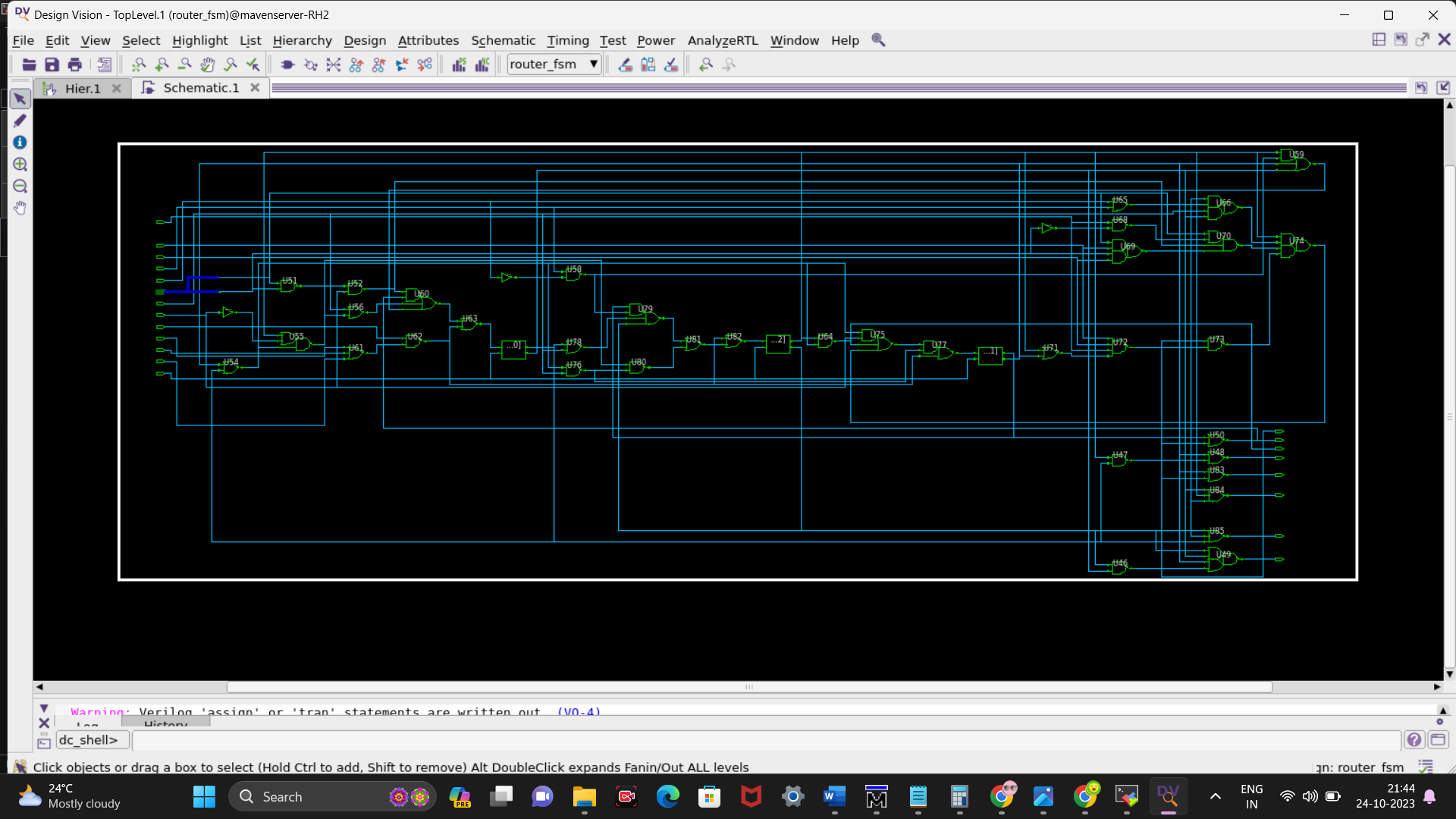
DA\_LFD\_LD\_FES\_LP\_CPE\_DA(); // 000, 010, 011, 101, 100, 111, 000(0,2,3,5,6,4,7,0)



DA\_LFD\_LD\_FES\_LAF\_LD\_LP\_CPE\_DA; // 0,2,3,5,6,3,4,7,0

DA\_LFD\_LD\_LP\_CPE\_FES\_LAF\_DA; // 0,2,3,4,7,5,6,0





5) register module

