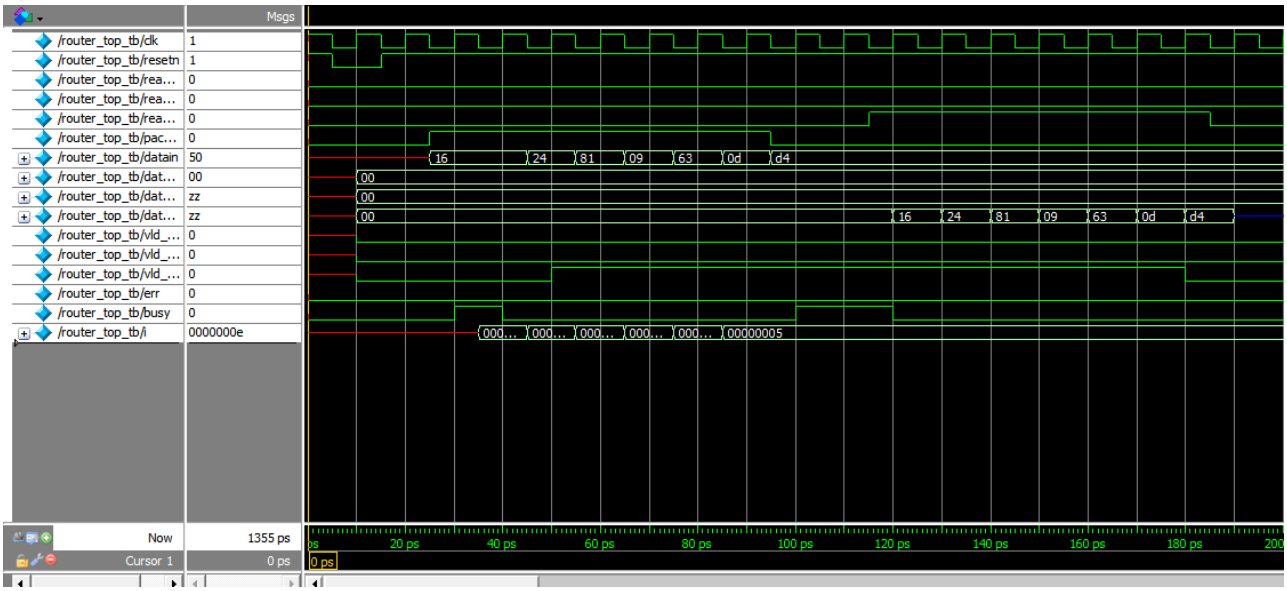
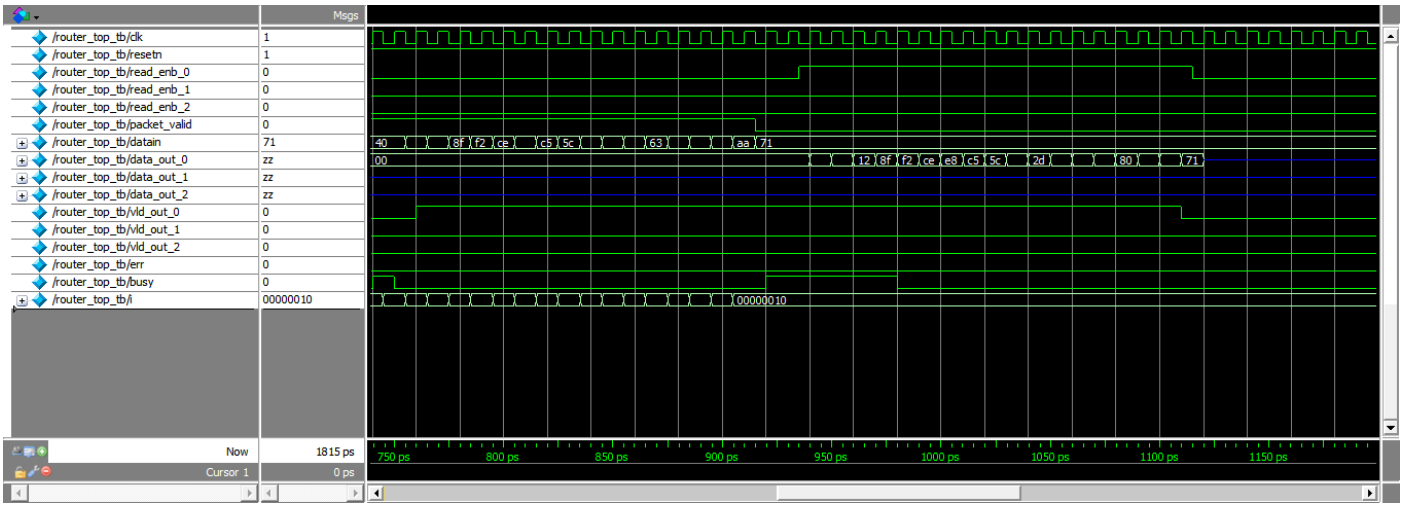
Simulation and Synthesis results:

1)Router Top module

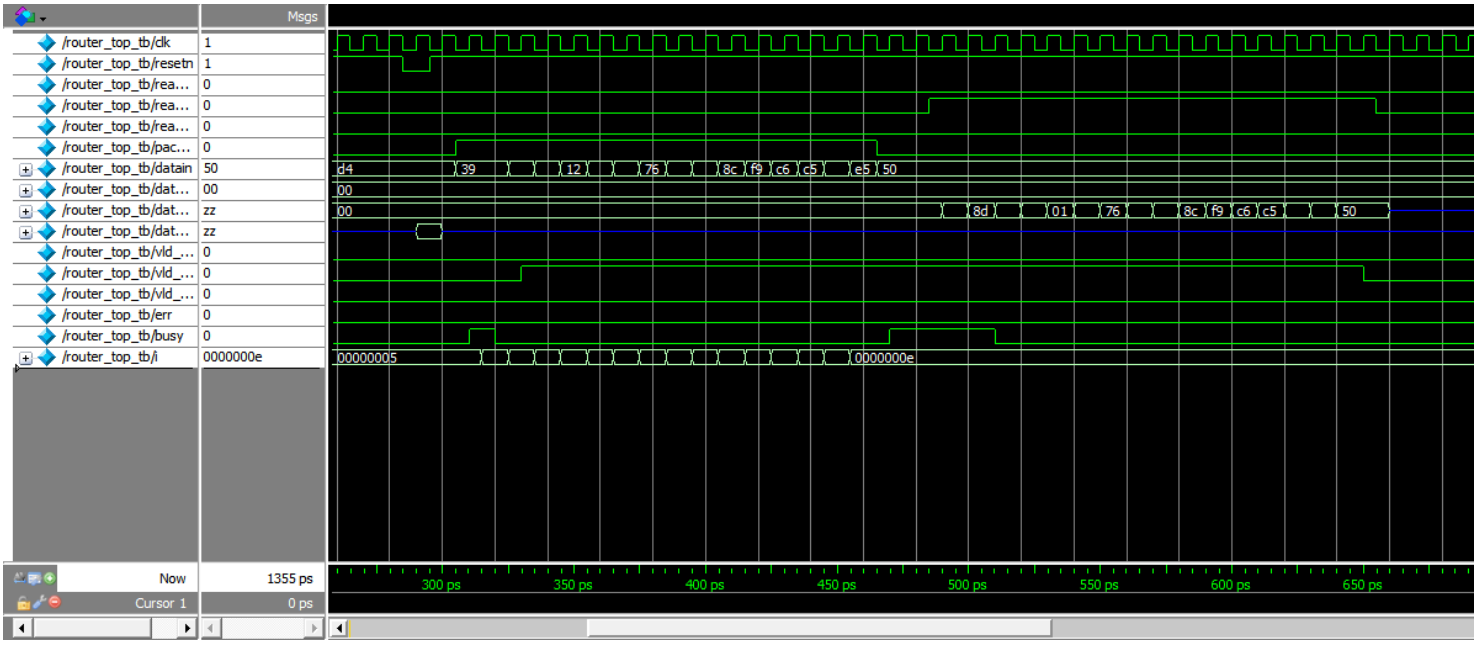
pktm_gen_5;

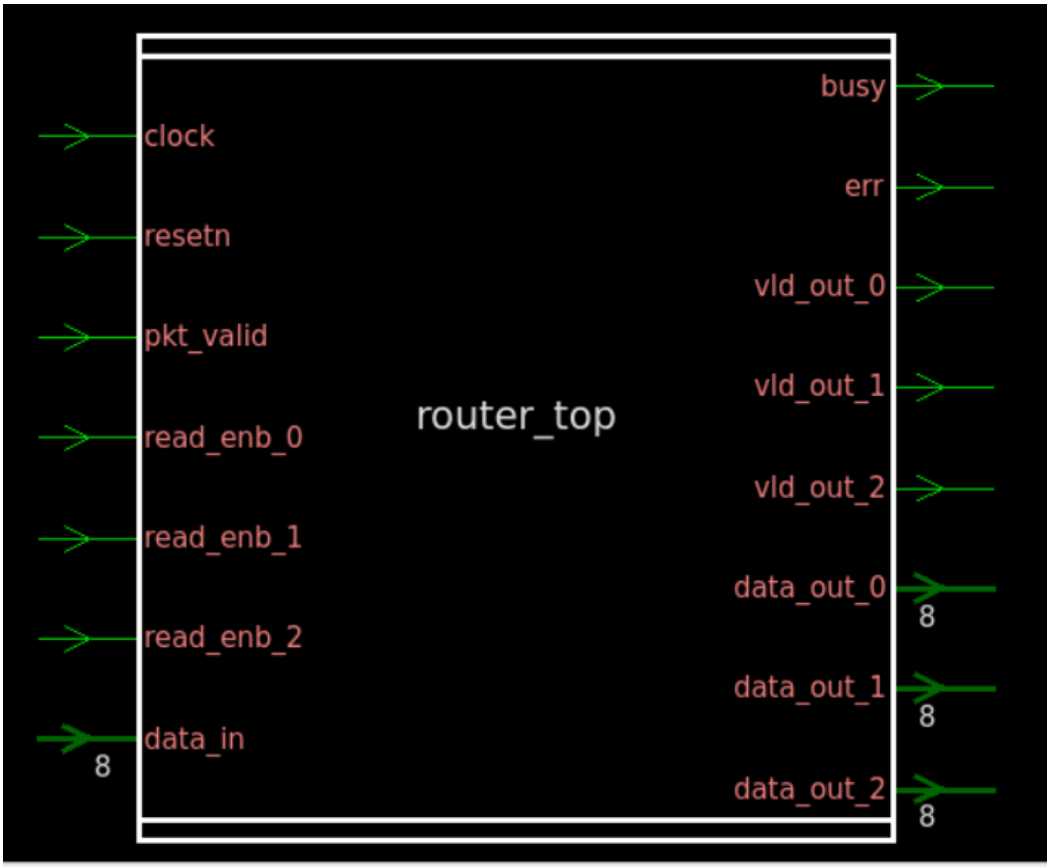


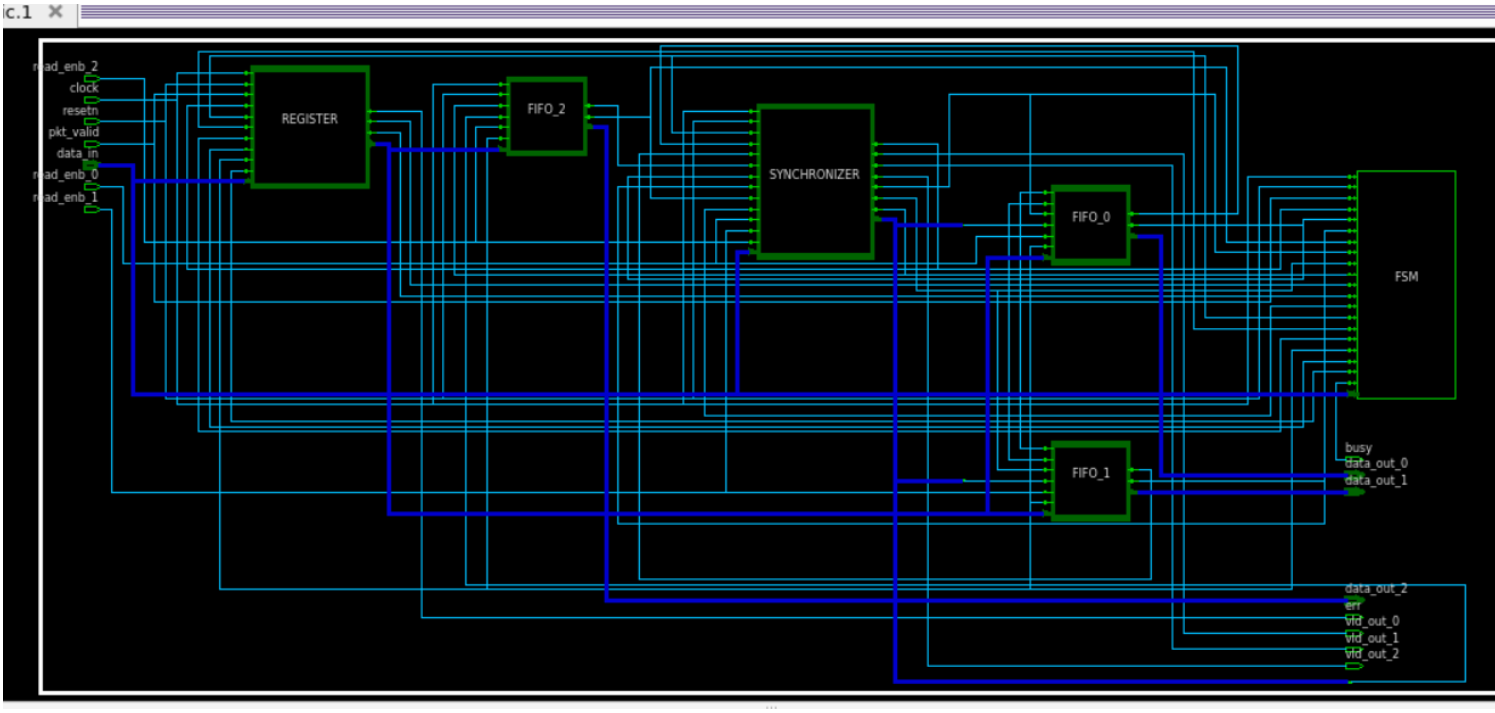
pktm_gen_16;



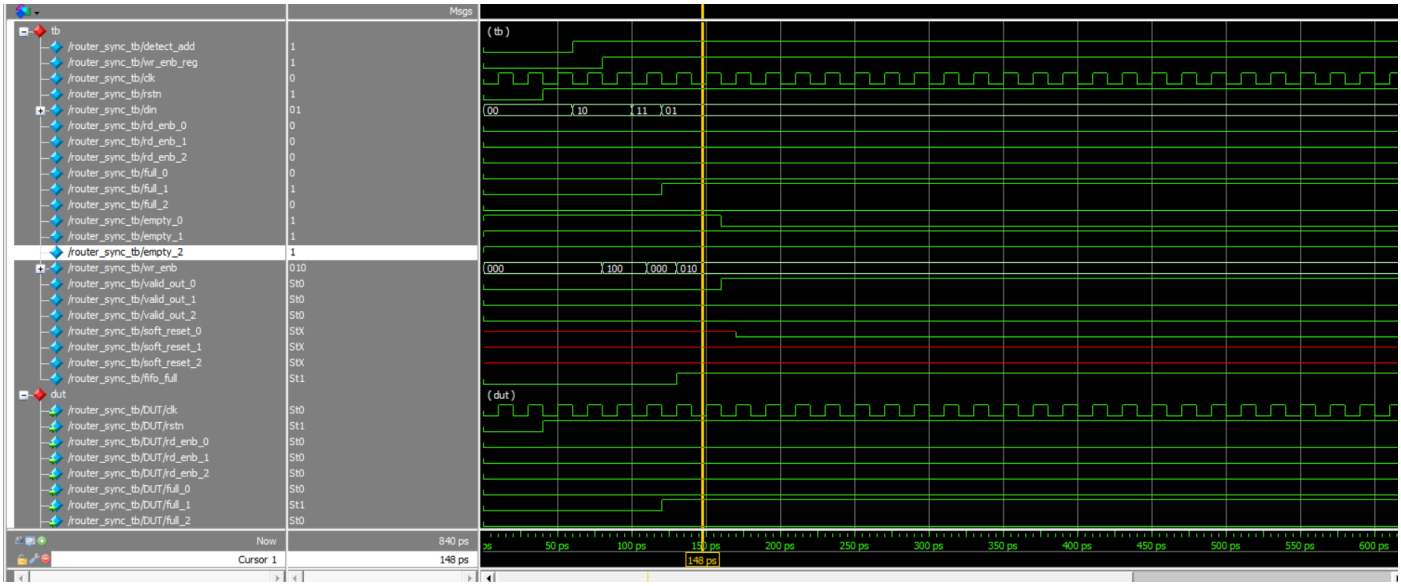
pktm_gen_14;

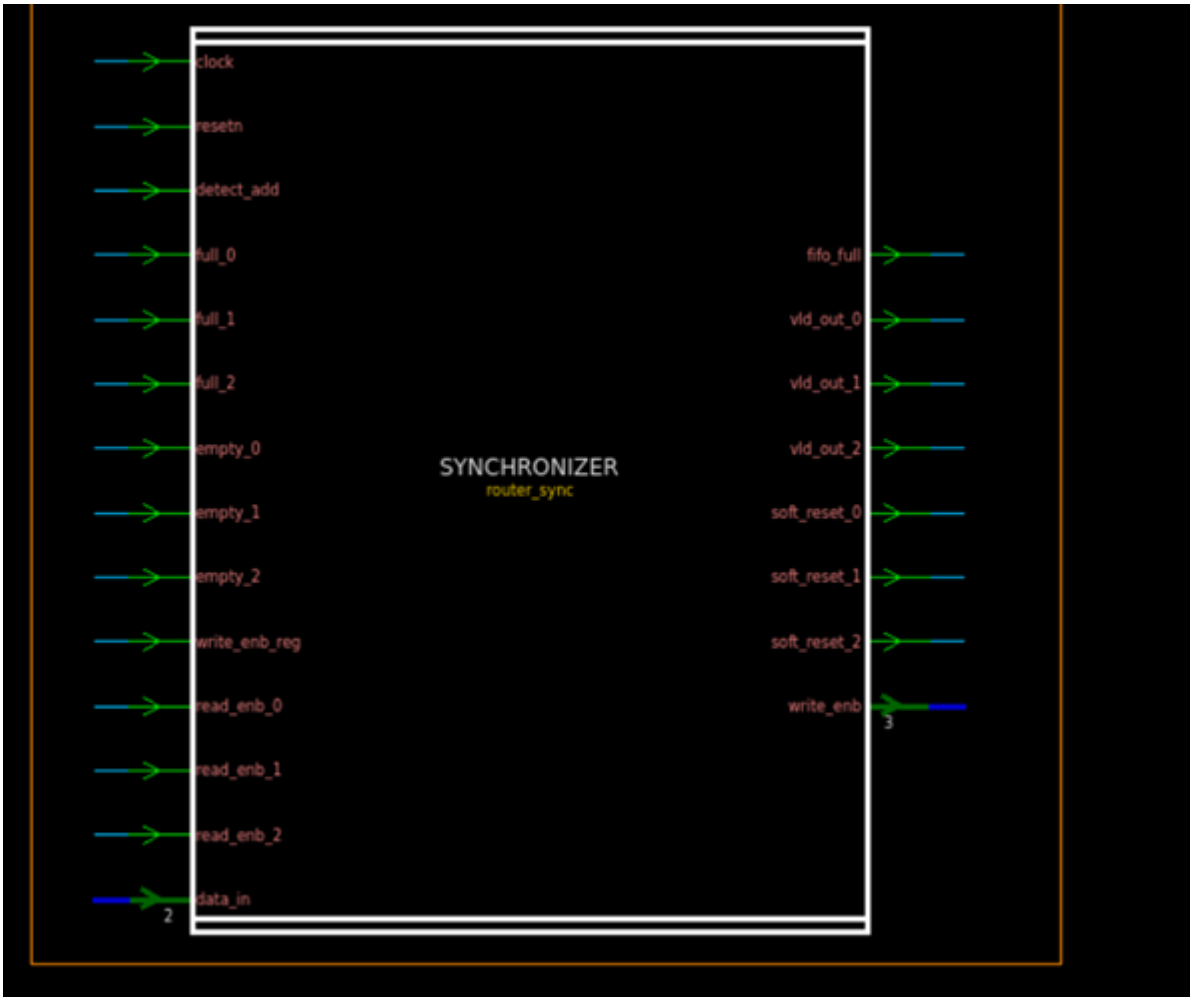

Msgs
/router_top_tb/clk
/router_top_tb/resetn
/router_top_tb/rea...
/router_top_tb/rea...
/router_top_tb/rea...
/router_top_tb/pac...
/router_top_tb/datain
/router_top_tb/dat...
/router_top_tb/dat...
/router_top_tb/dat...
/router_top_tb/vld_...
/router_top_tb/vld_...
/router_top_tb/vld_...
/router_top_tb/err
/router_top_tb/busy
/router_top_tb/i
1
1
0
0
0
0
50
00
zz
zz
0
0
0
0
0
0000000e
d4
39
12
76
8c
f9
c6
c5
e5
50
00
00
8d
01
76
8c
f9
c6
c5
50
00000005
0000000e
Now
1355 ps
Cursor 1
0 ps
300 ps
350 ps
400 ps
450 ps
500 ps
550 ps
600 ps
650 ps

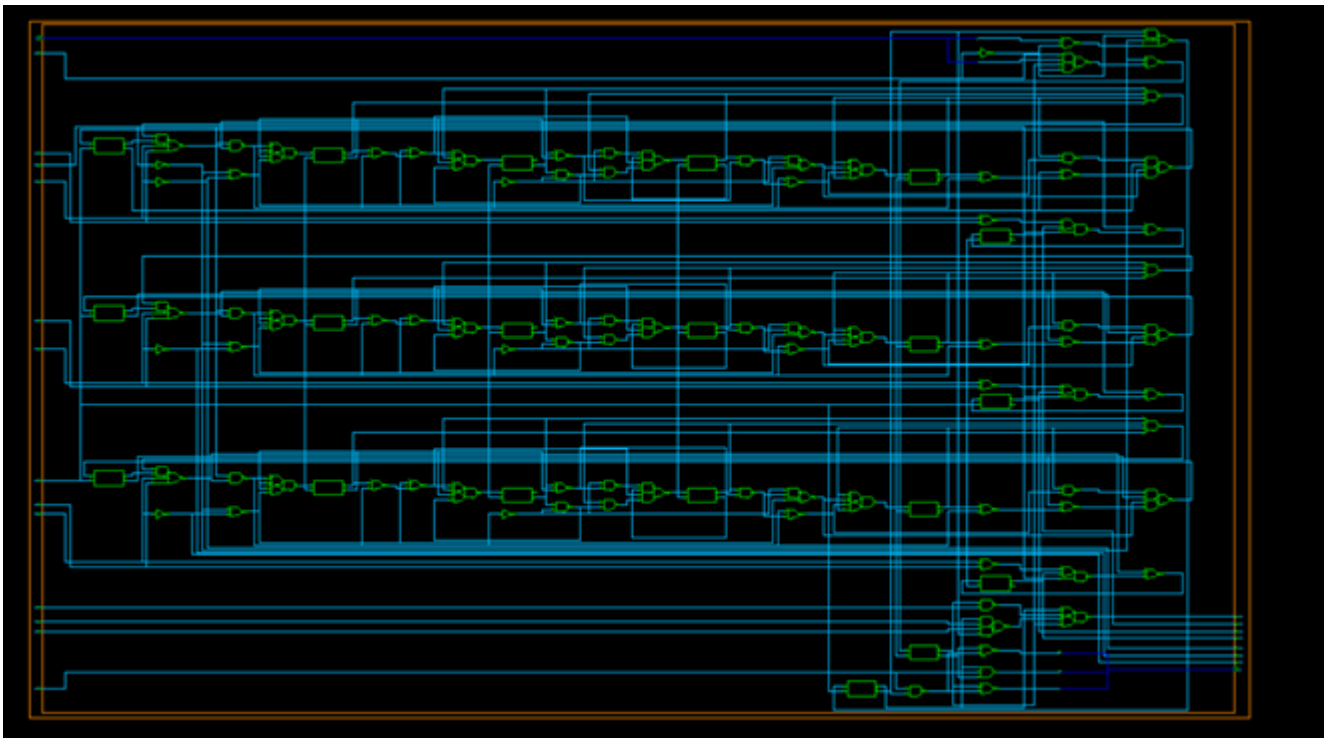

clock
resetn
pkt_valid
read_enb_0
read_enb_1
read_enb_2
data_in
8
router_top
busy
err
vld_out_0
vld_out_1
vld_out_2
data_out_0
8
data_out_1
8
data_out_2
8



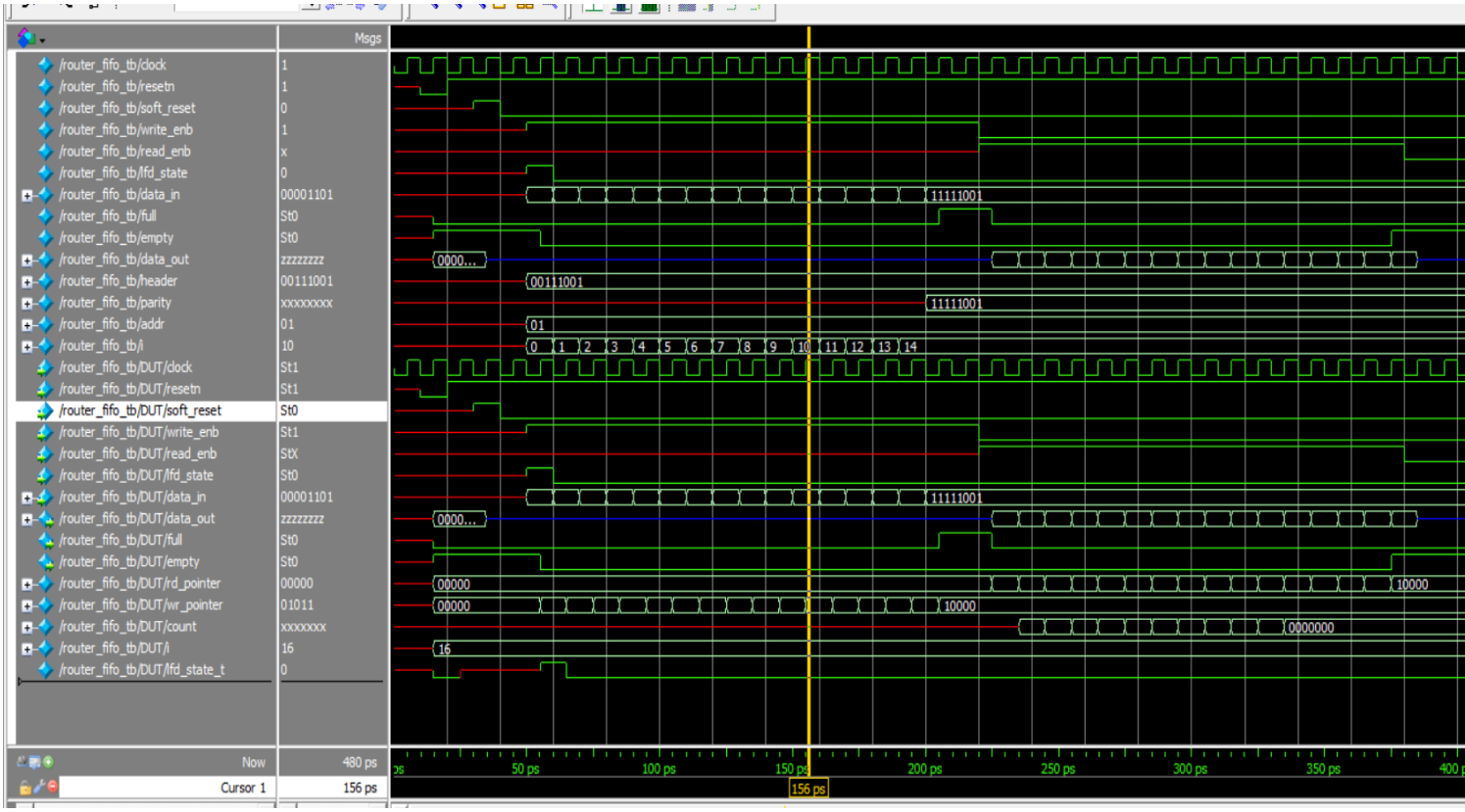
2)Synchroniser module

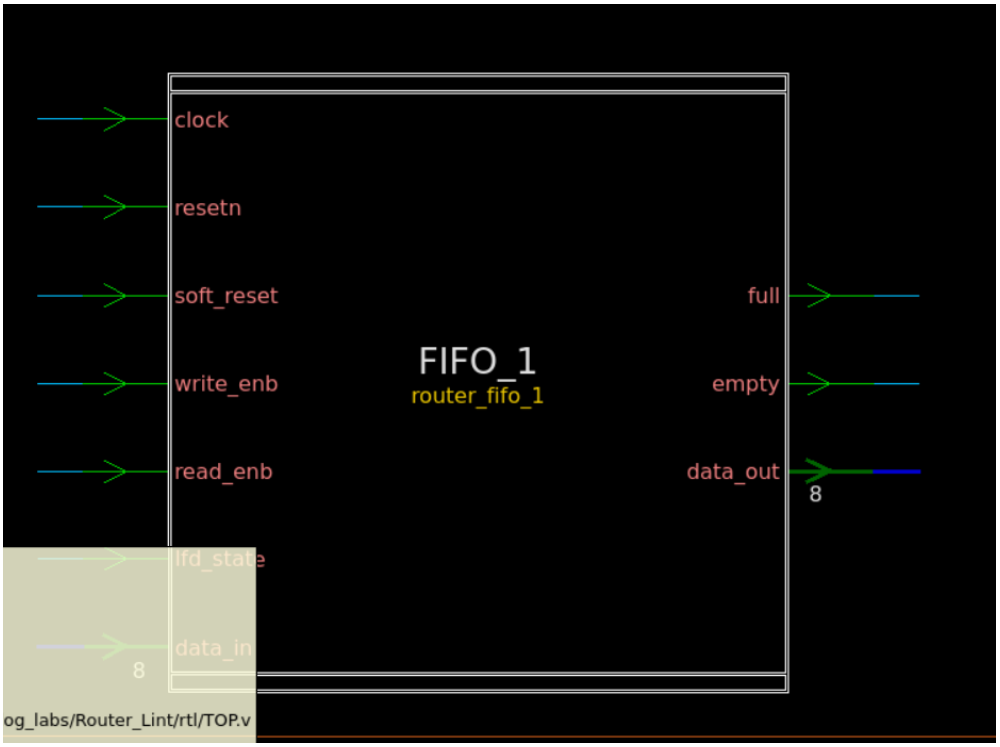


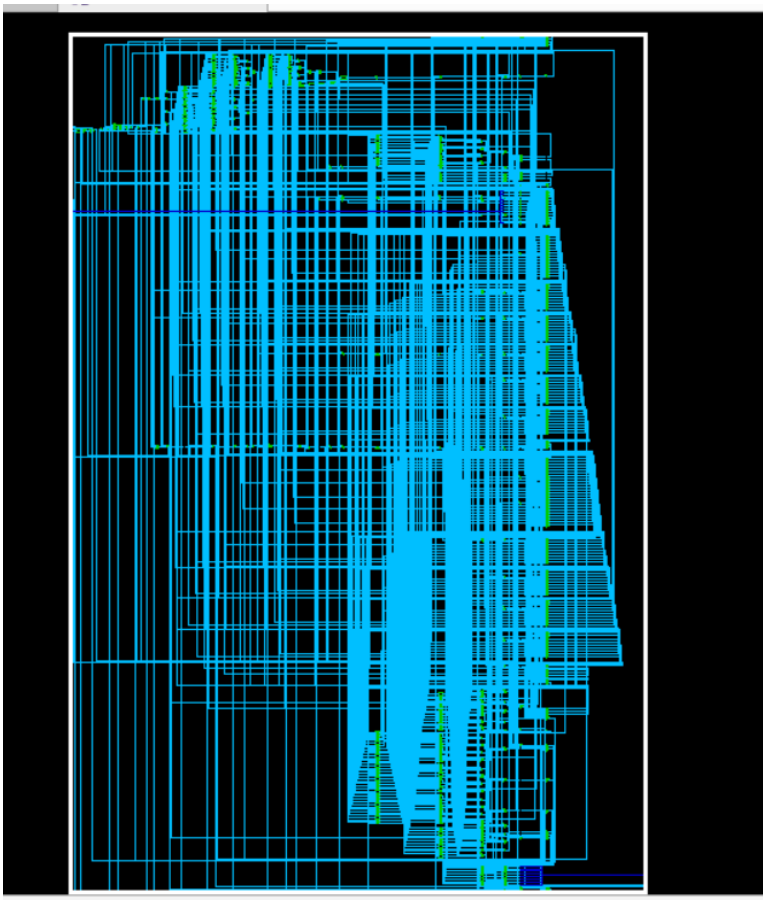




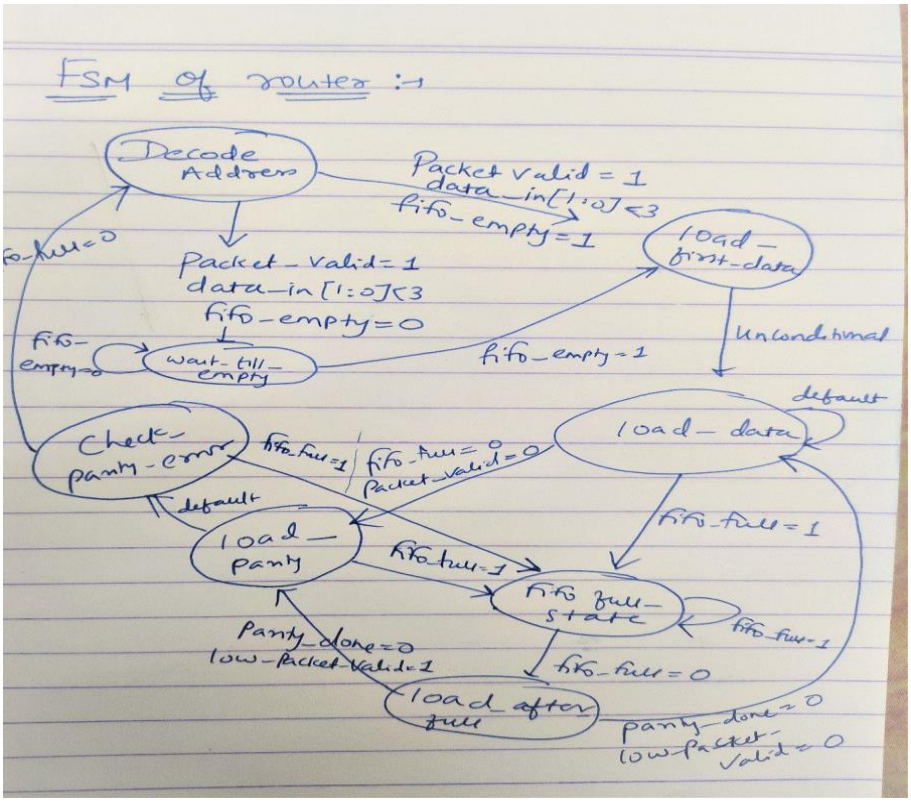
3)fifo module


Msgs
/router_fifo_tb/clock
/router_fifo_tb/resetn
/router_fifo_tb/soft_reset
/router_fifo_tb/write_enb
/router_fifo_tb/read_enb
/router_fifo_tb/lfd_state
/router_fifo_tb/data_in
/router_fifo_tb/full
/router_fifo_tb/empty
/router_fifo_tb/data_out
/router_fifo_tb/header
/router_fifo_tb/parity
/router_fifo_tb/addr
/router_fifo_tb/i
/router_fifo_tb/DUT/clock
/router_fifo_tb/DUT/resetn
/router_fifo_tb/DUT/soft_reset
/router_fifo_tb/DUT/write_enb
/router_fifo_tb/DUT/read_enb
/router_fifo_tb/DUT/lfd_state
/router_fifo_tb/DUT/data_in
/router_fifo_tb/DUT/data_out
/router_fifo_tb/DUT/full
/router_fifo_tb/DUT/empty
/router_fifo_tb/DUT/rd_pointer
/router_fifo_tb/DUT/wr_pointer
/router_fifo_tb/DUT/count
/router_fifo_tb/DUT/i
/router_fifo_tb/DUT/lfd_state_t
Now
Cursor 1
156 ps

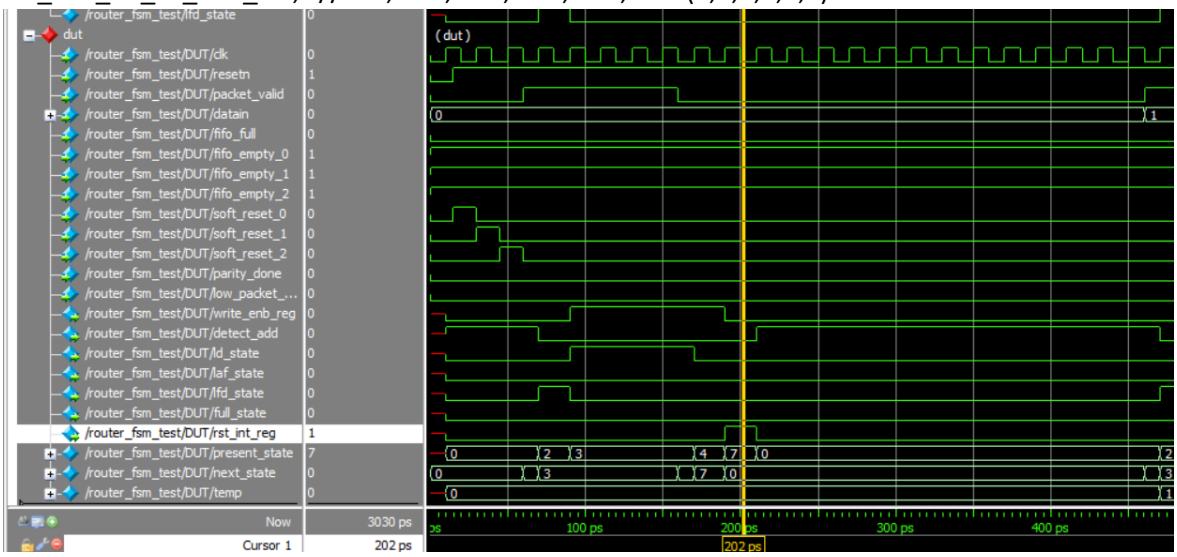

clock
resetn
soft_reset
write_enb
read_enb
lfd_state
data_in
8
FIFO_1
router_fifo_1
full
empty
data_out
8
og_labs/Router_Lint/rtl/TOP.v



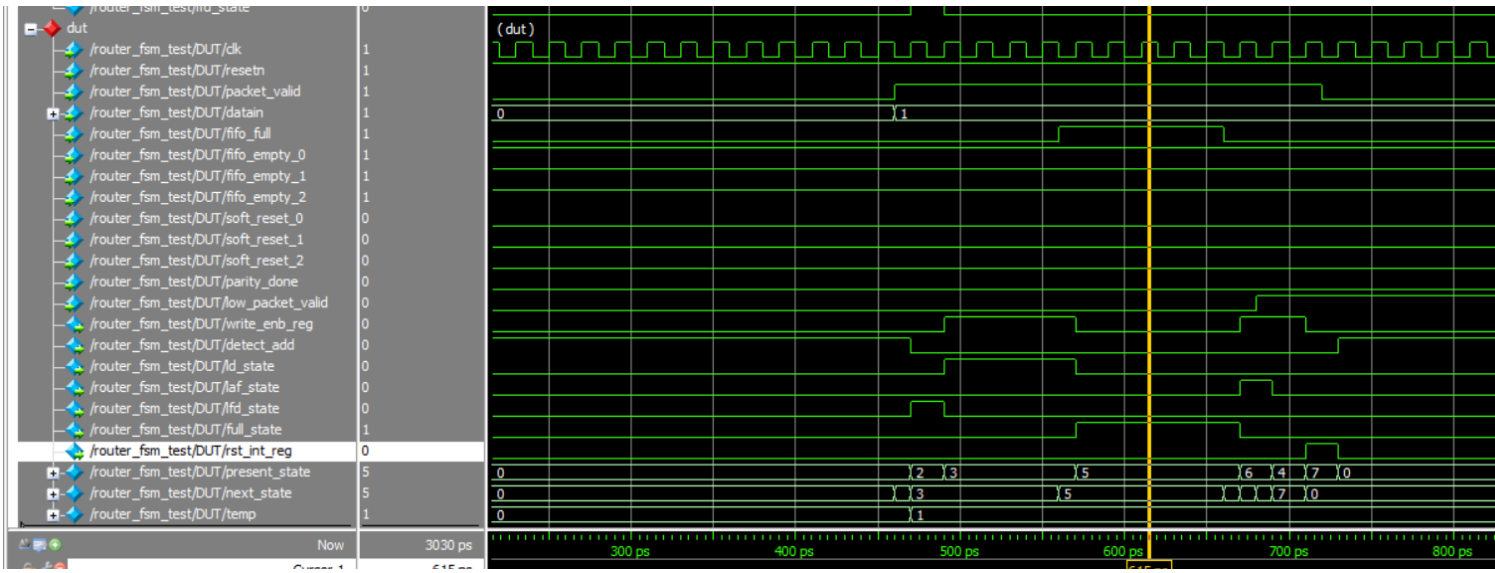
4)FSM module



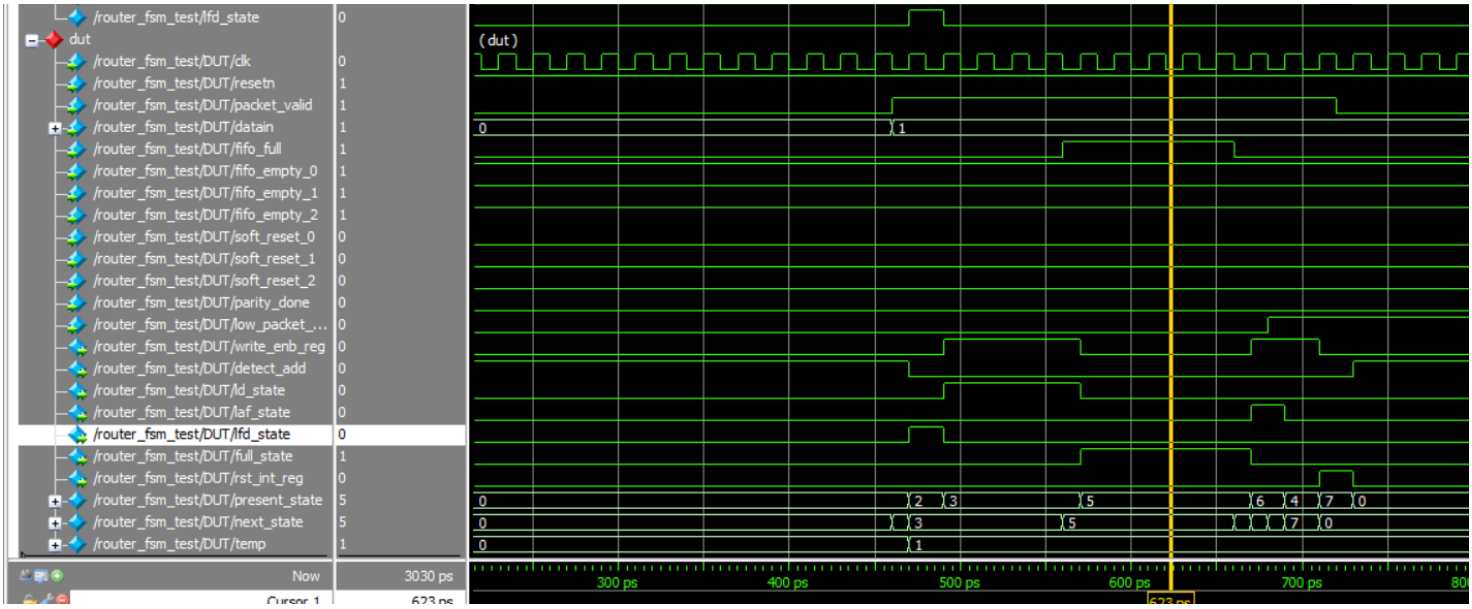
DA_LFD_LD_LP_CPE_DA; //000, 010, 011, 100, 111, 000 (0,2,3,4,7,0)



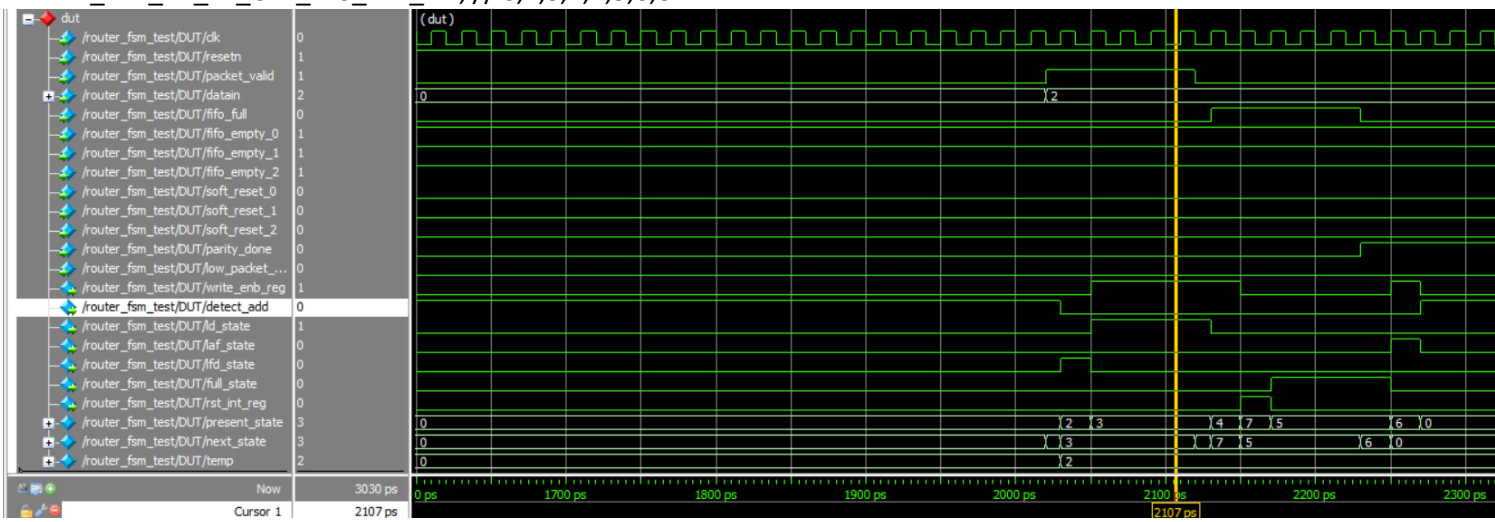
DA_LFD_LD_FES_LP_CPE_DA(); // 000, 010, 011, 101, 100, 111, 000(0,2,3,5,6,4,7,0)

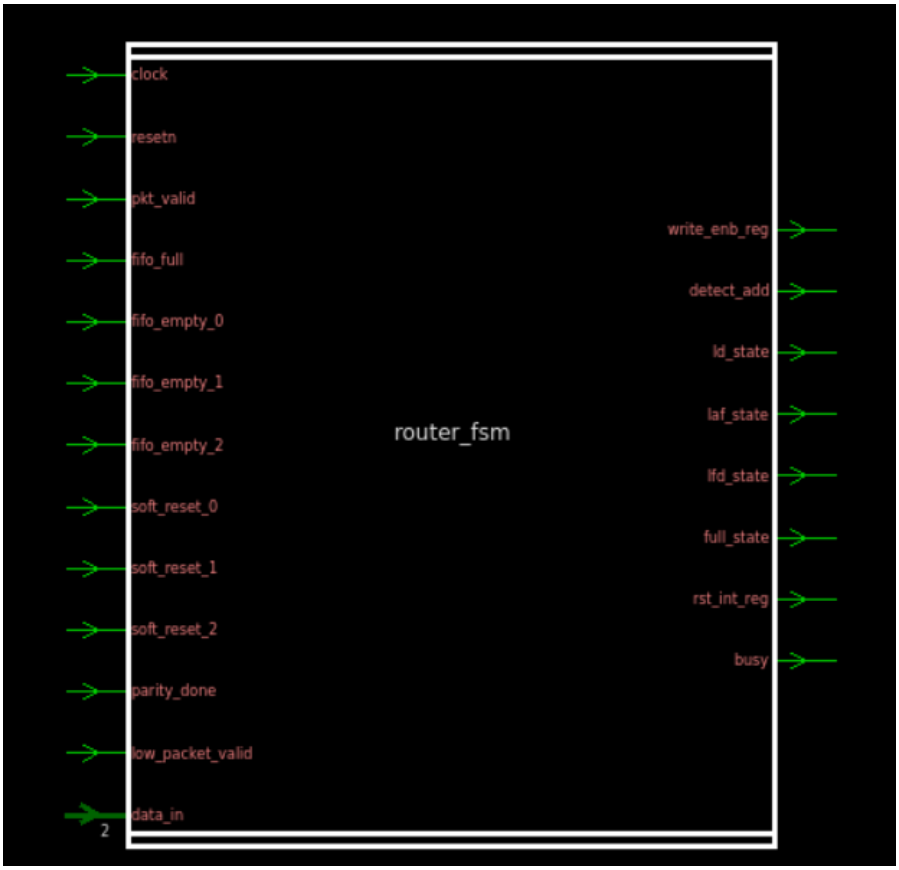


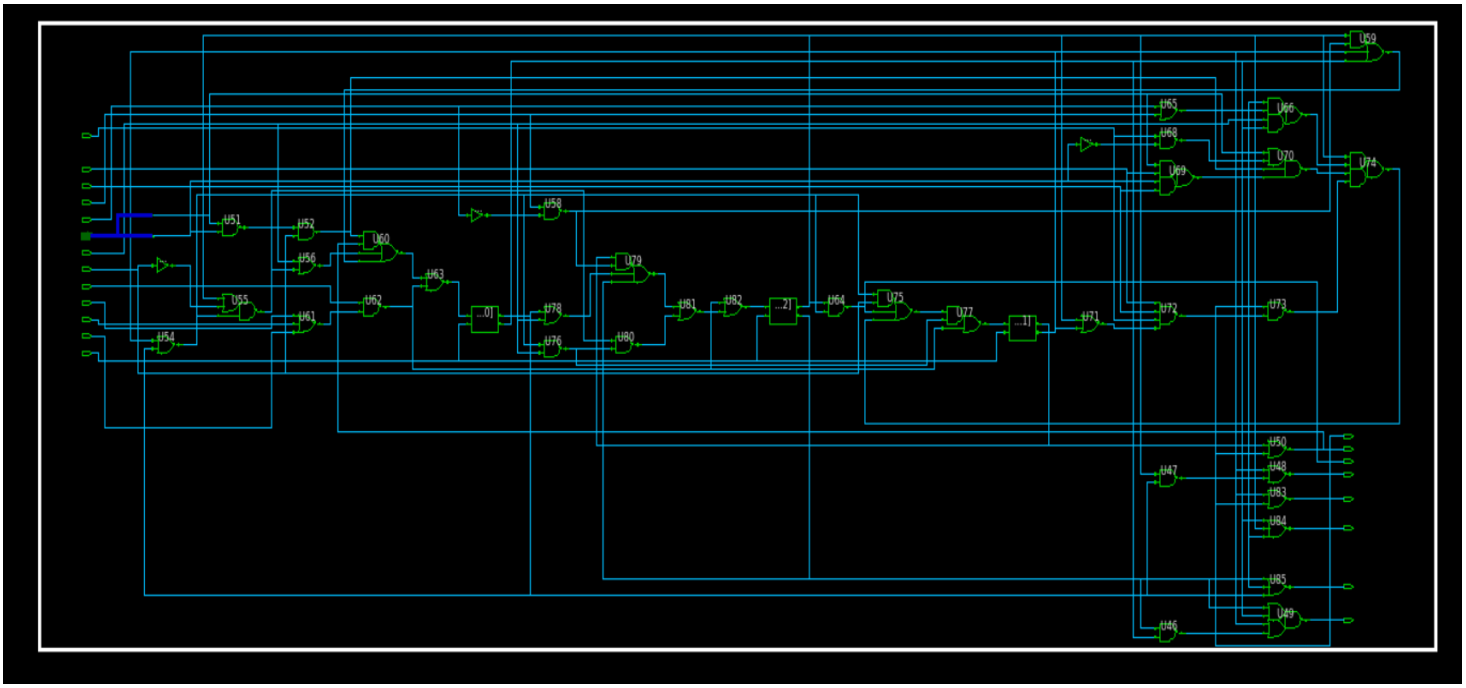
DA_LFD_LD_FES_LAF_LD_LP_CPE_DA; // 0,2,3,5,6,3,4,7,0



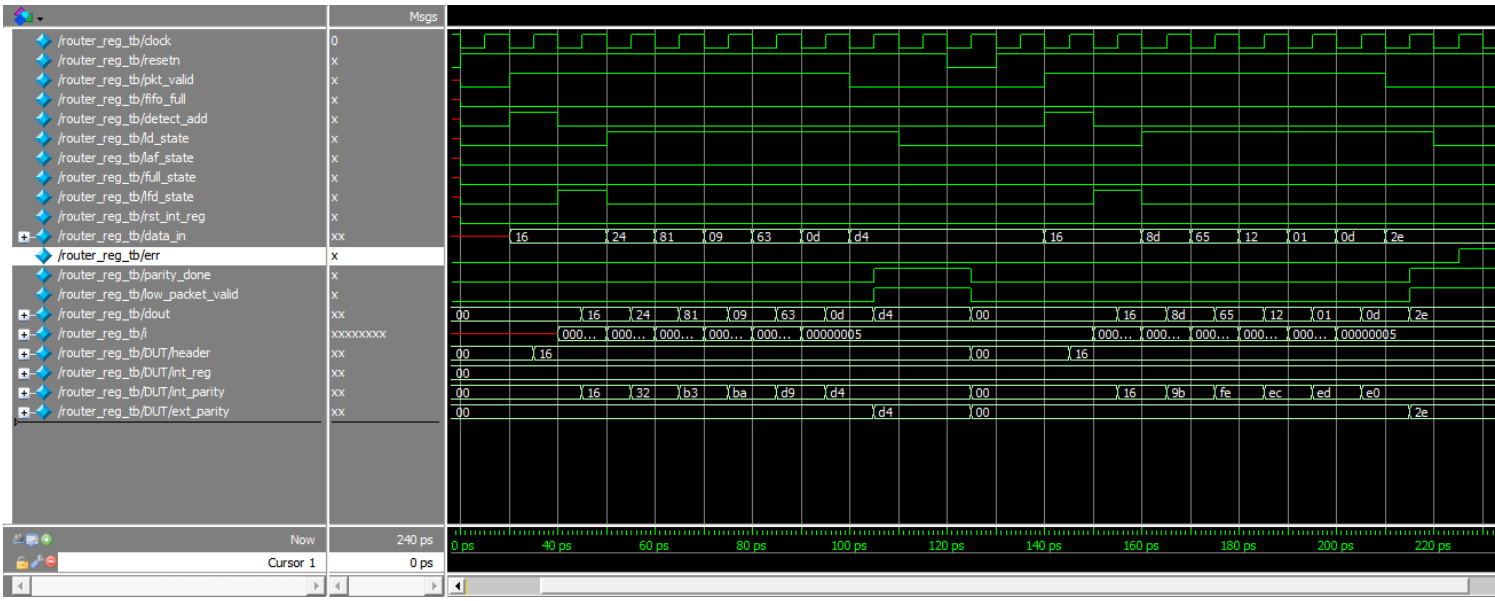
DA_LFD_LD_LP_CPE_FES_LAF_DA; // 0,2,3,4,7,5,6,0

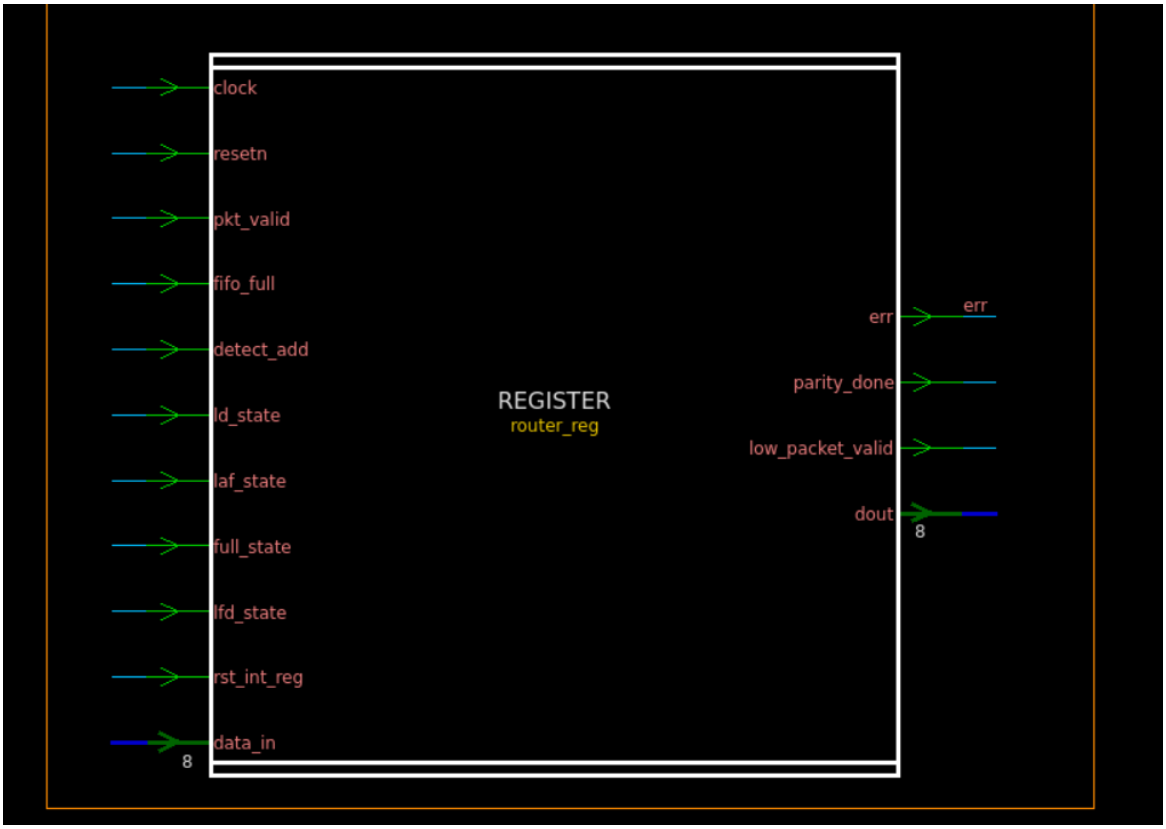


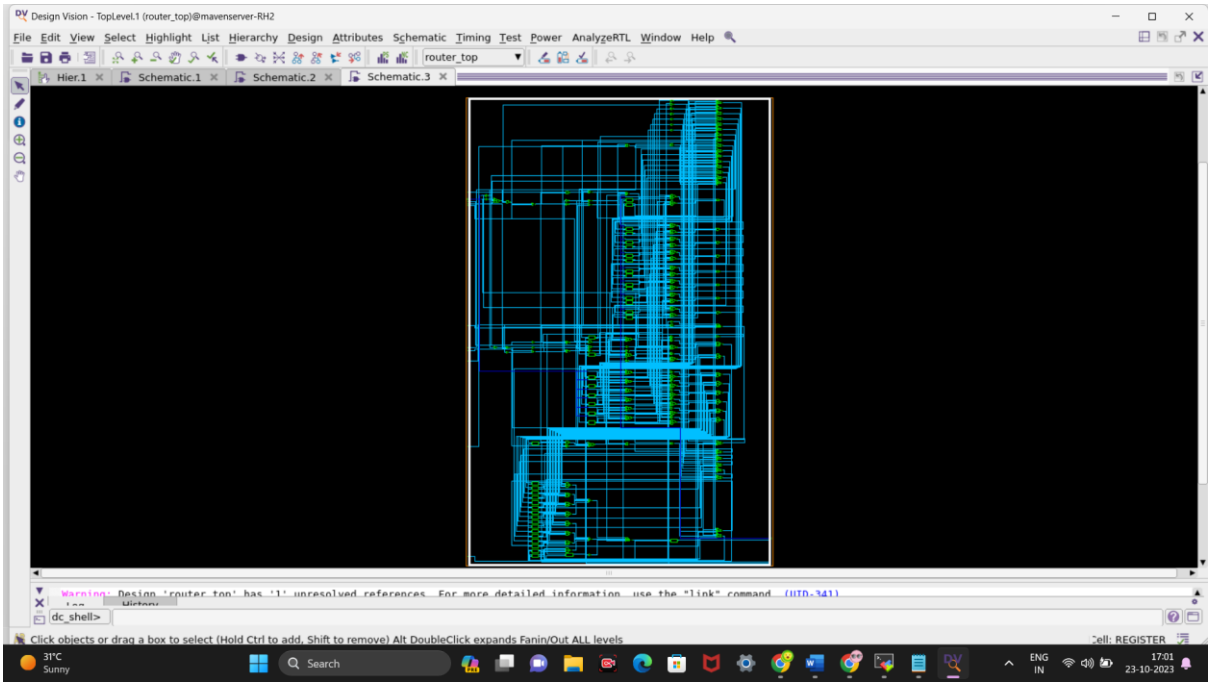

clock
resetn
pkt_valid
fifo_full
fifo_empty_0
fifo_empty_1
fifo_empty_2
soft_reset_0
soft_reset_1
soft_reset_2
parity_done
low_packet_valid
data_in
2
router_fsm
write_enb_reg
detect_add
ld_state
laf_state
lfd_state
full_state
rst_int_reg
busy



5) register module






Design Vision - TopLevel.1 (router_top)@mavenserver-RH2
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
router_top
Hier.1
Schematic.1
Schematic.2
Schematic.3
Warning: Design 'router_top' has '1' unresolved references. For more detailed information, use the "link" command. (UID-341)
dc_shell>
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
31°C
Sunny
Search
ENG
IN
17:01
23-10-2023