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Manual # 08

Required equipments:

Wires
Logic gates IC's
Bread Board
Digital experimental board
Electricity

Objective

How to make different types of encoder and decoders using different logic gates circuits

Types of Decoder

There are two types of decoders

Type 1:

2 to 4 line decoder

Type 2:

3 to 8 line decoder

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Performed experiments

Decoders

Types of decoders

Encoders

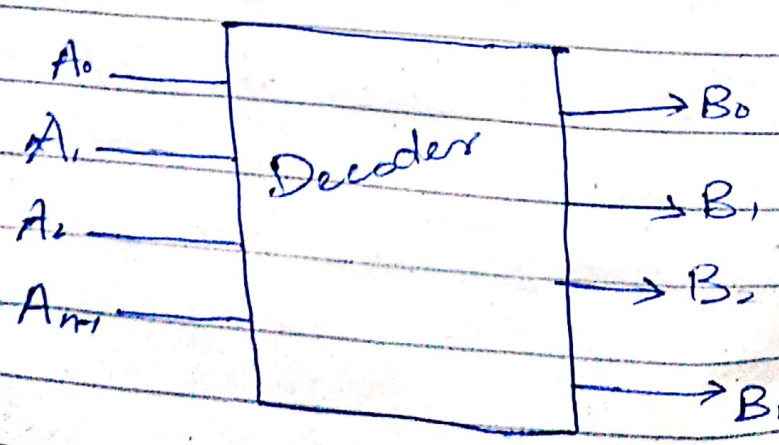
Types of Encoders

Used softwares

Logic.ly

Decoder

Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. A decoder accepts a set of inputs that represents a binary number and activates only that output corresponding to input numbers. All other remain inactive. It's operation is exactly reverse as that of the encoder



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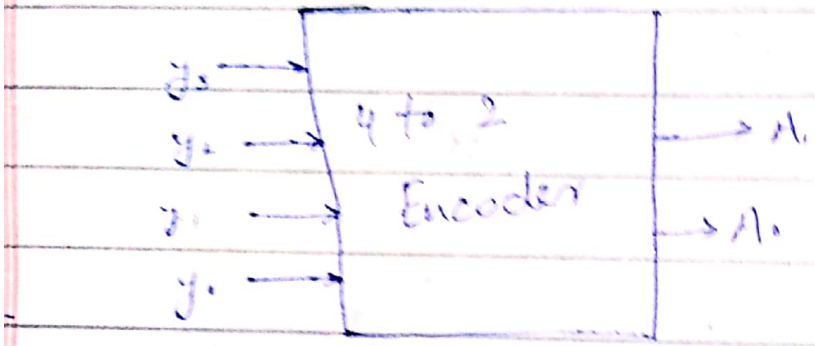
Encoder

An encoder is a combination circuit that converts binary information in the form of 2^n input lines into N output lines, which represent N bit code for the input

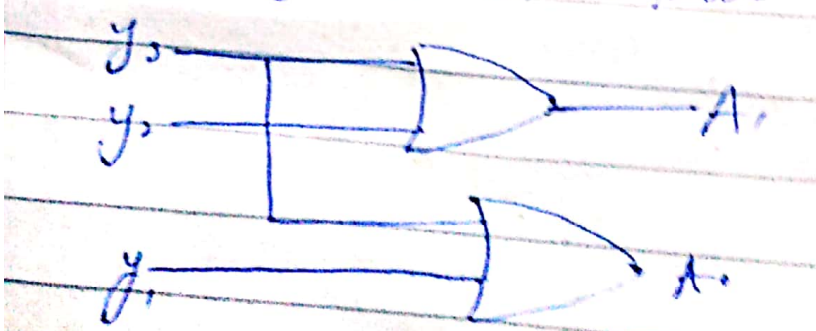


4X2 encoder truth table

Inputs				Outputs	
y_3	y_2	y_1	y_0	A_1	A_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

4X2 Encoder Diagram

By using two OR Gates



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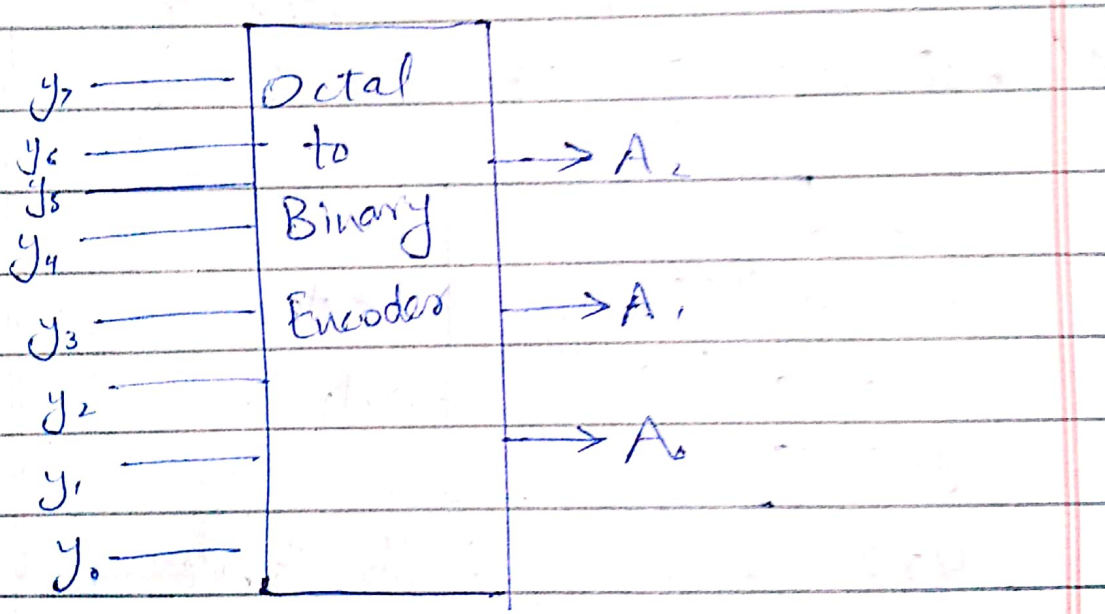
Octal to Binary Encoder

Octal to Binary Encoder has 8 inputs y_7 to y_0 and three output A_2, A_1, A_0



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Parity encode

y_3	y_2	y_1	y_0	A_1	A_0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	0	1	1	0	1	1
0	1	0	0	1	0	1
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	0	1
1	0	0	0	1	1	1
1	0	0	1	1	1	1
1	0	1	0	1	1	1
1	0	1	1	1	1	1
1	1	0	0	1	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

Priority Encode

If Two or more input lines are high at the same time. Then input with high priority be considered have 4 inputs y_0, y_1, y_2, y_3 & 2 outputs A_1 & A_0

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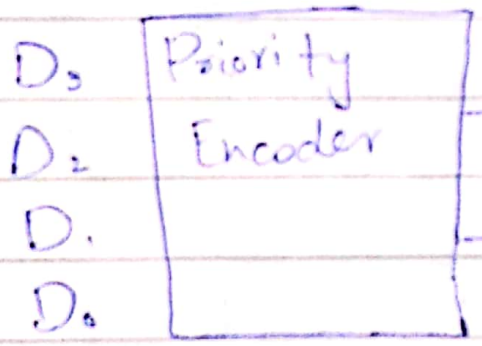
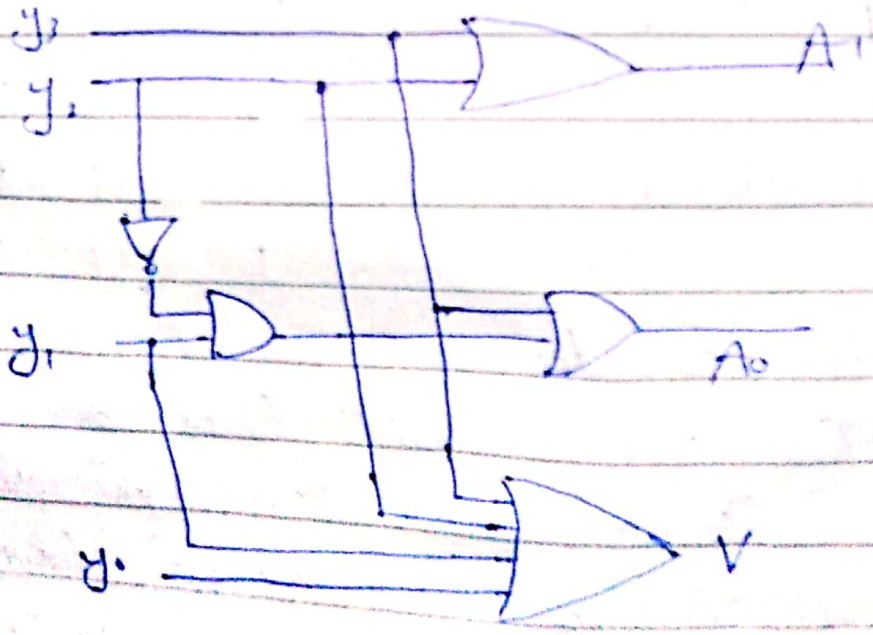
Inputs				Outputs		
y_3	y_2	y_1	y_0	A_1	A_0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Diagram of priority encoder



Priority Encoder Diagram



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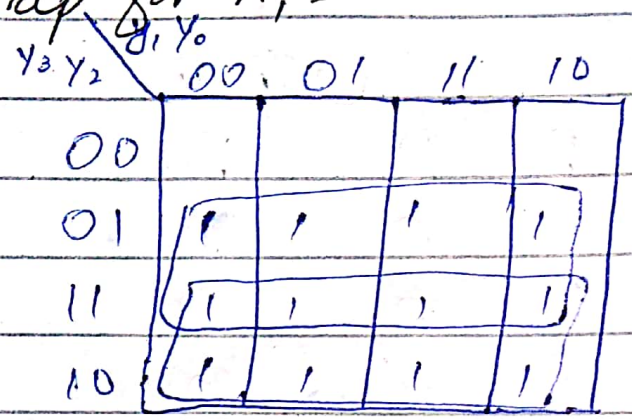
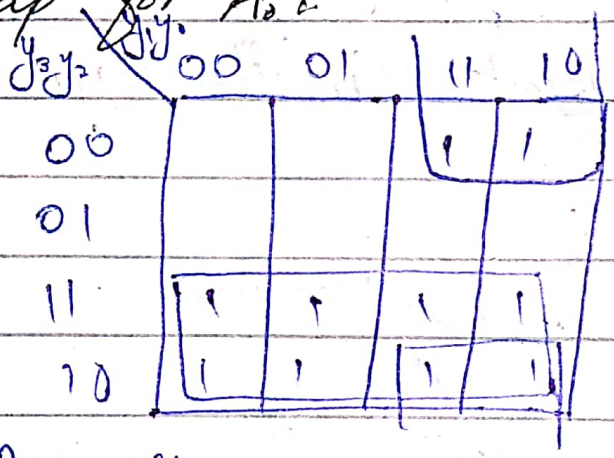
K-map for A_1 :



K-Map for A_0 :



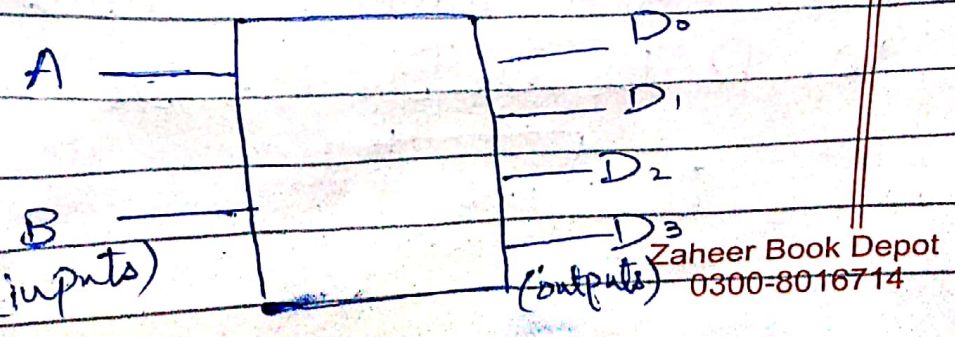
$A_1 = y_3 + y_2$

$A_0 = y_3 + y_2' y_1$

$V = y_3 + y_2 + y_1 + y_0$

2-4 Decoder

2 to 4 decoder has 2 inputs A_1 & A_2 and (4) four outputs y_3, y_2, y_1, y_0



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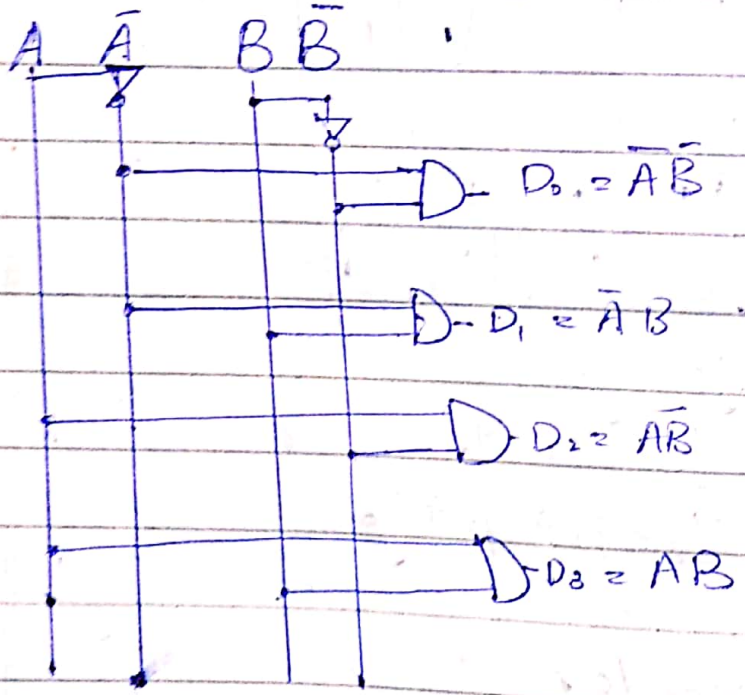
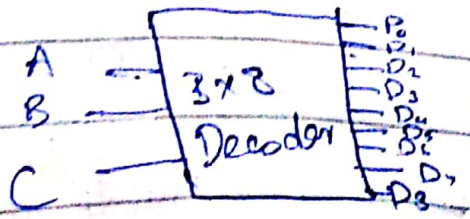
inputs		Outputs			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

2 to 4 Decoder circuit diagram



3 to 8 line Decoder

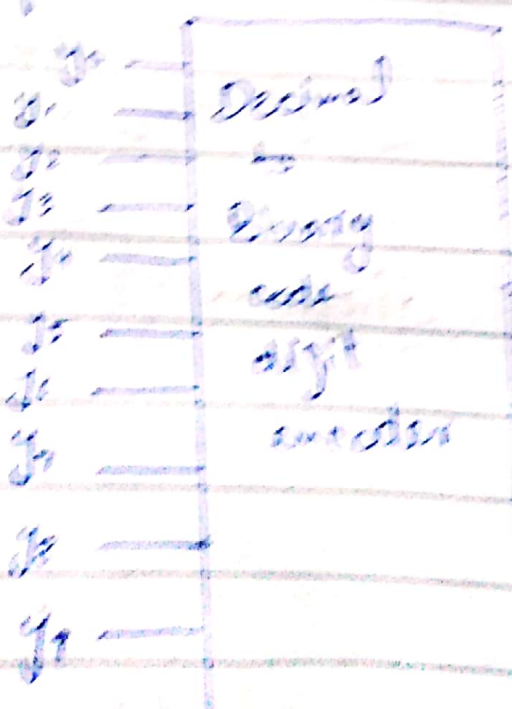
3 to 8 Decoder has 3 input A, B & C and total combination are $2^3 = 8$ and have 8 outputs $D_0, D_1, D_2, D_3, D_4, D_5, D_6, D_7$



Inputs			Outputs								
A	B	C	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	0	0	1	0	0	0	0	0	0	0	$D_0 = \bar{A}\bar{B}\bar{C}$
0	0	1	0	1	0	0	0	0	0	0	$D_1 = \bar{A}\bar{B}C$
0	1	0	0	0	1	0	0	0	0	0	$D_2 = \bar{A}B\bar{C}$
0	1	1	0	0	0	1	0	0	0	0	$D_3 = \bar{A}BC$
1	0	0	0	0	0	0	1	0	0	0	$D_4 = A\bar{B}\bar{C}$
1	0	1	0	0	0	0	0	1	0	0	$D_5 = A\bar{B}C$
1	1	0	0	0	0	0	0	0	1	0	$D_6 = AB\bar{C}$
1	1	1	0	0	0	0	0	0	0	1	$D_7 = ABC$

Decimal to BCD encoder

Decimal to binary code digit decoder encoder has 10 inputs and 4 outputs



Boolean expression for table

A $A = y_8 + y_9$

B $B = y_4 + y_5 + y_6 + y_7$

C $C = y_2 + y_3 + y_6 + y_7$

D $D = y_1 + y_3 + y_5 + y_7 + y_9$

Inputs										BCD Output			
y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7	y_8	y_9	A	B	C	D
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

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Conclusion:

We learnt in today lab how to design encoder and decoder and dg thier applications.