Advanced AI Driven Solution for IC Layout Deformation Prediction and Correction in Semiconductor Fabrication

Abstract

In the fabrication of integrated circuits (ICs), lithography plays a crucial role in transferring circuit layouts onto silicon wafers. However, during this process, shape deformations often occur due to diffraction, causing deviations from the intended design that can lead to performance degradation, increased power consumption, or even functional failure. To address these challenges, optical proximity correction (OPC) has traditionally been employed to adjust the mask design and minimize these distortions. While OPC has been effective, it faces scalability limitations as IC designs become more complex.

Recent advances have introduced machine learning methods, such as convolutional neural networks (CNNs) and deep neural networks (DNNs), to enhance lithographic deformation prediction and correction with greater accuracy and efficiency. However, even these methods encounter challenges related to precision, scalability, and runtime in modern IC manufacturing.

In our project, we propose solutions that build upon these advancements by leveraging state-of-the-art machine learning techniques, such as Vision Transformers (ViTs), Generative Adversarial Networks (GANs), and diffusion models. These techniques offer superior IC layout deformation prediction and correction, improving upon the performance of traditional OPC as well as CNN and DNN-based approaches. By integrating these advanced machine learning models, we aim to tackle the growing complexity of modern IC designs, enhancing accuracy, scalability, and efficiency in the semiconductor manufacturing process.

Our proposed AI-driven solutions demonstrate the potential for significant improvements in prediction accuracy, computational efficiency, and adaptability over CNN-based methods. While experimental evaluations are yet to be conducted, these solutions aim to reduce fabrication-induced defects and provide scalable, adaptable approaches for various fabrication scenarios. The research highlights promising AI-based strategies to address IC fabrication challenges, ultimately driving higher reliability and lower costs in semiconductor manufacturing.

1 Introduction

Integrated circuits (ICs) form the backbone of modern electronics, powering devices ranging from smartphones to advanced computing systems. As IC designs become more intricate, the manufacturing process faces increasing challenges, particularly in maintaining the accuracy of the fabricated layout. Deviations in the final IC product from the intended design, caused by various factors during photolithography and other processing steps, can significantly impact device performance. These shape deformations can lead to several issues, including:

- Increased power consumption
- Timing errors
- Functional failures
- Reduced yield and higher production costs

Photolithography remains the predominant technique used in IC fabrication, where a photomask is employed to project the circuit design onto a silicon wafer. However, due to optical proximity effects, mask errors, diffraction, and process variations, the final IC pattern often deviates from the original design. Although methods like Optical Proximity Correction (OPC) are utilized to reduce these deviations, they are often inadequate for highly complex or miniaturized designs.

Machine learning techniques, particularly Convolutional Neural Networks (CNNs), have been explored to predict and correct these deformations by learning from historical data, such as SEM images

and their corresponding layout designs. While CNNs offer some promise, they suffer from limitations in handling complex geometries, long training times, and high computational demands, making them difficult to scale effectively.

In this context, we propose several AI-driven solutions that can potentially address these challenges. Our proposed approaches leverage advanced machine learning techniques to improve the prediction, correction, and optimization of IC layouts. The key proposed methods include:

- **ViLitho (Vision Transformer-based IC Deformation Prediction):** A solution that utilizes Vision Transformers (ViTs) to predict deformations by analyzing SEM images and IC layout pairs. ViTs capture both local and global patterns using self-attention mechanisms, potentially offering improved accuracy in handling complex geometries compared to traditional CNN approaches.
- **GenLitho (Generative Adversarial Networks for Deformation Generation):** This method proposes using GANs to simulate fabrication-induced deformations by generating realistic variations of IC layouts, providing insights into how defects manifest under different fabrication conditions.
- **ViOPC (Vision Transformer-based Optical Proximity Correction):** A proposed approach applying ViT-driven techniques to optimize photomask designs. This method aims to correct predicted deformations, ensuring a closer match between the fabricated IC and its original design.
- **Diffusion Lithography Model:** A diffusion model-based solution for iteratively refining IC layout predictions. This approach would learn how deformations evolve at different stages of fabrication and apply corrections accordingly.
- **Hybrid Transformer-GAN Model:** A hybrid model combining the capabilities of GANs and Vision Transformers, proposed to provide end-to-end deformation prediction and correction with faster convergence and improved accuracy.

Our proposed AI-driven solutions demonstrate the potential for significant improvements in prediction accuracy, computational efficiency, and adaptability over CNN-based methods. While experimental evaluations are yet to be conducted, these solutions aim to reduce fabrication-induced defects and provide scalable, adaptable approaches for various fabrication scenarios. The research highlights promising AI-based strategies to address IC fabrication challenges, ultimately driving higher reliability and lower costs in semiconductor manufacturing.

The following sections of this proposal will provide further details on the architecture, methodology, and potential advantages of each of these proposed components, emphasizing how these solutions can help tackle the challenges associated with modern IC fabrication.

2 Problem Statement

During integrated circuit (IC) fabrication, shape deformations often deviate from the original layout, leading to performance degradation, increased power consumption, and potential functional failure. These distortions arise during key manufacturing stages, such as photolithography and etching. While Optical Proximity Correction (OPC) techniques have traditionally been employed to mitigate these issues, they face challenges related to scalability and high computational costs. Furthermore, existing machine learning approaches, including Convolutional Neural Networks (CNNs) and Deep Neural Networks (DNNs), encounter limitations in accurately modeling complex geometries in increasingly intricate IC designs.

To address these challenges, we propose AI-driven solutions that leverage advanced machine learning techniques, including Vision Transformers (ViTs), Generative Adversarial Networks (GANs), and diffusion models. These approaches aim to enhance the accuracy, scalability, and efficiency of IC layout deformation prediction and correction, offering improved performance over both traditional OPC and existing CNN/DNN-based methods.

Figure 1: Metal Layer Distorted Mask image Sample

3 Objectives

- **Propose Advanced AI Solutions:** Present various advanced AI methods, including Vision Transformers (ViTs), Generative Adversarial Networks (GANs), and diffusion models, as potential tools to predict and correct IC layout deformations during semiconductor fabrication.
- **Enhance Prediction Accuracy:** Propose the use of ViTs to accurately capture both local and global features from SEM images and layout design pairs, with the goal of improving the accuracy of deformation predictions.
- **Simulate Fabrication-Induced Deformations:** Explore the use of GANs to simulate realistic deformations caused by the fabrication process, aiming to provide better predictive insights into the impact of fabrication on design integrity.
- **Optimize Photomask Designs:** Propose the development of a Vision Transformer-based Optical Proximity Correction (ViOPC) method to refine photomask designs based on predicted deformations, ensuring a closer match between the fabricated IC and its intended design.
- **Iterative Learning through Diffusion Models:** Suggest the application of diffusion models to iteratively predict and correct IC layout deformations, improving understanding of how distortions evolve at various stages of the fabrication process.
- **Evaluate Proposed Methods Across Various Scenarios:** Evaluate the performance of the proposed AI-driven techniques across different fabrication scenarios, comparing their effectiveness against traditional CNN-based methods in terms of accuracy, efficiency, and adaptability.
- **Facilitate Real-World Applicability:** Ensure that the proposed AI techniques are versatile, scalable, and adaptable to the evolving demands of the semiconductor industry, with the goal of enhancing production yield, lowering costs, and improving design precision.

4 Proposed Methodology

4.1 Data Acquisition

Acquire high-quality datasets consisting of pairs of original IC layout designs and corresponding deformed layouts obtained from Scanning Electron Microscope (SEM) images during post-fabrication analysis. The datasets should represent various deformation types, materials, and manufacturing conditions to ensure a wide coverage of real-world fabrication scenarios.

4.2 Data Preprocessing

- **Normalization:** Standardize the IC layout and SEM data to ensure consistency in input scaling across the dataset.
- **Augmentation:** Apply data augmentation techniques to introduce additional deformation patterns, enhancing model robustness by increasing the diversity of the training data.
- **Segmentation:** Automatically segment the IC layouts into smaller regions, allowing the model to capture both local and global deformation details during the prediction process.

4.3 ViLitho: Vision Transformer-based IC Deformation Prediction

ViLitho utilizes Vision Transformers (ViTs) to predict IC deformations, effectively capturing both local and global layout features.

- **Self-Attention Mechanism:** The ViT model uses multi-head self-attention to analyze relationships between different layout regions, capturing intricate spatial dependencies.
- **Input Representation:** Convert IC layout and SEM images into suitable input tensors, employing positional encoding to preserve spatial information.
- **Training Process:** The model will be trained using a combination of supervised learning techniques with loss functions such as Mean Squared Error (MSE) or Structural Similarity Index (SSIM) to quantify prediction accuracy.
- **Output:** The refined IC layout generated by ViLitho will closely resemble the predicted deformations for each layout section.

4.4 GenLitho: GAN-based Deformation Simulation

GenLitho employs Generative Adversarial Networks (GANs) to simulate realistic deformations based on the predictions from ViLitho.

- **Generator Network:** Trains to create synthetic deformation patterns, simulating the impact of fabrication process variations on the IC layout.
- **Discriminator Network:** Evaluates the authenticity of generated deformations, providing feedback to improve the generator's output.
- **Adversarial Training:** The generator and discriminator undergo adversarial training, with the generator progressively improving its ability to simulate realistic deformations.
- **Output:** GenLitho produces a dataset of simulated deformations, augmenting the training data for ViLitho and enhancing the model's ability to generalize across different deformation types.

4.5 ViOPC: Vision Transformer-based Optical Proximity Correction

ViOPC refines photomask designs by leveraging Vision Transformers to optimize the layout based on predicted deformations.

- **Data Integration:** Inputs the original IC design and predicted deformations, optimizing mask patterns to ensure a more accurate final layout.
- **Correction Algorithms:** Integrate advanced correction algorithms, including inverse lithography, to adjust the photomask based on the predicted deformations.
- **Output:** ViOPC outputs an optimized photomask design that compensates for fabrication-induced deformations, ensuring higher fidelity in the produced IC layout.

4.6 Diffusion Lithography Model

Diffusion Model operates iteratively to refine predictions by learning deformation evolution at different fabrication stages.

- **Noising and Denoising:** The model applies noise to input layouts and learns to denoise them, simulating the effects of various manufacturing stages.
- **Stage-wise Training:** Train the model on data from various stages of the fabrication process, learning how deformations progress as the manufacturing advances.
- **Output:** The output includes refined IC layouts that represent the layout states at different fabrication stages, offering deeper insights into deformation correction.

4.7 Hybrid Transformer-GAN Model

Hybrid Model combines the strengths of Vision Transformers and GANs for an integrated, end-to-end solution for IC layout deformation prediction and correction.

- **Architecture:** Leverage a Vision Transformer backbone to extract geometric features, coupled with a GAN framework to generate and refine realistic deformations.
- **Training Regimen:** Use a combined loss function that measures both prediction accuracy and deformation realism, facilitating faster convergence and improved results.
- **Output:** The hybrid model generates corrected IC layouts, effectively incorporating both predicted deformations and realistic fabrication variability.

4.8 Evaluation Metrics

To assess the performance of the proposed AI-driven methodology, the following metrics will be employed:

- Mean Absolute Error (MAE) and Mean Squared Error (MSE) for quantitative evaluation of prediction accuracy.
- Structural Similarity Index (SSIM) and Peak Signal-to-Noise Ratio (PSNR) to evaluate the visual fidelity of predicted layouts against actual deformed layouts.
- Execution Time to measure the computational efficiency of each model.
- Fabrication Yield to assess the practical effectiveness of the correction techniques in a real-world IC fabrication context.

4.9 Implementation Plan

The project will follow a phased implementation strategy:

- **Phase 1: Data Collection and Preprocessing** – Gather and prepare the dataset for training and validation.
- **Phase 2: Model Development** – Design and implement the ViLitho, GenLitho, ViOPC, Diffusion Lithography, and Hybrid Transformer-GAN models.
- **Phase 3: Model Training and Optimization** – Train models on the prepared dataset, tuning hyperparameters to optimize performance.
- **Phase 4: Performance Evaluation** – Evaluate the models using the defined metrics and compare their effectiveness against traditional methods.
- **Phase 5: Documentation and Reporting** – Compile results, performance insights, and comparative analyses for dissemination.

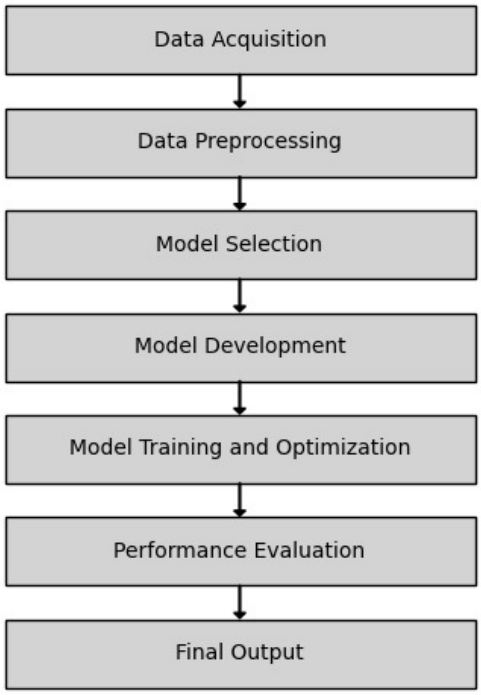

Figure 2: Block Diagram

5 Collaborative Technical Work

To ensure fair and balanced participation, all team members will be actively involved in the core technical components of the project, gaining experience in key technical areas. The following tasks will be undertaken collaboratively:

5.1 Data Acquisition and Preprocessing

Tasks:

- All members will work together on data cleaning and preprocessing. Each member will be assigned different parts of the dataset, such as one member focusing on handling SEM image data, another on layout design files, and the third on data augmentation.
- Collaborate to ensure consistent normalization, data alignment, and feature engineering.
- Share responsibility for writing scripts for data loading, cleaning, and preprocessing tasks.

Skills Gained: Data handling, cleaning, and preprocessing using Python libraries such as `Pandas`, `NumPy`, and `OpenCV`.

5.2 Model Development and Training

Tasks:

- Each team member will participate in model development, with specific models assigned for research and implementation. One member will focus on Vision Transformers (ViTs), another on Generative Adversarial Networks (GANs), and the third on Optical Proximity Correction using ViTs or CNNs.
- Team members will take turns developing, testing, and optimizing models to ensure the effectiveness of the overall framework.

- The team will jointly optimize and fine-tune models by sharing insights and results from experimentation.

Skills Gained: Deep learning with frameworks such as `TensorFlow` or `PyTorch`, model training, hyperparameter tuning, and optimization.

5.3 Model Evaluation and Results Analysis

Tasks:

- All members will collaborate on evaluating the models using key performance metrics such as Mean Absolute Percentage Error (MAPE), precision, recall, and detailed error analysis. To distribute the workload, the testing datasets will be divided.
- Each member will focus on analyzing and comparing the performance of different models (e.g., ViT vs. GAN) to identify strengths and weaknesses.
- Insights will be shared, and findings consolidated to produce a comprehensive analysis for the final report.

Skills Gained: Proficiency in model evaluation techniques, error analysis, and comparative performance analysis.

5.4 Integration and Testing

Tasks:

- We will collaborate on integrating various models into a unified AI framework. Each member will take on specific tasks, such as one focusing on integrating data preprocessing with model selection, another on model training, and the third on performance evaluation and output generation.
- We will work together to test and debug the entire framework to ensure smooth end-to-end model deployment.

Skills Gained: Full-stack AI pipeline integration, debugging techniques, and hands-on experience in end-to-end model deployment.

6 Non-Technical Work (Distributed Individually)

In addition to technical work, each team member will also take responsibility for specific non-technical tasks:

6.1 Student 1: Project Management and Coordination

Responsibilities:

- Oversee scheduling and coordination of team meetings.
- Track project milestones and ensure adherence to deadlines.
- Document project progress and provide regular updates to the team.

Skills Gained: Project management, communication, and time management.

6.2 Student 2: Literature Review and Report Writing

Responsibilities:

- Lead the writing of the literature review section, gathering and synthesizing relevant research on traditional and AI-based approaches to IC layout deformation prediction.
- Compile technical documentation for the methodology and results.

Skills Gained: Research, technical writing, and documentation skills.

6.3 Student 3: Presentation and Documentation

Responsibilities:

- Develop the final presentation, including diagrams, charts, and summaries of project outcomes.
- Organize and maintain documentation, ensuring it is easily accessible during project reviews and presentations.

Skills Gained: Presentation development, document organization, and attention to detail.

7 Project Timeline

The project is structured into five phases, spanning a total of 12 months. The detailed timeline is as follows:

7.1 Phase 1: Data Collection and Preprocessing (Months 1-2)

- Gather IC layout datasets from various semiconductor fabrication sources.
- Conduct data preprocessing activities, including normalization, augmentation, and segmentation to enhance dataset quality.

7.2 Phase 2: Model Development (Months 3-5)

- Develop the ViLitho model for initial deformation prediction.
- Implement GenLitho for generating realistic deformations using GANs.
- Create the ViOPC model for optical proximity correction.
- Design the diffusion lithography model to facilitate iterative deformation predictions.
- Integrate a hybrid Transformer-GAN model that combines the capabilities of all models for enhanced prediction and correction.

7.3 Phase 3: Model Training and Optimization (Months 6-8)

- Train each model component using the prepared datasets.
- Conduct hyperparameter tuning for each model to optimize performance.
- Fine-tune the hybrid model to effectively integrate the strengths of the individual models.

7.4 Phase 4: Performance Evaluation and Comparative Analysis (Months 9-10)

- Assess the performance of all models using evaluation metrics such as Mean Squared Error (MSE), Structural Similarity Index (SSIM), Peak Signal-to-Noise Ratio (PSNR), and Fabrication Yield.
- Conduct a comparative analysis of the proposed framework against traditional CNN-based approaches to highlight improvements.

7.5 Phase 5: Documentation and Dissemination of Results (Months 11-12)

- Compile comprehensive documentation of the research, detailing the methodology, results, and analysis.
- Disseminate findings through journal publications, technical reports, and conference presentations to reach a wider audience.

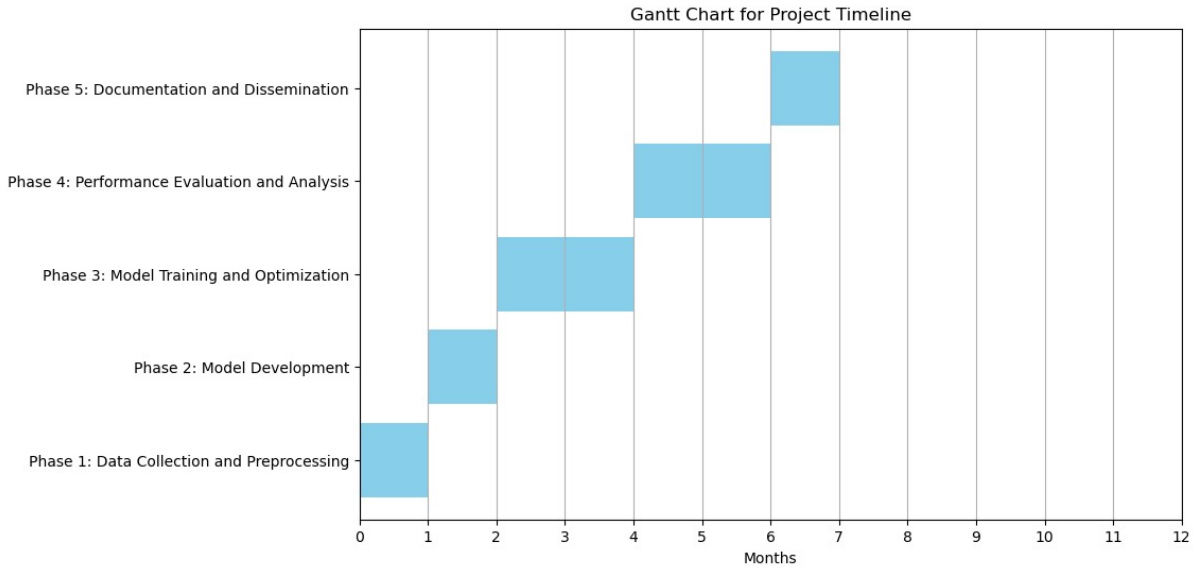

Figure 3: Gantt Chart

8 Flowchart

Figure 1 illustrates the flowchart of the proposed framework, depicting the sequence of the main components from data preprocessing to the final IC layout correction. The flowchart outlines the interconnections and processes involved, facilitating a clear understanding of the framework's operational workflow.

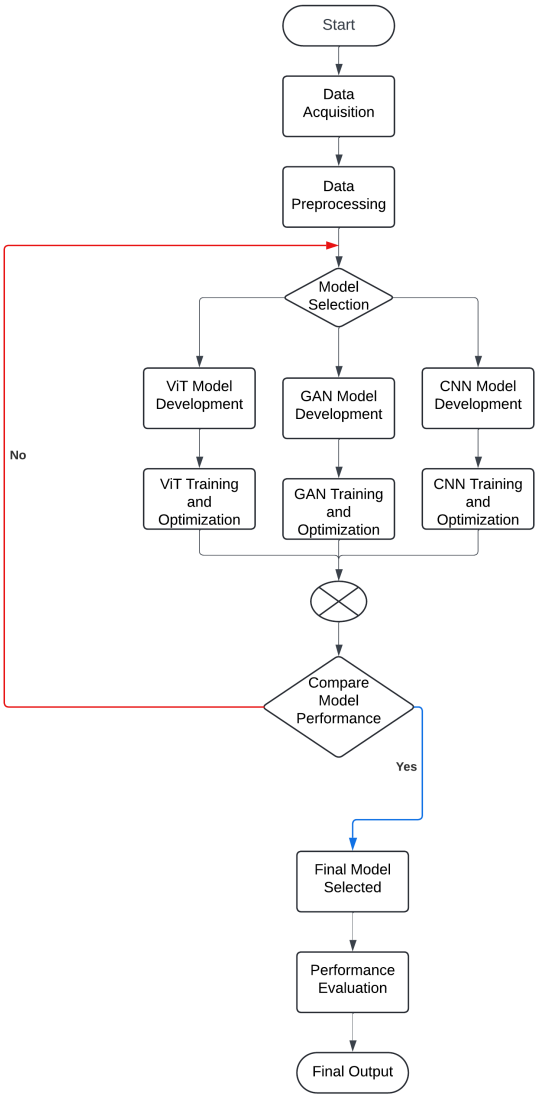

Figure 4: Flow Chart

Sustainable Development Goals Achieved by Our Project

1. **Goal 9: Industry, Innovation, and Infrastructure**
   Description: Our project promotes sustainable industrialization and fosters innovation in semiconductor manufacturing processes. By leveraging advanced technologies like Vision Transformers and GANs, we enhance the efficiency and effectiveness of IC production, contributing to the development of resilient infrastructure.

2. **Goal 12: Responsible Consumption and Production**
   Description: By improving the accuracy and efficiency of IC layout deformation prediction and correction, our project reduces waste and enhances resource utilization in the fabrication process. This aligns with the goal of ensuring sustainable consumption and production patterns.

3. **Goal 7: Affordable and Clean Energy**
   Description: Enhanced IC designs from our project can lead to more energy-efficient devices, contributing to the availability of affordable and clean energy solutions. Improved semiconductor performance can help reduce energy consumption in electronics and other applications.

4. **Goal 11: Sustainable Cities and Communities**
   Description: Advanced IC technologies can support the development of smart city solutions and

sustainable urban environments. Efficient semiconductor devices can lead to smarter infrastructure, improving the quality of life in urban areas.

5. **Goal 13: Climate Action**
   Description: By promoting more efficient semiconductor manufacturing processes and contributing to the development of energy-efficient devices, our project indirectly supports climate action through reduced energy consumption and lower carbon emissions associated with electronic devices.

6. **Goal 4: Quality Education**
   Description: Our project involves research and development that contributes to education and knowledge-sharing in the field of semiconductor technologies and machine learning, fostering skills development in these areas.

7. **Goal 8: Decent Work and Economic Growth**
   Description: By driving innovation and efficiency in the semiconductor industry, our project contributes to economic growth and the creation of quality jobs within the tech sector.

9 Acknowledgements

We extend our sincere gratitude to the semiconductor fabrication facilities for providing access to the IC layout and deformation datasets essential for this research. We also appreciate the support of the research teams and institutions that contributed to the development and success of this project.

10 Conclusion

Our project addresses the significant challenge of IC layout deformations arising from semiconductor fabrication processes. Traditional convolutional neural network (CNN)-based methods for predicting and correcting these deformations have exhibited limitations in both accuracy and scalability. In response, we propose an advanced AI framework that integrates cutting-edge techniques, including Vision Transformers (ViTs), Generative Adversarial Networks (GANs), and Diffusion Models, to enhance prediction accuracy and operational efficiency.

By leveraging the unique strengths of each approach, the proposed solution facilitates precise predictions of IC layout deformations, optimizes photomask designs, and offers robust solutions adaptable to a wide range of fabrication scenarios. Our methodology emphasizes data-driven approaches and hybrid model integration, ensuring that it can scale effectively to meet the demands of increasingly complex IC designs.

The successful implementation of this research will establish a foundation for next-generation AI-driven solutions in the semiconductor industry, promoting consistency and precision in IC manufacturing. Additionally, the project's structured division of tasks, timeline, and flowchart will provide a clear roadmap for systematic progress toward achieving our objectives. Ultimately, this work aims to mitigate the adverse effects of fabrication deformations, reduce production costs, and enhance the overall reliability of semiconductor devices.

11 Future Work

The proposed AI Solution aims to enhance the accuracy and efficiency of IC layout deformation prediction and correction. Future work will focus on the following key aspects:

- **Integration with Real-Time Fabrication Processes:** Enhancing the framework for application in real-time IC fabrication, allowing for corrective measures to be implemented during the manufacturing process.
- **Scalability to Advanced Technology Nodes:** Adapting the models for use in advanced technology nodes (e.g., sub-5nm processes), where deformation challenges are more pronounced and require innovative solutions.
- **Incorporating Physics-Based Models:** Integrating data-driven AI models with physics-based lithography simulations to establish a more comprehensive approach to deformation prediction.

- **Cross-Technology Generalization:** Assessing the framework's capability to generalize across various semiconductor technologies, materials, and fabrication techniques to ensure broad applicability.

12 References

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