2022 Digital IC Design
Homework 4: Edge-Based Line Average interpolation

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Simulation Result

Functional simulation	Pass	Gate-level simulation	Pass	Clock width	18.07 (ns)	Gate-level simulation time	52747.6(ns)

your pre-sim result of test patterns

```
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ---------------------------------------------------------------
#
# ** Note: $finish    : D:/DIC2022/file/testfixture.v(176)
#    Time: 52739360 ps  Iteration: 0  Instance: /TB_ELA
```

your post-sim result of test patterns

```
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ---------------------------------------------------------------
#
# ** Note: $finish    : D:/DIC2022/file/testfixture.v(176)
#    Time: 52747598 ps  Iteration: 0  Instance: /TB ELA
```

Synthesis Result

Total logic elements	334
Total memory bit	0
Embedded multiplier 9-bit element	0

your flow summary

Flow Summary	
Flow Status	Successful - Wed May 18 08:21:16 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	334 / 68,416 (< 1 %)
Total combinational functions	330 / 68,416 (< 1 %)
Dedicated logic registers	115 / 68,416 (< 1 %)
Total registers	115
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

本次作業主要可以分成兩個部分，第一個部分是以 verilog 完成 ELA 的演算法，在一開始會將 wen 訊號以及 req 訊號拉起，開始讀入檔案，讀完檔案後，會根據各個像素去找他的六個相鄰點，先判斷是左邊界、右邊界或是非邊界的狀況，根據不同的狀況，去算出該插入點的對應數值，把每一格數值求出，就可以與 golden data 比對是否正確。

第二個部分則是透過 python 完成圖片與 golden 資料的輸出，這邊使用的是 python 3.9.7 及 python-opencv 與 numpy，產生的方式與 verilog 差異不大。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns) = 334 × 52747 = 17617498 ns*