

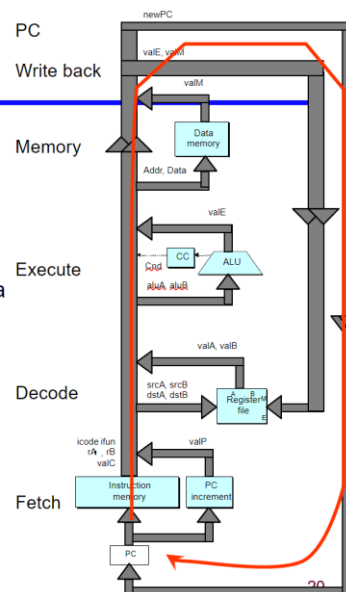
SEQ Hardware Structure

State

- Program counter register (PC)
- Condition code register (CC)
- Register File
- Data memory: for reading/writing data
- Instruction memory: for reading instructions

Instruction Flow

- Read instruction at address specified by PC
- Process through stages
- Update program counter



SEQ Stages

Fetch

- Read instruction from [instruction memory](#)

Decode

- Read operands from [registers](#)

Execute

- Compute value or address

Memory

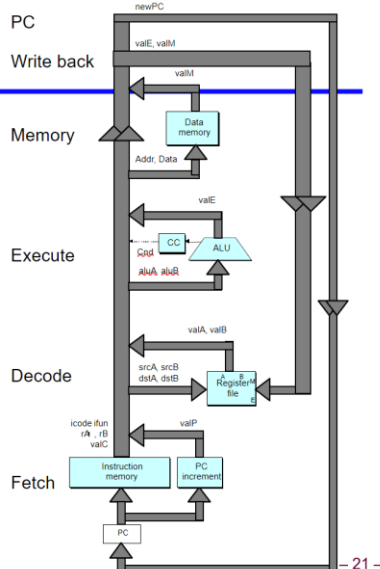
- Read or write data

Write Back

- Write to [registers](#)

PC

- Update [program counter](#)



Computed Values (to be used in the following slides)

Fetch

- [icode](#) Instruction code
- [ifun](#) Instruction function
- [rA](#) Instr. Register A
- [rB](#) Instr. Register B
- [valC](#) Instruction constant
- [valP](#) Incremented PC

Decode

- [srcA](#) Register ID A
- [srcB](#) Register ID B
- [dstE](#) Destination Register E
- [dstM](#) Destination Register M
- [valA](#) Register value A
- [valB](#) Register value B

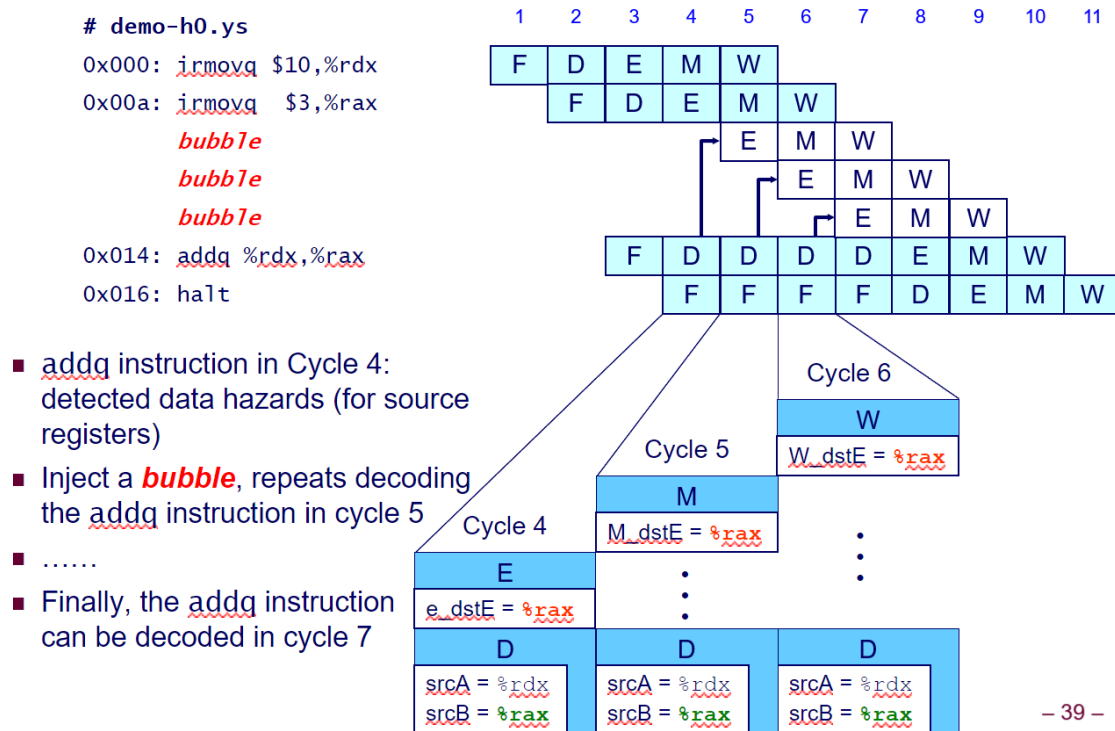
Execute

- [valE](#) ALU result
- [Cnd](#) Branch/move flag

Memory

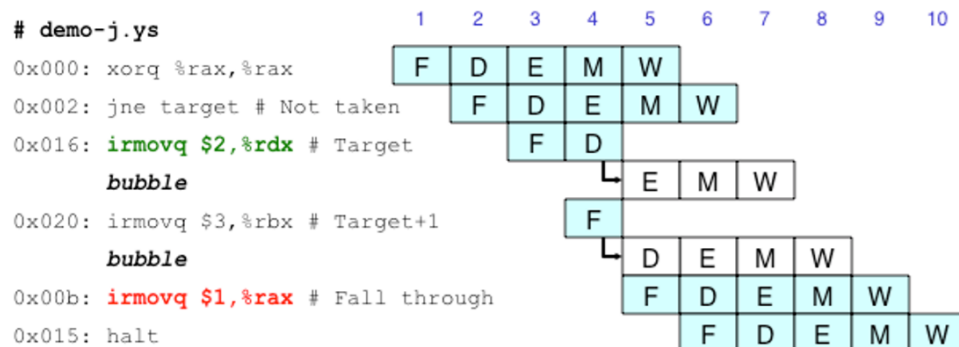
- [valM](#) Value from memory

Solution: Stalling



等到完成 write back 后再继续

Handling Misprediction



Predict branch as taken

- Fetch 2 instructions at target

Cancel when mispredicted

- Detect branch not-taken in execute stage
- On following cycle, replace instructions in execute and decode by bubbles
- No side effects have occurred yet

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在 JXX 判断过程中，先对预测的分支运行一部分；待到 jxx 的 execute 完成后，如果预测错误，则从头开始对另一分支进行运行。