USB Gain/Phase Analyzer

Watson Capstone Projects (WCP52)

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November 28, 2014
Revision: –

Submitted in partial fulfillment of the requirements of ME 493/EECE 487
in the Fall Semester of 2008.

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Executive Summary

In the current market, electronics lab equipment that can analyze a frequency response by gain and phase (a vector analyzer) is very expensive, often reaching into the tens of thousands of dollars. They are large, heavy instruments, and are not portable between home, class and a lab. A direct result of this high cost is that they are generally unobtainable for teachers to use in classrooms and labs to enhance their education techniques and for students to use as a hands on tool for circuit analysis projects. Due to their lack of portability, those teachers who do have access to a vector analyzer can not use its vast functionality for demonstrations of a circuit's behavior in front of a classroom or in a lab with many students.

It is our goal to remedy this situation by creating a low cost, portable device that can provide an analysis of gain and phase in a graph.

This gain/phase analyzer can be produced and sold for approximately $100. The device is portable and can be carried between home, work, labs, classrooms, etc and is very easy to set up with a USB connection to a computer and a power outlet.

Additionally, our device is an open source project, with all hardware and software source available online. Thus, any capable students or engineers will have ability to learn how it works and modify the design any way they choose. This can be a great way for students to gain some hands-on experience in learning some advanced circuit design techniques and microcontroller programming. Additionally, one can apply one's own creativity and ingenuity to improve the design of this project; making a better device for future teachers and students.

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1. Problem Definition

Tools such as vector analyzers are heavy and expensive, costing tens of thousands of dollars. There is need of a tool for students and teachers to help teach electronics and similar courses. Currently, there are no feasibly affordable tools to show the frequency response and phase of a circuit, amplifier, or control loop, and the learning experience is hindered by this gap.

1.1. Problem Scope

This project will produce a portable frequency response analyzer. It will communicate data with a computer through USB which will form a Bode plot of the frequency response and calculate the phase of the circuit.

1.2. Technical Review

Proper circuit analysis is a fundamental practice in the field of engineering, since it is necessary for every electronic device on the market. As a result, it is the goal of every engineering institution to give students a strong basis in circuit design and analysis.

Currently, this is done mainly through lecture and labs. A professor stands in front of a classroom and delivers a lecture based on powerpoint slides that they have created. It is expected that, from this, students grasp the concepts necessary to make them proficient in working with electronics. Although this may be a seemingly efficient way to broadcast the fundamentals to many people, it must be augmented with practice.

Then, there is the lab section of the class. Students are asked to put together a circuit and then observe it using a measuring device. Unfortunately, few such devices are available for frequency-domain work.

It is the goal of this project to help remedy this situation. This USB Gain/Phase Analyzer is a cheap, portable tool. With this, a teacher would have the ability to bring circuits to class and actually demonstrate fundamentals to their students. This would inevitably enhance the effectiveness of their lectures because students would see how these circuits respond in application. The aim, here, is to help a teacher captivate his/her students.

Additionally, the analyzer is a tool that students can afford. In a lab, they could now be asked to design something, increasing the creative thinking of the prospective engineer. With this tool, they can now do more meaningful analysis and see their devices' behaviors on real world signals. Also, the device is portable enough that students could take it home and do lab work there, without needing to spend thousands of dollars on lab equipment.

1.3. Design Requirements

1.3.1. Context-Level Constraints

This project is producing one gain/phase analyzer system. As shown in Figure 1: Gain/Phase Analyzer Context Diagram, the device connects to a PC for user control and viewing of data. It has one Drive output, with which it applies a stimulus to a Device Under Test (DUT), and two Sense inputs, with which it detects the amplitude and phase of signals before and after the DUT. The device will also have an Adapter port, with which it can connect to external adapters for measuring various types of DUTs. The gain/phase analyzer system, in addition to the hardware, comprises PC Software with which the end user may start analyses and view results.

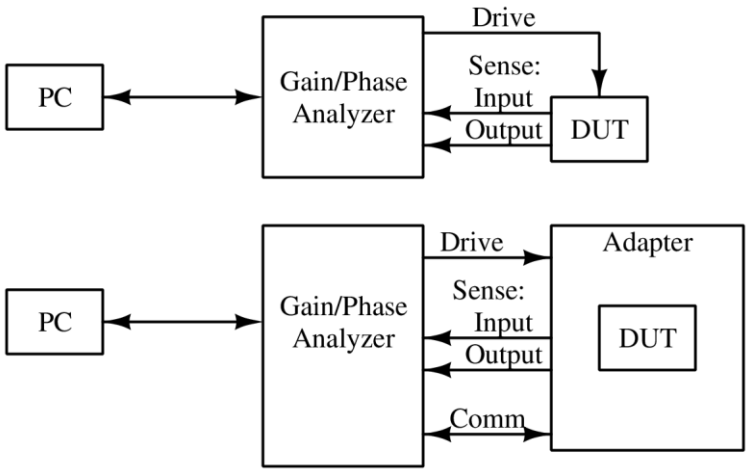


Figure 1: Gain/Phase Analyzer Context Diagram

1.3.2. System-Level Constraints

As shown in Figure 2: Gain/Phase Analyzer System Diagram, the analyzer uses a *Synthesizer* to generate the stimulus signal, and an *Output Amplifier* to provide the stimulus signal to the DUT, at up to 1.25 V RMS and up to 150 MHz. *Input Filters*, an *Input Switching Network* and the *Input Detector* provide a signal corresponding to the amplitude of the signals at the Sense ports. The Input Switching Network can also select a *Phase Reference* to be summed with the signals for phase measurement. These are digitized by an *Analog-Digital Converter* to be processed by the *Microprocessor*. The Microprocessor then interfaces with the *Software* via the *PC Interface*.

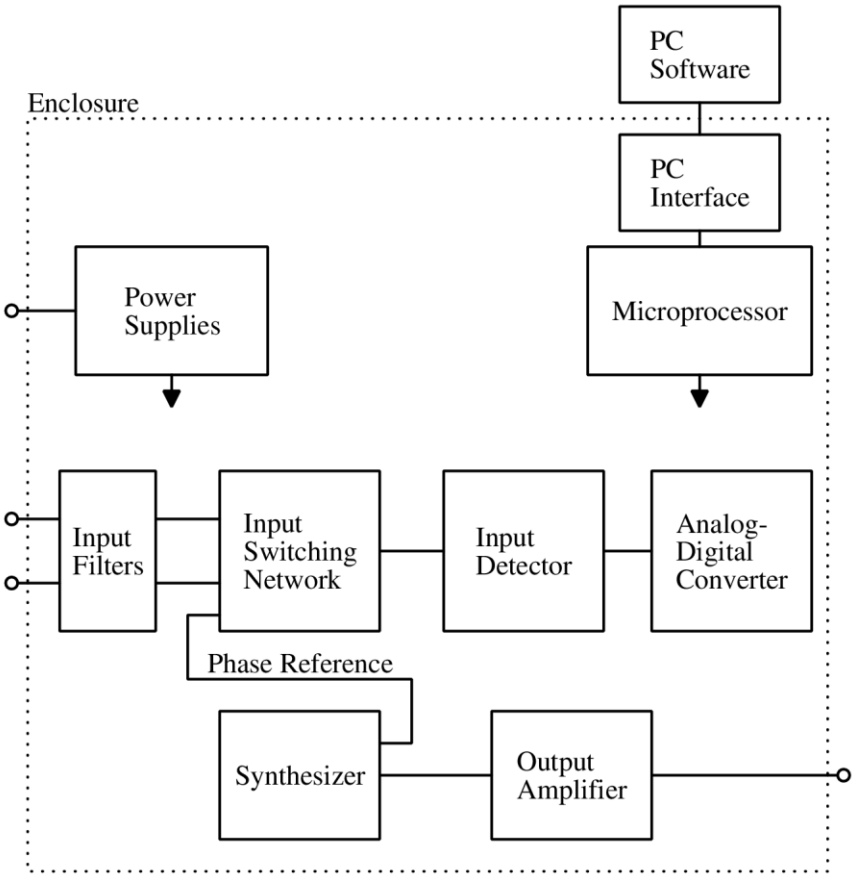


Figure 2: Gain/Phase Analyzer System Diagram

2. Design Description

2.1. Overview

A Gain/Phase Analyzer is an instrument used to plot the frequency response of a network or amplifier. The project, sponsored by Professor Kyle Temkin, specifies a small, computer controlled gain/phase analyzer for use by students and individuals. It can stimulate and then measure filters, amplifiers and control systems, allowing their behavior to be plotted and analyzed. The device is to be developed as an open-source project, so that students may study its inner workings.

2.2. Detailed Description

Our project is one without many various and viable implementation possibilities. As such, many major decisions will involve study of other instrumentation which performs similar tasks, including a few open-source network analyzers. Trade study will be used as required for selecting high-cost components or designs of subsystems, and this will be addressed as necessary during the development cycle. Hardware is being designed and

implemented in different stages in order to ease the process of design. Software will be created with the purpose of interfacing with the microcontroller.

2.2.1. Synthesizer

The first subsystem that will be built is the frequency synthesizer. This needs to generate a frequency up to 150 MHz. For this design the circuit uses the AD9958 Direct Digital Synthesis (DDS) chip and a 'video' op-amp to produce the correct output.

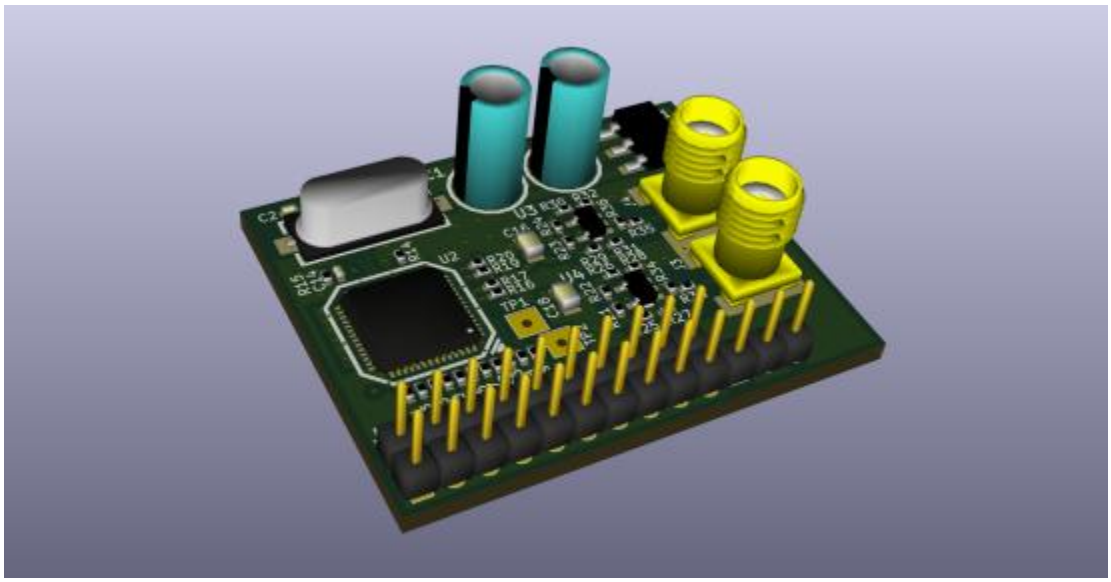


Figure 3: Synthesizer PCB, 3D Render

In the final product, we may integrate an optional CPLD or FPGA to allow the user to drive the modulation feature of the DDS chip; for the purposes of testing we have tied the modulation inputs straight to ground, as we do not require them.

2.2.2. Input Front-end

The next section of the design is the input front-end subsystem.

Figure 4: Input Front-end PCB, 3D Render

Our input front-end must take the signals from the front-panel input connectors and present them in a form which can be directly sampled by the microcontroller's analog-to-digital converter. The signals first pass through a simple input protection circuit. This consists of a small-footprint SMD fuse in series with the input and a clamping arrangement set around 3.3V (23 dBm peak). After the input protection, the two input signals enter a switching circuit to select between them. This allows all of the following circuitry to be shared between channels, minimizing cost and inter-channel variation. This is followed by a buffer, which isolates the input signal from the following power combiner and filter. After that, a power combiner adds in a variable phase reference, which allows the system to measure the input signal's phase, and a filter cuts the signal off at 300 MHz. The filtered signal then passes into a logarithmic detector with integrated low-pass filter, which presents a voltage proportional to the logarithm of the input amplitude to the microcontroller.

2.2.3. Output Amplifier

The next section of the design is the output amplifier subsystem.

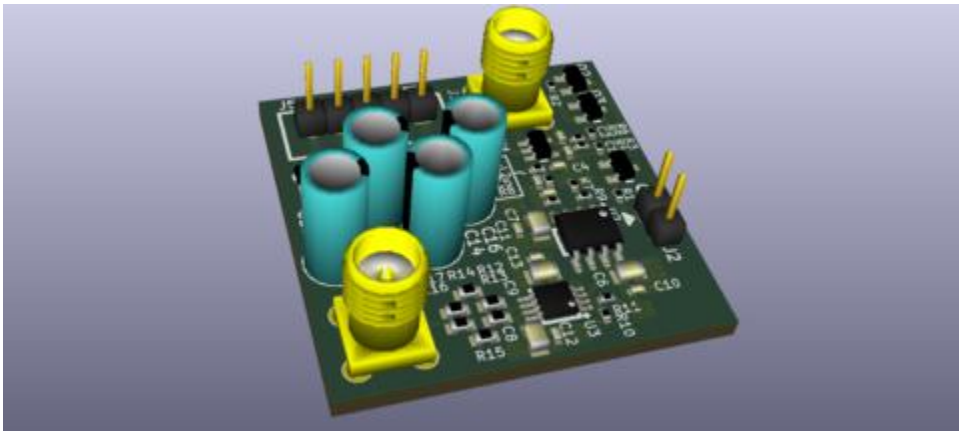


Figure 5: Output Amplifier PCB, 3D Render

The output amplifier must take small signals, at –8.5 dBm as they arrive from the synthesizer, and output the full 15 dBm signal. For design margin, a 16.5 dBm output amplitude is assumed. This gives a required gain of 25 dB. An additional 6 dB gain is required to compensate for the insertion loss of the termination, giving a total required gain of 31 dB. A gain of 31 dB from 1 kHz (practically DC) to 150 MHz is difficult to achieve, particularly with the very large absolute amplitude of 21 dBm at the output. We chose to use two gain stages of 15.5 dB each. The final stage is a THS3001 operational amplifier, as it supports the high slew rate, high voltage and high output current required. This is a very expensive amplifier, though, so we used the AD8000 (similar specifications, but with a lower maximum supply voltage) for the first stage. The synthesizer allows amplitude control, but this control is applied at the digital stage, resulting in a loss of DAC resolution. To get more range at full resolution, we included a MAADSS0008 switchable 15 dB attenuator in the output amplifier's signal path.

2.2.4. Microprocessor

For our system's microprocessor, we used the Atmel SAM4S16C ARM Cortex-M4 microcontroller. In the final product, we will switch to a less expensive microcontroller in the SAM4S line with a smaller amount of memory, after we have determined the amount needed.

In the current prototype, we are using the Atmel SAM4S Xplained evaluation kit; the final product will use the chip by itself.

2.3. Use

The purpose of this device is to provided students with tangible data when analyzing circuits. As shown in Figure 1: Gain/Phase Analyzer Context Diagram, the device is to be connected between a PC and a device under test; the user can initiate an analysis using the supplied software.

3. Next Steps

The purpose of this semester is to be able to present a prototype of our design. Each part will be connected to one another and will show how the final product will function. All of the prototype PCBs have been designed now, but have not been fully tested.

The next step for hardware is to finish assembling and testing the PCBs. After this, the hardware engineers will switch and help the software development until next semester, when the final PCB will be designed.

The next step for software is to continue working on the microcontroller firmware, and then write a simple, prototype script which can produce a rough, uncalibrated frequency response plot to demonstrate the device's functionality.

4. References

[1] C. Pavlina *et al.*, *USB Gain/Phase Analyzer Project Requirements Specification*, Rev. –, 2014.

[2] *AD8000: 1.5 GHz Ultrahigh Speed Op Amp*, Rev. B, Analog Devices, Norwood, MA, 2013.

[3] *AD9958: 2-Channel, 500 MSPS DDS with 10-Bit DACs*, Rev. B, Analog Devices, Norwood, MA, 2013.

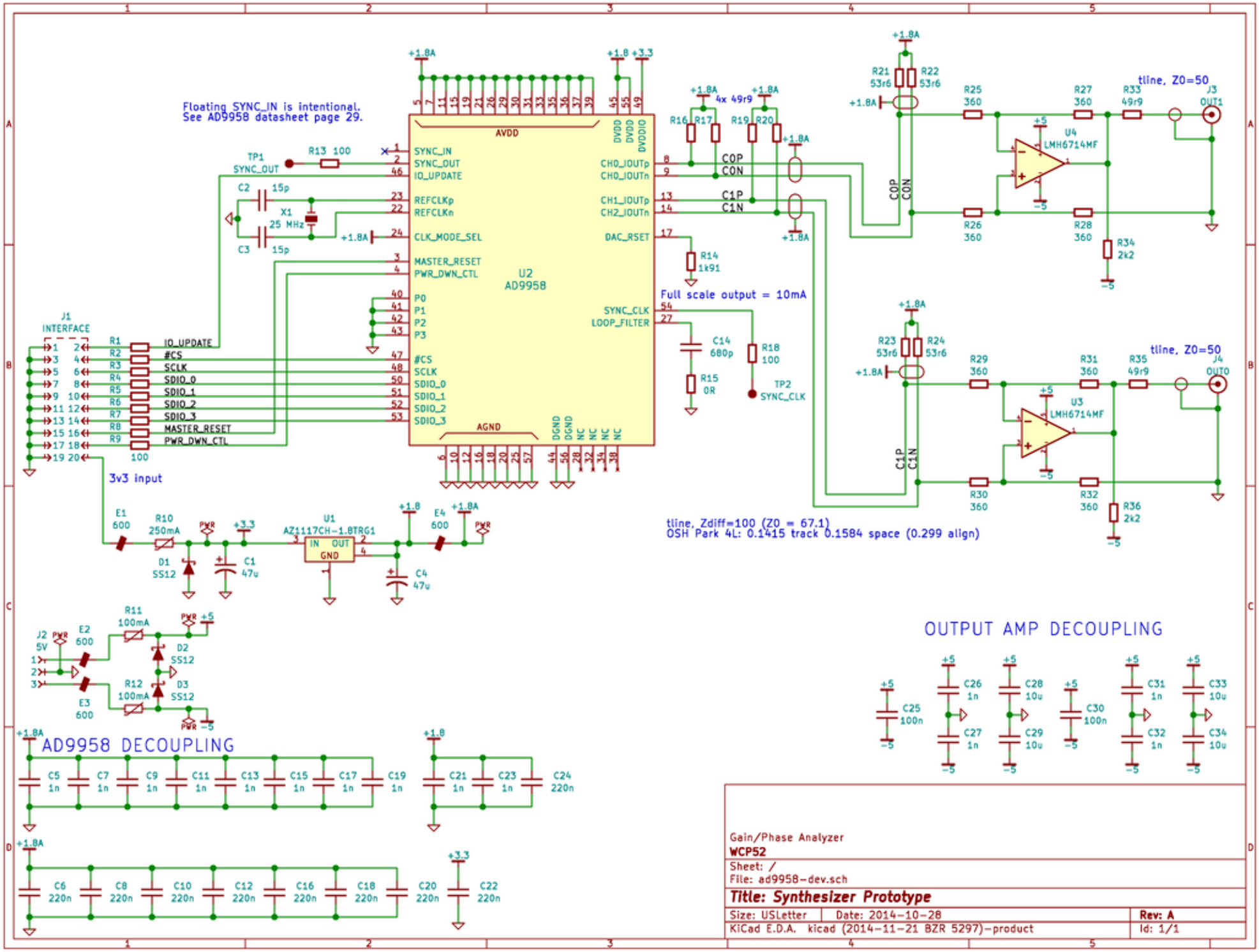
[4] *MAADSS0008: Digital Attenuator, 1-Bit, 15 dB, DC – 2.0 GHz*, Rev. V1, M/A-COM.

[5] *SAM4S Series ARM-based Flash MCU Datasheet*, Atmel, San Jose, CA, 2014.

[6] *THS3001: 420-MHz High-Speed Current-Feedback Amplifier*, Texas Instruments, Dellas, TX, 2009.

Appendix A Computer Code

Appendix B CAD Drawings


Floating SYNC_IN is intentional.
See AD9958 datasheet page 29.
U2
AD9958
AVDD
AGND
DVDD
DVDD
DVDDIO
DGND
DGND
NC
NC
NC
NC
SYNC_IN
SYNC_OUT
IO_UPDATE
REFCLKp
REFCLKn
CLK_MODE_SEL
MASTER_RESET
PWR_DWN_CTL
P0
P1
P2
P3
#CS
SCLK
SDIO_0
SDIO_1
SDIO_2
SDIO_3
CH0_IOUTp
CH0_IOUTn
CH1_IOUTp
CH2_IOUTn
DAC_RSET
SYNC_CLK
LOOP_FILTER
TP1
SYNC_OUT
R13 100
C2 15p
C3 15p
X1
25 MHz
R14
1k91
Full scale output = 10mA
C14
680p
R15
0R
R18
100
TP2
SYNC_CLK
J1
INTERFACE
R1 IO_UPDATE
R2 #CS
R3 SCLK
R4 SDIO_0
R5 SDIO_1
R6 SDIO_2
R7 SDIO_3
R8 MASTER_RESET
R9 PWR_DWN_CTL
100
3v3 input
E1
600
R10
250mA
D1
SS12
C1
47u
U1
AZ1117CH-1.8TRG1
IN
OUT
GND
C4
47u
E4
600
R11
100mA
D2
SS12
R12
100mA
D3
SS12
J2
5V
E2
600
E3
600
R16
R17
4x 49r9
R19
R20
COP
CON
C1P
C1N
R21
53r6
R22
53r6
R23
53r6
R24
53r6
R25
360
R26
360
R27
360
R28
360
R29
360
R30
360
R31
360
R32
360
R33
49r9
R34
2k2
R35
49r9
R36
2k2
U4
LMH6714MF
U3
LMH6714MF
J3
OUT1
J4
OUT0
tline, Z0=50
tline, Z0=50
tline, Zdiff=100 (Z0 = 67.1)
OSH Park 4L: 0.1415 track 0.1584 space (0.299 align)
OUTPUT AMP DECOUPLING
C25 100n
C26 1n
C27 1n
C28 10u
C29 10u
C30 100n
C31 1n
C32 1n
C33 10u
C34 10u
AD9958 DECOUPLING
C5 1n
C7 1n
C9 1n
C11 1n
C13 1n
C15 1n
C17 1n
C19 1n
C21 1n
C23 1n
C24 220n
C6 220n
C8 220n
C10 220n
C12 220n
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C22 220n
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Rev: A
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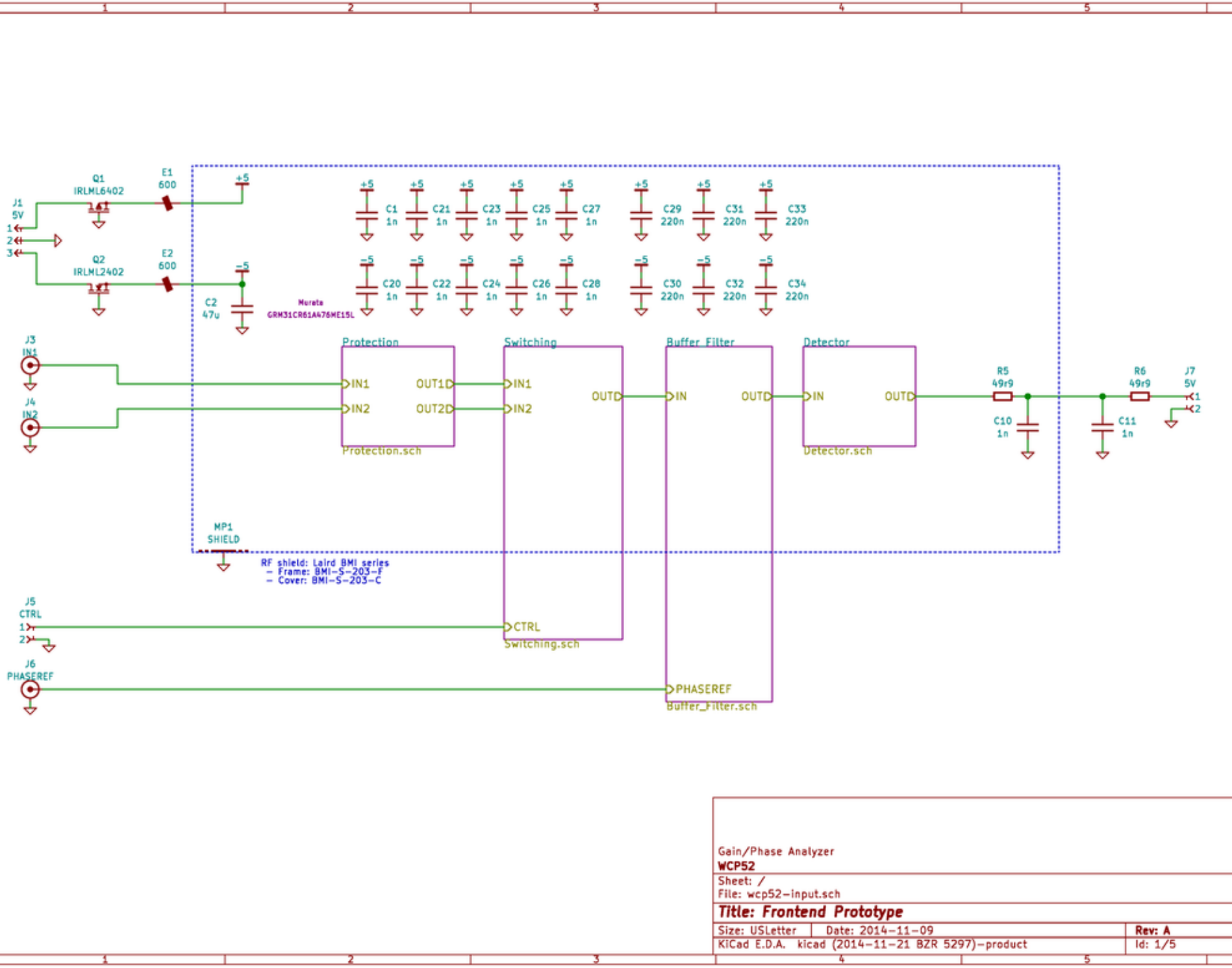

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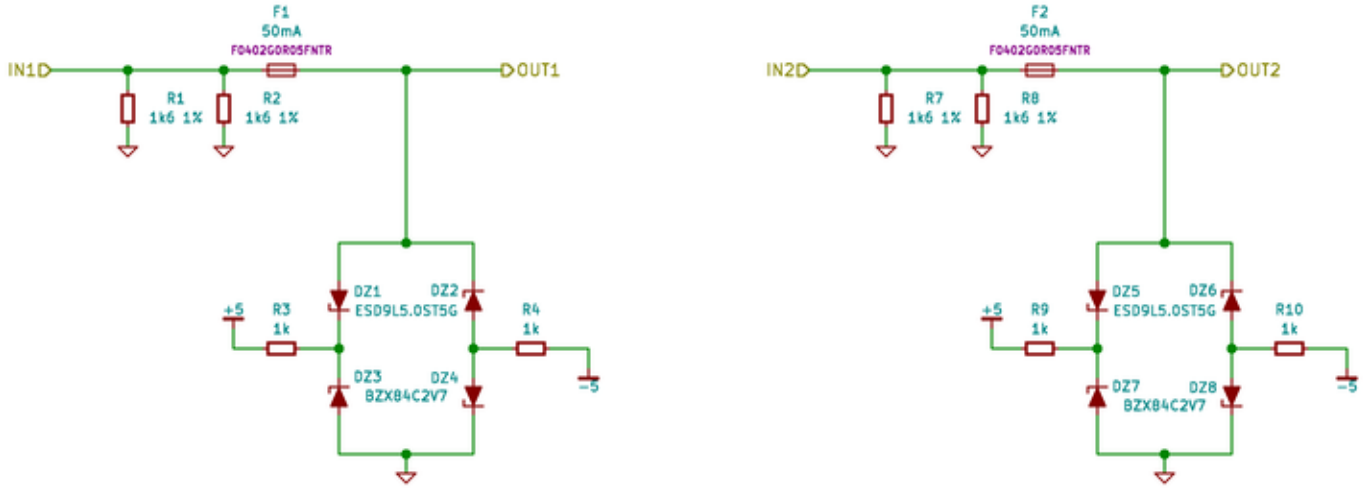

Gain/Phase Analyzer
WCP52

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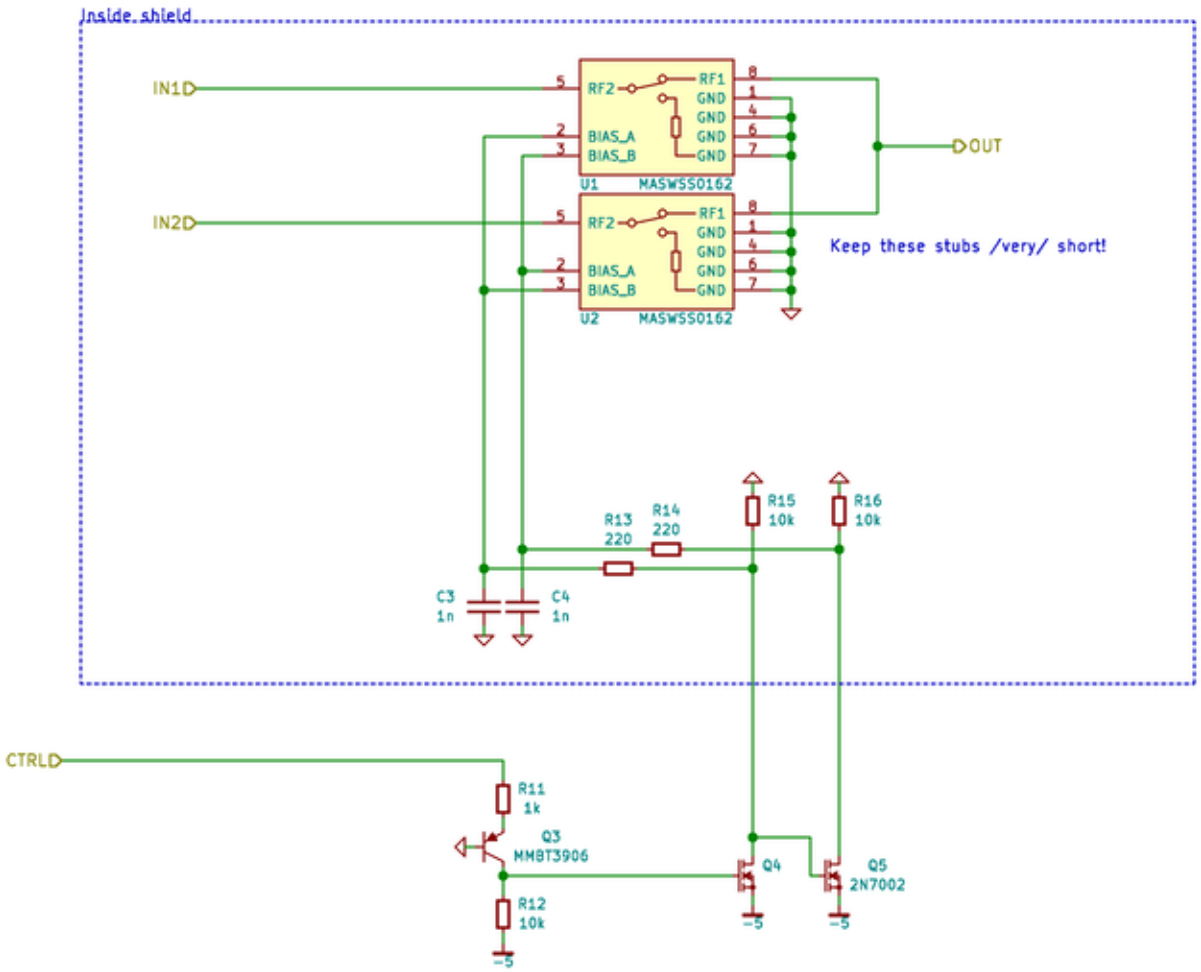

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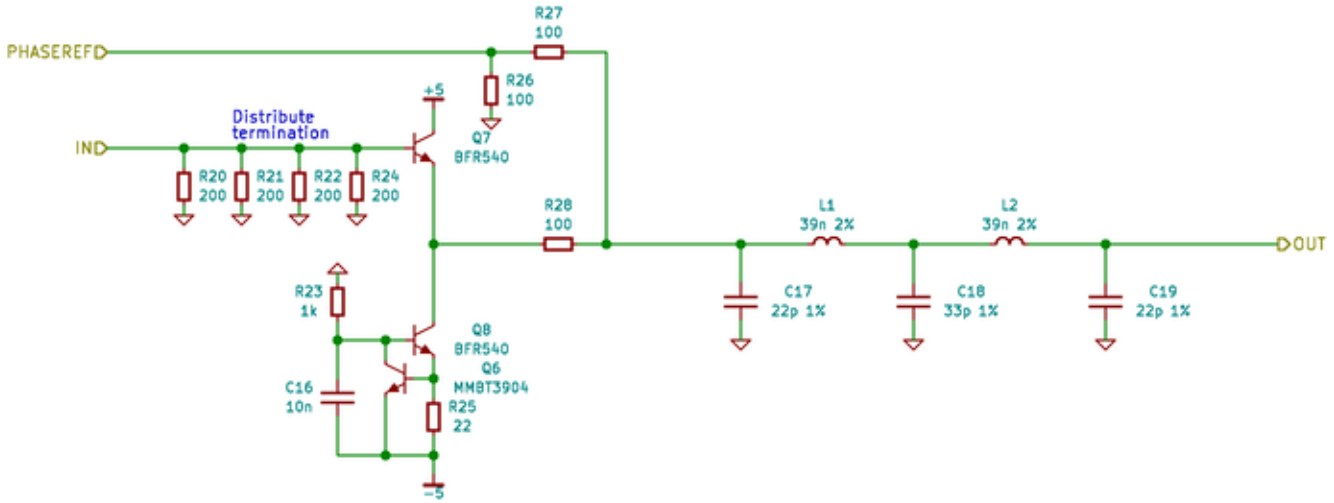

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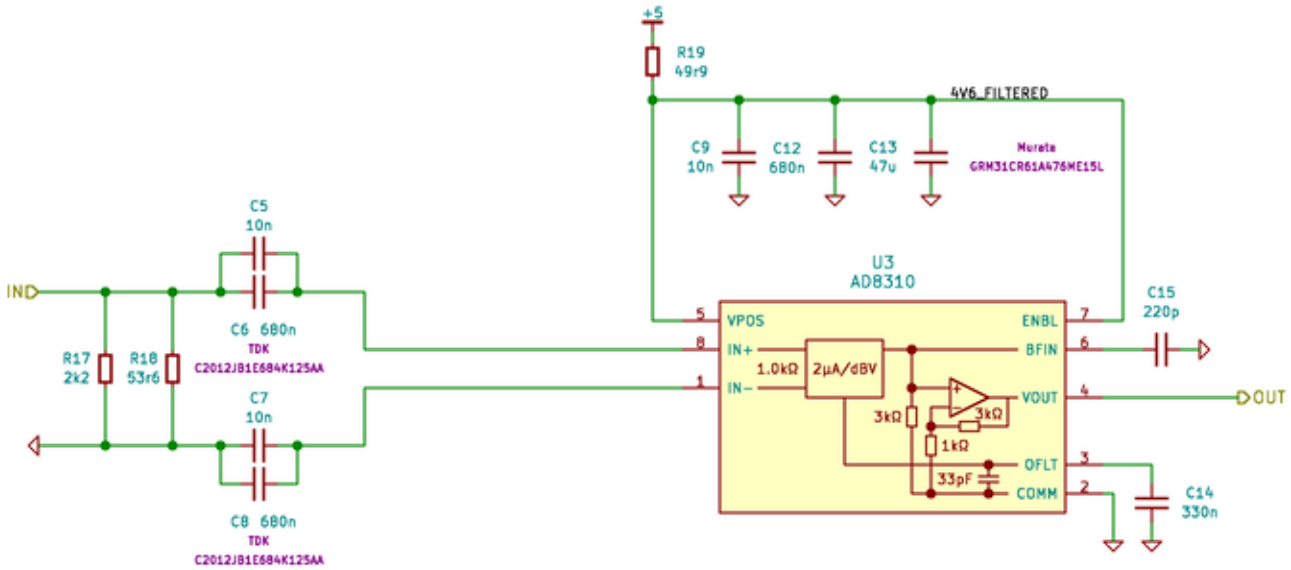

Gain/Phase Analyzer
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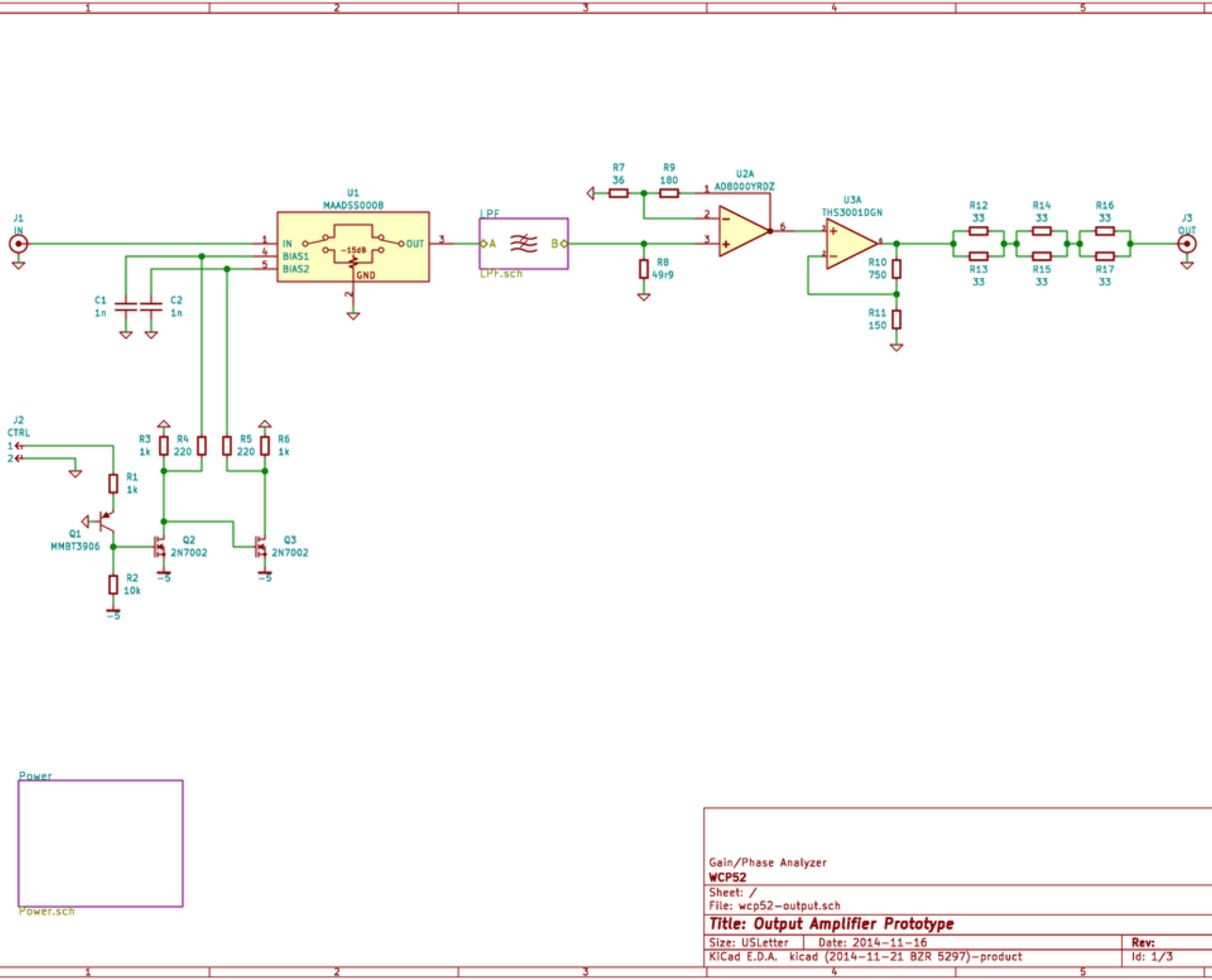
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U1
MAADSS0008
IN
BIAS1
BIAS2
GND
OUT
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C1
1n
C2
1n
LPF
A
B
LPF.sch
R7
36
R9
180
U2A
AD8000YRDZ
R8
49r9
U3A
THS3001DGN
R10
750
R11
150
R12
33
R13
33
R14
33
R15
33
R16
33
R17
33
J3
OUT
J2
CTRL
R1
1k
R2
10k
R3
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R4
220
R5
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R6
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Q1
MMBT3906
Q2
2N7002
Q3
2N7002
Power
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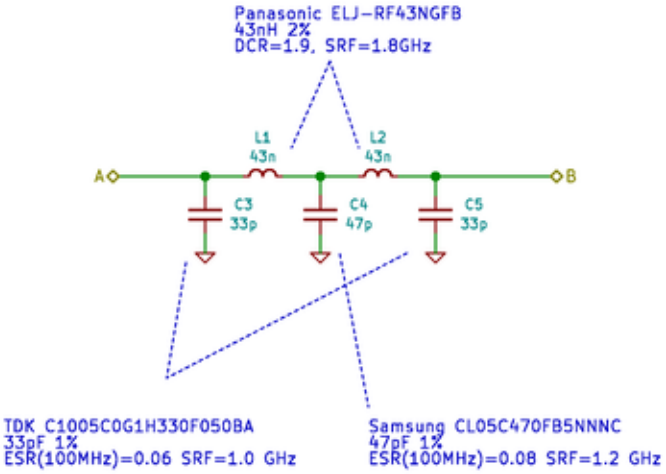
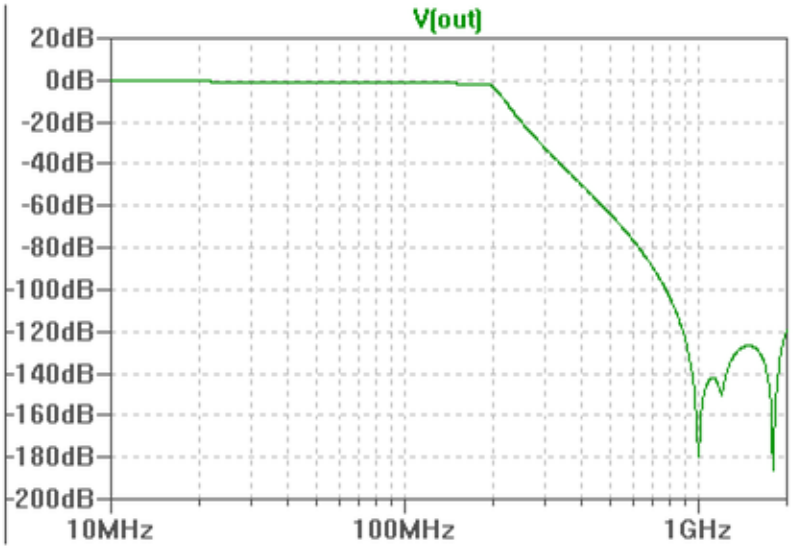


Voltage insertion gain of output filter:



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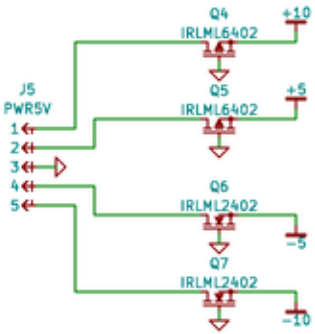
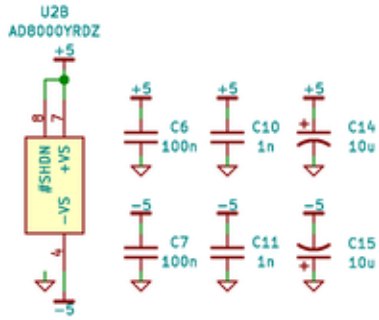
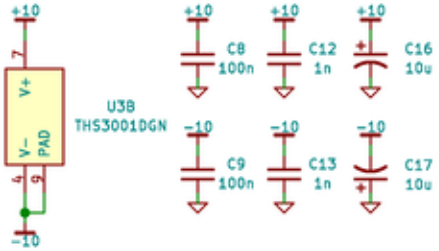




Decoupling: ADI recommends a low-impedance 100nF capacitor directly next to each supply pin, claiming that lower capacitances do not aid decoupling but can help bypass high frequency noise to ground. This is why the 100nF capacitor is closest to the chip, not the 1nF.

The 10uF capacitor is a low-impedance type as well, but still not as low as a high-performance MLCC to avoid causing regulator oscillations.



Decoupling: TI's recommendations were very similar to ADI's, so the same decoupling pattern was used.

Gain/Phase Analyzer
WCP52

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