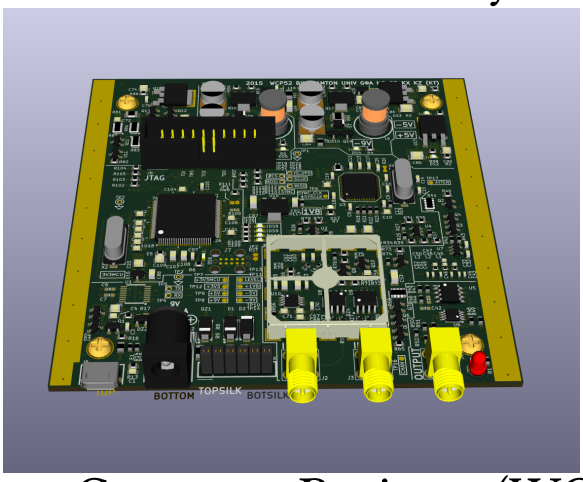
USB Gain/Phase Analyzer



Watson Capstone Projects (WCP52)

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Executive Summary

In the current market, electronics lab equipment that can analyze a frequency response by gain and phase (a vector analyzer) is very expensive, often reaching into the tens of thousands of dollars. They are large, heavy instruments, and are not portable between home, class and a lab. A direct result of this high cost is that they are generally unobtainable for teachers to use in classrooms and labs to enhance their education techniques and for students to use as a hands-on tool for circuit analysis projects. Due to their lack of portability, those teachers who do have access to a vector analyzer can not use its vast functionality for demonstrations of a circuit's behavior in front of a classroom or in a lab with many students.

It is our goal to remedy this situation by creating a low cost, portable device that can provide an analysis of gain and phase in a graph.

This gain/phase analyzer can be produced and sold for approximately $100. The device is portable and can be carried between home, work, labs, classrooms, etc and is very easy to set up with a USB connection to a computer and a power outlet.

Additionally, our device is an open source project, with all hardware and software source available online. Thus, any capable students or engineers will have ability to learn how it works and modify the design any way they choose. This can be a great way for students to gain some hands-on experience in learning some advanced circuit design techniques and microcontroller programming. Additionally, one can apply onefis own creativity and ingenuity to improve the design of this project; making a better device for future teachers and students.

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1 Problem Definition

Tools such as vector analyzers are heavy and expensive, costing tens of thousands of dollars. There is need of a tool for students and teachers to help teach electronics and similar courses. Currently, there are no feasibly affordable tools to show the frequency response and phase of a circuit, amplifier, or control loop, and the learning experience is hindered by this gap.

1.1 Problem Scope

This project will produce a portable frequency response analyzer. It will communicate data with a computer through USB in order to form a Bode plot of the frequency and phase response of the circuit.

1.2 Technical Review

Proper circuit analysis is a fundamental practice in the field of engineering, since it is necessary for every electronic device on the market. As a result, it is the goal of every engineering institution to give students a strong basis in circuit design and analysis.

Currently, this is done mainly through lecture and labs. A professor stands in front of a classroom and delivers a lecture based on PowerPoint slides that they have created. It is expected that, from this, students grasp the concepts necessary to make them proficient in working with electronics. Although this may be a seemingly efficient way to broadcast the fundamentals to many people, it must be augmented with practice.

Then, there is the lab section of the class. Students are asked to put together a circuit and then observe it using a measuring device. Unfortunately, few such devices are available for frequency-domain work.

It is the goal of this project to help remedy this situation. This USB Gain/Phase Analyzer is a cheap, portable tool. With this, a teacher would have the ability to bring circuits to class and actually demonstrate fundamentals to their students. This would inevitably enhance the effectiveness of their lectures because students would see how these circuits respond in application. The aim, here, is to help a teacher captivate his/her students.

Additionally, the analyzer is a tool that students can afford. In a lab, they could now be asked to design something, increasing the creative thinking of the prospective engineer. With this tool, they can now do more meaningful analysis and see their devices' behaviors on real world signals. Also, the device is portable enough that students could take it home and do lab work there, without needing to spend thousands of dollars on lab equipment.

1.3 Design Requirements

1.3.1 Context-Level Constraints

This project is producing one gain/phase analyzer system. As shown in Figure 1, the device connects to a PC for user control and viewing of data. It has one Drive output, with which it applies a stimulus to a Device Under Test (DUT), and two Sense inputs, with which it detects the amplitude and phase of signals before and after the DUT. The device will also have an Adapter port, with which it can connect to external adapters for measuring various types of DUTs. The gain/phase analyzer system, in addition to the hardware, comprises PC Software with which the end user may start analyses and view results.

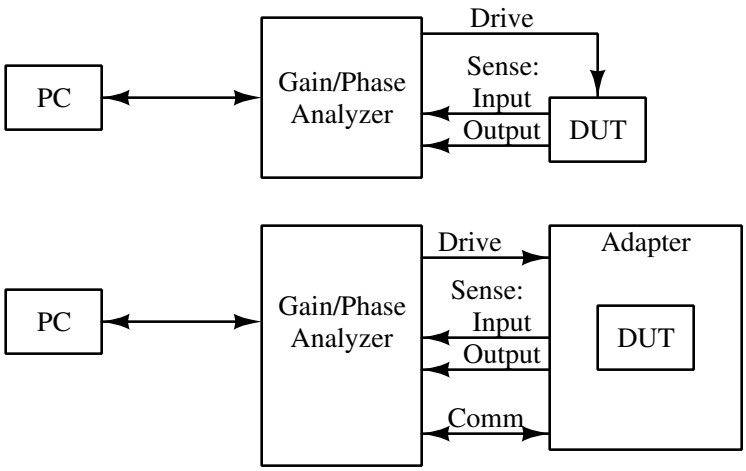

Figure 1: Gain/Phase Analyzer Context Diagram

1.3.2 System-Level Constraints

As shown in Figure 2, the analyzer uses a *Synthesizer* to generate the stimulus signal, and an *Output Amplifier* to provide the stimulus signal to the DUT, at up to 1.25 V RMS and up to 150 MHz. *Input Filters*, an *Input Switching Network* and the *Input Detector* provide a signal corresponding to the amplitude of the signals at the Sense ports. The Input Switching Network can also select a *Phase Reference* to be summed with the signals for phase measurement. These are digitized by an *Analog-Digital Converter* to be processed by the *Microprocessor*. The Microprocessor then interfaces with the *Software* via the *PC Interface*.

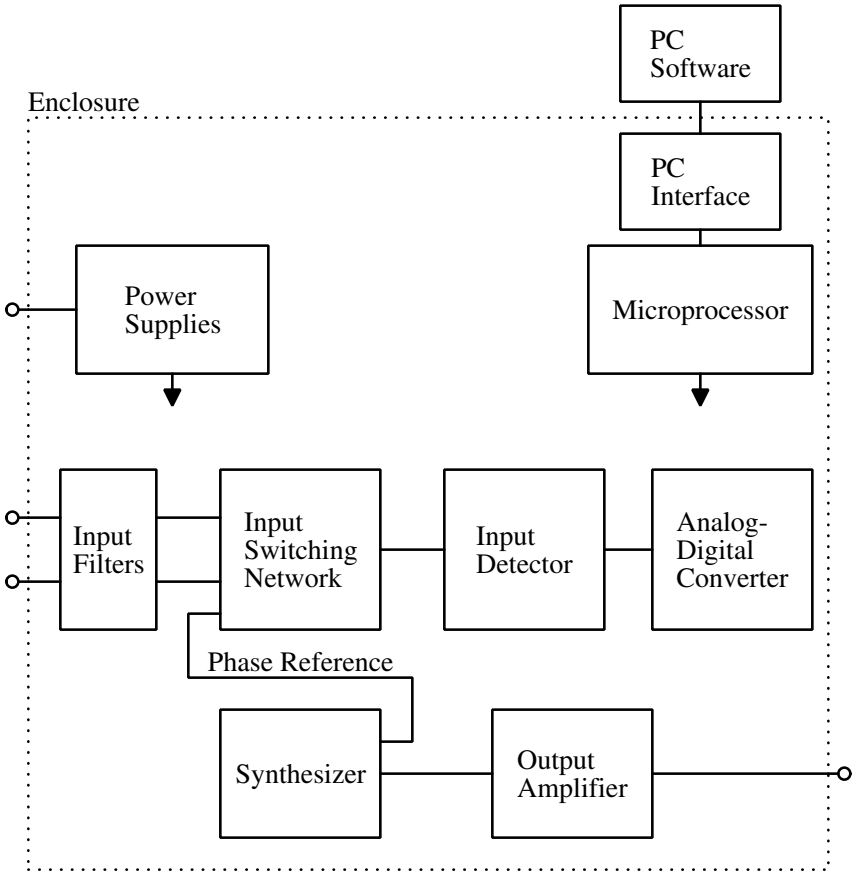

Figure 2: Gain/Phase Analyzer System Diagram

2 Design Description

2.1 Overview

A Gain/Phase Analyzer is an instrument used to plot the frequency response of a network or amplifier. The project, sponsored by Professor Kyle Temkin, specifies a small, computer controlled gain/phase analyzer for use by students and individuals. It can stimulate and then measure filters, amplifiers and control systems, allowing their behavior to be plotted and analyzed. The device is to be developed as an open-source project, so that students may study its inner workings.

2.2 Detailed Description

Our project lacks many various and viable implementation possibilities. As such, many major decisions will involve study of other instrumentation which performs similar tasks, including a few open-source network analyzers. Trade study will be used as required for selecting high-cost components or designs of subsystems, and this will be addressed as necessary during the development cycle. Hardware is being designed and implemented in different stages in order to ease the process of design. Software will be created with the purpose of interfacing with the microcontroller.

2.2.1 Synthesizer

The first subsystem that will be built is the frequency synthesizer. This needs to generate a frequency up to 150 MHz. For this design, the circuit uses the AD9958 Direct Digital Synthesis (DDS) chip and a 'video' op-amp to produce the correct output.

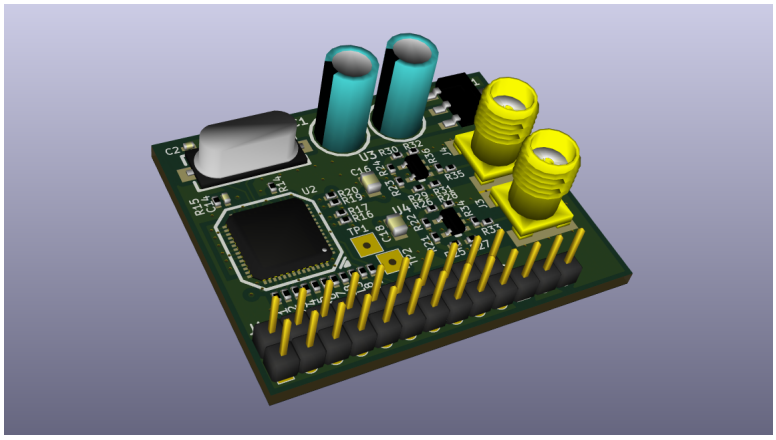

Figure 3: Synthesizer PCB, 3D render

In the final product, we may integrate an optional CPLD or FPGA to allow the user to drive the modulation feature of the DDS chip; for the purposes of testing we have tied the modulation inputs straight to ground, as we do not require them.

2.2.2 Input Front-end

The next section of the design is the input front-end subsystem.

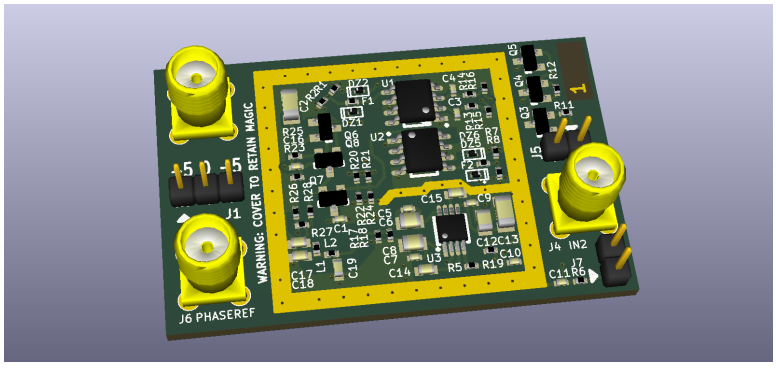

Figure 4: Input Front-end PCB, 3D render

Our input front-end must take the signals from the front-panel input connectors and present them in a form which can be directly sampled by the microcontroller's analog-to-digital converter. The signals first pass through a simple input protection circuit. This consists of a small-footprint SMD fuse in series with the input and a clamping arrangement set around 3.3 V (23 dBm peak). After the input protection, the two input signals enter a switching circuit to select between them. This allows all of the following circuitry to be shared between channels, minimizing cost and inter-channel variation. This is followed by a buffer, which isolates the input signal from the following power combiner and filter. After that, a power combiner adds in a variable phase reference, which allows the system to measure the input signal's phase, and a filter cuts the signal off at 300 MHz. The filtered signal then passes into a

logarithmic detector with integrated low-pass filter, which presents a voltage proportional to the logarithm of the input amplitude to the microcontroller.

2.2.3 Output Amplifier

The next section of the design is the output amplifier subsystem.

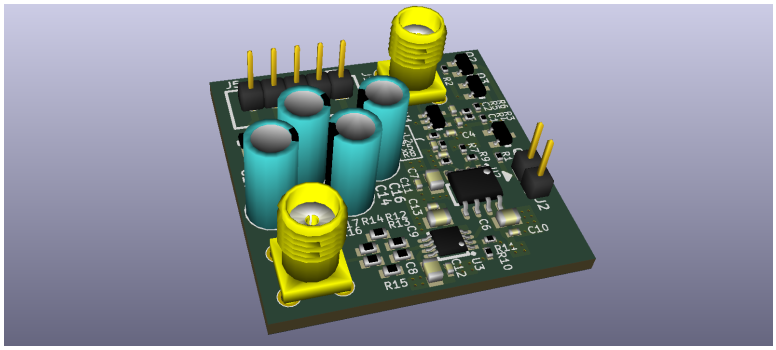

Figure 5: Output Amplifier PCB, 3D render

The output amplifier must take small signals, at fi?!8.5 dBm as they arrive from the synthesizer, and output the full 15 dBm signal. For design margin, a 16.5 dBm output amplitude is assumed. This gives a required gain of 25 dB. An additional 6 dB gain is required to compensate for the insertion loss of the termination, giving a total required gain of 31 dB. A gain of 31 dB from 1 kHz (practically DC) to 150 MHz is difficult to achieve, particularly with the very large absolute amplitude of 21 dBm at the output. We chose to use two gain stages of 15.5 dB each. The final stage is a THS3001 operational amplifier, as it supports the high slew rate, high voltage and high output current required. This is a very expensive amplifier, though, so we used the AD8000 (similar specifications, but with a lower maximum supply voltage) for the first stage. The synthesizer allows amplitude control, but this control is applied at the digital stage, resulting in a loss of DAC resolution. To get more range at full resolution, we included a MAADSS0008 switchable 15 dB attenuator in the output amplifier's signal path.

2.2.4 Microprocessor

For our system's microprocessor, we used the Atmel SAM4S16C ARM Cortex-M4 microcontroller. In the final product, we will switch to a less expensive microcontroller in the SAM4S line with a smaller amount of memory, after we have determined the amount needed.

In the current prototype, we are using the Atmel SAM4S Xplained evaluation kit; the final product will use the chip by itself.

2.3 Use

The purpose of this device is provide students with tangible data when analyzing circuits. As shown in Figure 1, the device is to be connected between a PC and a device under test; the user can initiate an analysis using the supplied software.

3 Evaluation

3.1 Overview

Our system was designed through a combination of computer simulation, and prototype testing. After carefully designing each subsystem, per-subsystem PCBs were fabricated and interconnected to build a prototype, which was thoroughly tested before the final PCB was designed and fabricated.

As our project is a piece of electrical test equipment, the majority of the tests are electrical in nature. The tests for requirements 3.2.2 and 3.2.3 (output signal characteristics) require an oscilloscope with at least 300 MHz bandwidth. The remaining electrical tests require only a basic multimeter, and often use the instrument to verify itself. For example, 3.2.4 (sensitivity) is verified by measuring the reported amplitude from the output amplifier, and comparing that to the input noise floor. Requirement 3.2.6 (accuracy) is verified by examining the normalized sweep of a flat-response attenuator. Some requirements, for example 3.2.1 (type of plot), 3.3.1 – 3.3.3 (interface design), and 3.6.4 (direct control) are verified simply by observing how the instrument responds to PC control. Others, for example 3.3.4 (panel connectors), 3.6.1 (Operator's Manual), 3.6.2 (Protocol Guide), and 3.6.3 (surface-mount technology) are verified by observing the instrument and accompanying materials themselves.

The full project requirements can be found in Appendix A, and the full test procedures can be found in Appendix B.

3.2 Testing and Results

The full test procedures can be found in Appendix B.

> As the full tests have not been performed at the time of this draft, *Italicized* text is used as a placeholder for missing results.

Requirement WCP52.3.1.1 — Required mode: Idle

This requirement simply means that the device must have a mode in which it is not performing analysis. *We measured the output signal in this state, and it measured —* µV*peak to peak. We demonstrated that the "sample" annunciator was not lit.*

Requirement WCP52.3.1.2 — Required mode: Analysis

This requirement means that the device must have a non-idle mode in which it is performing its primary function. This does not require a separate demonstration; the fact that it performs correctly in the demonstration for WCP52.3.2.6 shows that it must be capable of performing analysis.

Requirement WCP52.3.2.1 — Bode plot

By providing sample data to the PC software and causing it to display a plot, we demonstrated that the software is capable of displaying a Bode plot.

Requirement WCP52.3.2.3 — Test signal frequency

We used an oscilloscope to measure the output of the instrument at nominal frequencies of 1 kHz, 10 MHz, 75 MHz, and 150 MHz. *The maximum deviation from nominal was —%, which is within the 2.5 % required by the test procedure.*

Requirement WCP52.3.2.3 — Test signal amplitude

We used an oscilloscope to measure the amplitude of the instrument's output at nominal frequencies of 1 kHz, 20 MHz, and 100 MHz. *The measured amplitudes were, respectively, — V RMS, — V RMS, and — V RMS.* These are all above the required minimum of 1.25 V RMS.

Requirement WCP52.3.2.4 — Sensitivity

First, we measured the instrument's noise floor at 100 kHz, which is the absolute limit to its sensitivity. *The noise floor was —dB.* This ensures that any measured amplitude above this is the true amplitude, not the noise floor itself. Then, we measured the relative attenuation of a 40 dB nominal attenuator, verifying that the signal could be seen above the noise floor. This shows that the instrument is capable of viewing signals at least 40 dB less than its output amplitude.

Requirement WCP52.3.2.5 — Extended sensitivity

The fact that the noise floor above was also under a threshold of -65 dB satisfies the requirement for extended sensitivity.

Requirement WCP52.3.2.6 — Accuracy — Amplitude

We measured an attenuator specified for —*dB*, and the instrument claimed an attenuation of —*dB*. This is within the required 3 dB accuracy limit.

Requirement WCP52.3.2.6 — Accuracy — Phase

We measured the phase shift due to propagation delay of a section of RG-316 coaxial cable. The nominal phase shifts are:

Frequency	Phase shift
10 kHz	0.02°
1 MHz	1.74°
10 MHz	17.4°
25 MHz	43.5°

We measured phase shifts of:

Frequency	Phase shift
10 kHz	0.02°
1 MHz	1.74°
10 MHz	17.4°
25 MHz	43.5°

These measurements are within —°of nominal, which satisfies the 5°requirement.

Requirement WCP52.3.2.7 — Extended accuracy

The fact that the measurements above are also within 1 dB and 1°satisfies the requirement for extended accuracy.

Requirement WCP52.3.2.8 — Interface safety

To test this, we issued the `LOWLEVEL:SET GPIO_LEVEL` command, and recieved back the message `Pin 'GPIO_LEVEL' is not an output!`. This verifies that the instrument will not set an output value on an input pin.

Requirement WCP52.3.3.1 — Interface

This requirement is satisfied by the fact that WCP52.3.2.1 through WCP52.3.2.8 were satisfied, which all required a PC interface.

Requirement WCP52.3.3.2 — Communications type

We connected a serial terminal to the device and issued the `*IDN?` command, which produced *the response*. These are both text commands, verifying that the instrument uses a text-based serial protocol.

Requirement WCP52.3.3.3 — Communications medium

The use of a USB-compatible serial terminal in verifying WCP52.3.3.2 also demonstrated WCP52.3.3.3.

Requirement WCP52.3.3.4 — Panel connectors

We demonstrated that the connectors on the front panel are SMA connectors.

Requirement WCP52.3.3.5 — Auxiliary connector

We measured the voltages on the power supply pins of the auxiliary connector; they were +-- V and —-- V.

Requirement WCP52.3.6.1 — Operator's manual

We presented the PDF operator's manual, and showed the 'Theory of Operation' and 'Operational Instructions' sections in it. The latter section had test setups for characterizing both filters and control loops.

Requirement WCP52.3.6.2 — Protocol guide

We showed that there is a protocol guide inside the Operator's Manual, which lists the SCPI commands and their formats.

Requirement WCP52.3.6.3 — SMT

We showed that all parts on the PCB were surface-mount with the following exceptions:

DS1 — front panel LED — exemption: front panel

J1 — power jack — exemption: connector, front panel

J2 — input jack #1 — exemption: connector, front panel

J3 — input jack #2 — exemption: connector, front panel

J4 — output jack — exemption: connector, front panel

J5 — auxiliary jack — exemption: connector, front panel

J8 — JTAG port — exemption: connector

L6 — buck-boost inductor — exemption: inductor $>$ 5 mm diam

L7 — buck inductor — exemption: inductor $>$ 5 mm diam

Also, we showed that the only leadless parts were those that are directly responsible for the device's function:

U3 — DDS — directly satisfies WCP52.3.2.2

Requirement WCP52.3.6.4 — Direct control

We showed the following commands in the protocol guide: `LOWLEVEL:SET`, `LOWLEVEL:GET`, `LOWLEVEL:SPITX`, `LOWLEVEL:ADC`.

Requirement WCP52.3.6.5 — Electrical safety

We measured the voltages present on the pins of the auxiliary connector with a multimeter; they were, respectively, *3.3 V, 3.3 V, 8.5 V, -9.3 V, 3.3 V, 0.0 V*. We then measured the maximum amplitude of a signal from the output connector; the maximum peak was 4.5 V. These are all within the 15 V limit.

3.3 Assessment

In the end, our design met all of the mandatory requirements, and most of the optional ones. This is overall a useful design. It can measure filters over a wide range with reasonable accuracy. It is simple to use, robust against input overloads, output overloads, and incorrect power supply. The system is fully open-source, so users can modify and develop on it as they please, and students can learn from its operation.

The design has a few drawbacks, however. First, power consumption is high, as the power supply is inefficient. This was necessary within the development budget and time, as a more efficient power supply design would also produce more noise that could interfere with the measurements. Multiple prototypes and significant analysis and testing could have been required. Second, output phase noise is relatively high at high frequencies. This could cause measurement error particularly when measuring devices with nonlinearities or when attempting to measure very close to a strong resonance. However, this noise is inherent in a design with a fixed sample rate, and correcting this would require a significant increase in complexity of clock generation. Third, the output can have somewhat significant DC offset voltages (up to around 100mV), which is not a huge problem but could be surprising to some users. A coupling capacitor after the differential amplifier stage would fix this, but using the correct one would require significant testing and would risk introducing amplitude loss at either the high or the low end. Fourth, the frontend is not selective; it always measures the total input power over its full bandwidth. A frontend with a selective mixer to measure only signals at the same frequency as the output frequency would greatly increase the measurement noise floor and improve the behavior with nonlinear devices-under-test.

4 Schedule and Budget

The project budget is shown in Table 1.

Item	**Original Estimate ($)**	**Actual to Date ($)**	**Estimate to Completion ($)**	**Estimate at Completion ($)**
Synthesizer prototype and parts	$60	$60	$0	$60
Input prototype and parts	$70	$70	$0	$70
Output amplifier proto. and parts	$90	$91	$0	$91
Power supply proto. and parts	$0	$0	$0	$0
Final PCB and parts	$210	$210	$0	$210
Enclosure	$20	$21	$0	$21
Misc.	$50	$0	$0	$0
Total	$500	$452	$0	$452

Table 1: Project Budget

Table 2 shows the project schedule.

Description	Percent Complete	Date Completed
Requirements specification	100%	October 17, 2014
Development plan	100%	October 31, 2014
Synthesizer prototype built	100%	November 14, 2014
Input frontend prototype built	100%	December 1, 2014
Output amplifier prototype built	100%	December 5, 2014
Microcontroller experimentation	100%	December 16, 2014
Corrections made to prototypes	100%	February 26, 2015
Power supply design	100%	February 28, 2015
USB communications completed	100%	March 4, 2015
Final PCB layout	100%	March 14, 2015
Command parser completed	100%	March 19, 2015
Final PCB assembled	100%	April 8, 2015
Final testing	50%	—
PC software completed	95%	—
Owner's manual	75%	—

Table 2: Project Schedule

5 Future Plans

As it is, this is a solid design, and ready to be delivered. As the full board can be assembled almost entirely by automated pick-and-place, these can be delivered as a prepared package, or they could be delivered as kits with components and an assembly guide.

However, we recommend simultaneously beginning a second revision. The drawbacks mentioned in the Assessment should be corrected. Additionally, the BOM cost could be lowered in a few areas, such as replacing expensive wideband operational amplifiers with transistor amplifiers, or even possibly redesigning the synthesis subsystem to avoid using the purpose-specific DDS integrated circuit (it might be possible to use a relatively high speed FPGA, at a reduction of about half the cost).

Additionally, the PC software can be enhanced. More analysis functions can be written, and the software could be made to integrate with existing packages such as Octave.

6 References

[1] Alpha & Omega Semiconductor, "AOD417 P-Channel Enhancement Mode Field Effect Transistor," AOD417 datasheet, 2008. http://aosmd.com/pdfs/datasheet/AOD417.pdf

[2] S. W. Amos and M. James, "Sawtooth generators," in *Principles of Transistor Circuits*, 9th ed. Oxford: Newnes, 2003, ch. 14, pp. 281–292.

[3] Analog Devices, Inc., "2-Channel, 500 MSPS DDS with 10-Bit DACs," AD9958 datasheet, April 2013 [Revision B]. http://www.analog.com/media/cn/technical-documentation/data-sheets/AD9958.pdf

[4] Diodes Incorporated, "Low Dropout Linear Regulator," AZ1117C datasheet, October 2014 [Revision 3–2]. http://www.diodes.com/datasheets/AZ1117C.pdf

[5] P. Horowitz and W. Hill, "Voltage regulators and power circuits," in *The Art of Electronics*, 2nd ed. Cambridge: Cambridge, 1989, ch. 6, pp. 307–389.

[6] M/A-COM Technology, "GaAs SPST Switch," MASWSS0162 datasheet [Revision V3]. http://cdn.macom.com/DataSheets/MASWSS0162.pdf

[7] Microchip Technology, "Low Quiescent Current LDO," MCP1700 datasheet, October 2013 [Revision C]. http://ww1.microchip.com/downloads/en/DeviceDoc/20001826C.pdf

[8] ON Semiconductor, "500 mA Negative Voltage Regulators," MC79M00 series datasheet, July 2013 [Revision 15]. http://www.onsemi.com/pub_link/Collateral/MC79M00-D.PDF.

[9] STMicroelectronics, "Precision 500 mA regulators," L78M datasheet, June 2014 [Revision 20]. http://www.st.com/web/en/resource/technical/document/datasheet/CD00000447.pdf

[10] Texas Instruments, "TL43xx Precision Programmable Reference," TL431 datasheet, Aug. 2004 [Revised Jan. 2015]. http://www.ti.com/lit/ds/symlink/tl431.pdf

[11] J. Tucker, "Using a buck converter in an inverting buck-boost topology," *Analog Applications Journal*, Texas Instruments, fourth quarter 2007, pp. 16–19. http://www.ti.com/lit/an/slyt286/slyt286.pdf

A Project Requirements

3.1: Required States and Modes

This system requires the following modes:

3.1.1: Idle

The signal source and detection subsystems are inactive, and the system is waiting for commands.

3.1.2: Analysis

The system is performing a gain/phase analysis.

3.2: System Capability Requirements

3.2.1: Bode plot

The analyzer shall be able to display a plot on the operator's PC in the form of a Bode plot.

3.2.2: Test signal frequency

The analyzer shall be capable of sourcing test signals between 1 kHz and 150 MHz. (Not applicable: state WCP52-3.1.1 — idle)

3.2.3: Test signal amplitude

The analyzer shall be capable of output amplitudes up to 1.25 V RMS at frequencies up to 100 MHz. (Not applicable: state WCP52-3.1.1 — idle)

3.2.4: Sensitivity

The analyzer shall be able to detect signals down to at least 40 dB below the output amplitude. (Not applicable: state WCP52-3.1.1 — idle)

3.2.5: Extended sensitivity

The analyzer should be able to detect signals down to at least 60 dB below the output amplitude. (Not applicable: state WCP52-3.1.1 — idle)

3.2.6: Accuracy

Amplitude accuracy shall be within 3 dB, and phase accuracy within 5°.

3.2.7: Extended accuracy

Amplitude accuracy should be within 1 dB, and phase accuracy within 1°, for frequencies less than 20 MHz.

3.2.8: Interface safety

The hardware shall not be able to be damaged by its remote interface, unless an "unlock" command has been issued.

3.3: System External Interface Requirements

3.3.1: Interface

The analyzer shall interface with a PC.

3.3.2: Communications type

The analyzer should use a text-driven protocol.

3.3.3: Communications medium

The analyzer should use a common, standard communication protocol, for example, USB-CDC.

3.3.4: Panel connectors

The analyzer shall use either SMA or BNC connectors to interface to the device under test (DUT).

3.3.5: Auxiliary connector

The analyzer shall provide power via a front-panel connection for use with external DUT adapters. The voltage should be at least ± 7 V, and up to 40 mA should be available.

3.4: System Internal Interface Requirements

All internal interfaces are left to the system designers.

3.5: System Internal Data Requirements

All decisions about internal data are left to the system designers.

3.6: Other System Requirements

3.6.1: Operator's Manual

The system should include a simple operator's manual, which should include a brief Theory of Operation explaining its design, instructions for using each function, and example test setups for characterization of filters and control loops.

3.6.2: Protocol Guide

The system shall include a protocol guide, showing how to communicate with it.

3.6.3: SMT

The PCB shall be produced using surface-mount technology as much as is reasonable, without no-lead packages unless absolutely required.

3.6.4: Direct control

The interface should expose direct control of the hardware functions, allowing additional features to be implemented.

3.6.5: Electrical safety

The system shall have no voltages greater than 30 V peak-to-peak accessible externally.

3.7: Precedence and Criticality of Requirements

All requirements have equal weight.

B Test Procedures

3.1.1: Required mode: Idle

The idle state of the signal source is to be verified by viewing the signal from the "output" connector on an oscilloscope. Any signal present must be less than 5 V peak to peak.

The idle state of the detection subsystem is verified by viewing the status annunciators on the printed circuit board. The annunciator designated "sample" must not light.

3.1.2: Required mode: Analysis

This requirement is satisfied peripherally by the completion of requirement 3.2.6.

3.2.1: Bode plot

Cause the software to display any data, and verify that it is in the form of a Bode plot. This means that there should be two plots, both with a horizontal axis of 'frequency', one with a vertical axis of 'gain' in decibels, and one with a vertical axis of 'phase' in degrees.

This data can be generated by the instrument (satisfying this requirement peripherally by the completion of requirement 3.2.6), or by any other means.

3.2.2: Test signal frequency

To test this requirement, connect a patch cable between the "Output" connector and an oscilloscope with at least 150 MHz bandwidth. Either using the PC software or manual control via a serial terminal, command the instrument to generate signals with frequencies of 1 kHz, 10 MHz, 75 MHz, and 150 MHz. Using the oscilloscope's frequency display, verify that each signal's frequency is within 2.5 % of its nominal value.

3.2.3: Test signal amplitude

To test this requirement, connect a patch cable between the "Output" connector and an oscilloscope with at least 300 MHz bandwidth. Either using the PC software or manual control via a serial terminal, command the instrument to generate signals with frequencies of 1 kHz, 20 MHz, and 100 MHz, all with maximum amplitude. Using the oscilloscope's amplitude display, verify that all signals have an amplitude of at least 1.25 V RMS.

3.2.4: Sensitivity

1. Connect a patch cable between "Output" and "Input 1".
2. Command instrument to generate a signal of 100 kHz and maximum amplitude.
3. Query reported amplitude.
4. Remove patch cable, query reported amplitude. This noise floor must be at least 45 dB lower than the amplitude in step 3.
5. Reinstall patch cable with a 40 dB attenuator in series. The −40 dB signal must be visible.

3.2.5: Extended sensitivity

To test this optional requirement, perform the same test as in requirement 3.2.4, but verify that the final reported amplitude is at least 65 dB lower than the first reported amplitude.

3.2.6: Accuracy

Amplitude

Connect a pair of patch cables in series using a cable coupler, and connect this pair between the "Output" connector and the "Input 1" connector. Configure the PC software for a full sweep from 1 kHz to 150 MHz not including phase analysis. Perform normalization. Then, remove the cable coupler and insert a 50 Ω attenuator with specified attenuation between 5 dB and 15 dB and bandwidth of at least 200 MHz. Perform analysis. Verify that the reported gain is within 3 dB of the specified gain of the attenuator at all frequencies.

Phase

Connect a patch cable with length under 150 mm between "Output" and "Input 1". Configure for a sweep from 10 kHz to 25 MHz, normalize. Using an SMA coupler, add a patch cable made from 1 m of RG-316 coaxial cable in series. This cable is expected to exhibit the following phase shift due to propagation delay:

Frequency	Phase shift
10 kHz	0.02°
1 MHz	1.74°
10 MHz	17.4°
25 MHz	43.5°

Ensure that the propagation delay reported is within 5° of this at these frequencies.

3.2.7: Extended accuracy

To test this optional requirement, perform the test for requirement 3.2.6, with the following modifications: the upper sweep limit should be 20 MHz, reported gain must be within 1 dB of the specified attenuator gain, and phase shift must be within 1° of zero (above −1° and below +1°) at all frequencies.

3.2.8: Interface safety

To test this requirement, use the interface control commands to attempt to set a GPIO pin which serves as a signal input to be an output instead. The system must respond with an error.

3.3.1: Interface

This requirement is satisfied peripherally by the completion of requirements 3.2.1 through 3.2.8, which all required PC interfacing to complete.

3.3.2: Communications type

To test this requirement, connect the instrument to a PC. Connect a serial terminal application to it, and perform at least one command that produces a response. Demonstrate that the command and response comprise displayable text symbols.

3.3.3: Communications medium

This requirement is demonstrated peripherally as part of demonstrating requirement 3.3.2: the ability for a standard serial console to talk to the instrument demonstrates that the instrument was using a standard protocol.

3.3.4: Panel connectors

To test this requirement, observe the front panel of the device, and see that the RF connectors are either SMA or BNC.

3.3.5: Auxiliary connector

Using a multimeter, measure all pins on the "Auxiliary" connector, verifying that there are power supply pins with a voltage present of at least $+7$ V and -7 V. -7 V. Then, switch the multimeter to ammeter mode, and connect in series a selected resistor. Probe these pins again, and verify that at least 40 mA is supplied.

The resistor is to be selected such that it will draw at least 40 mA at the voltage that was measured on the connectors. This resistance may depend on the actual voltage that was present, which is allowed to be *above* the required ± 7 V.

3.6.1: Operator's Manual

Demonstrate the existence of a manual in digital format, containing at least the following sections: Theory of Operation, Operational Instructions. Demonstrate that there exist example test setups for characterization of filters and of control loops.

3.6.2: Protocol Guide

Demonstrate the existence of documentation explaining the protocol with which a PC communicates with the instrument. This documentation may be part of the Operator's Manual, or it may be separate.

3.6.3: SMT

Demonstrate that the parts on the PCB are surface-mount devices, with the following allowed exceptions:

- Connectors: through-hole connections have higher mechanical stability
- Inductors and capacitors larger than 5 mm in diameter: through-hole parts have higher mechanical stability

Demonstrate that the only leadless devices on the PCB are essential for its function. This may be a result of directly satisfying an above requirement. An anticipated example is device U3, an Analog Devices AD9958BCPZ digital frequency synthesizer, which directly satisfies requirement 3.2.2 (test signal frequency between 1 kHz and 150 MHz).

3.6.4: Direct control

Viewing the protocol guide, demonstrate the existence of:

- A command to set the output value of an arbitrary GPIO pin.
- A command to query the input value of an arbitrary GPIO pin.
- A command to transmit arbitrary data via the on-board SPI interface.
- A command to query the direct output value of the analog-to-digital converter.

3.6.5: Electrical safety

To test this requirement, connect the “common” input of a multimeter to the instrument ground, and verify that no signals on the “Auxiliary” connector are more positive than 15 V or more negative than −15 V. Then, connect a patch cable between the “Output” connector and an oscilloscope. Do not terminate the end. Command the instrument to generate a frequency of 100 kHz and maximum amplitude. Using the oscilloscope’s amplitude display, verify that the positive and negative peaks are no more positive than 15 V and no more negative than −15 V.

C Computer Code

```
10 PRINT "HELLO WORLD"
20 GOTO 10
```

D CAD Drawings