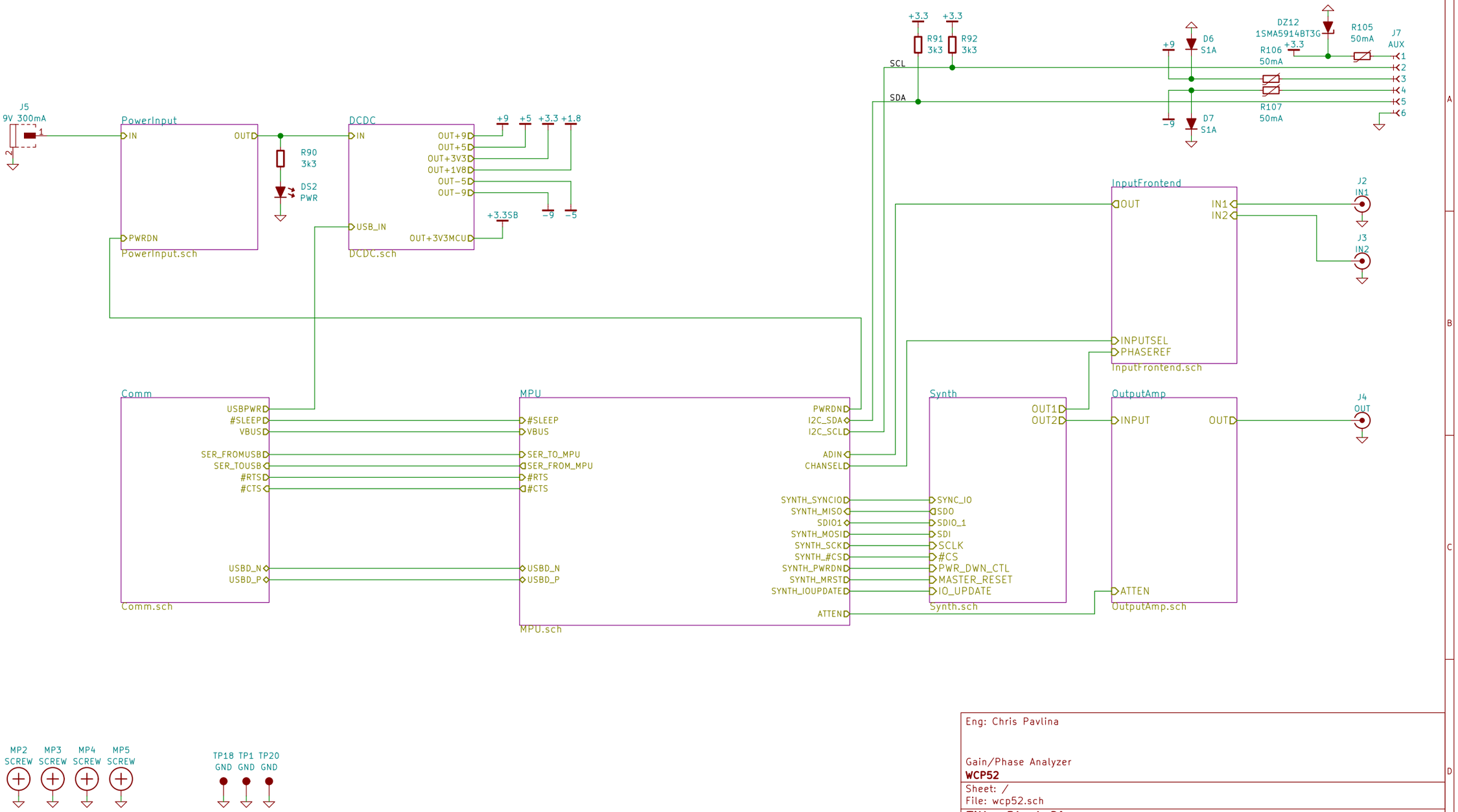
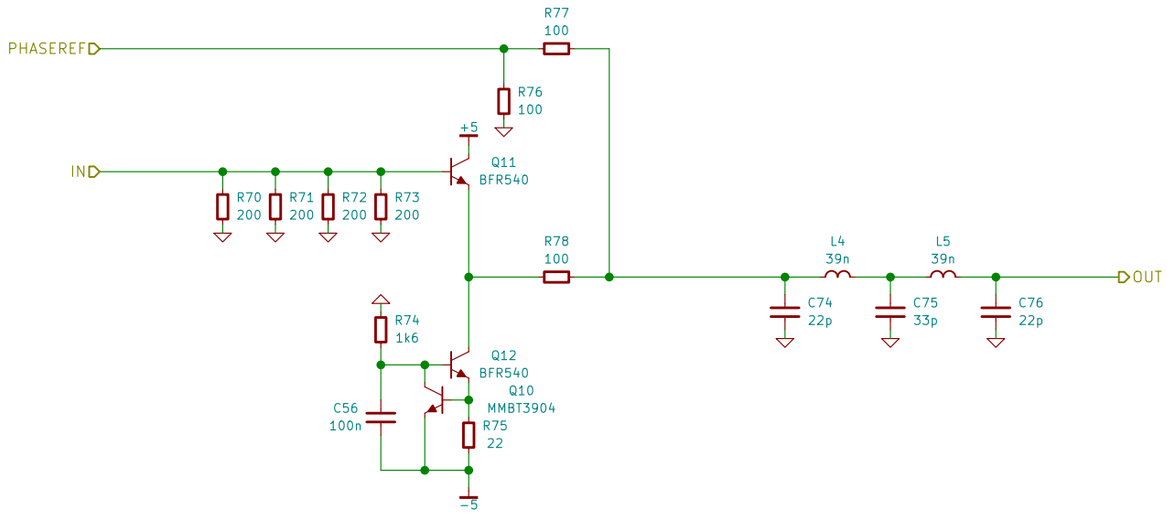
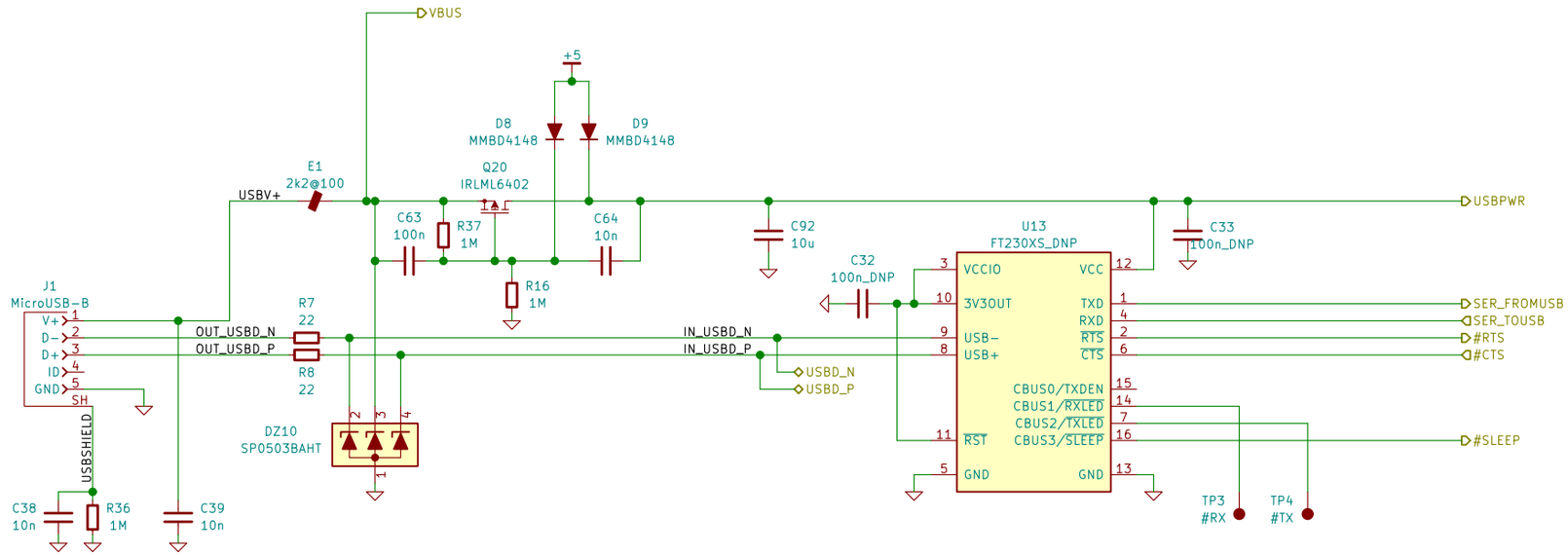


Eng: Chris Pavlina	
Gain/Phase Analyzer	
WCP52	
Sheet: /	
File: wcp52.sch	
Title: Block Diagram	
Size: USLegal	Date: 2015-03-10
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 1/13

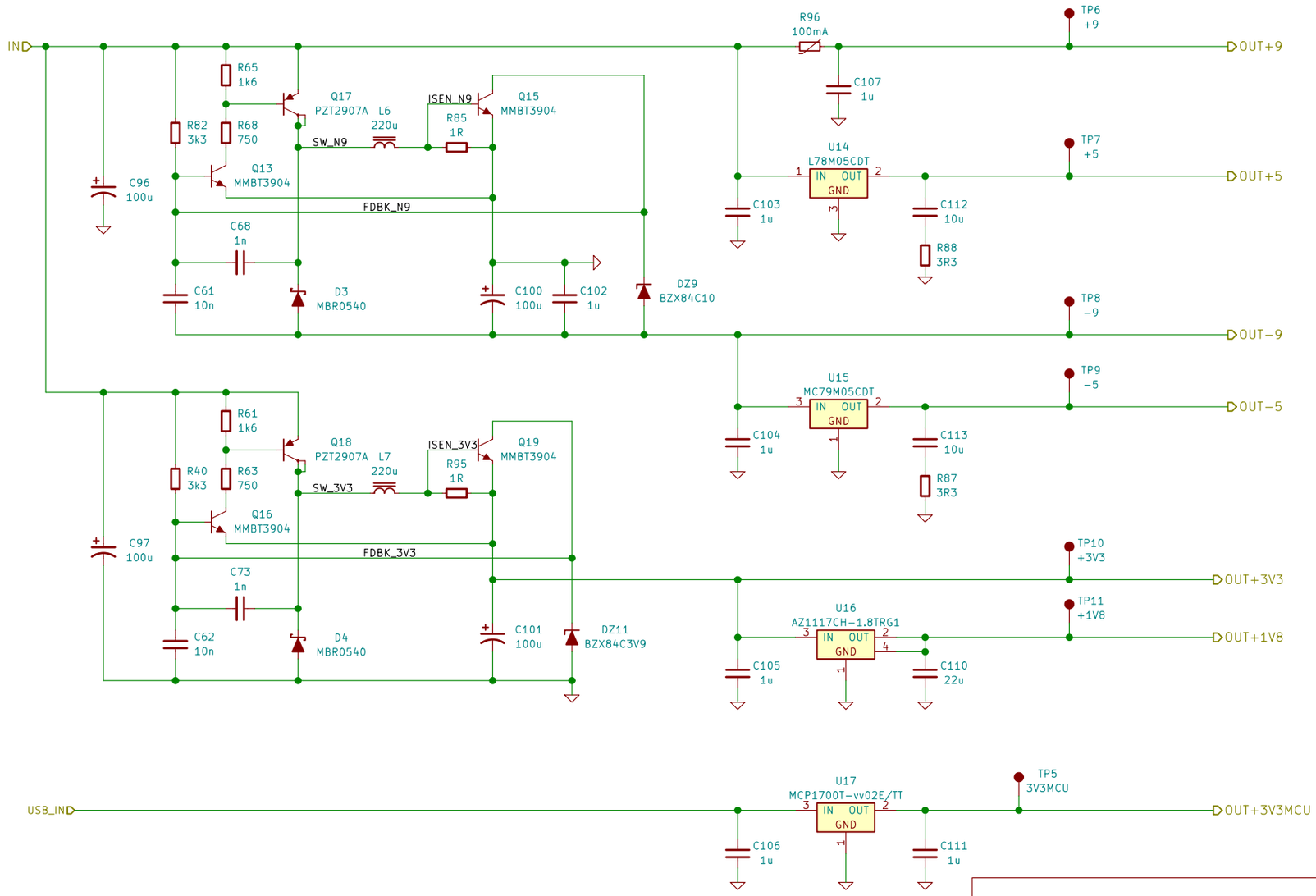


Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/Buffer_Filter/ File: Buffer_Filter.sch	
Title: Input Buffer and Filter	
Size: USLegal	Date: 2015-03-10
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 9/13

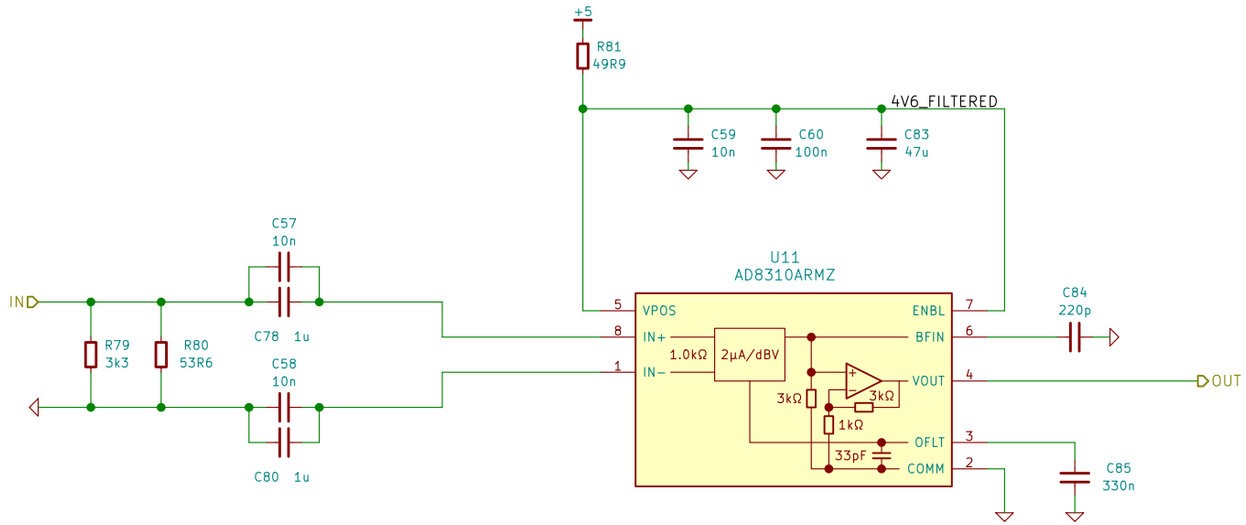
Rev:



Eng: Chris Pavlina		
Gain/Phase Analyzer **WCP52**		
Sheet: /Comm/ File: Comm.sch		
Title:		
Size: USLegal	Date: 2015-03-10	**Rev:**
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product		Id: 2/13

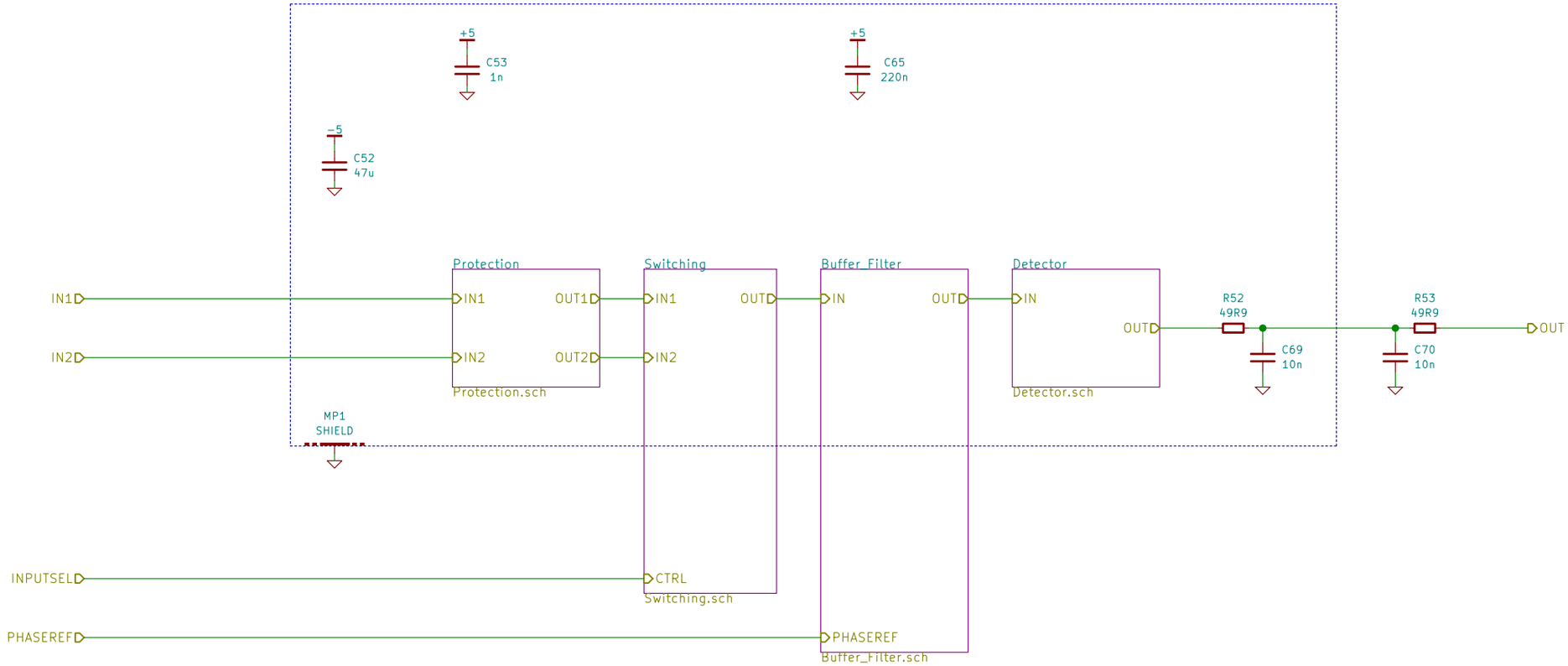


Sheet: /DCDC/	
File: DCDC.sch	
Title:	
Size: USLegal	Date: 2015-03-10
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 12/13

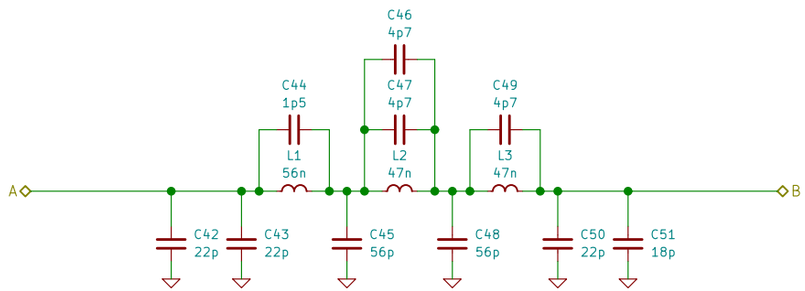


Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/Detector/ File: Detector.sch	
Title: Logarithmic Detector	
Size: USLegal	Date: 2015-03-10
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 10/13

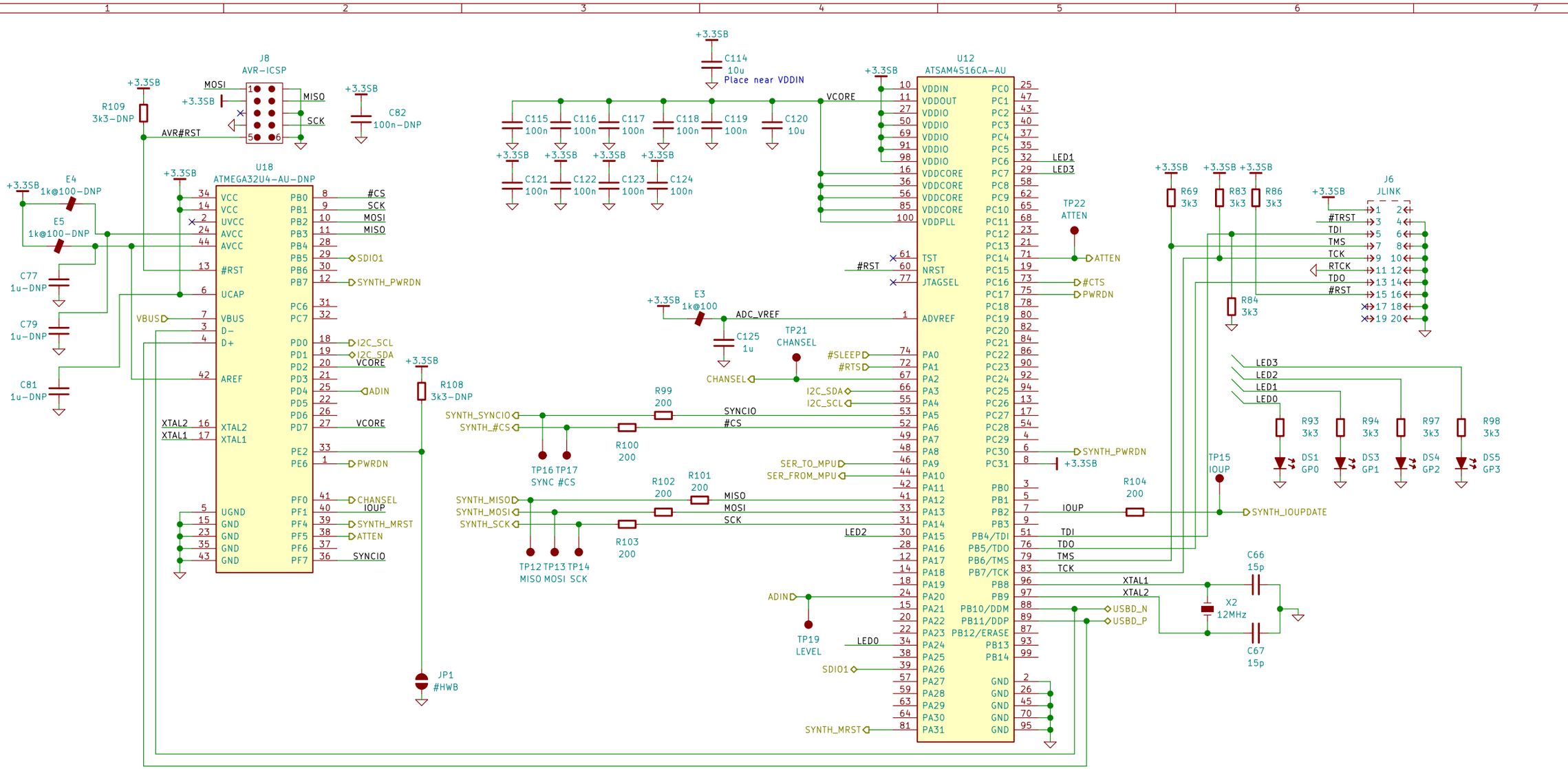
Rev:



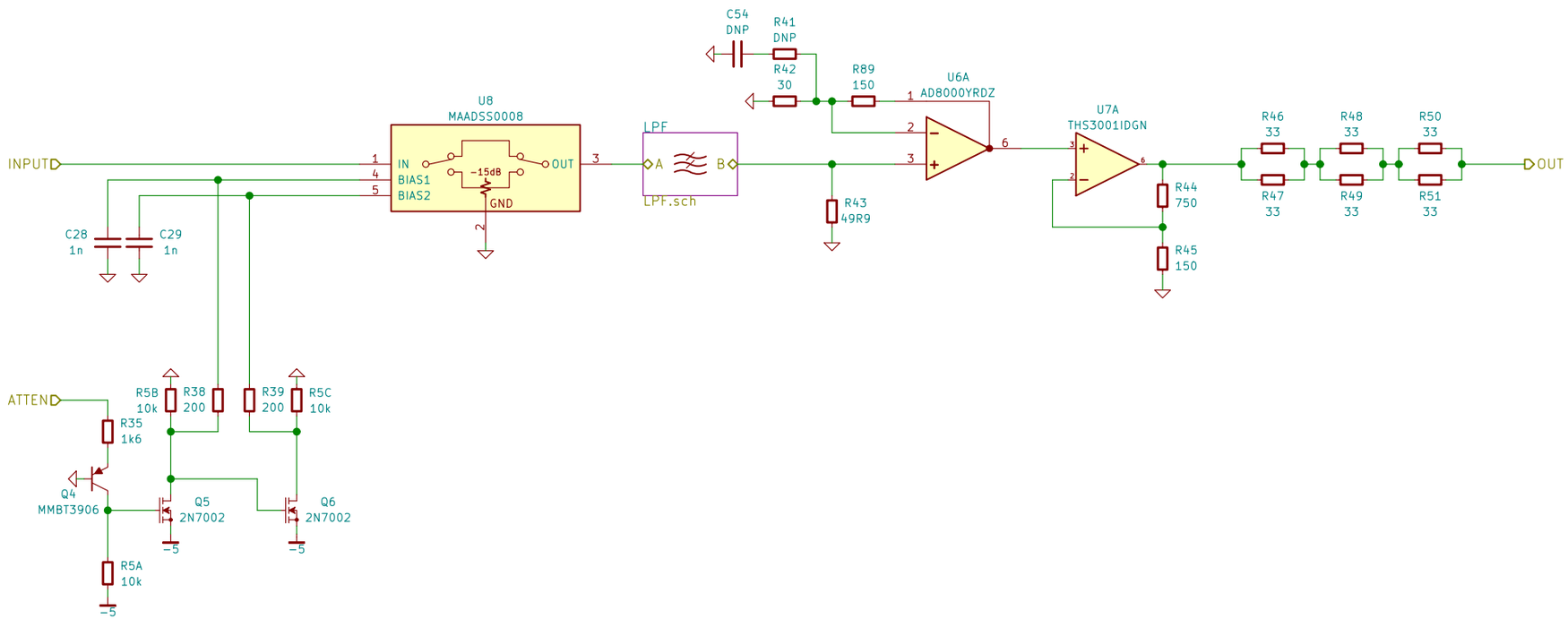
Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/ File: InputFrontend.sch	
Title: Input Frontend	
Size: USLegal	Date: 2015-03-10
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 6/13
	Rev:

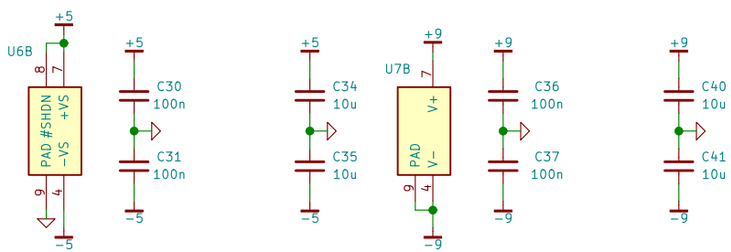


Eng: Chris Pavlina		
Gain/Phase Analyzer **WCP52**		
Sheet: /OutputAmp/LPF/ File: LPF.sch		
Title: LPF for Output Amplifier		
Size: USLegal	Date: 2015-03-10	**Rev:**
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product		Id: 5/13

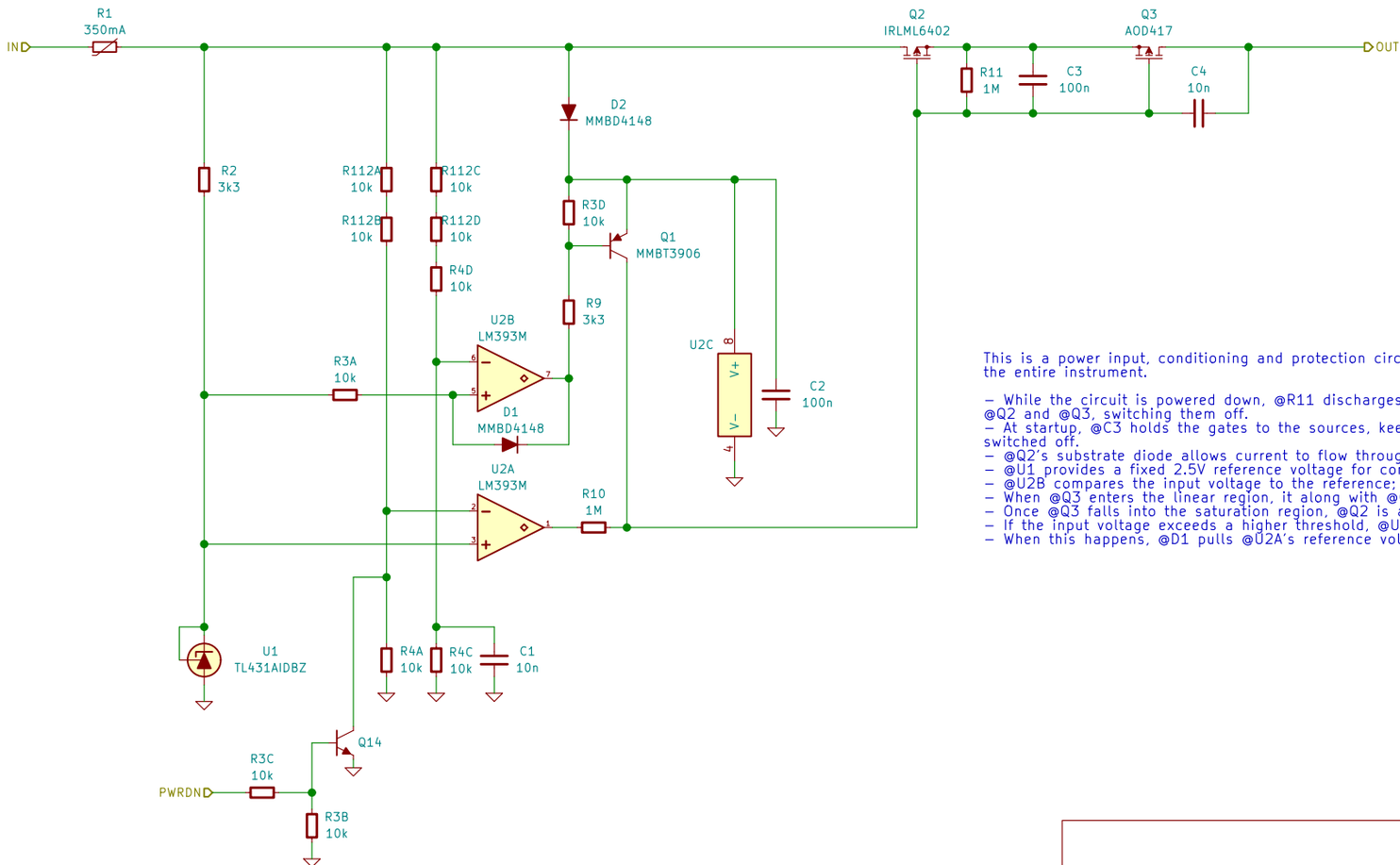


Eng: Chris Pavlina	
Gain/Phase Analyzer	
WCP52	
Sheet: /MPU/	
File: MPU.sch	
Title: MPU	
Size: USLegal	Date: 2015-03-10
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 13/13


INPUT
U8
MAADSS0008
IN
BIAS1
BIAS2
-15dB
OUT
GND
C28
1n
C29
1n
LPF
A
B
LPF.sch
C54
DNP
R41
DNP
R42
30
R89
150
U6A
AD8000YRDZ
R43
49R9
U7A
THS3001IDGN
R44
750
R45
150
R46
33
R47
33
R48
33
R49
33
R50
33
R51
33
OUT
ATTEN
R35
1k6
R5B
10k
R38
200
R39
200
R5C
10k
Q4
MMBT3906
Q5
2N7002
Q6
2N7002
R5A
10k



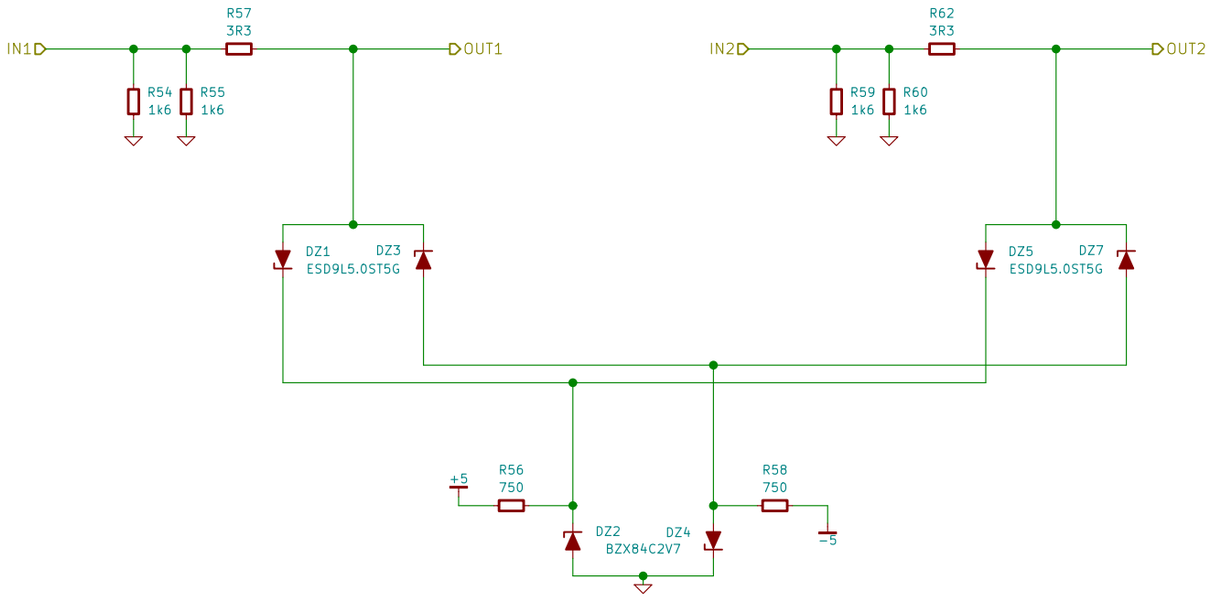
Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /OutputAmp/ File: OutputAmp.sch	
Title: Output Amplifier	
Size: USLegal — Date: 2015-03-10	**Rev:**
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 4/13



This is a power input, conditioning and protection circuit for the entire instrument.

- While the circuit is powered down, @R11 discharges the gates of @Q2 and @Q3, switching them off.
- At startup, @C3 holds the gates to the sources, keeping them switched off.
- @Q2's substrate diode allows current to flow through despite the FET being switched off, but @Q3's diode fa
- @U1 provides a fixed 2.5V reference voltage for comparison.
- @U2B compares the input voltage to the reference; when it exceeds a threshold, the output falls to 0V and b
- When @Q3 enters the linear region, it along with @C4 forms a circuit known as a Miller integrator, integratin
- Once @Q3 falls into the saturation region, @Q2 is also in this region, bypassing its substrate diode and prov
- If the input voltage exceeds a higher threshold, @U2A switches on. This saturates @Q1, yanking the gates of
- When this happens, @D1 pulls @U2A's reference voltage down, latching the circuit in this position. It will not

Sheet: /PowerInput/ File: PowerInput.sch		
Title:		
Size: USLegal	Date: 2015-03-10	**Rev:**
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product		Id: 11/13



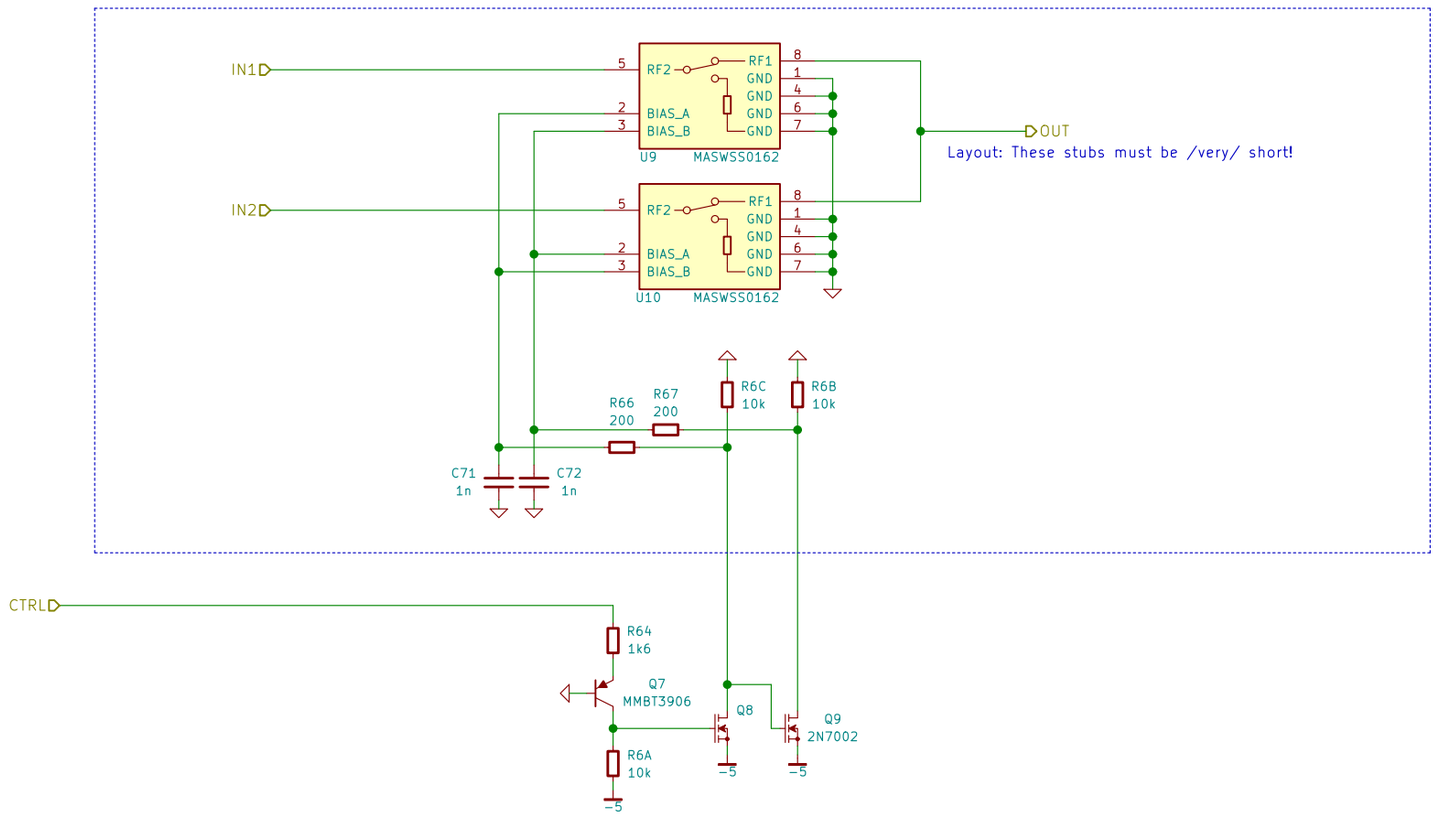
Eng: Chris Pavlina

Gain/Phase Analyzer
WCP52

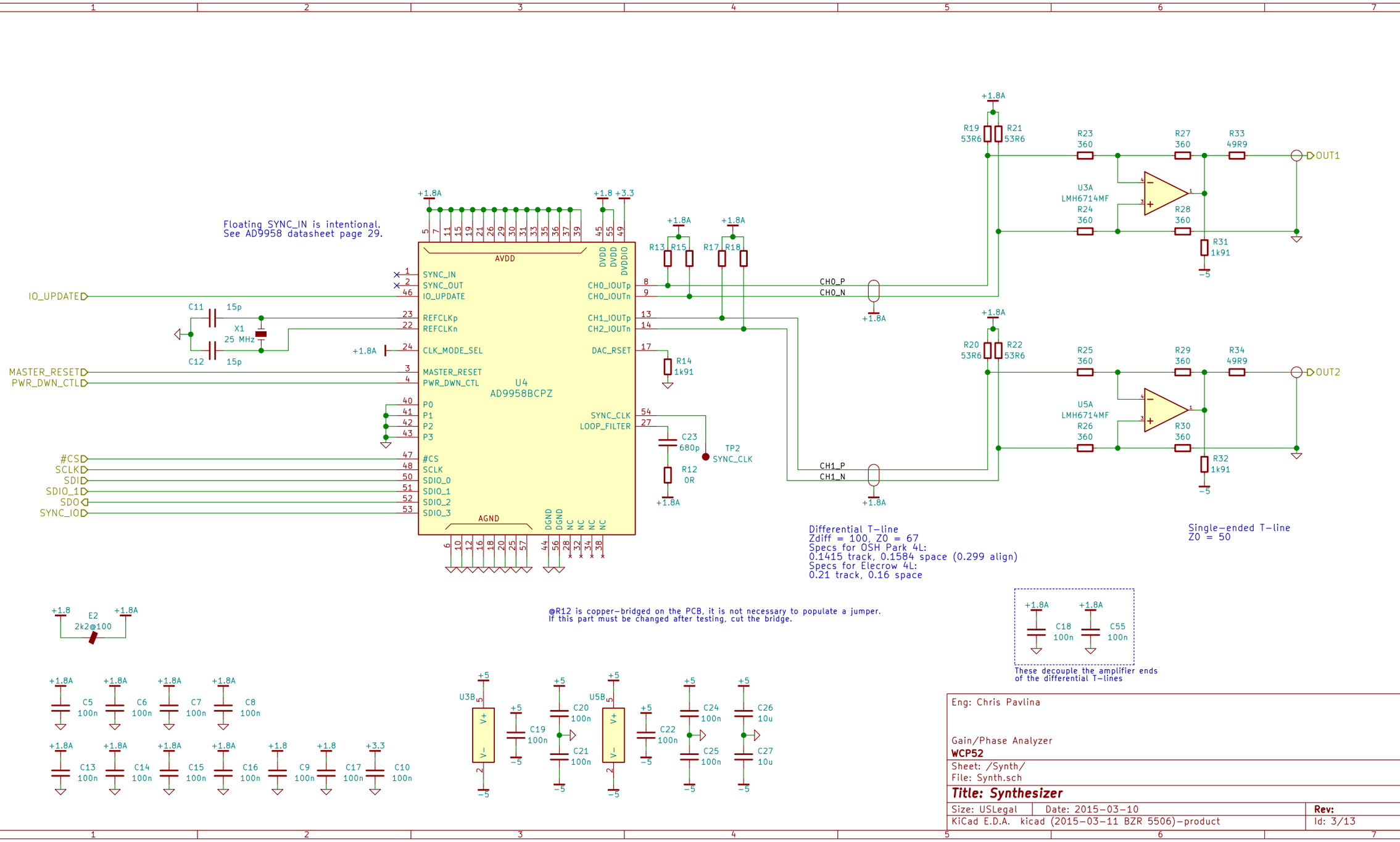
Sheet: /InputFrontend/Protection/
File: Protection.sch

Title: Input Protection

Size: USLegal	Date: 2015-03-10	**Rev:**
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product		Id: 7/13



Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/Switching/ File: Switching.sch	
Title: Input Switching	
Size: USLegal | Date: 2015-03-10	**Rev:**
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product	Id: 8/13


Floating SYNC_IN is intentional.
See AD9958 datasheet page 29.
U4
AD9958BCPZ
AVDD
DVDD
DVDDIO
AGND
DGND
NC
SYNC_IN
SYNC_OUT
IO_UPDATE
REFCLKp
REFCLKn
CLK_MODE_SEL
MASTER_RESET
PWR_DWN_CTL
P0
P1
P2
P3
#CS
SCLK
SDIO_0
SDIO_1
SDIO_2
SDIO_3
CH0_IOUTp
CH0_IOUTn
CH1_IOUTp
CH2_IOUTn
DAC_RSET
SYNC_CLK
LOOP_FILTER
IO_UPDATE
MASTER_RESET
PWR_DWN_CTL
#CS
SCLK
SDI
SDIO_1
SDO
SYNC_IO
X1
25 MHz
C11 15p
C12 15p
R14 1k91
R12 0R
C23 680p
TP2
SYNC_CLK
CH0_P
CH0_N
CH1_P
CH1_N
U3A
LMH6714MF
U5A
LMH6714MF
R19 53R6
R21 53R6
R20 53R6
R22 53R6
R23 360
R24 360
R25 360
R26 360
R27 360
R28 360
R29 360
R30 360
R33 49R9
R34 49R9
R31 1k91
R32 1k91
OUT1
OUT2
Differential T-line
Zdiff = 100, Z0 = 67
Specs for OSH Park 4L:
0.1415 track, 0.1584 space (0.299 align)
Specs for Elecrow 4L:
0.21 track, 0.16 space
Single-ended T-line
Z0 = 50
@R12 is copper-bridged on the PCB, it is not necessary to populate a jumper.
If this part must be changed after testing, cut the bridge.
E2
2k2@100
C18 100n
C55 100n
These decouple the amplifier ends
of the differential T-lines
C5 100n
C6 100n
C7 100n
C8 100n
C13 100n
C14 100n
C15 100n
C16 100n
C9 100n
C17 100n
C10 100n
U3B
C19 100n
C20 100n
C21 100n
U5B
C22 100n
C24 100n
C25 100n
C26 10u
C27 10u
Eng: Chris Pavlina
Gain/Phase Analyzer
WCP52
Sheet: /Synth/
File: Synth.sch
Title: Synthesizer
Size: USLegal
Date: 2015-03-10
Rev:
KiCad E.D.A. kicad (2015-03-11 BZR 5506)-product
Id: 3/13