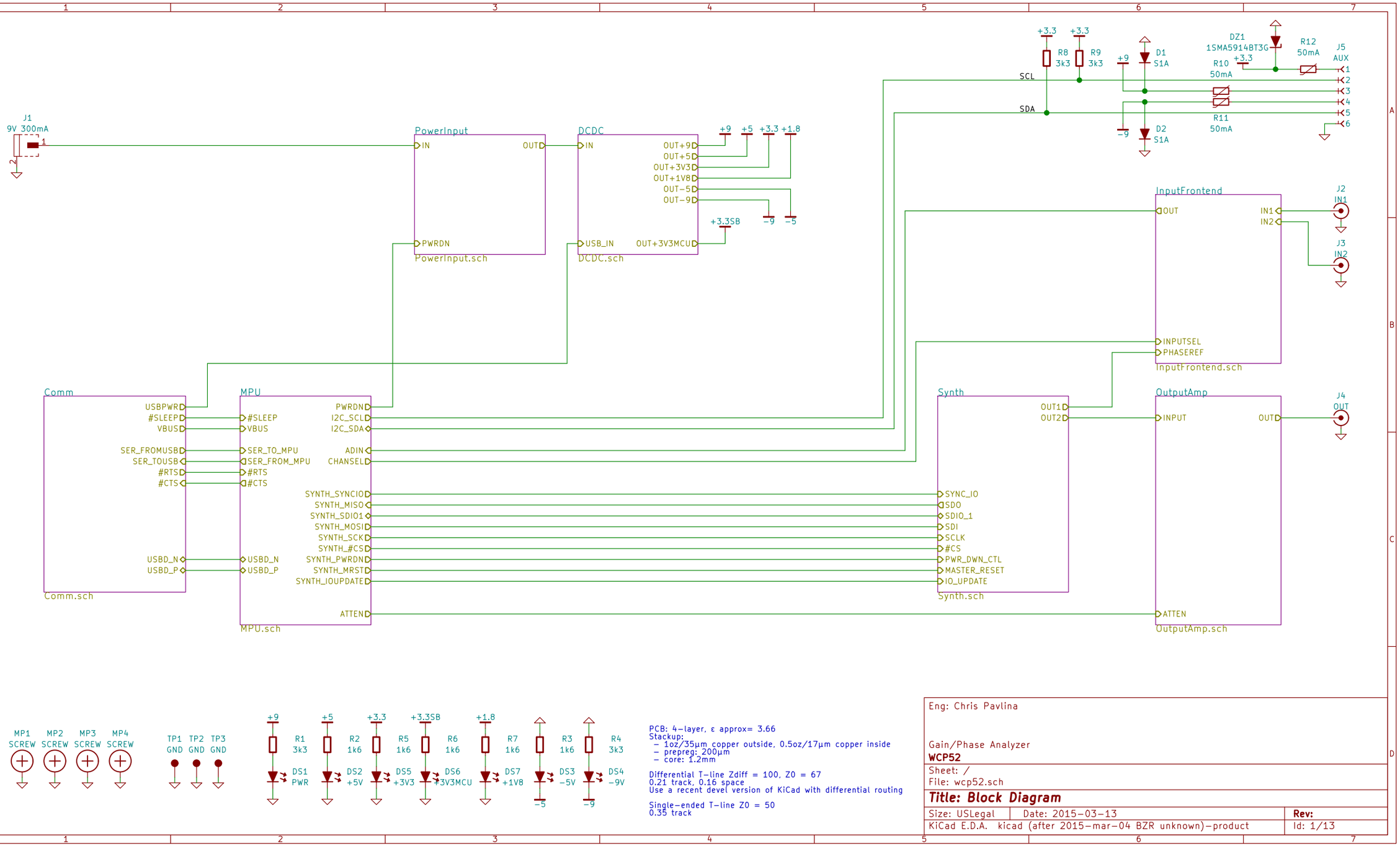
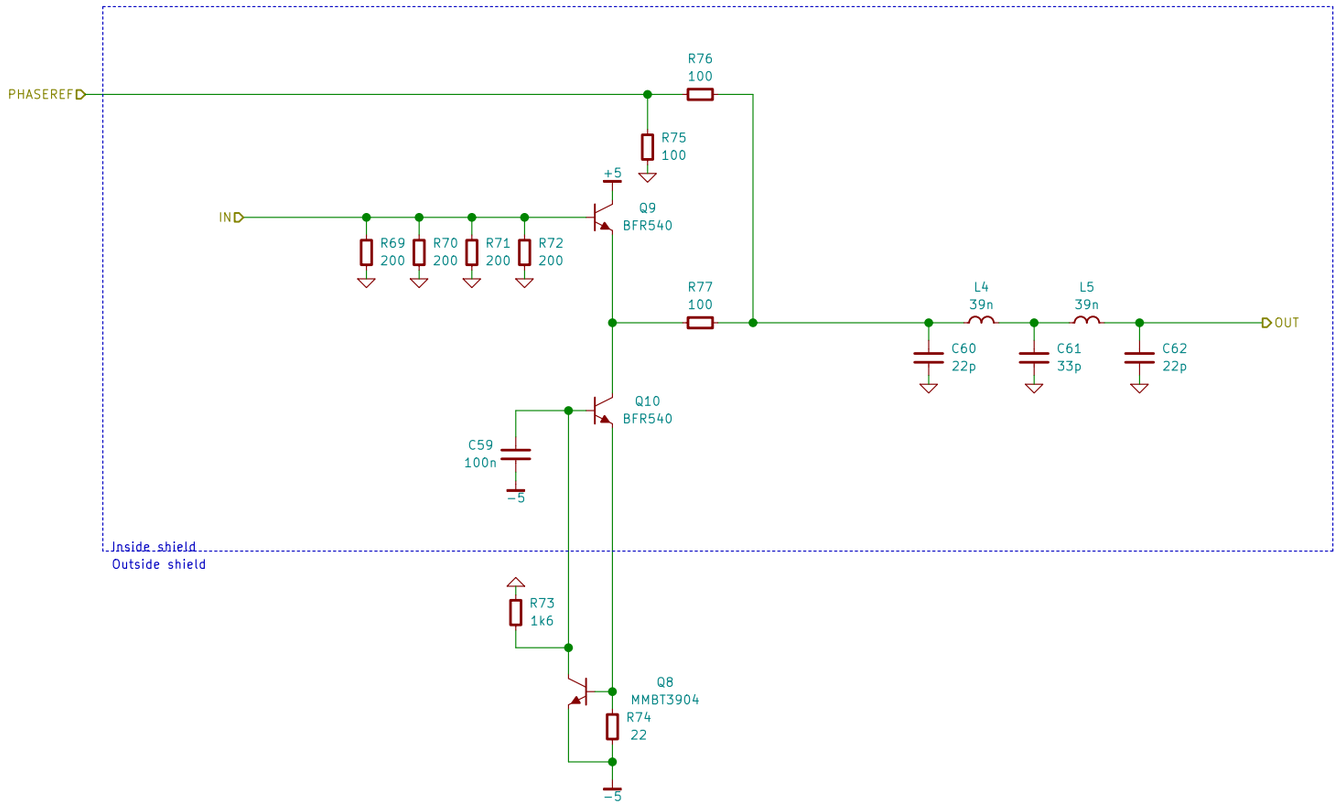
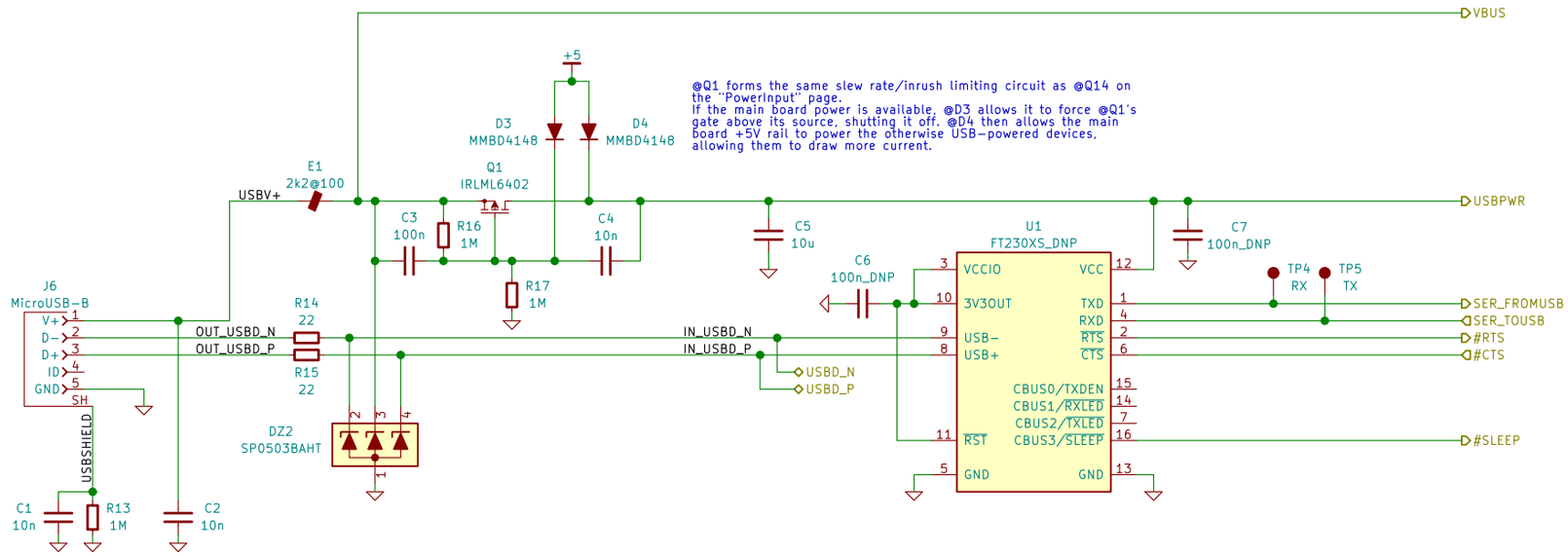
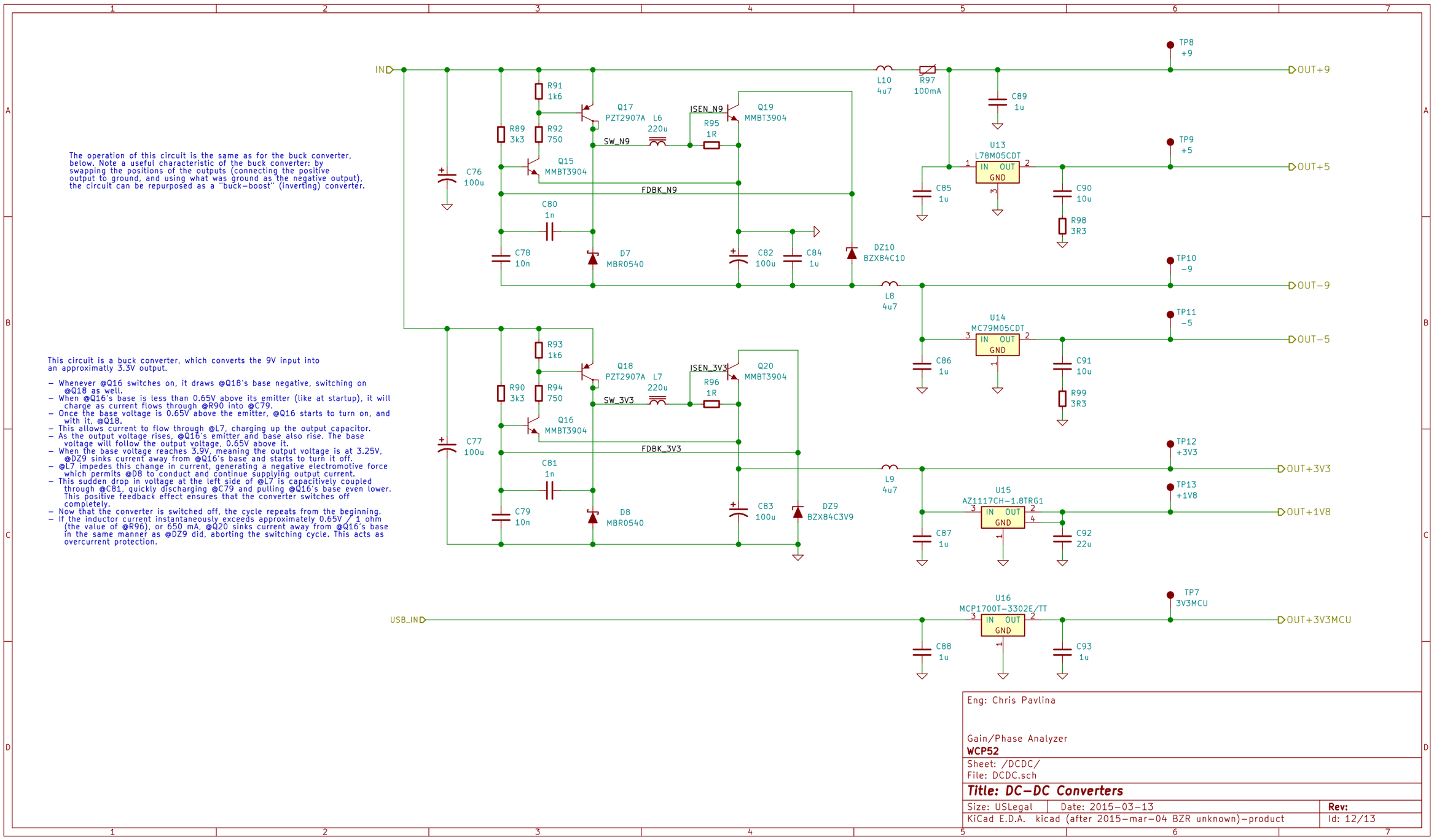

J1
9V 300mA
PowerInput
IN
OUT
PWRDN
PowerInput.sch
DCDC
IN
OUT+9
OUT+5
OUT+3V3
OUT+1V8
OUT-5
OUT-9
USB_IN
OUT+3V3MCU
DCDC.sch
+9
+5
+3.3
+1.8
+3.3SB
-9
-5
+3.3
R8 3k3
R9 3k3
SCL
SDA
D1 S1A
D2 S1A
DZ1 1SMA5914BT3G
R12 50mA
R10 50mA
R11 50mA
J5 AUX
InputFrontend
OUT
IN1
IN2
INPUTSEL
PHASEREF
InputFrontend.sch
J2 IN1
J3 IN2
Comm
USBPWR
#SLEEP
VBUS
SER_FROMUSB
SER_TOUSB
#RTS
#CTS
USBD_N
USBD_P
Comm.sch
MPU
#SLEEP
VBUS
SER_TO_MPU
SER_FROM_MPU
#RTS
#CTS
USBD_N
USBD_P
PWRDN
I2C_SCL
I2C_SDA
ADIN
CHANSEL
SYNTH_SYNCIO
SYNTH_MISO
SYNTH_SDIO1
SYNTH_MOSI
SYNTH_SCK
SYNTH_#CS
SYNTH_PWRDN
SYNTH_MRST
SYNTH_IOUPDATE
ATTEN
MPU.sch
Synth
OUT1
OUT2
SYNC_IO
SDO
SDIO_1
SDI
SCLK
#CS
PWR_DWN_CTL
MASTER_RESET
IO_UPDATE
Synth.sch
OutputAmp
INPUT
OUT
ATTEN
OutputAmp.sch
J4 OUT
MP1 SCREW
MP2 SCREW
MP3 SCREW
MP4 SCREW
TP1 GND
TP2 GND
TP3 GND
R1 3k3
DS1 PWR
R2 1k6
DS2 +5V
R5 1k6
DS5 +3V3
R6 1k6
DS6 +3V3MCU
R7 1k6
DS7 +1V8
R3 1k6
DS3 -5V
R4 3k3
DS4 -9V
PCB: 4-layer, ε approx= 3.66
Stackup:
- 1oz/35µm copper outside, 0.5oz/17µm copper inside
- prepreg: 200µm
- core: 1.2mm
Differential T-line Zdiff = 100, Z0 = 67
0.21 track, 0.16 space
Use a recent devel version of KiCad with differential routing
Single-ended T-line Z0 = 50
0.35 track
Eng: Chris Pavlina
Gain/Phase Analyzer
WCP52
Sheet: /
File: wcp52.sch
Title: Block Diagram
Size: USLegal
Date: 2015-03-13
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 1/13

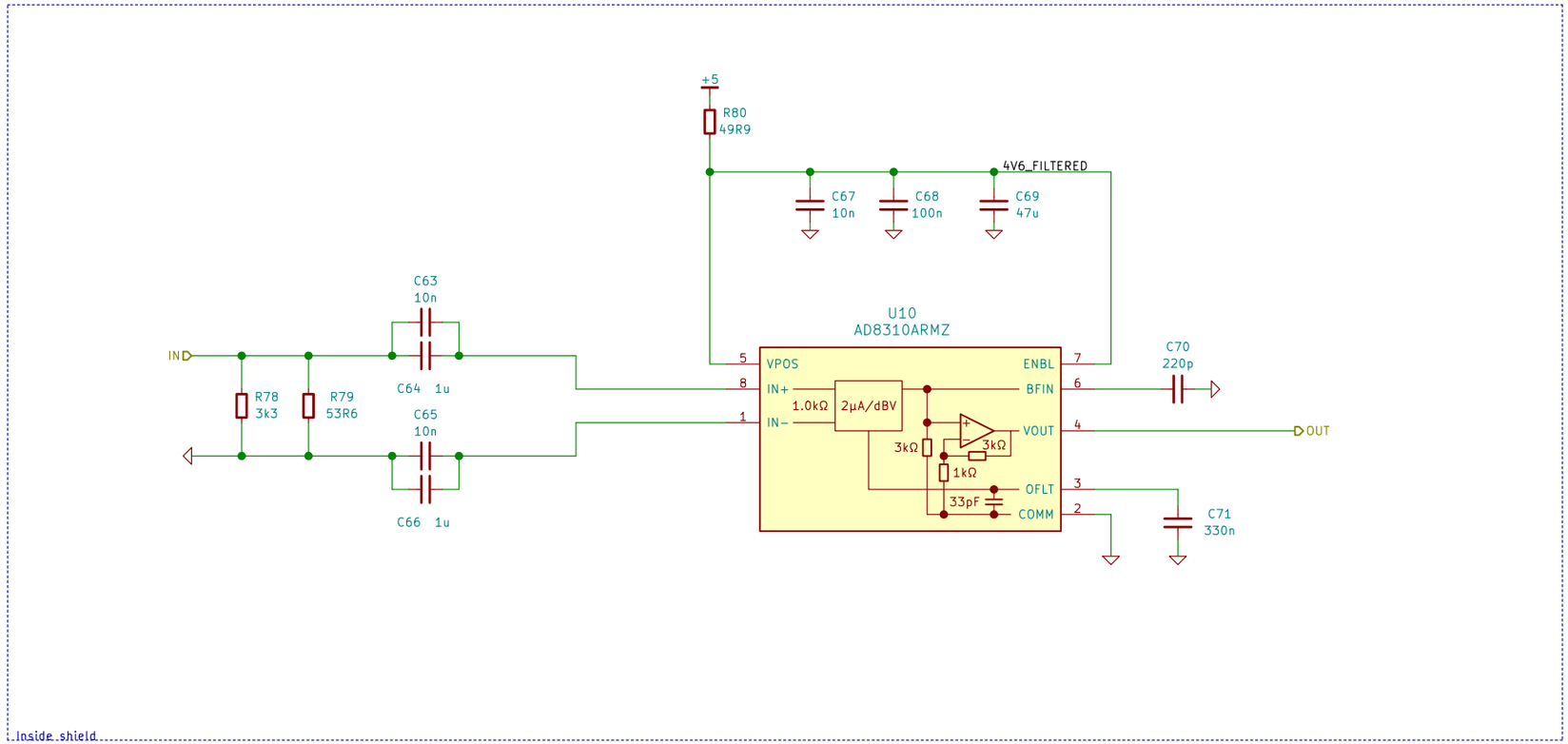


Eng: Chris Pavlina		
Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/Buffer_Filter/ File: Buffer_Filter.sch		
Title: Input Buffer and Filter		
Size: USLegal	Date: 2015-03-13	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 9/13

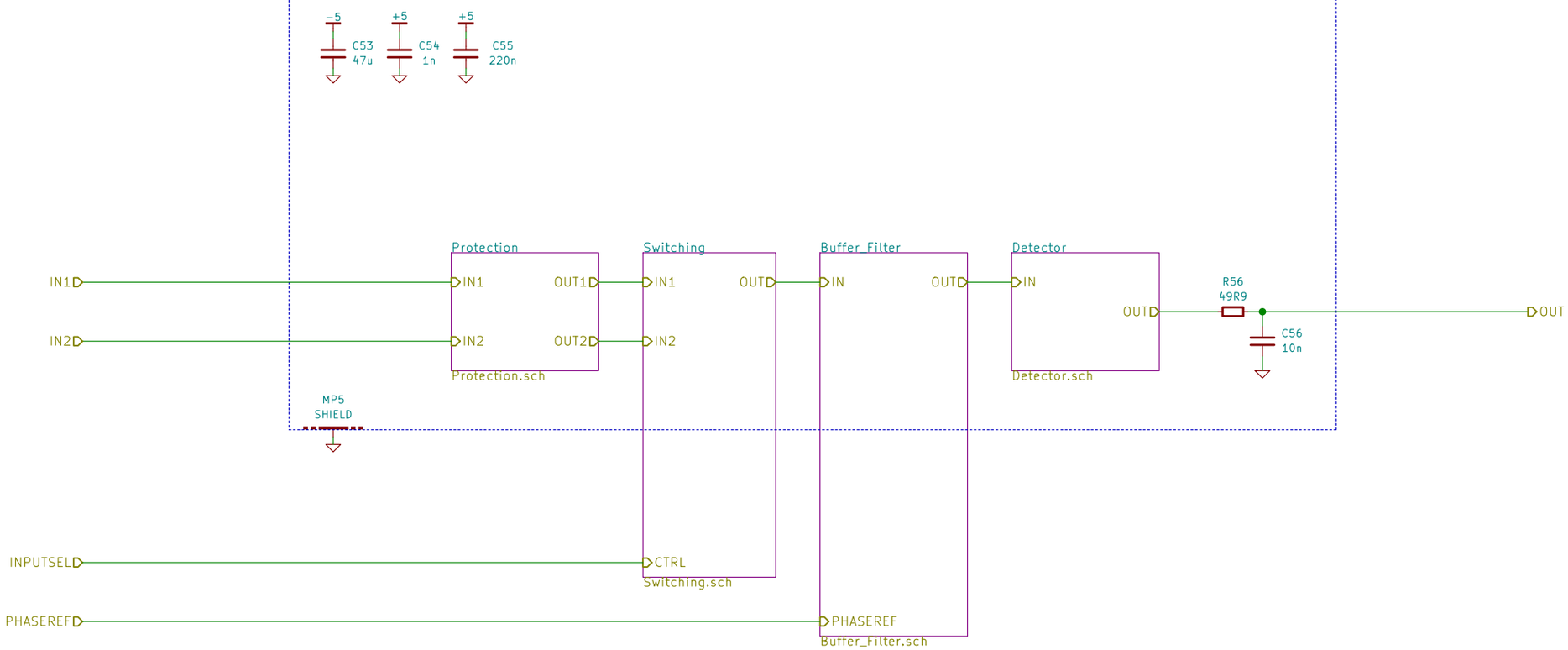


Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /Comm/ File: Comm.sch	
Title: USB Communications	
Size: USLegal | Date: 2015-03-13	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 2/13


The operation of this circuit is the same as for the buck converter, below. Note a useful characteristic of the buck converter: by swapping the positions of the outputs (connecting the positive output to ground, and using what was ground as the negative output), the circuit can be repurposed as a "buck-boost" (inverting) converter.
This circuit is a buck converter, which converts the 9V input into an approximatly 3.3V output.
– Whenever @Q16 switches on, it draws @Q18's base negative, switching on @Q18 as well.
– When @Q16's base is less than 0.65V above its emitter (like at startup), it will charge as current flows through @R90 into @C79.
– Once the base voltage is 0.65V above the emitter, @Q16 starts to turn on, and with it, @Q18.
– This allows current to flow through @L7, charging up the output capacitor.
– As the output voltage rises, @Q16's emitter and base also rise. The base voltage will follow the output voltage, 0.65V above it.
– When the base voltage reaches 3.9V, meaning the output voltage is at 3.25V, @DZ9 sinks current away from @Q16's base and starts to turn it off.
– @L7 impedes this change in current, generating a negative electromotive force which permits @D8 to conduct and continue supplying output current.
– This sudden drop in voltage at the left side of @L7 is capacitively coupled through @C81, quickly discharging @C79 and pulling @Q16's base even lower. This positive feedback effect ensures that the converter switches off completely.
– Now that the converter is switched off, the cycle repeats from the beginning.
– If the inductor current instantaneously exceeds approximately 0.65V / 1 ohm (the value of @R96), or 650 mA, @Q20 sinks current away from @Q16's base in the same manner as @DZ9 did, aborting the switching cycle. This acts as overcurrent protection.
IN
USB_IN
L10 4u7
R97 100mA
L8 4u7
L9 4u7
R91 1k6
R89 3k3
R92 750
Q17 PZT2907A
L6 220u
Q15 MMBT3904
ISEN_N9
Q19 MMBT3904
R95 1R
SW_N9
FDBK_N9
C76 100u
C80 1n
C78 10n
D7 MBR0540
C82 100u
C84 1u
DZ10 BZX84C10
R93 1k6
R90 3k3
R94 750
Q18 PZT2907A
L7 220u
Q16 MMBT3904
ISEN_3V3
Q20 MMBT3904
R96 1R
SW_3V3
FDBK_3V3
C77 100u
C81 1n
C79 10n
D8 MBR0540
C83 100u
DZ9 BZX84C3V9
C89 1u
U13 L78M05CDT
IN OUT GND
C85 1u
C90 10u
R98 3R3
U14 MC79M05CDT
C86 1u
C91 10u
R99 3R3
U15 AZ1117CH-1.8TRG1
C87 1u
C92 22u
U16 MCP1700T-3302E/TT
C88 1u
C93 1u
TP8 +9
TP9 +5
TP10 -9
TP11 -5
TP12 +3V3
TP13 +1V8
TP7 3V3MCU
OUT+9
OUT+5
OUT-9
OUT-5
OUT+3V3
OUT+1V8
OUT+3V3MCU
Eng: Chris Pavlina
Gain/Phase Analyzer
WCP52
Sheet: /DCDC/
File: DCDC.sch
Title: DC-DC Converters
Size: USLegal
Date: 2015-03-13
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 12/13

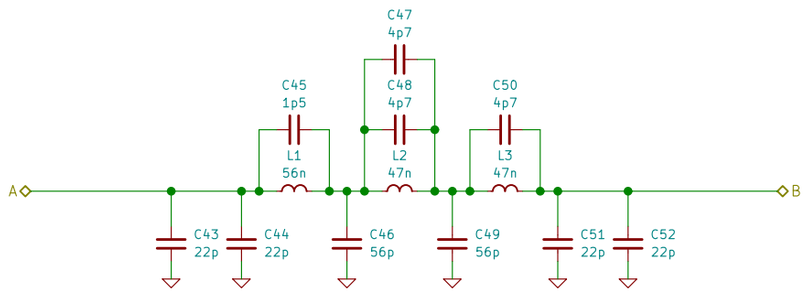


Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/Detector/ File: Detector.sch	
Title: Logarithmic Detector	
Size: USLegal	Date: 2015-03-13
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 10/13

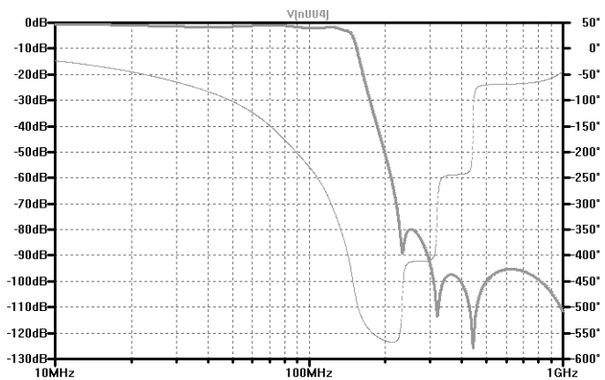


Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/ File: InputFrontend.sch	
Title: Input Frontend	
Size: USLegal	Date: 2015-03-13
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 6/13

Rev:

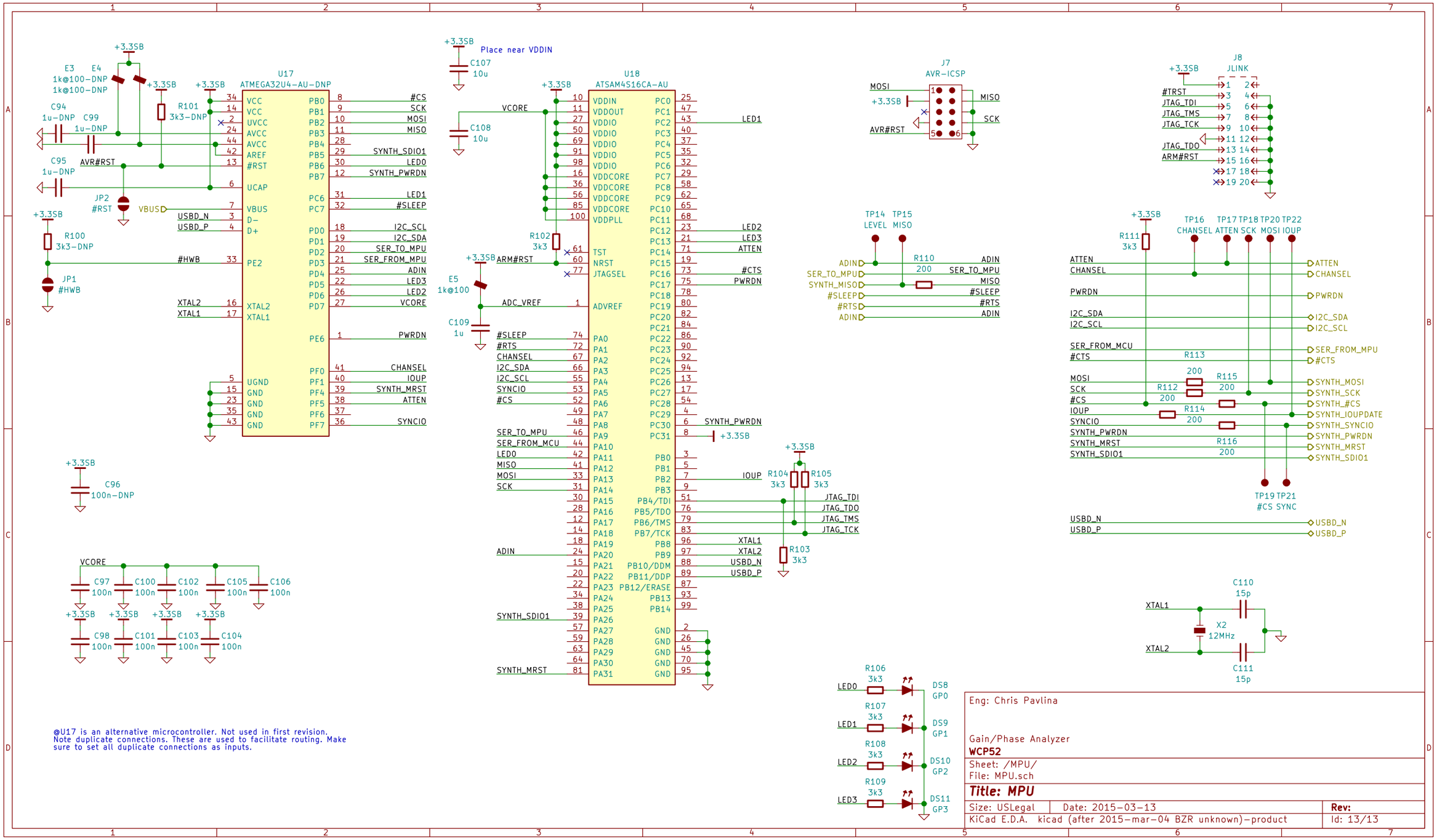


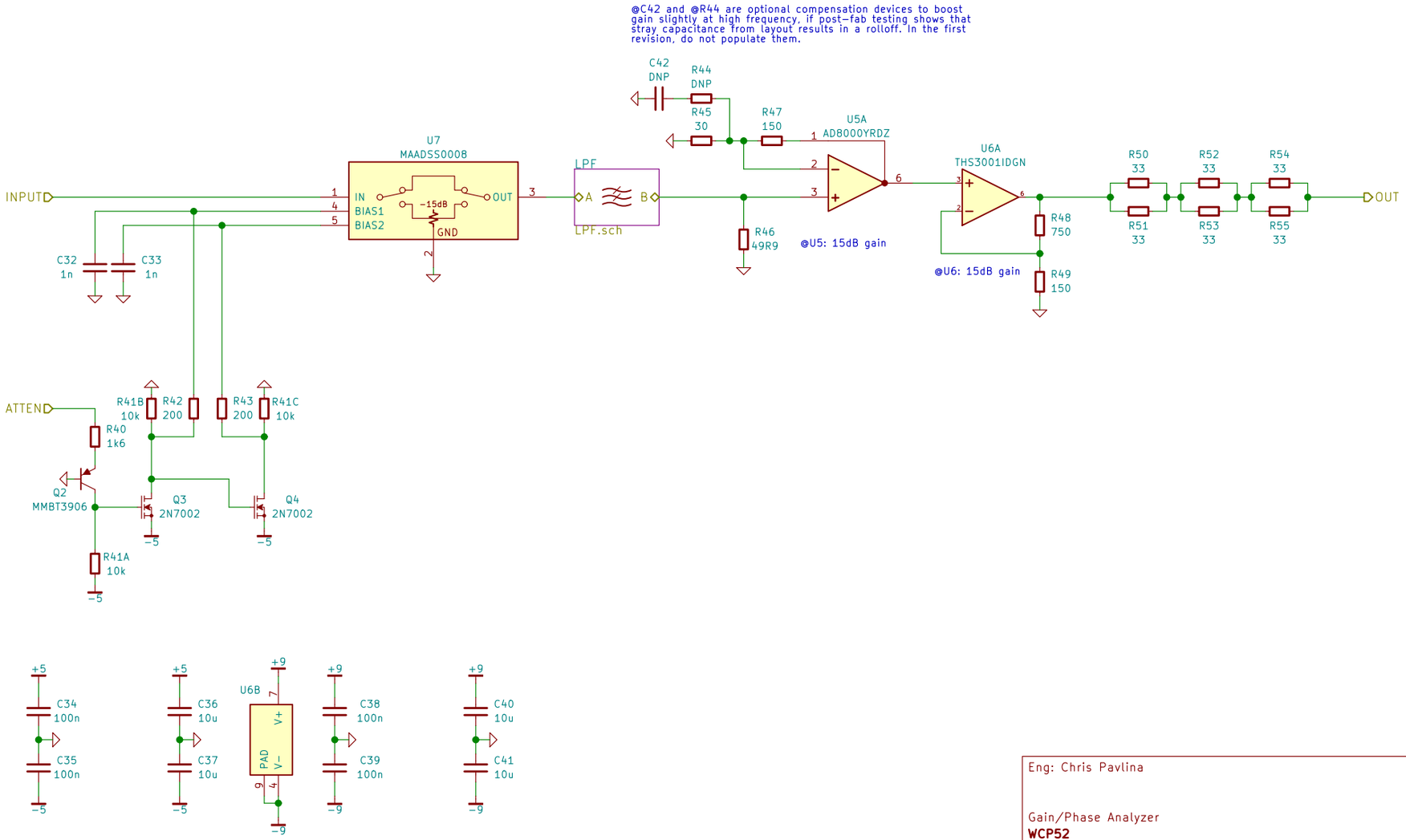
Intended frequency response of filter:



Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /OutputAmp/LPF/ File: LPF.sch	
Title: LPF for Output Amplifier	
Size: USLegal	Date: 2015-03-13
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 5/13

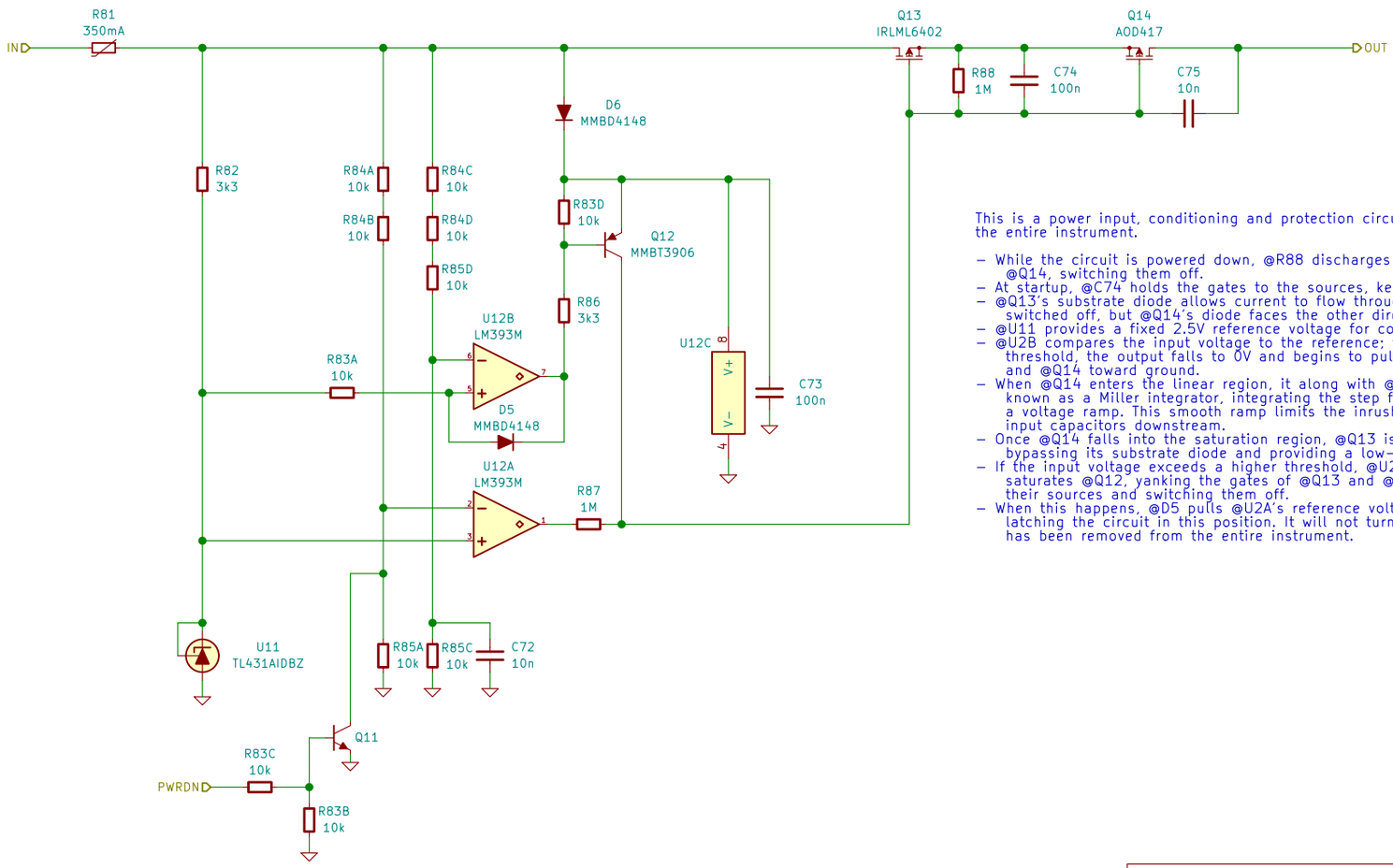
Rev:


U17
ATMEGA32U4-AU-DNP
U18
ATSAM4S16CA-AU
Place near VDDIN
J7
AVR-ICSP
J8
JLINK
E3 E4
1k@100-DNP
1k@100-DNP
C94 1u-DNP
C99 1u-DNP
C95 1u-DNP
R101 3k3-DNP
R100 3k3-DNP
JP1 #HWB
JP2 #RST
C96 100n-DNP
C97 C100 C102 C105 C106 100n
C98 C101 C103 C104 100n
C107 10u
C108 10u
C109 1u
E5 1k@100
R102 3k3
R103 3k3
R104 3k3
R105 3k3
R106 3k3
R107 3k3
R108 3k3
R109 3k3
R110 200
R111 3k3
R112 200
R113 200
R114 200
R115 200
R116 200
TP14 LEVEL
TP15 MISO
TP16 CHANSEL
TP17 ATTEN
TP18 SCK
TP20 MOSI
TP22 IOUP
TP19 #CS
TP21 SYNC
C110 15p
C111 15p
X2 12MHz
DS8 GP0
DS9 GP1
DS10 GP2
DS11 GP3
+3.3SB
VCORE
AVR#RST
VBUS
USBD_N
USBD_P
#HWB
XTAL2
XTAL1
ADC_VREF
ARM#RST
#SLEEP
#RTS
CHANSEL
I2C_SDA
I2C_SCL
SYNCIO
#CS
SER_TO_MPU
SER_FROM_MCU
LED0
MISO
MOSI
SCK
ADIN
SYNTH_SDIO1
SYNTH_MRST
PWRDN
IOUP
ATTEN
SYNTH_PWRDN
LED1
LED2
LED3
#CTS
SYNTH_MOSI
SYNTH_SCK
SYNTH_#CS
SYNTH_IOUPDATE
SYNTH_SYNCIO
SYNTH_PWRDN
SYNTH_MRST
SYNTH_SDIO1
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
ARM#RST
#TRST
@U17 is an alternative microcontroller. Not used in first revision.
Note duplicate connections. These are used to facilitate routing. Make sure to set all duplicate connections as inputs.
Eng: Chris Pavlina
Gain/Phase Analyzer
WCP52
Sheet: /MPU/
File: MPU.sch
Title: MPU
Size: USLegal
Date: 2015-03-13
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 13/13



Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /OutputAmp/ File: OutputAmp.sch	
Title: Output Amplifier	
Size: USLegal	Date: 2015-03-13
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 4/13

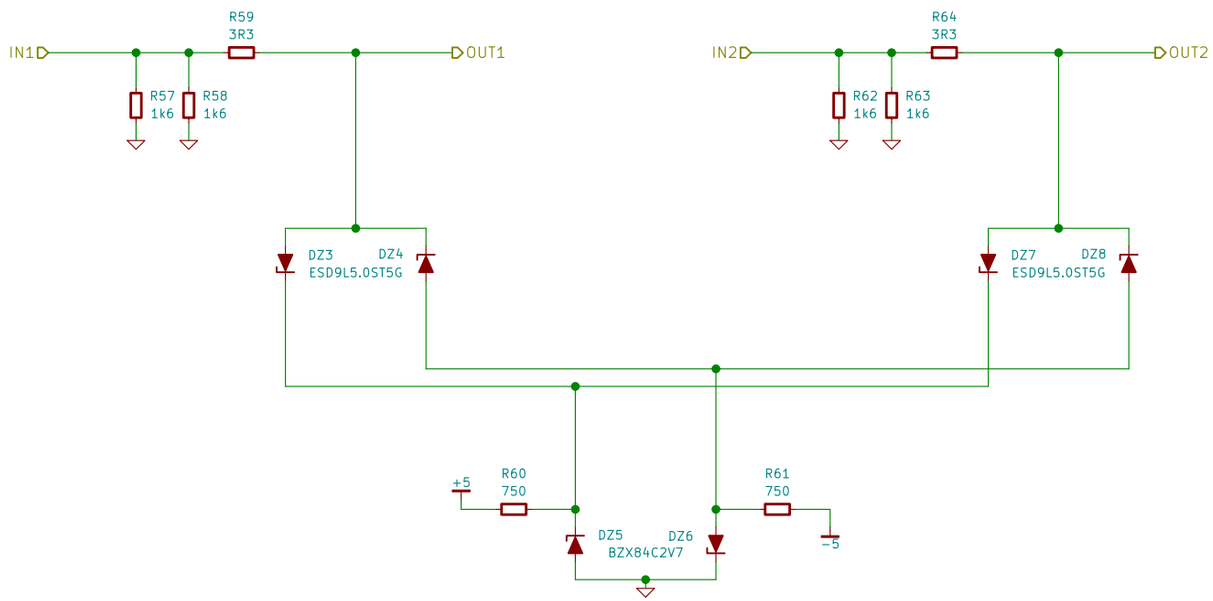
Rev:



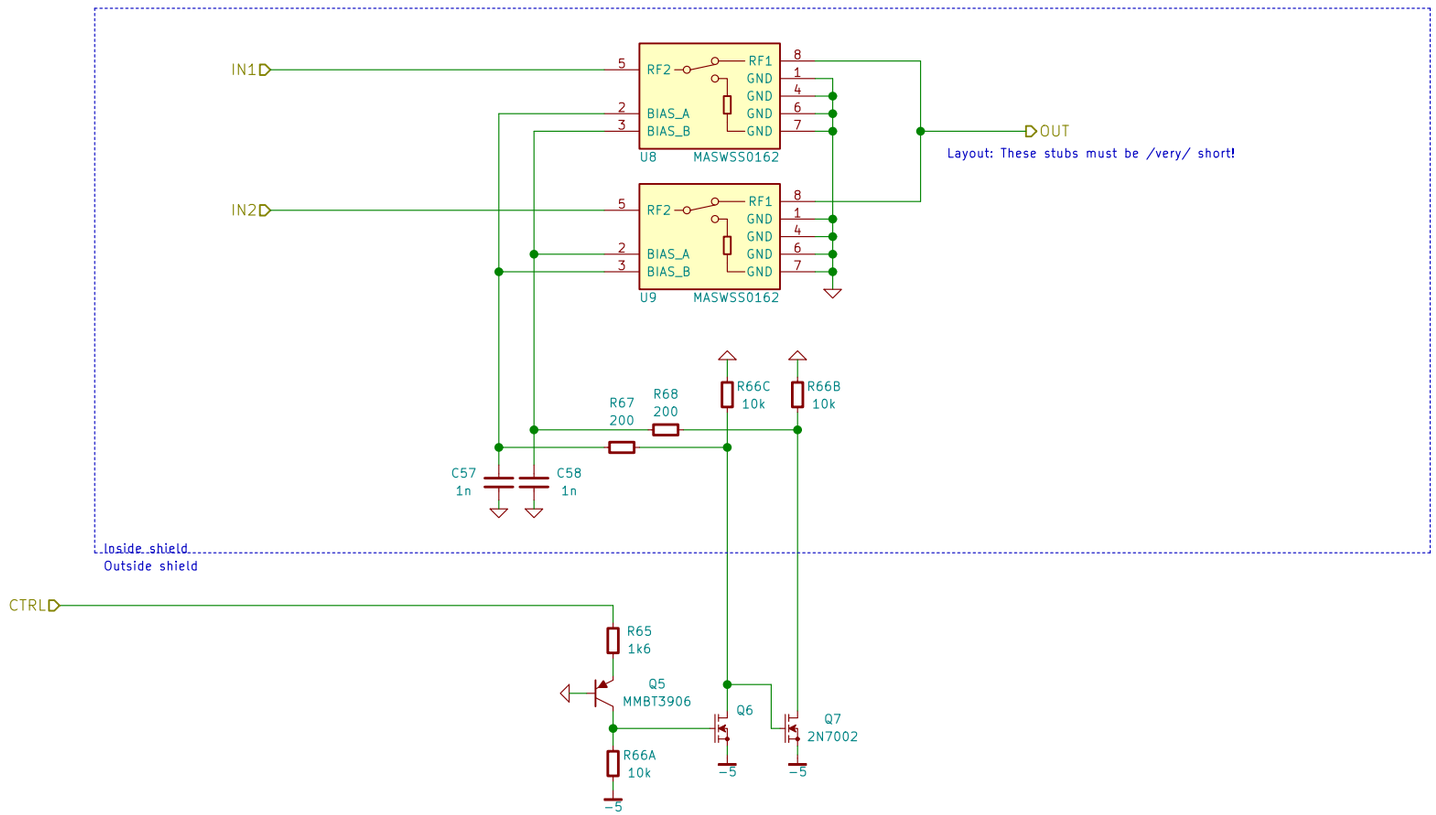
This is a power input, conditioning and protection circuit for the entire instrument.

- While the circuit is powered down, @R88 discharges the gates of @Q13 and @Q14, switching them off.
- At startup, @C74 holds the gates to the sources, keeping them switched off.
- @Q13's substrate diode allows current to flow through despite the FET being switched off, but @Q14's diode faces the other direction and does not.
- @U11 provides a fixed 2.5V reference voltage for comparison.
- @U2B compares the input voltage to the reference; when it exceeds a threshold, the output falls to 0V and begins to pull the gates of @Q13 and @Q14 toward ground.
- When @Q14 enters the linear region, it along with @C75 forms a circuit known as a Miller integrator, integrating the step from @U2B to produce a voltage ramp. This smooth ramp limits the inrush current charging any input capacitors downstream.
- Once @Q14 falls into the saturation region, @Q13 is also in this region, bypassing its substrate diode and providing a low-impedance path for current.
- If the input voltage exceeds a higher threshold, @U2A switches on. This saturates @Q12, yanking the gates of @Q13 and @Q14 back up towards their sources and switching them off.
- When this happens, @D5 pulls @U2A's reference voltage down, latching the circuit in this position. It will not turn back on until power has been removed from the entire instrument.

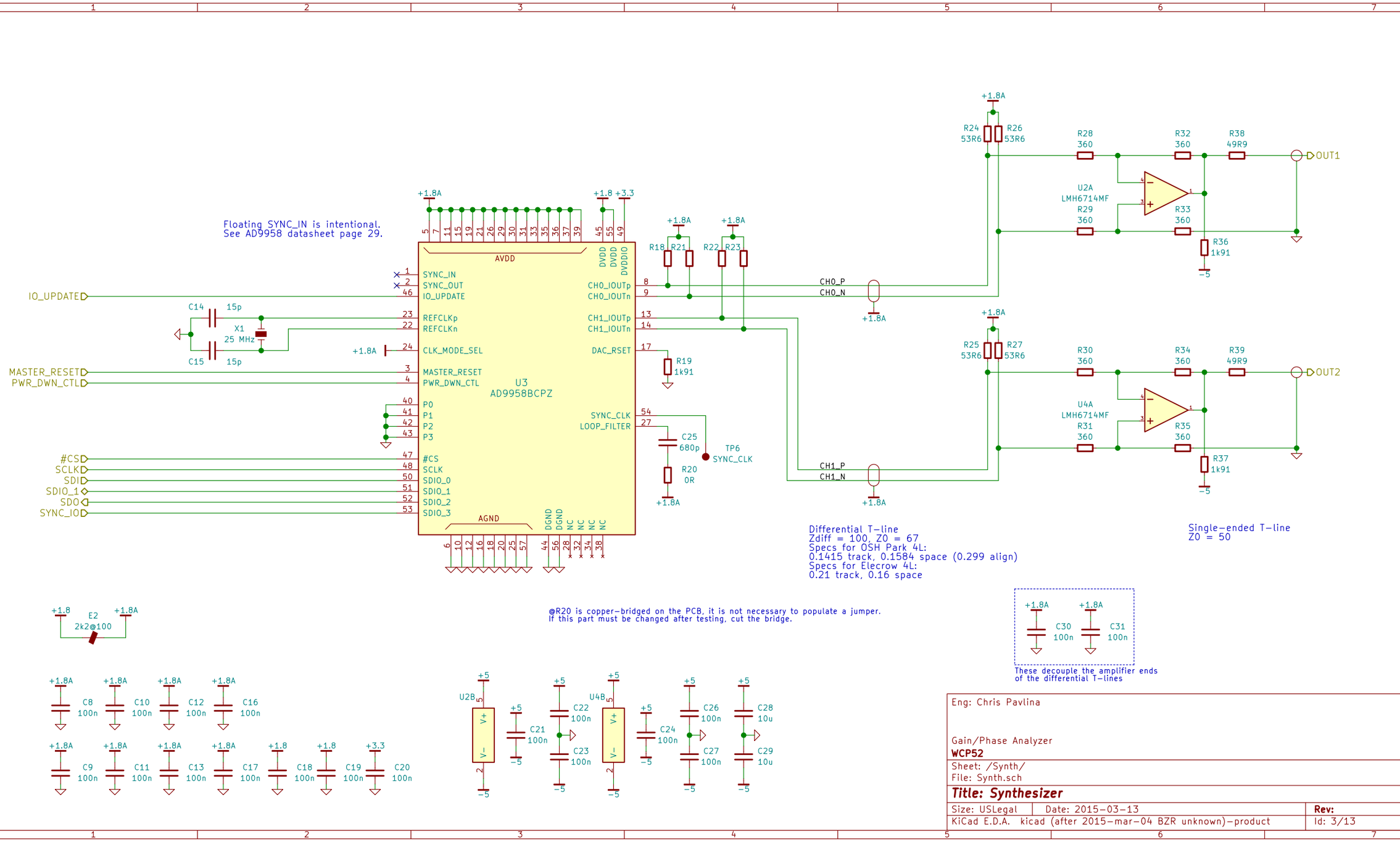
Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /PowerInput/ File: PowerInput.sch	
Title: Power Input Circuit	
Size: USLegal	Date: 2015-03-13
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 11/13



Eng: Chris Pavlina		
Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/Protection/ File: Protection.sch		
Title: Input Protection		
Size: USLegal	Date: 2015-03-13	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 7/13



Eng: Chris Pavlina	
Gain/Phase Analyzer **WCP52**	
Sheet: /InputFrontend/Switching/ File: Switching.sch	
Title: Input Switching	
Size: USLegal | Date: 2015-03-13	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product	Id: 8/13


Floating SYNC_IN is intentional.
See AD9958 datasheet page 29.
U3
AD9958BCPZ
AVDD
DVDD
DVDDIO
AGND
DGND
NC
SYNC_IN
SYNC_OUT
IO_UPDATE
REFCLKp
REFCLKn
CLK_MODE_SEL
MASTER_RESET
PWR_DWN_CTL
P0
P1
P2
P3
#CS
SCLK
SDIO_0
SDIO_1
SDIO_2
SDIO_3
CH0_IOUTp
CH0_IOUTn
CH1_IOUTp
CH1_IOUTn
DAC_RSET
SYNC_CLK
LOOP_FILTER
IO_UPDATE
MASTER_RESET
PWR_DWN_CTL
#CS
SCLK
SDI
SDIO_1
SDO
SYNC_IO
X1
25 MHz
C14 15p
C15 15p
R18 R21 R22 R23
R19 1k91
R20 0R
C25 680p
TP6
SYNC_CLK
CH0_P
CH0_N
CH1_P
CH1_N
R24 53R6
R26 53R6
R25 53R6
R27 53R6
R28 360
R29 360
R30 360
R31 360
R32 360
R33 360
R34 360
R35 360
R36 1k91
R37 1k91
R38 49R9
R39 49R9
U2A
LMH6714MF
U4A
LMH6714MF
OUT1
OUT2
Differential T-line
Zdiff = 100, Z0 = 67
Specs for OSH Park 4L:
0.1415 track, 0.1584 space (0.299 align)
Specs for Elecrow 4L:
0.21 track, 0.16 space
Single-ended T-line
Z0 = 50
E2
2k2@100
@R20 is copper-bridged on the PCB, it is not necessary to populate a jumper.
If this part must be changed after testing, cut the bridge.
C30 100n
C31 100n
These decouple the amplifier ends
of the differential T-lines
C8 100n
C10 100n
C12 100n
C16 100n
C9 100n
C11 100n
C13 100n
C17 100n
C18 100n
C19 100n
C20 100n
U2B
U4B
C21 100n
C22 100n
C23 100n
C24 100n
C26 100n
C27 100n
C28 10u
C29 10u
Eng: Chris Pavlina
Gain/Phase Analyzer
WCP52
Sheet: /Synth/
File: Synth.sch
Title: Synthesizer
Size: USLegal
Date: 2015-03-13
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 3/13