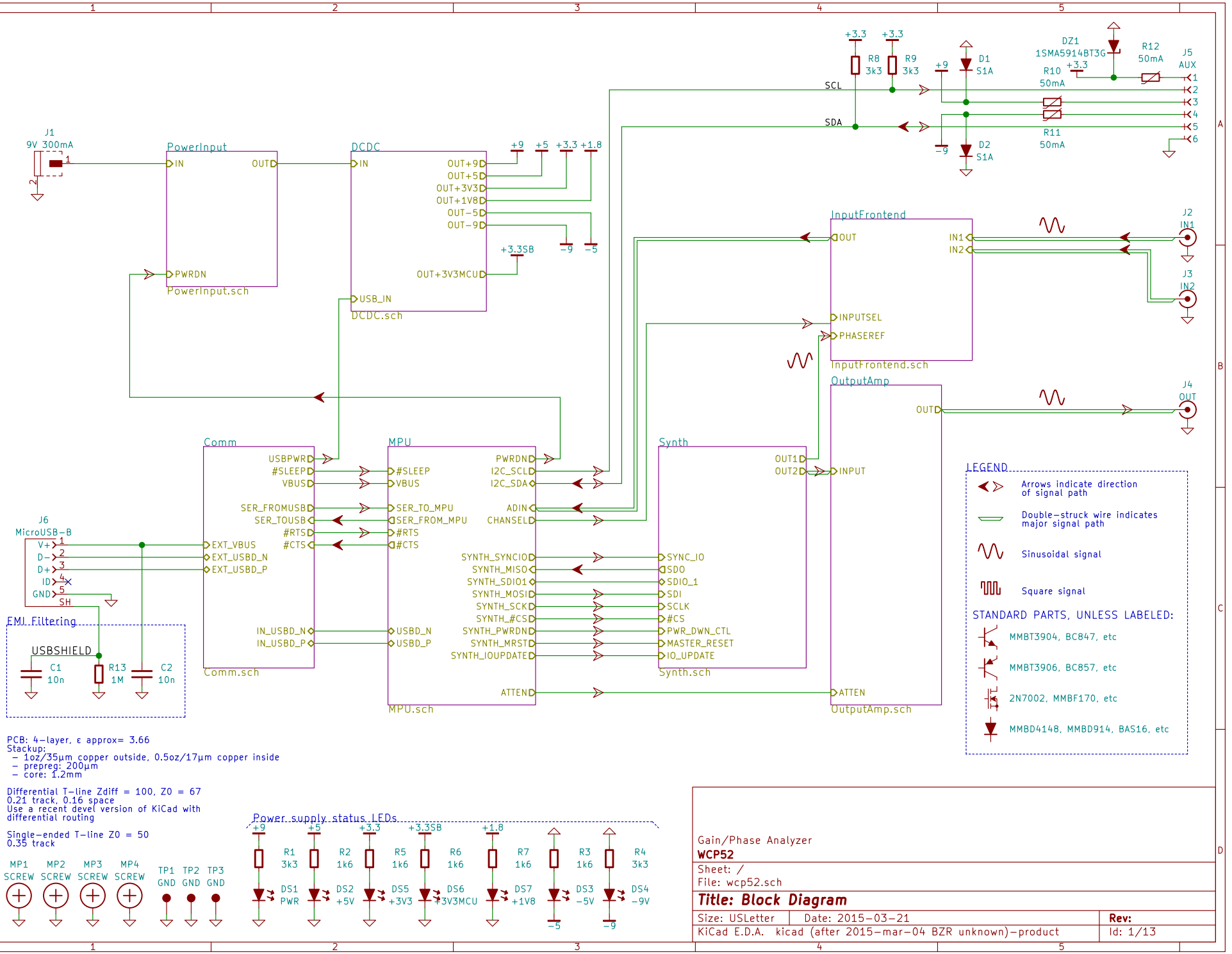
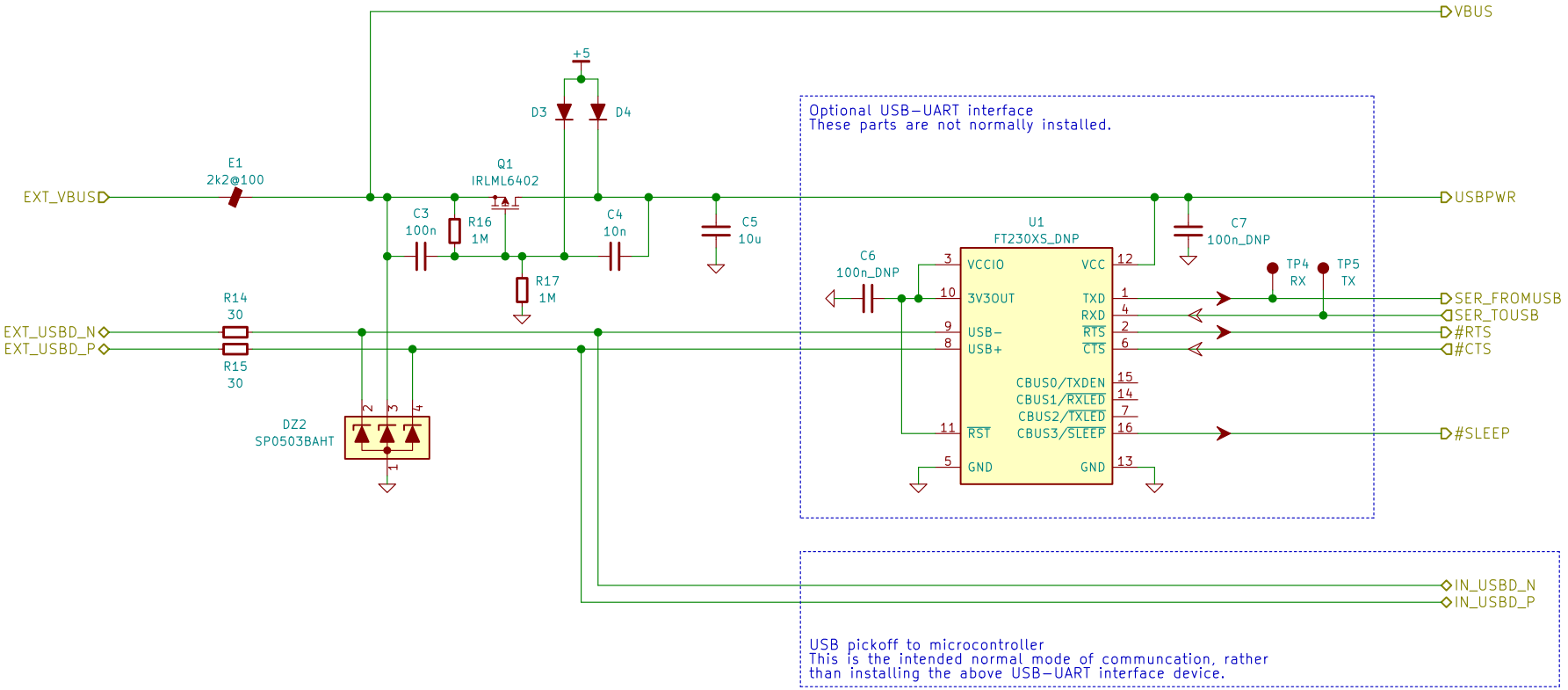

J1
9V 300mA
PowerInput
IN
OUT
PWRDN
PowerInput.sch
DCDC
IN
OUT+9
OUT+5
OUT+3V3
OUT+1V8
OUT-5
OUT-9
OUT+3V3MCU
USB_IN
DCDC.sch
+3.3SB
+3.3
+1.8
-9
-5
R8 3k3
R9 3k3
SCL
SDA
D1 S1A
D2 S1A
DZ1 1SMA5914BT3G
R10 50mA
R11 50mA
R12 50mA
J5 AUX
InputFrontend
OUT
IN1
IN2
INPUTSEL
PHASEREF
InputFrontend.sch
J2 IN1
J3 IN2
OutputAmp
OUT
INPUT
ATTEN
OutputAmp.sch
J4 OUT
Comm
USBPWR
#SLEEP
VBUS
SER_FROMUSB
SER_TOUSB
#RTS
#CTS
EXT_VBUS
EXT_USBD_N
EXT_USBD_P
IN_USBD_N
IN_USBD_P
Comm.sch
MPU
#SLEEP
VBUS
SER_TO_MPU
SER_FROM_MPU
#RTS
#CTS
USBD_N
USBD_P
PWRDN
I2C_SCL
I2C_SDA
ADIN
CHANSEL
SYNTH_SYNCIO
SYNTH_MISO
SYNTH_SDIO1
SYNTH_MOSI
SYNTH_SCK
SYNTH_#CS
SYNTH_PWRDN
SYNTH_MRST
SYNTH_IOUPDATE
ATTEN
MPU.sch
Synth
OUT1
OUT2
INPUT
SYNC_IO
SDO
SDIO_1
SDI
SCLK
#CS
PWR_DWN_CTL
MASTER_RESET
IO_UPDATE
Synth.sch
J6
MicroUSB-B
V+
D-
D+
ID
GND
SH
EMI Filtering
USBSHIELD
C1 10n
R13 1M
C2 10n
LEGEND
Arrows indicate direction of signal path
Double-struck wire indicates major signal path
Sinusoidal signal
Square signal
STANDARD PARTS, UNLESS LABELED:
MMBT3904, BC847, etc
MMBT3906, BC857, etc
2N7002, MMBF170, etc
MMBD4148, MMBD914, BAS16, etc
PCB: 4-layer, ε approx= 3.66
Stackup:
- 1oz/35µm copper outside, 0.5oz/17µm copper inside
- prepreg: 200µm
- core: 1.2mm
Differential T-line Zdiff = 100, Z0 = 67
0.21 track, 0.16 space
Use a recent devel version of KiCad with differential routing
Single-ended T-line Z0 = 50
0.35 track
MP1 SCREW
MP2 SCREW
MP3 SCREW
MP4 SCREW
TP1 GND
TP2 GND
TP3 GND
Power supply status LEDs
R1 3k3
R2 1k6
R5 1k6
R6 1k6
R7 1k6
R3 1k6
R4 3k3
DS1 PWR
DS2 +5V
DS5 +3V3
DS6 +3V3MCU
DS7 +1V8
DS3 -5V
DS4 -9V
Gain/Phase Analyzer
WCP52
Sheet: /
File: wcp52.sch
Title: Block Diagram
Size: USLetter
Date: 2015-03-21
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 1/13

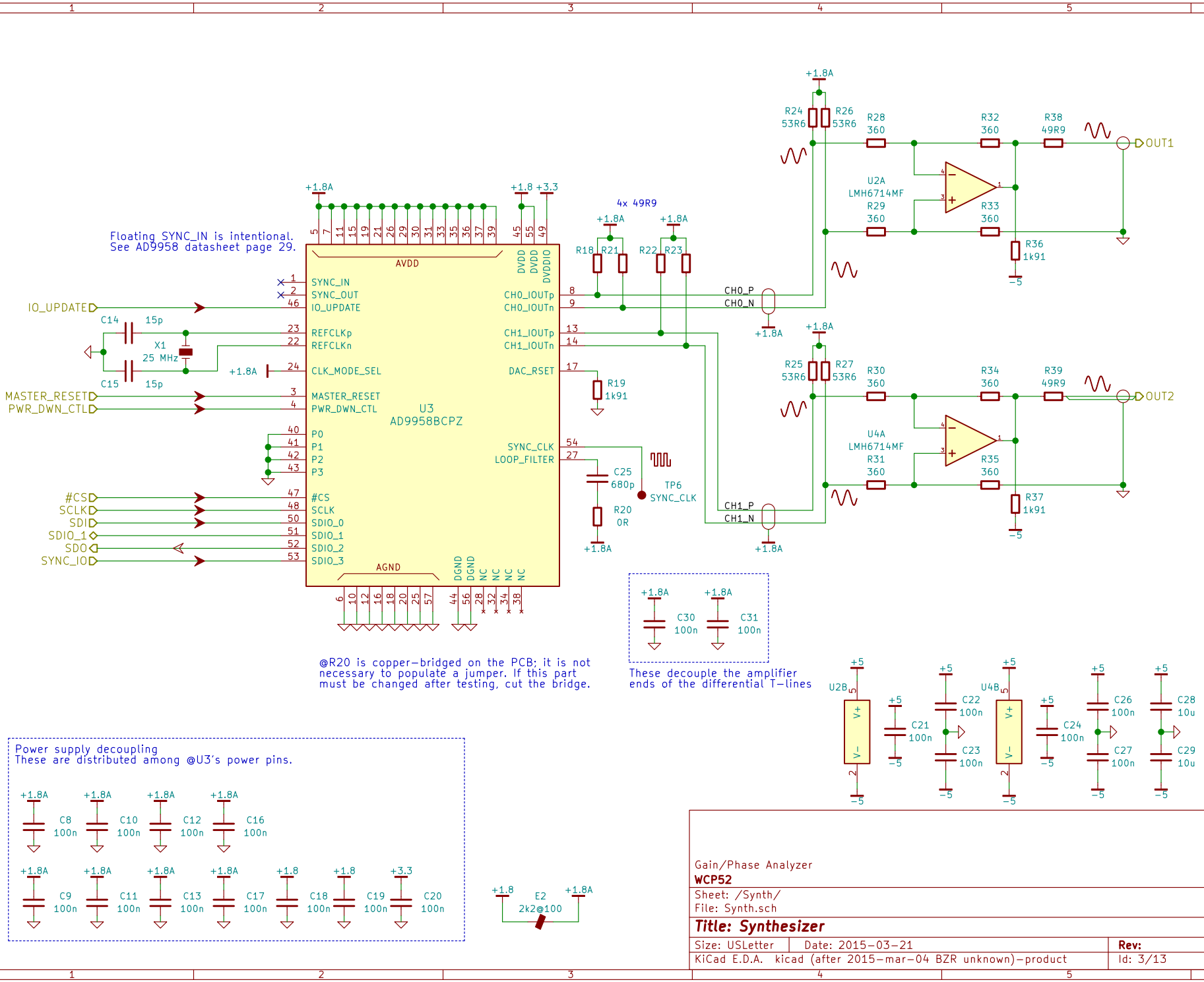


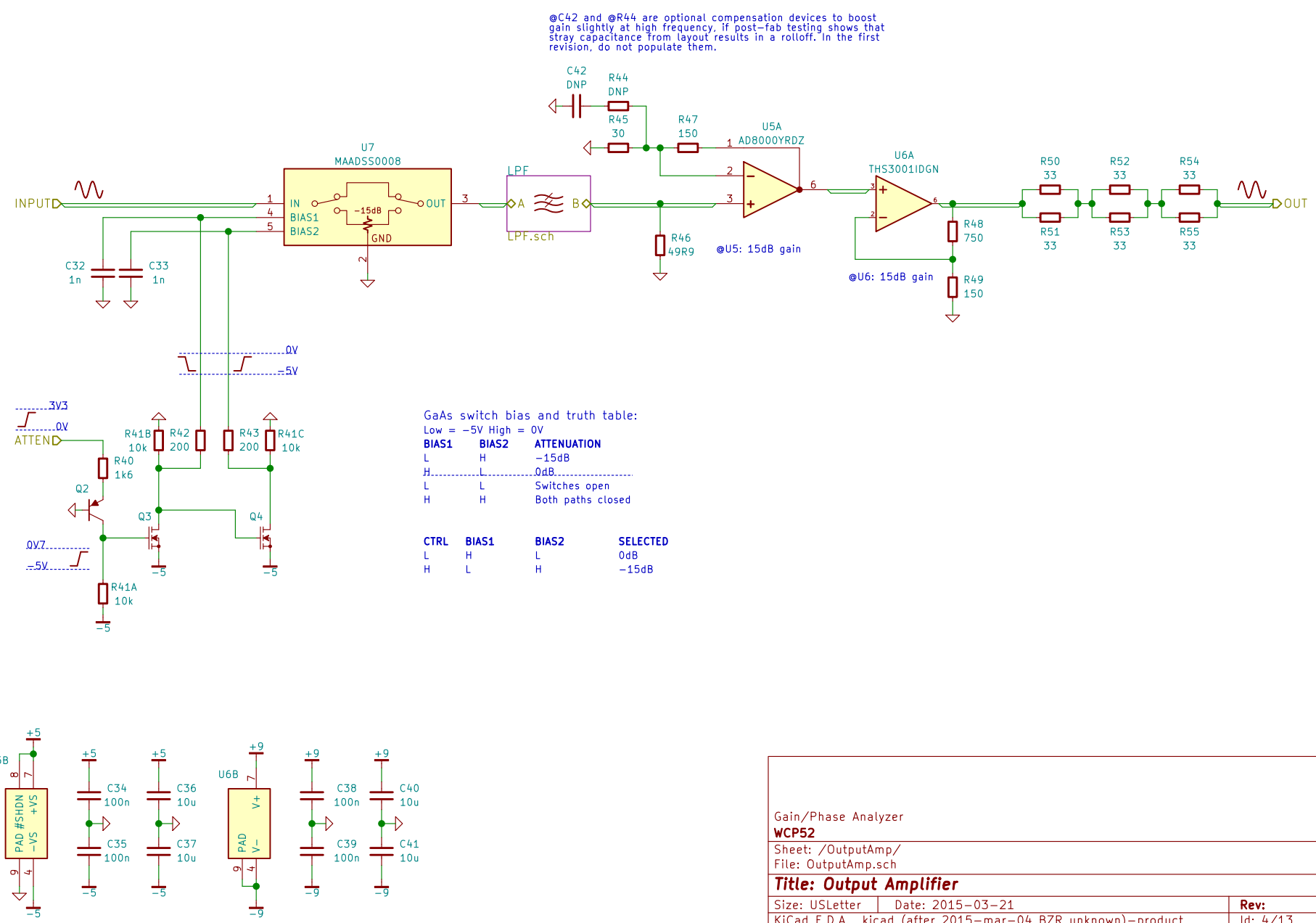
Gain/Phase Analyzer
WCP52

Sheet: /Comm/
File: Comm.sch

Title: USB Communications

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 2/13

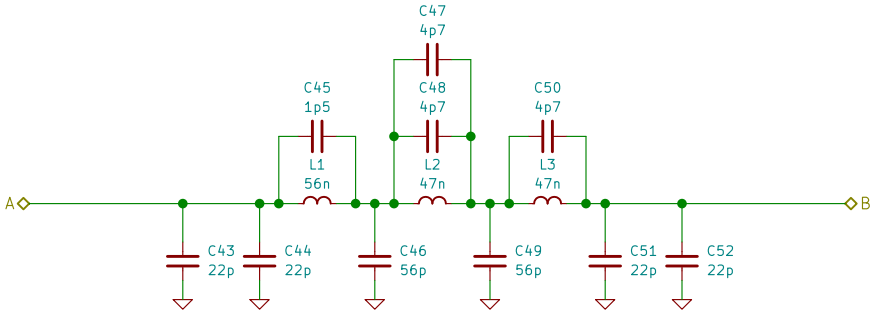

Floating SYNC_IN is intentional.
See AD9958 datasheet page 29.
U3
AD9958BCPZ
SYNC_IN
SYNC_OUT
IO_UPDATE
REFCLKp
REFCLKn
CLK_MODE_SEL
MASTER_RESET
PWR_DWN_CTL
P0
P1
P2
P3
#CS
SCLK
SDIO_0
SDIO_1
SDIO_2
SDIO_3
CH0_IOUTp
CH0_IOUTn
CH1_IOUTp
CH1_IOUTn
DAC_RSET
SYNC_CLK
LOOP_FILTER
AVDD
AGND
DVDD
DVDDIO
DGND
NC
IO_UPDATE
MASTER_RESET
PWR_DWN_CTL
#CS
SCLK
SDI
SDIO_1
SDO
SYNC_IO
C14 15p
C15 15p
X1
25 MHz
R18 R21
R22 R23
4x 49R9
R19 1k91
R20 0R
C25 680p
TP6
SYNC_CLK
CH0_P
CH0_N
CH1_P
CH1_N
R24 53R6
R26 53R6
R25 53R6
R27 53R6
U2A
LMH6714MF
U4A
LMH6714MF
R28 360
R29 360
R30 360
R31 360
R32 360
R33 360
R34 360
R35 360
R36 1k91
R37 1k91
R38 49R9
R39 49R9
OUT1
OUT2
+1.8A
+1.8
+3.3
@R20 is copper-bridged on the PCB; it is not necessary to populate a jumper. If this part must be changed after testing, cut the bridge.
C30 100n
C31 100n
These decouple the amplifier ends of the differential T-lines
U2B
U4B
C21 100n
C22 100n
C23 100n
C24 100n
C26 100n
C27 100n
C28 10u
C29 10u
Power supply decoupling
These are distributed among @U3's power pins.
C8 100n
C10 100n
C12 100n
C16 100n
C9 100n
C11 100n
C13 100n
C17 100n
C18 100n
C19 100n
C20 100n
E2
2k2@100
Gain/Phase Analyzer
WCP52
Sheet: /Synth/
File: Synth.sch
Title: Synthesizer
Size: USLetter
Date: 2015-03-21
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 3/13



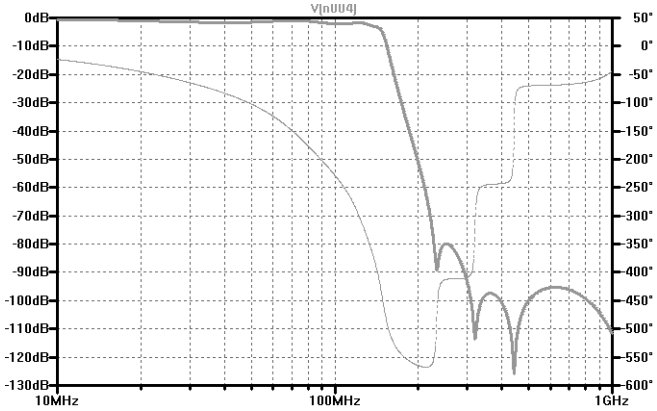
Gain/Phase Analyzer
WCP52
Sheet: /OutputAmp/
File: OutputAmp.sch

Title: Output Amplifier

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 4/13



Intended frequency response of filter:

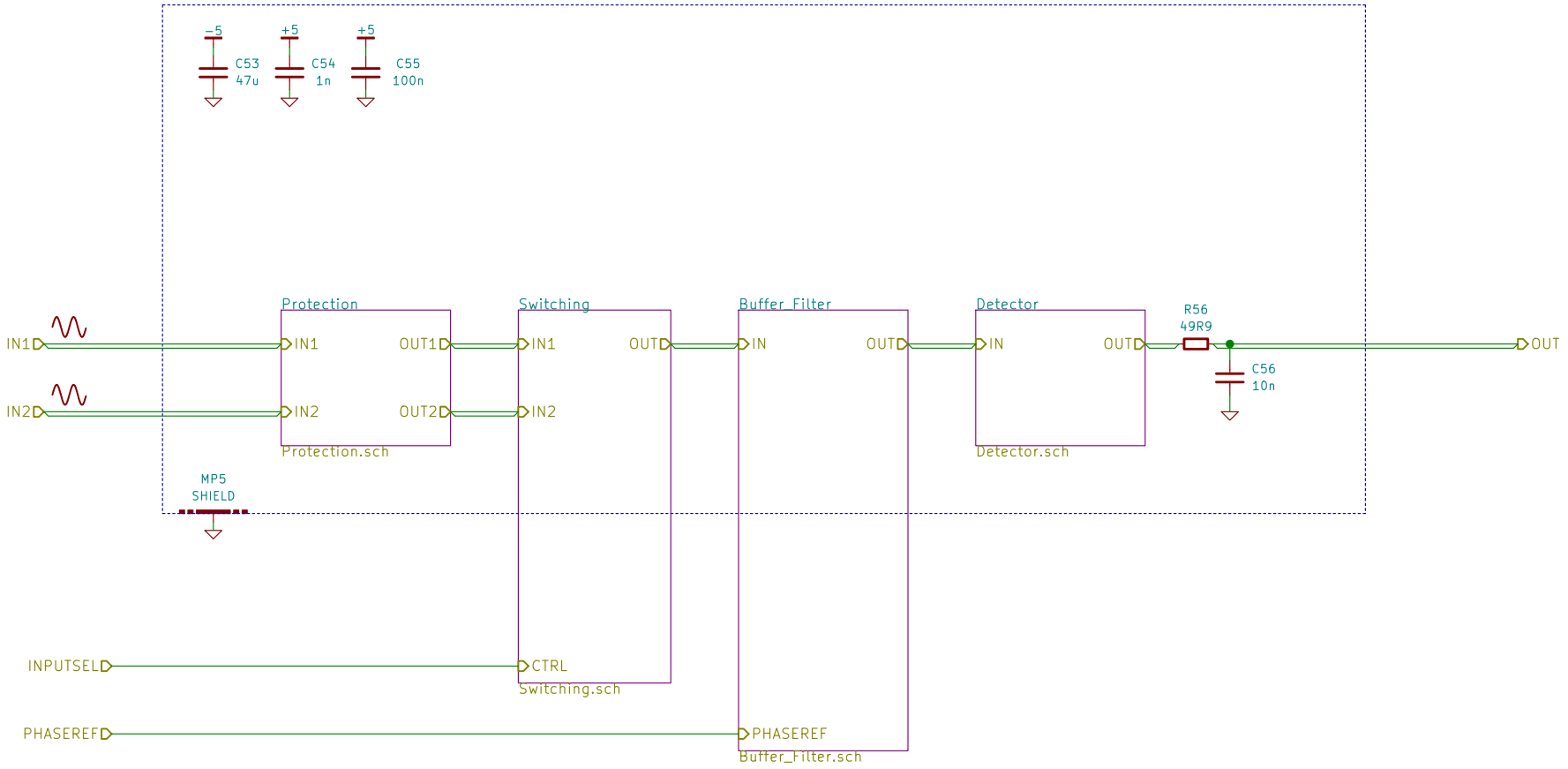


Gain/Phase Analyzer
WCP52

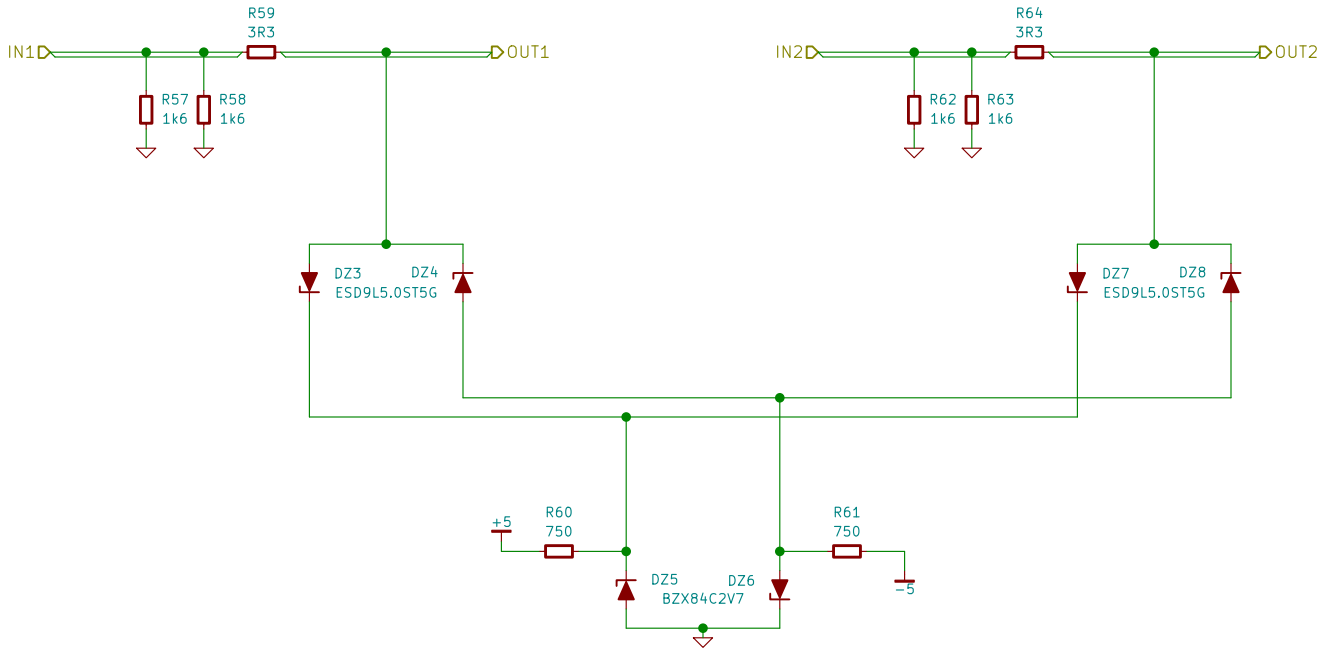
Sheet: /OutputAmp/LPF/
File: LPF.sch

Title: LPF for Output Amplifier

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 5/13



Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/ File: InputFrontend.sch		
Title: Input Frontend		
Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 6/13

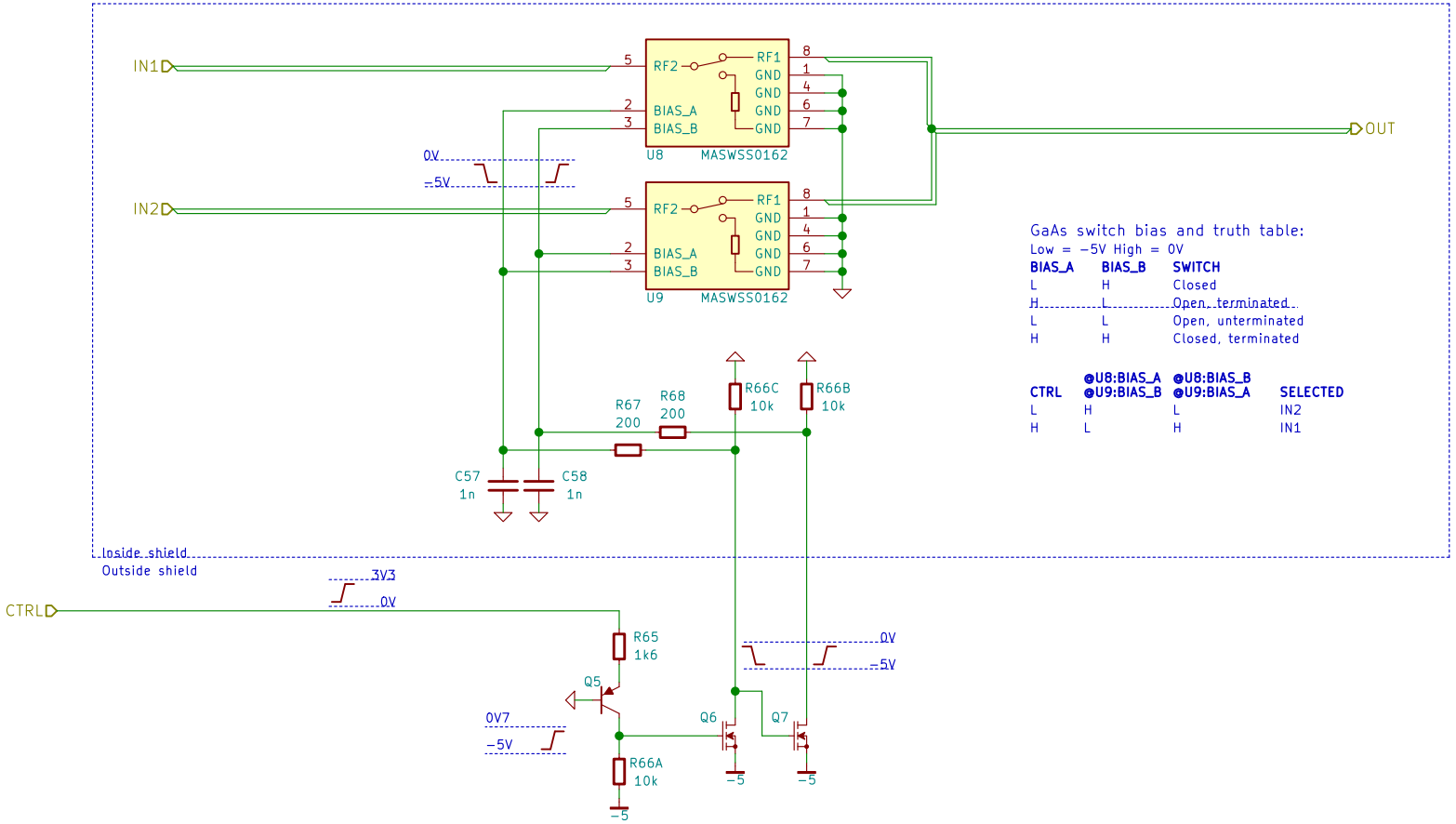


Gain/Phase Analyzer
WCP52

Sheet: /InputFrontend/Protection/
File: Protection.sch

Title: Input Protection

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 7/13

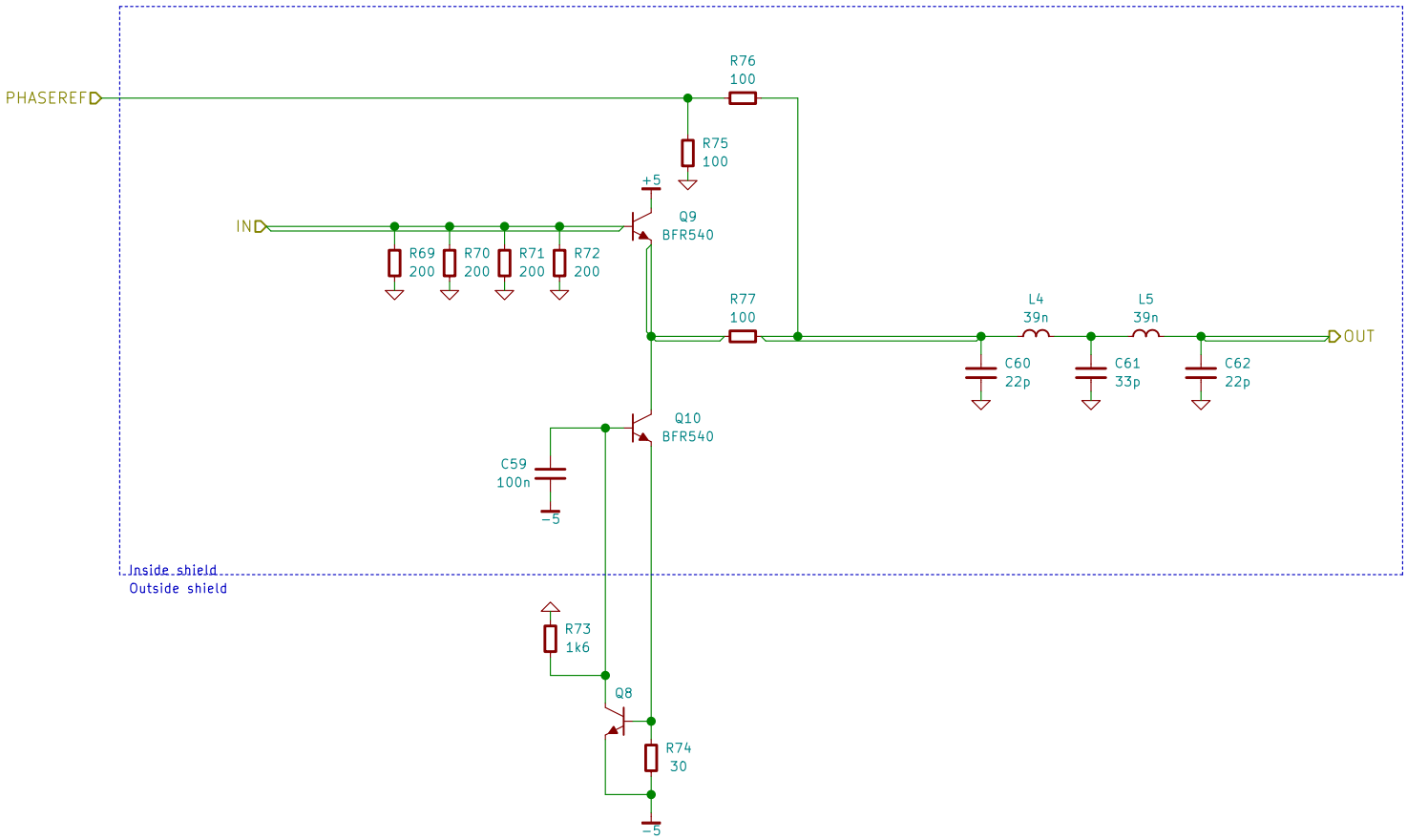


Gain/Phase Analyzer
WCP52

Sheet: /InputFrontend/Switching/
File: Switching.sch

Title: Input Switching

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 8/13



Gain/Phase Analyzer

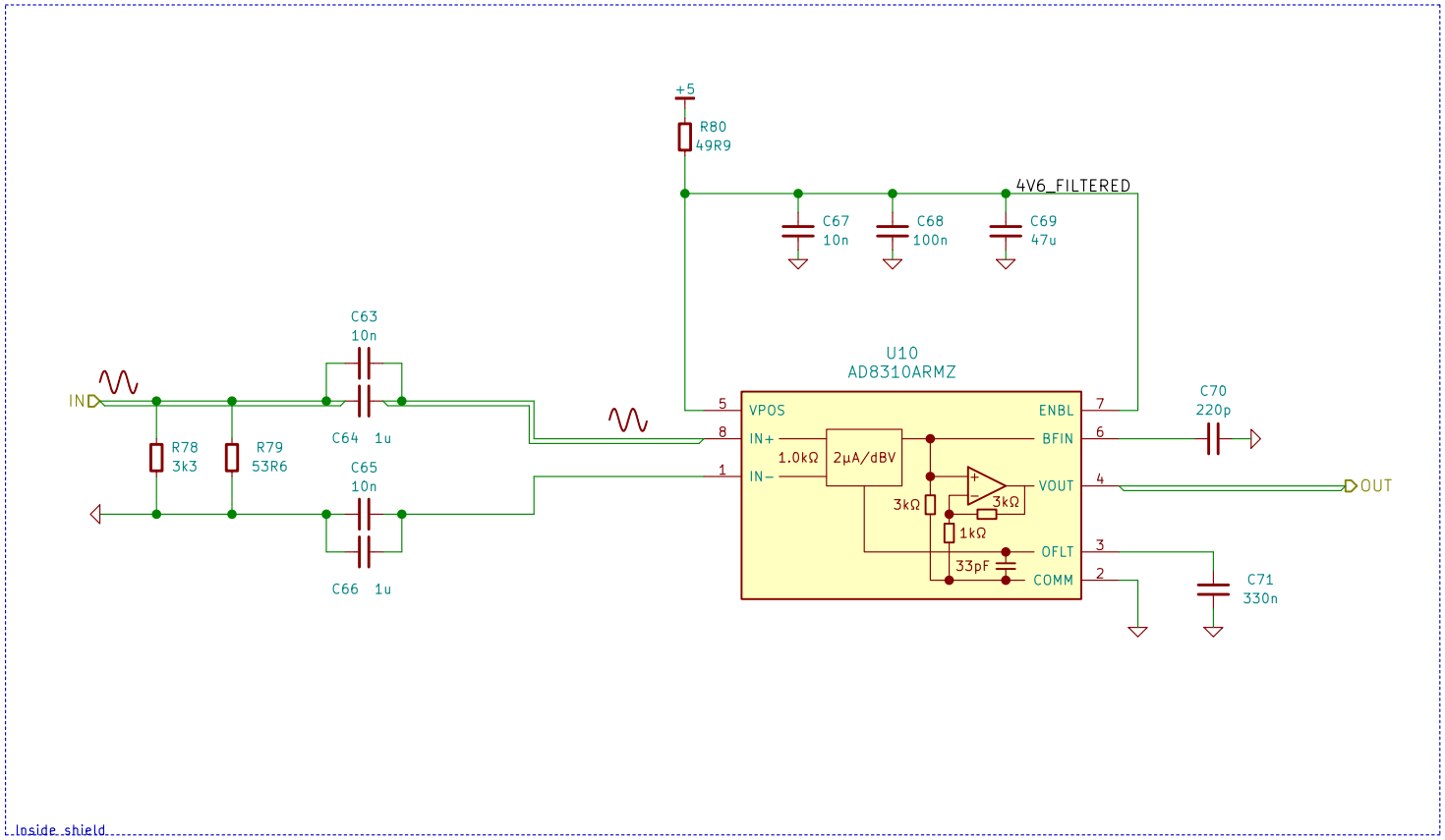
WCP52

Sheet: /InputFrontend/Buffer_Filter/

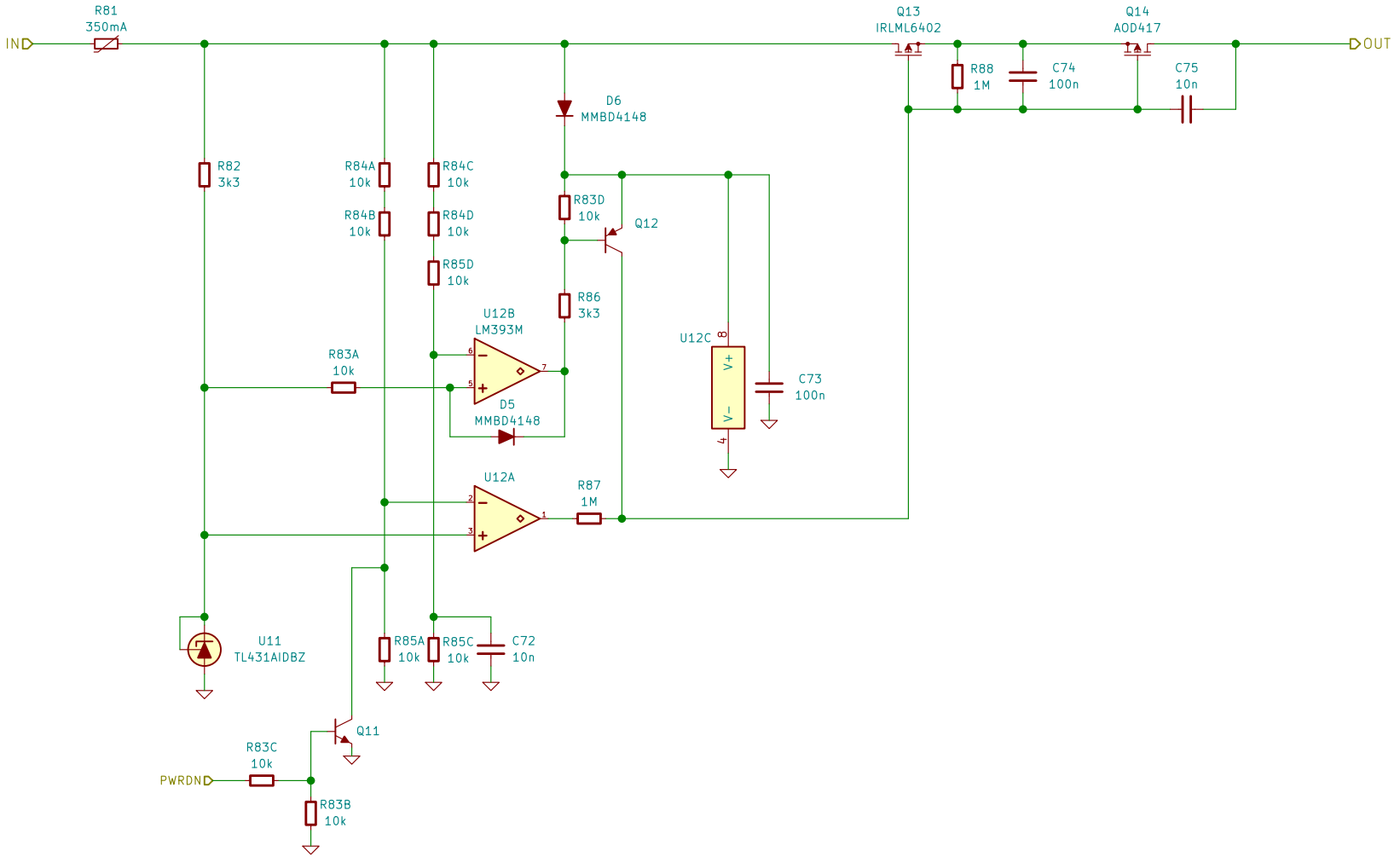
File: Buffer_Filter.sch

Title: Input Buffer and Filter

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 9/13



Gain/Phase Analyzer **WCP52**		
Sheet: /InputFrontend/Detector/ File: Detector.sch		
Title: Logarithmic Detector		
Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 10/13

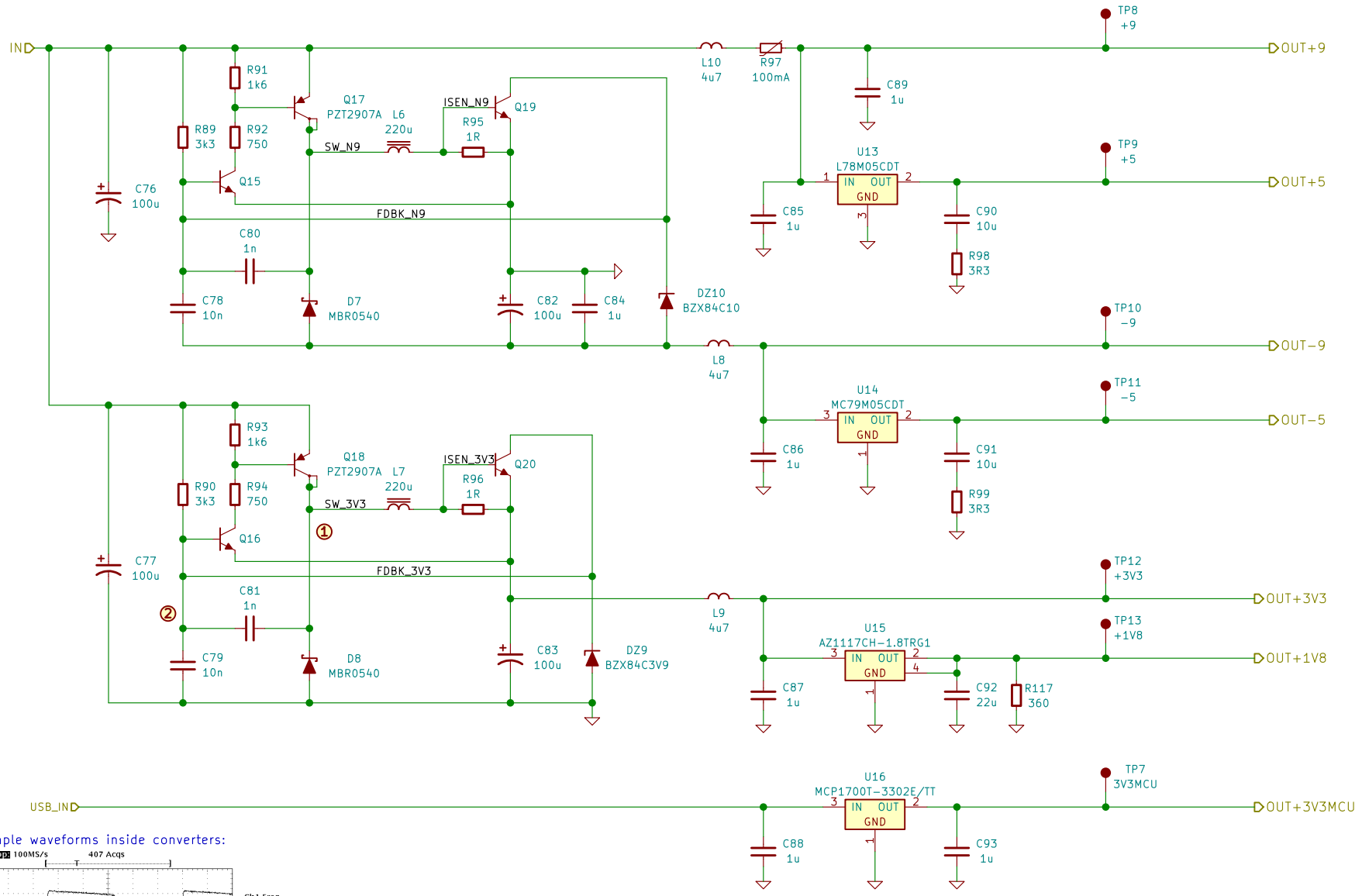


Gain/Phase Analyzer
WCP52

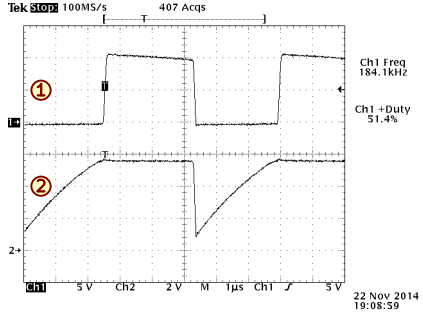
Sheet: /PowerInput/
File: PowerInput.sch

Title: Power Input Circuit

Size: USLetter	Date: 2015-03-21	**Rev:**
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product		Id: 11/13



Example waveforms inside converters:

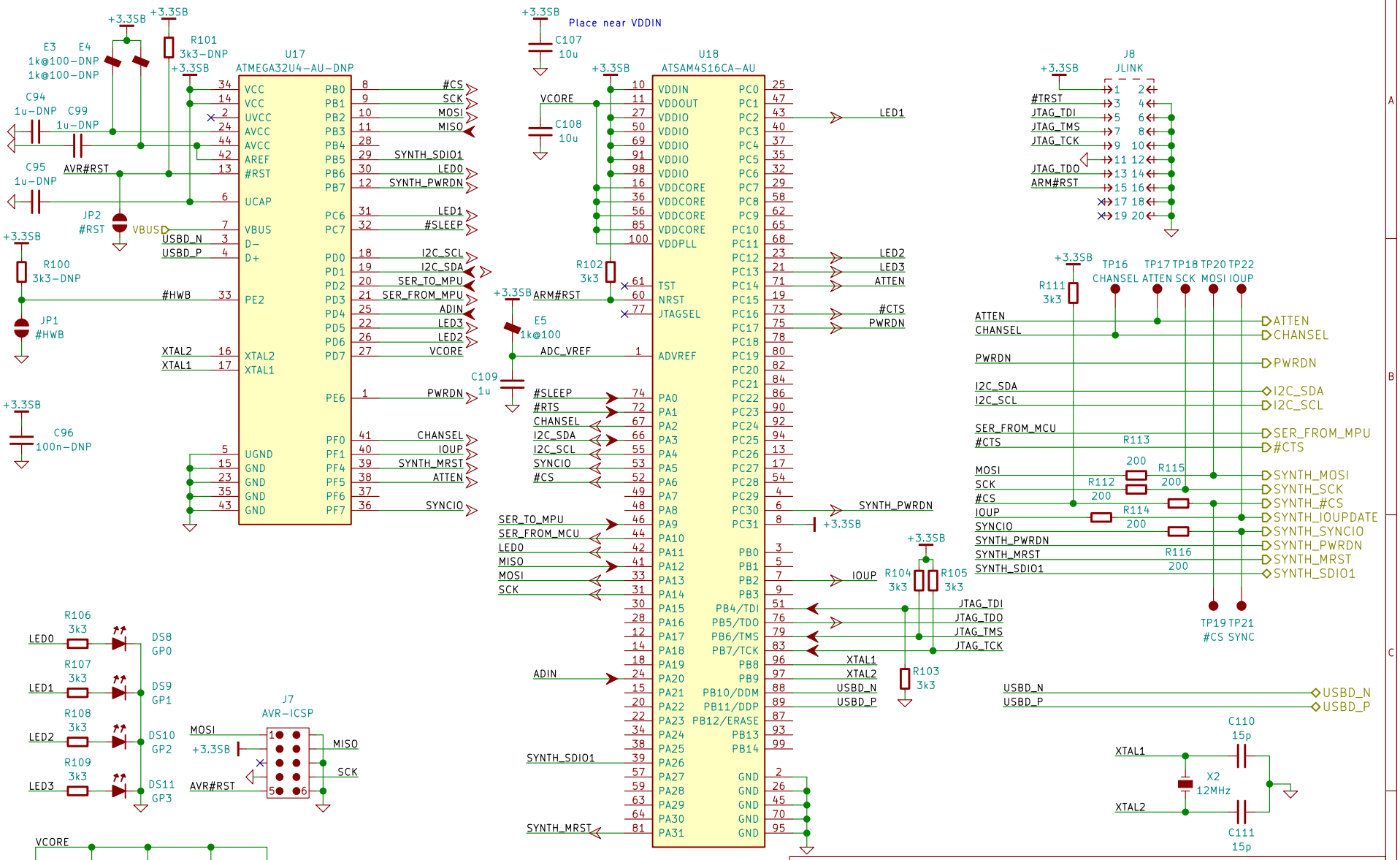


Gain/Phase Analyzer
WCP52

Sheet: /DCDC/
File: DCDC.sch

Title: DC−DC Converters

Size: USLetter	Date: 2015−03−21	**Rev:**
KiCad E.D.A. kicad (after 2015−mar−04 BZR unknown)−product		Id: 12/13


U17
ATMEGA32U4-AU-DNP
U18
ATSAM4S16CA-AU
Place near VDDIN
J8
JLINK
J7
AVR-ICSP
E3 E4
1k@100-DNP
1k@100-DNP
R101
3k3-DNP
C94
1u-DNP
C99
1u-DNP
C95
1u-DNP
AVR#RST
JP2
#RST
VBUS
R100
3k3-DNP
JP1
#HWB
C96
100n-DNP
C107
10u
C108
10u
R102
3k3
E5
1k@100
C109
1u
ADC_VREF
ARM#RST
VCORE
R106
3k3
R107
3k3
R108
3k3
R109
3k3
LED0
LED1
LED2
LED3
DS8
GP0
DS9
GP1
DS10
GP2
DS11
GP3
C97
100n
C100
100n
C102
100n
C105
100n
C106
100n
C98
100n
C101
100n
C103
100n
C104
100n
TP14
LEVEL
TP15
MISO
R110
200
ADIN
SER_TO_MPU
SYNTH_MISO
#SLEEP
#RTS
R111
3k3
TP16
CHANSEL
TP17
ATTEN
TP18
SCK
TP20
MOSI
TP22
IOUP
R112
200
R113
200
R114
200
R115
200
R116
200
TP19
#CS
TP21
SYNC
R104
3k3
R105
3k3
R103
3k3
C110
15p
X2
12MHz
C111
15p
XTAL1
XTAL2
@U17 is an alternative microcontroller. Not used in first revision.
Note duplicate connections. These are used to facilitate routing. Make
sure to set all duplicate connections as inputs.
Gain/Phase Analyzer
WCP52
Sheet: /MPU/
File: MPU.sch
Title: MPU
Size: USLetter
Date: 2015-03-21
Rev:
KiCad E.D.A. kicad (after 2015-mar-04 BZR unknown)-product
Id: 13/13