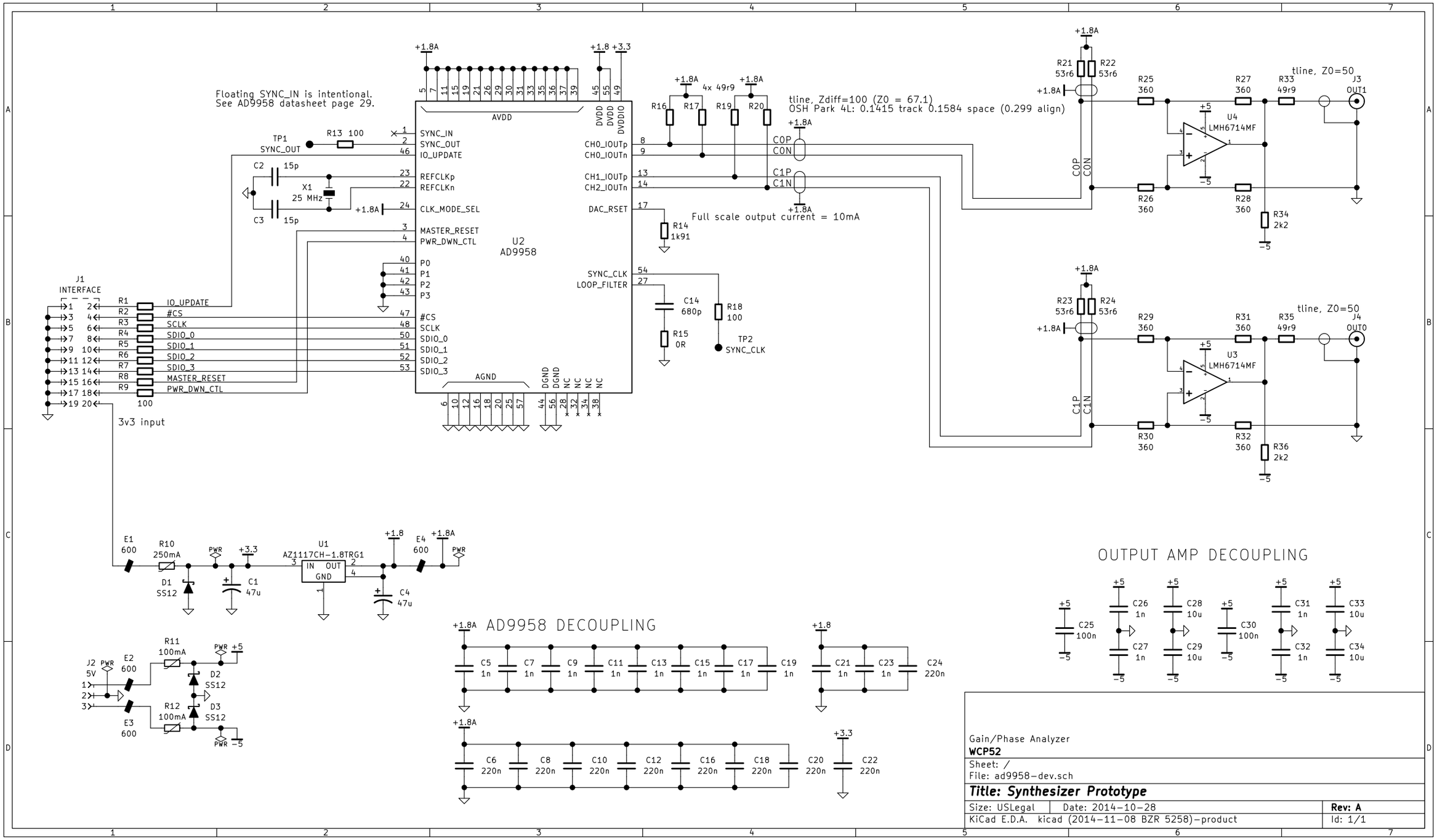
Floating SYNC_IN is intentional.
See AD9958 datasheet page 29.
U2
AD9958
AVDD
AGND
DVDD
DVDDIO
DGND
SYNC_IN
SYNC_OUT
IO_UPDATE
REFCLKp
REFCLKn
CLK_MODE_SEL
MASTER_RESET
PWR_DWN_CTL
P0
P1
P2
P3
#CS
SCLK
SDIO_0
SDIO_1
SDIO_2
SDIO_3
CH0_IOUTp
CH0_IOUTn
CH1_IOUTp
CH2_IOUTn
DAC_RSET
SYNC_CLK
LOOP_FILTER
NC
TP1
SYNC_OUT
R13 100
C2 15p
C3 15p
X1
25 MHz
J1
INTERFACE
3v3 input
tline, Zdiff=100 (Z0 = 67.1)
OSH Park 4L: 0.1415 track 0.1584 space (0.299 align)
4x 49r9
Full scale output current = 10mA
R14
1k91
C14
680p
R15
0R
R18
100
TP2
SYNC_CLK
COP
CON
C1P
C1N
U4
LMH6714MF
U3
LMH6714MF
tline, Z0=50
J3
OUT1
J4
OUT0
R21 53r6
R22 53r6
R23 53r6
R24 53r6
R25 360
R26 360
R27 360
R28 360
R29 360
R30 360
R31 360
R32 360
R33 49r9
R34 2k2
R35 49r9
R36 2k2
E1 600
R10 250mA
D1 SS12
C1 47u
U1
AZ1117CH-1.8TRG1
IN OUT GND
C4 47u
E4 600
PWR
J2 5V
E2 600
E3 600
R11 100mA
R12 100mA
D2 SS12
D3 SS12
AD9958 DECOUPLING
C5 1n
C7 1n
C9 1n
C11 1n
C13 1n
C15 1n
C17 1n
C19 1n
C21 1n
C23 1n
C24 220n
C6 220n
C8 220n
C10 220n
C12 220n
C16 220n
C18 220n
C20 220n
C22 220n
OUTPUT AMP DECOUPLING
C25 100n
C26 1n
C27 1n
C28 10u
C29 10u
C30 100n
C31 1n
C32 1n
C33 10u
C34 10u
Gain/Phase Analyzer
WCP52
Sheet: /
File: ad9958-dev.sch
Title: Synthesizer Prototype
Size: USLegal
Date: 2014-10-28
Rev: A
KiCad E.D.A. kicad (2014-11-08 BZR 5258)-product
Id: 1/1