Simple Coincidence firmware on V1495

Introduction

This document gives instruction on the simple coincidence firmware that was built for the CAEN V1495 FPGA module

The base address of the V1495 is 0x32100000

The registers must be read/written in D32 mode.

Front panel

Input

Input signals are provided to the ‘A’ input port. Other inputs are ignored.

Output

A ‘A395D’ mezzanine card should be installed in the ‘F’ port.

Note that LEMO 0 is the bottom connector

LEMO connector	Output description
0	Output of coincidence logic
1	A(0) before delay and gate
2	A(0) after delay and gate
3	A(1) before delay and gate
4	A(1) after delay and gate
5	A(2) before delay and gate
6	A(2) after delay and gate
7	Unconnected

Channels 1-6 can be used to tune the delay and gate width of channel 0-2.

Read/Write registers. Registers must be read/written in D32 mode		
Name	Address	Description
Reset	0x1012	Performs a reset when read or written (value doesn't matter)
Pre-logic delay		Number of 125MHz clock ticks to delay a channel. Each 32-bit register handles 4 input channels. For example, the register 0x101C set to a value of 0xABCDEF01 would apply a delay of 0x01 to channel 0 0xEF to channel 1 0xCD to channel 2 0xAB to channel 3
Channel 0-3	0x101C	
Channel 4-7	0x101E	
Channel 8-11	0x1020	
Channel 12-15	0x1022	
Channel 16-19	0x1024	
Channel 20-23	0x1026	
Channel 24-27	0x1028	
Channel 28-31	0x102A	
Pre-logic gate width		Length of gate in 125MHz clock ticks. Each 32-bit register handles 4 input channels For example, the register 0x102C set to a value of 0xABCDEF01 would apply a gate width of 0x01 to channel 0 0xEF to channel 1 0xCD to channel 2 0xAB to channel 3
Channel 0-3	0x102C	
Channel 4-7	0x102E	
Channel 8-11	0x1030	
Channel 12-15	0x1032	
Channel 16-19	0x1034	
Channel 20-23	0x1036	
Channel 24-27	0x1038	
Channel 28-31	0x103A	
Channel enable	0x103C	Enable/disable channels for coincidence logic. Each bit of the 32-bit register corresponds to a channel of the 'A' input For example, setting this register to 0x00000003 will enable channel 0 and 1, disabling the other channels.
Logic type	0x1010 mode	Type of logic for coincidence logic. Only the LSB is used. To set the coincidence to 'AND', this register should be set to 0x00000000. To set the coincidence to 'OR', this register should be set to 0x00000001

Read-only registers. Registers must be read in D32 mode		
Name	Address	Description
Firmware version	0x100C	Firmware version. Fixed at 0x00000002
Coincidence counter	0x100E	Counts the number of times the coincidence logic has triggered.

Discriminator settings for tests

When developing this firmware, I used a CAEN V812B discriminator. Here are the registers settings I used.

The base address of the V812B is 0x88AF0000

One can confirm the V812B is working by reading register 0xFA, which should return 0xFAF5

The V812B uses D16 for register read/write.

Suggested register settings for CAEN V812B Registers must be written in D16 mode		
Name	Address	Suggested value
Channel 0 threshold	0x00	0x10
Channel 1 threshold	0x02	0x10
Output width	0x40	0x01
Channel enable	0x4A	0x03 (enables channels 0, 1)

Further channel thersholds can be set as needed. The threshold register address is 2x(channel #).

To enable further channels, set the corresponding bits of register 0x4A

Detailed register information can be found in the CAEN V812B manual.